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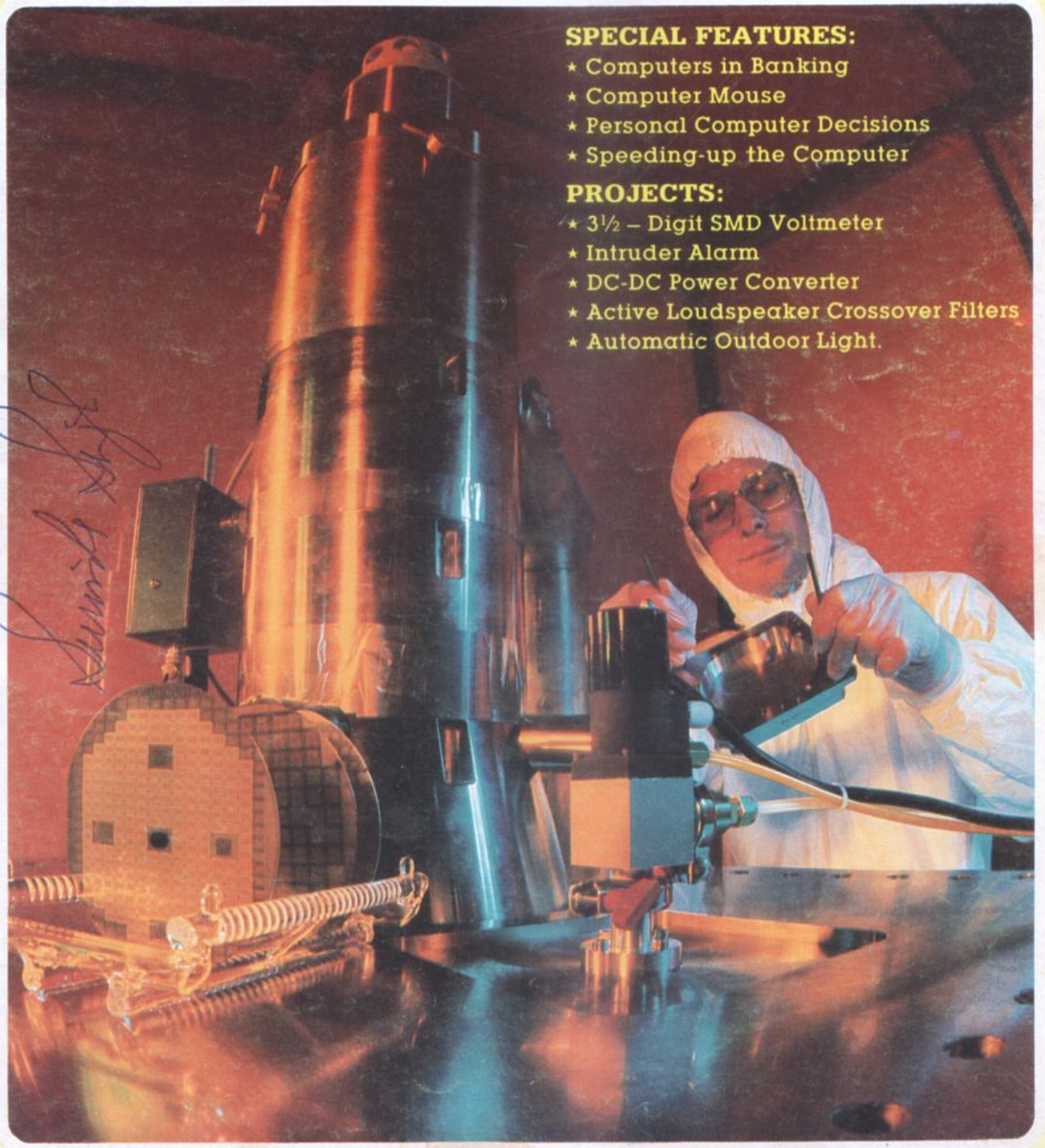

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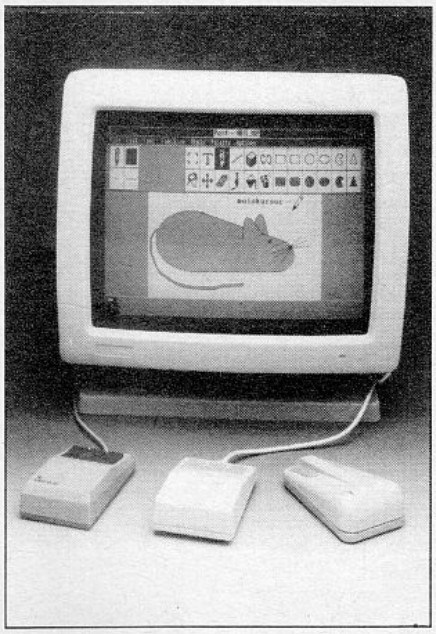
CONTENTS

COMPUTER MOUSE

J. Ruffell

Raptly looking at the screen and cheerfully moving the mouse around on our desks to make our way through menus, few of us appear to be aware of the operation of the most popular pointing device for computer applications.

A computer mouse is also called a *pointing device* because it allows the cursor (usually an arrow or crosshairs) to be moved across the computer screen. You use your hand to control the direction and speed of the cursor. Many mouse-oriented programs allow you to select an option from a menu on the screen simply by pointing at it and clicking a button on the mouse. The mouse has become so popular because it obviates keyboard commands that distract the attention from the screen and are relatively slow and susceptible to errors. Another major application of the computer, drawing, would be unthinkable without a mouse.



Principle of operation

One aspect common to all computer mice is that movement is converted into signals that can be handled by a computer. This is achieved basically as shown in Fig. 1. An auxiliary spindle presses a small ball lightly against two spindles that are mounted at right angles to each other. Its own weight, and in some cases the auxiliary spindle also, keeps the ball in contact with the desk surface or mouse pad. The movement of the ball is hardly obstructed because the areas where the spindles touch the ball are small. The friction is, however, sufficient to cause the spindles to rotate if the ball is moved horizontally (x component) or vertically (y component) in a two-dimensional plane. In this manner, the spindles extract the horizontal and vertical components from the mouse movement. These two components are converted into four electrical signals. This is done by mounting a slotted disk on to each spindle. The slots are arranged such that the light beam of one optocoupler is fully passed when the other optocoupler is about half way open. As the spindle rotates, the optocouplers produce two rectangular signals with a phase difference of 90°. The direction of travel of the spindle (in one plane) can be deduced from the phase relation of the two signals. The number of periods of the rectangular signal indicates the relative distance covered by the ball, and its speed.

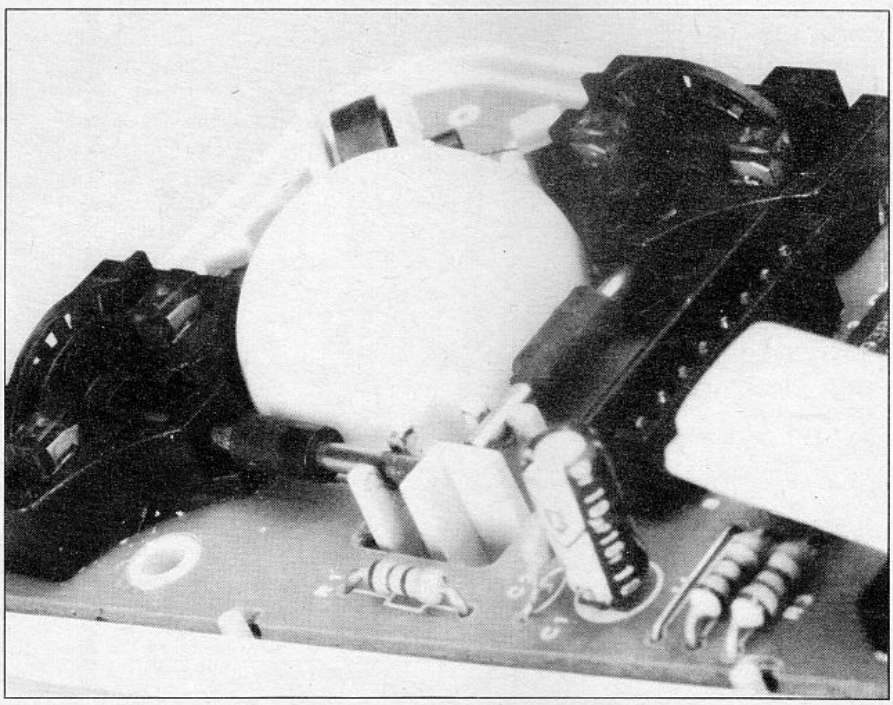


Fig. 1. Basic construction of a mouse that converts ball movement into electrical signals.

Figure 3 shows how the two rectangular signals are used to deduce the direction of travel of the mouse. One optocoupler signal is called *reference*, the other *direction*. The reference signal determines the instant the minimum step size (distance travelled) is reached in the direction indicated by the direction signal. This instant is marked by one of the level transitions (pulse edges) of the reference signal. Since most computer interrupts are called by negative pulse edges, it is convenient to look at the 1-to-0 transition of the reference signal. As shown in Fig. 3a, the direction signal is logic high at the negative edge of the reference signal. For the opposite direction, however (Fig. 3b), the direction signal is low at the negative edge of reference signal. In terms of programming, this means that the number representing the cursor position on the screen must be changed on the falling edge of the reference signal. In this software routine, the direction signal must be read to determine whether the cursor position must be incremented or decremented at a particular step size, e.g., one screen position. If, after first connecting a mouse and installing the software

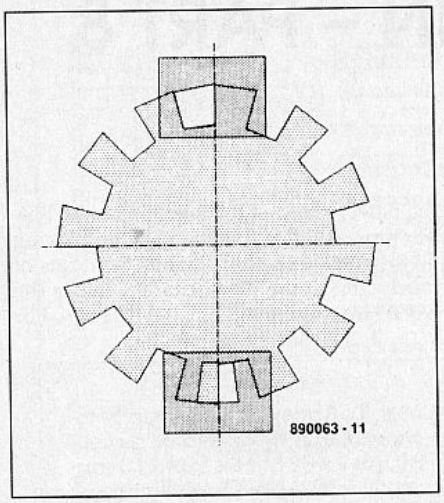


Fig. 2. Slotted discs and optocouplers are used to digitise ball movement.

driver, the cursor movement is opposite to that of the mouse, the reference and direction signals probably need to be swapped.

The above description of the basic operation of a mouse applies, at least in principle, to most other pointing devices that allow the user to control the cursor position on the screen direct by moving the mouse accordingly. There are, however, also applications that require a different approach. Take, for instance, a program that enables a drawing on paper to be copied into the computer by means of a mouse. In this case it is the drawing, not the computer screen, that determines the cursor position. This type of mouse is known as a *digitiser*, and is usually supplied with a special pad. The paper is inserted between the digitiser and the pad. The window in the digitiser 'sees' the pad surface through the paper. Because the pad 'communicates' with the digitiser, an output signal is available that enables the computer to determine the absolute position above the pad, and, of course, above the paper, which is secured on it. Lifting the digitiser and putting it down again a little further is therefore perfectly acceptable, since the new position is detected immediately. This is in contrast with a ball-type mouse, which can not supply positional information if it is lifted from the desk.

Another system to convey positional information to the computer is a combination of a graticule pad and a mouse with built-in reflection sensors. The internal operation is functionally similar to that of the discs and spindles in the ball-type mouse. The optocouplers are replaced by sensors that detect the light reflected by the pad. The function of the discs is taken over by the pad with its pattern of light and dark areas. Like the ball-type mouse, the optical mouse produces a reference and a direction signal. Its clear advantage is, of course, the absence of moving parts. However, the optical mouse also has its disadvantages: these are mainly that the pad has to be kept clean, and that the pattern on it is critical.

To the computer

The simplest way to convey the rectangular output signals supplied by the mouse is, of course, by means of a cable. The computer has either a built-in mouse adapter ('bus mouse', e.g. the Amstrad PC1512/1640 series), or a standard RS232 serial port to which a mouse with built-in 'intelligence' can be connected (e.g., most standard IBM PCs and compatibles). The latter mice are often microcontroller-driven, and supplied with a special software program, called the mouse driver, that enables the PC to translate data received at high speed via the RS232 port to be translated into cursor movement. The current required for powering the circuit in the RS232 mouse is obtained from the computer's serial port. This is possible only by virtue of the low current drain of the serial mouse.

The latest in pointing device technology is the wireless mouse, which communicates with the computer via an infra-red link. Position output and the way the data is processing in the driver are, however, not different from those of the conventional 'mouse with tail'.

Signal processing

As already stated, the mouse signals are usually processed by means of a driver program installed on the computer. Most computer users will content themselves with being able to automatically install the mouse with the correct parameters as part of the system configuration programs called at power-on. For advanced applications, however, mouse manufacturers like Genius supply a programming guide and auxiliary programs (e.g., Genius Menu Maker) that give the user the opportunity to implement his own pull-down menus and mouse control in a particular program.

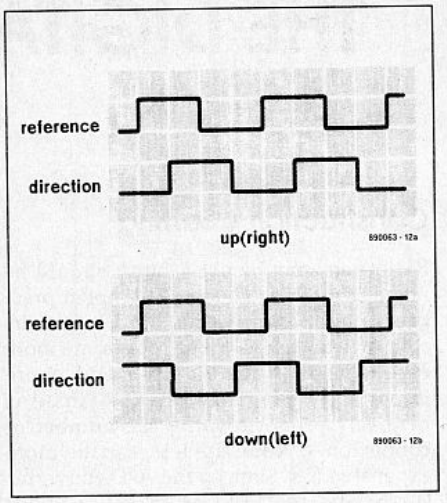


Fig. 3. The phase relation between the reference and direction signals is used to deduce the direction of travel.

Among the many functions of the driver or the microcontroller in the serial mouse is *adaptive resolution control*, or control of the step size as a function of mouse speed. If the mouse speed exceeds a certain predefined value, the cursor step size is automatically increased. The advantage of this system is that a relatively small mouse movement enables large distances to be covered rapidly on the screen.

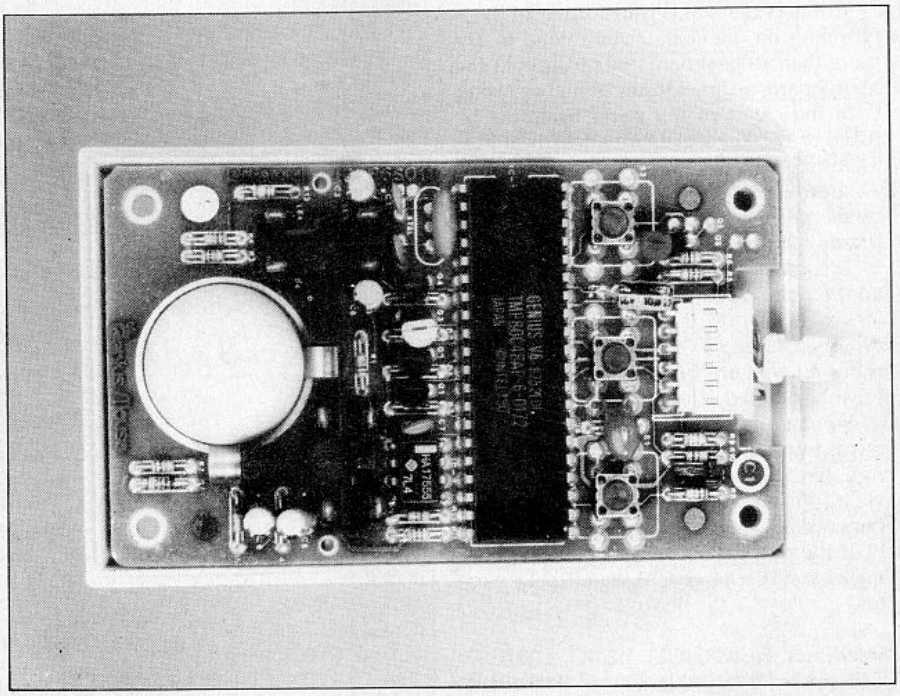


Fig. 4. Serial mouse with on-board CMOS microcontroller to guarantee a low current drain from the RS-232 port on the computer.

THE DIGITAL MODEL TRAIN – PART 8

by T. Wigmore

Construction & testing

IC sockets may be used, but it should be noted that this is no longer accepted practice, at least as far as standard logics circuits are concerned. Some sockets are more expensive than the IC itself and, more importantly, the reliability of a circuit is inversely proportional to the number of connexion s. None the less, for the more expensive ICs, such as the A-D converter (IC25) and the EPROM (IC13), a good-quality socket is recommended. Bear in mind also that the printed-circuit board is through-plated: any desoldering of ICs is, therefore, a tricky operation. So, check and double-check whether the IC is the correct one before soldering it on to the board.

The parts list shows ICs of the HC- and HCT-type. The HC-types may be replaced by HCT-types, but HCT-types should NOT be replaced by HC-types.

Power supply. Start by fitting D38–D41, D36, C24, C25 and C27. Next, fit IC29 on to the relevant heat sink and mount the resulting assembly on to the board. There are tracks underneath the heat sink that are protected by a thin layer of lacquer only: it is therefore necessary to give these extra insulation (by, for instance, a suitably-sized piece of thin cardboard or old PCB or insulating tape). The IC should be fixed to the heat sink with an M-3 bolt, nut and washer, and a generous amount of heat conducting paste.

Connect the mains transformer to the ~ terminals on the PCB. If you intend to use more than 10 keyboards in addition to the main board, a transformer of higher rating than indicated in the parts list must be used, or the keyboards (dealt with in Part 9) must have a separate power supply. Assuming that the keyboards will be fed by the present supply, wire link A must be fitted.

It is possible to use a suitable mains adapter provided this delivers 9 V at not less than 800 mA. If the adapter delivers a direct voltage, D39 and D40 may be replaced by wire links and D38 and D41 must be omitted.

Switch on the mains and check that the output voltage of IC29 is 5 V ±5%. If it is not, disconnect the mains, discharge C25 via a 100 Ω resistor, and check all the components and the preceding work thoroughly. If the output is all right, switch off the mains and discharge C25 via a 100 Ω resistor.

Oscillator. Fit IC8, IC21, R2, R3, C22, C37, C40 and the crystals on to the board. Switch on the mains and verify that a symmetrical signal of 2.458 MHz exists on pin 12, and a signal of 614 kHz on pin 8 of IC8.

Microprocessor. Fit IC4, R8, R12, R18, R19, R24, C34, D34 (observe polarity!), T1, IC24, R13 and C23. These components constitute the power-up reset for microprocessor IC4. The operation of IC4 is tested by placing an instruction on the data bus by means of hardware. In the first instance, this is the STOP instruction (76_H: 01110110_B). For

Parts list

Resistors:
R1 = 100Ω
R2;R3 = 4k7
R4;R5;R11;R12;R17–R20;R22;R23;R24 = 10k
R6;R10 = SIL resistor array 10k
R7;R8;R15 = 330Ω
R9;R14;R16 = 47k
R13 = 15k
R21 = 6k8

Capacitors:
C1–C16 = 10n (pitch 5 mm)
C17 = 47p
C18;C19 = 100µ; 25V
C20;C21 = 220n
C22 = 33p
C23 = 4µ7; 6V3; tantalum
C24;C27 = 470n
C28–C42 = 100n (pitch 7.5 mm)
C25 = 2200µ; 16V; axial
C26 = 10µ; 6V3; tantalum

Semiconductors:
D1–D32;D37 = 1N4148
D33 = green LED
D34 = red LED
D35 = yellow LED
D36 = 1N4001
D38–D41 = 1N5401
T1;T3 = BC557
T2 = BC547
IC1 = 74HC(T)245
IC2 = 74HC(T)74
IC3 = Z80PIO (Z8420 or Z84C20)
IC4 = Z80CPU (Z8400 or Z84C00)
IC5;IC6 = 74HCT238
IC7 = 74HCT139
IC8 = 74HCT93
IC9 = MC1489 or SN75189
IC10 = MC1488 or SN75188
IC11;IC26 = 74HCT32
IC12 = Z80CTC (Z8430 or Z84C30)
IC13 = 2764 (ESS572)
IC14 = 6264
IC15 = 78L12
IC16 = 79L12
IC17;IC19 = 74HCT174
IC18 = 4066
IC20 = 74HCT244
IC21 = 74HCT04
IC22;IC23 = 74HCT374
IC24 = 74HCT74
IC25 = ADC0816
IC27 = MC145026
IC28 = 74HCT138
IC29 = 7805

Note: ICs from the HC-series may be replaced by HCT-equivalents. Do not use a HC type if a HCT type is stated. LS-types are not suitable because of their higher current consumption.

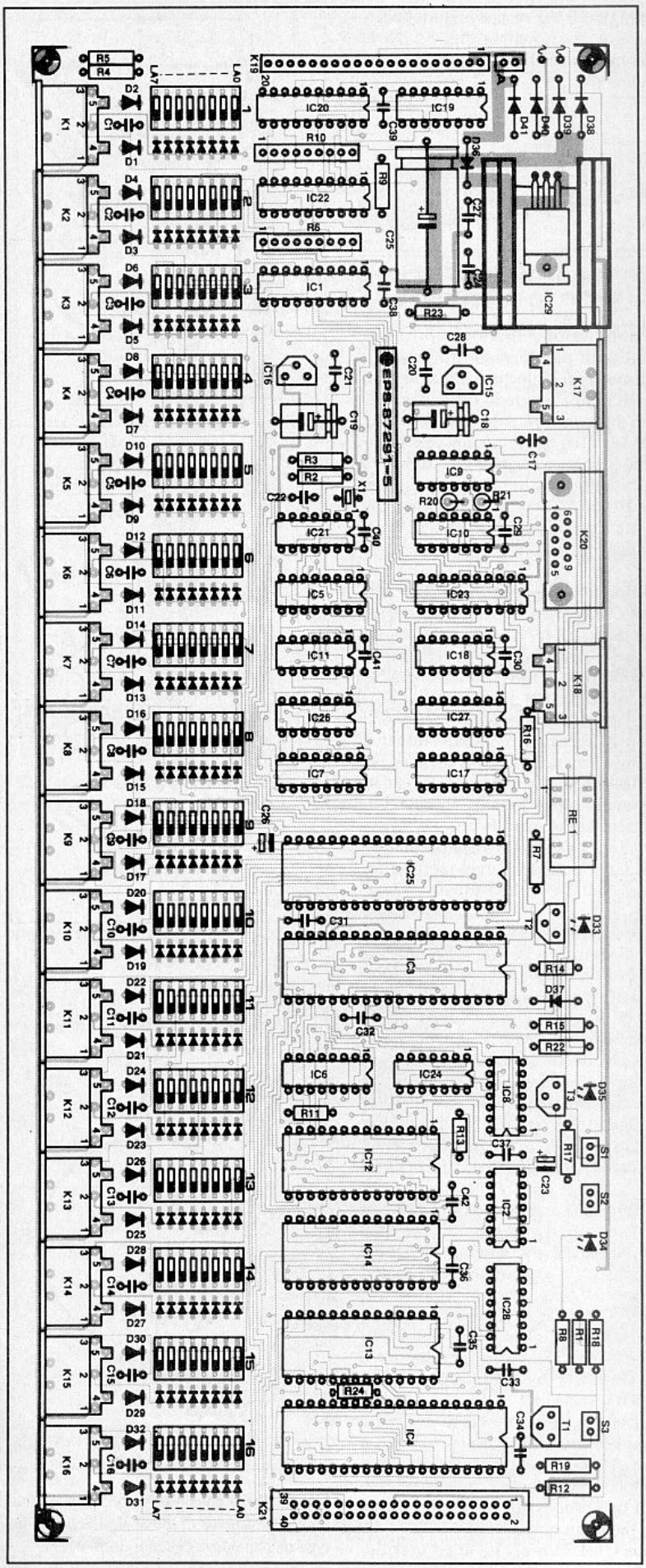
Miscellaneous:
K1–K18 = 5-way 180° DIN socket for PCB mounting.
36 off M2×5 screws for securing K1–K18.
K19 = 20-way SIL female header; angled; 0.1-in. pitch (e.g., Assmann AWRF A20Z).
K20 = 9-way feamle sub-D connector; angled; for PCB mounting.
2 off M3×8 screws for securing K20.
K21 = optional 40-way for future extensions.
RE1 = DIL reed-relay; 5 V coil voltage; e.g., Siemens V23100-V4005-A000.
X1 = quartz crystal 4.9152 MHz.
S1;S3 = push-to-make button.
S2 = push-to-break button.
Heat-sink for IC29: size 30×37.5 mm (e.g., SK09 from Dau Components/Fischer).
Mains transformer 8 V or 9 V @ 1 A min. sec.
PCB Type 87291-5

Additionally required for each loco controller (max. 16 allowed):

Loco controller:
Potentiometer 100k linear (rotary or slide type) with knob.
5-way DIN-plug; 180°.
One (EEDTS) or two (Märklin-system) SPST switches.

Loco address settings (4 options):
1) fixed address setting:
diodes 1N4148, max. 6
2) variable address setting:
8 diodes 1N4148 and 1 8-way DIP switch block.
3) variable addresss setting:
8 diodes 1N4148
16-way header with 2×8 contacts in 0.1-in. raster.
max. 6 jumpers
4) extra-flexible address setting:
as option 3 but instead of jumpers:
16-way flatcable connector
2 BCD-encoded thumbwheel switches

* number of sockets depends on number of connected loco controllers. Socket K18 is preferably a 6-way type for PCB mounting.



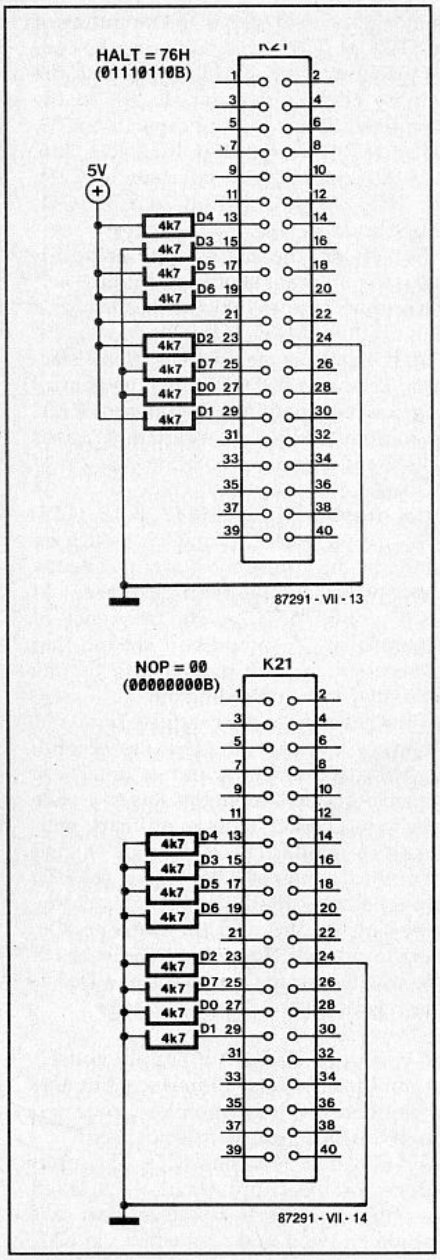


Fig. 49. Operation of the microprocessor is tested by instructions on the data bus formed by resistors. The STOP instruction (01110110_B) is formed as shown at the top, and the NOP instruction (00000000) as shown in the lower illustration.

this, eight 4k7 resistors are connected as shown in Fig. 49a to where later (possibly) K21 will be connected. When the mains is switched on, D34 should light. Switch off the mains and place the NOP instruction (00000000) on to the data bus as shown in Fig. 49b. Switch on the mains and check the data bus for any short-circuits. Pin A0 should have a symmetrical square wave of 307 kHz; A1 one of 307/2 kHz; A2 one of 307/4 kHz; and so on up to A15, which should have one of 9.375 kHz.

Fig. 50. Component layout of the double-sided, through-plated main printed circuit board. The board is illustrated here on a scale of 95:100.

Memory. The next step is the mounting of the EPROM (IC13) that con tains the control program, the RAM (IC14) and the memory address decoder (IC28). At the same time, fit decoupling capacitors C33, C35 and C36. Next, fit IC3, IC12, R11, R16, R17, R9 (immediately adjacent to C25), R22, R15, D35, T3, IC7, IC26, C32, C41, C42, S1 and S2.

Switch on the mains and press S1, when the program should go into the service routine, indicated by the flashing in a 1 Hz rhythm of D35. If this happens, IC3, IC12, IC4 and the memories work satisfactorily. If, however, D33 lights, the control program has gone into the internal RAM test routine: this is almost certainly caused by IC13 and associated components.

Serial output. Fit IC11, IC17, IC18, IC23, IC27, C30, R7, R14, D33 and T2. Switch on the mains and press S1: a low-frequency square wave should then be present at pins Q0 to Q7 of IC23. The frequency of that signal at Q0 should be 1 Hz and that at successive output pins should be one half of that at the preceding pin.

Pin Q0 becomes alternatively high and low every half second; Q1 every second; Q2 every two seconds; and so on. These frequencies were chosen this low to enable them to be checked with an ordinary multimeter. A similar check must be carried out at the outputs of IC17. Again, the first output becomes alternatively high and low every half second and the last one, Q6, every 16 seconds. Note that D35 flashes in unison with output Q0 of IC23, and D33 in unison with Q6 of IC17.

±12 V supply. The ±12 V supply is used not only for the RS232 interface, but also for the booster. It is, therefore, required even if the RS232 interface is not used.

Fit C18–C21, IC15 and IC16. The input voltage for the supply (±20 V) is taken from the booster board (see Part 6 - September 1989) and connected via K17. This connector is shown in the parts list as a 5-way DIN socket, but a (hard-to-obtain) 6-pin type is preferred, because this prevents the connecting cable from being plugged into one of the other DIN connectors by accident. Because of the presence of the ±20 V potentials that would almost certainly have disastrous consequences.

The wires in the cable between the main board and the booster board must be connected to identically-numbered pins on K1 and K17. If a 6-way type (which has different pin numbers) is used for K17, stick to the numbers given on the boards.

Switch on the mains to the booster unit (NOT to the main board). The potential at pin 1 of K18 (with respect to pin 2) should be –20 V and that at pin 3 (again with respect to pin 2) should be +18 V. The output voltage of IC15 should be +12 V and that of IC16, –12 V.

A-D converter and locomotive address decoder. Fit R1, R4, R5, C26, C31, C38, IC1, IC2, IC25 and resistor-array R6. Instead of an array, eight 10 kΩ resistors may be fitted vertically as shown in Fig. 51. Note that the common earth connexion must be at the underside.

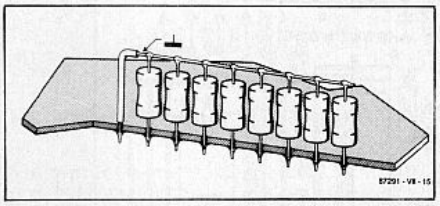


Fig. 51. Instead of resistor-arrays R6 and R10, eight 10 kΩ resistors may be fitted vertically.

To enable writing the loco addresses associated with the loco controllers, IC6 and (if more than eight loco controls will be used) IC5 are needed. Loco controls may then be connected to K9–K16. The controller with the highest connector number has the highest priority if the addresses are coded identically. In other words, if in positions 10 and 14 the controllers have the address 00, that in position 14 will have priority over that in 10.

Construction of a loco controller. The A-D converter can not be tested until a loco controller is available. From a circuit point of view, these controllers are fairly simple: three possible designs are shown in Fig. 52. For each of these designs a 5-way DIN plug (180°), a 100 kΩ potentiometer and one or two switches are required. Note that the housing of the DIN plug is used as the sixth (earth) pin.

It is possible to connect the loco controllers direct to the main board, i.e., without plugs and sockets. This is a particularly logical (and less expensive) method for controllers that are to be built in permanently.

Each loco controller is associated with one or two switches for the switching on and off of the controller, the setting of the type of data format and, possibly, the additional decoder switching function.

If a mixture of Elektor Electronics and Märklin loco decoders is used, the controller design shown in Fig. 52a should be used. The design in Fig. 52b is intended for Elektor Electronics controllers and that in Fig. 52c for Märklin or the modified Elektor Electronics controller (see Part 3 - April 1989).

A controller is considered to be out of action if both pin 4 and pin 5 of the DIN connector are open and therefore also if the relevant DIN connector on the main board is not connected up.

Switch S1 in Fig. 7b and 7c may be replaced by a wire link at the relevant DIN connector. A controller can then be taken out of action only by removing the plug from the DIN socket.

If the connexions between the main board and the controllers are fairly long, it is recommended to use screened cable.

Each loco controller needs a filter capacitor and two diodes, all of which may be fitted on the main board.

Diodes D1–D32 must be fitted vertical-

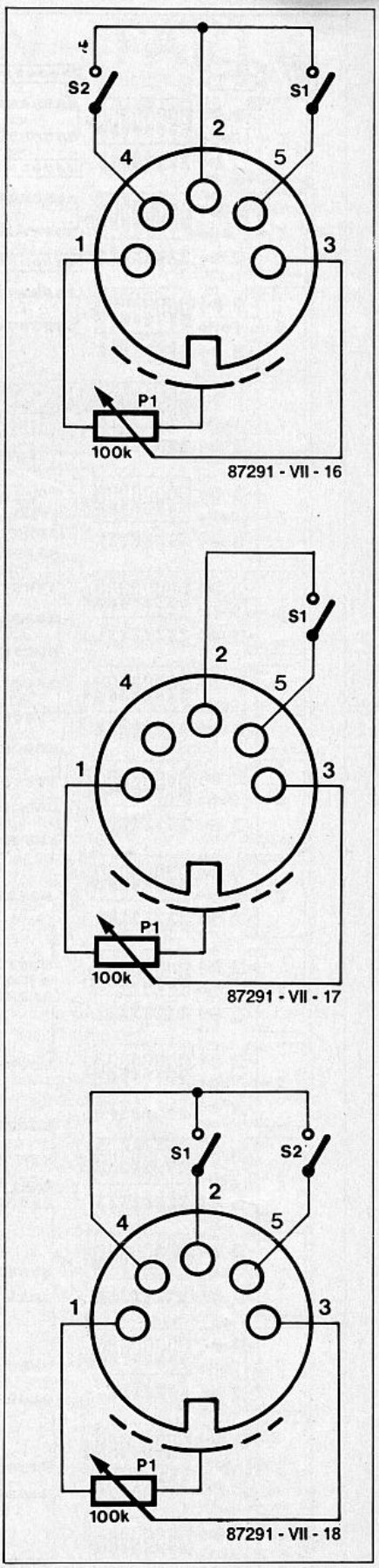


Fig. 52. Three possible designs of a locomotive controller. Choice of the design depends on the type of locomotive decoder used.

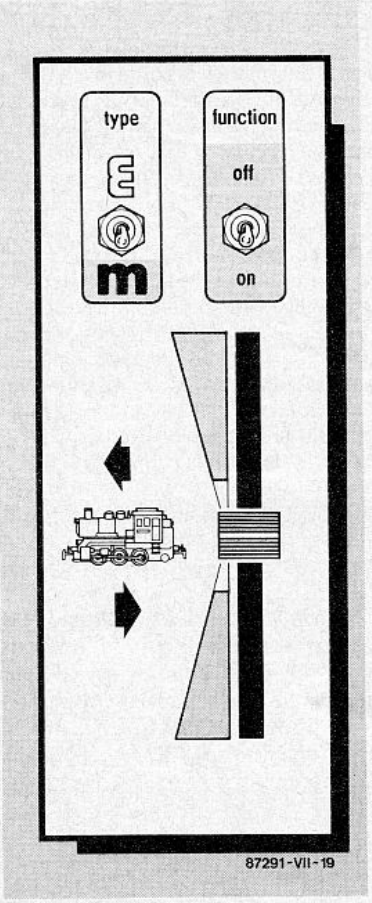


Fig. 53. Possible design of a front panel for the loco controllers.

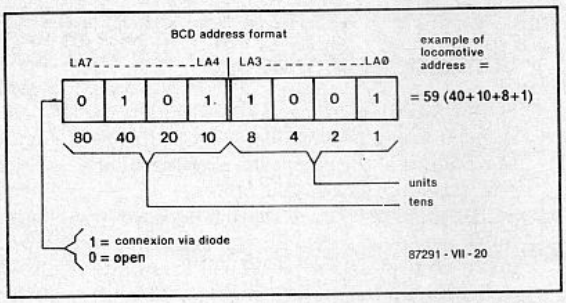


Fig. 54. Loco addresses (00–80) must be presented in BCD format.

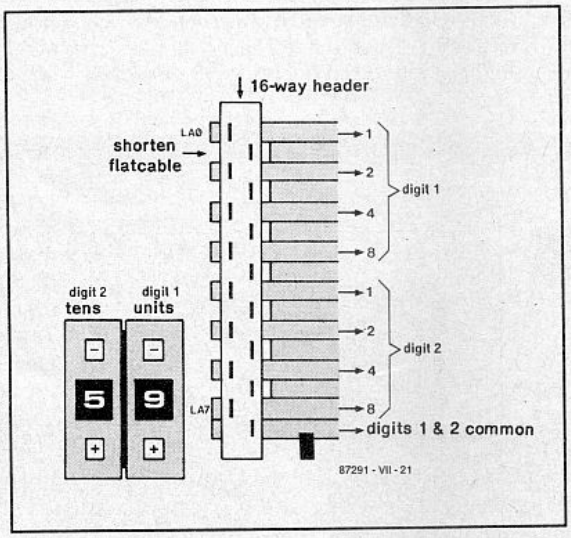


Fig. 55. Thumb-wheel switches may be connected via flatcable. Unused wires should not be connected to prevent unnecessary capacitive loads.

ly.

Since the DIN sockets are subject to fairly large mechanical strains during the insertion and withdrawal of plugs, they should be fixed to the board with M2×5 nuts and bolts or with small self-tapping screws before the solder connexions are made.

Loco controllers and the A-D converter may be tested by connecting them to K16, which is the most important loco controller socket. The setting of the loco addresses will come later: for the time being, they will be written as 00.

Switch on the mains to the main board, but do NOT press S1. The normal control program will then be active. After a moment or two press S1 when D33 should light. Also, the signals resulting from the A-D conversion are present at outputs D3–D7 of IC25, while at pins 6 and 9 of IC2 the switch position may be verified: if the output is 0, the switch is closed and if it is 1, the switch is closed.

Output relay. Fit Re1, D37, IC10, R20, R21 and C29. When the mains is switched on, pin 3 of IC10 should have a d.c. potential of –10 V to –12 V. When S1 ('go') is pressed, the output relay will be energized in unison with the lighting of D33.

Also, the same potential as at pin 3 of IC10 should be present at pin 4 of K17. When in this condition a loco controller is connected, the potential should vary slightly when the potentiometer is adjusted. The degree of the variation depends on the loco address. This voltage is no longer a true d.c. potential as may be verified with an oscilloscope, which will show the repeatedly sent loco control instructions whose rear portion varies according to the position of the potentiometers and function switches, while their front portion varies according to the relevant loco address.

Setting the loco addresses. In general, loco addresses must be presented in BCD format as shown in Fig. 54. Valid addresses are in the range 00–80 (note that Märklin does not count 00 as a valid address). Invalid addresses are simply ignored. A number of possibilities of setting the addresses is shown in Fig. 56.

The method of Fig. 56a is by far the least expensive, but has the disadvantage that addresses can be changed only with the aid of a soldering iron.

The method in Fig. 56b is the one used in the present design. The DIL switches permit setting and altering the addresses at any given moment, even during operation of the system.

It is also possible to program the loco addresses via the RS232 port: this method will be discussed in a later instalment.

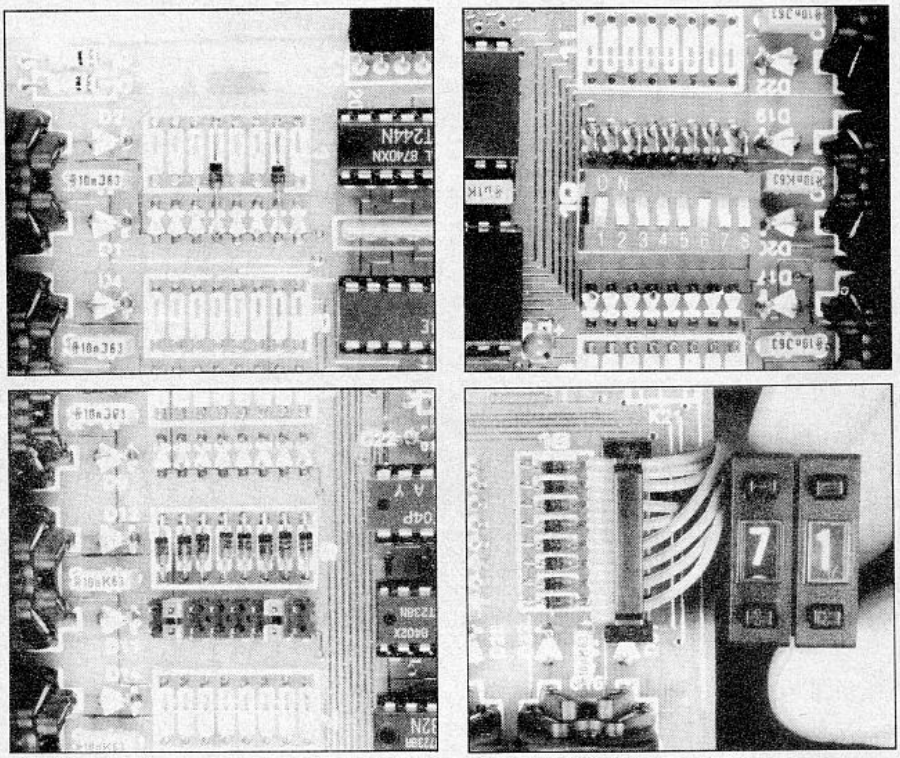


Fig. 56. Four possibilities of setting loco addresses: (a) with diodes (address = 48); (b) with diodes and DIL switches (address = 21); (c) with diodes and shorting plugs (address = 42); (d) with diodes and thumb-wheel switches (address = 71).

Keyboard interface. This section of the board need, of course, only be populated if

it is intended to connect keyboards (which will be dealt with in next month's instalment) to the main board.

Fit resistor-array R10 (but see Fig. 51), R23, C28, IC19, IC20, IC21 and K19. The choice of a single-in-line type for K19 was deliberate, because if the keyboards are installed permanently, they may be connected by means of wire links instead of by relatively expensive plugs.

RS232 interface. To populate the last section of the main board,fit IC9, C17, K20 and K18.

The installation of the main board is left to your own requirements, but bear in mind that keyboards must be connected to the left-hand side of the (flat) case

Some operational tips

Loco controllers are scanned from left to right. If several controllers are set to the same address, the one at the extreme right will have priority over the others.

As in the Märklin system, it is possible to set the speed of one locomotive with a given controller and then use that controller for a different loco address, without affecting the operation of the first loco.

If the mains is not connected to the system and S1 is pressed, the green LED (D33) will light, but go out as soon as S1 is released.

The system can not and will not send data until the booster is switched on and the go key (S1) has been pressed. If the connexion with the booster is broken, the system will automatically come to a halt.

The system ignores brief (< 0.5 s) short-circuits. Again, if the system switches itself off, it may be reactuated by pressing S1.

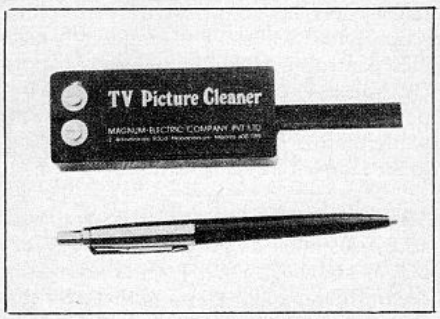
In emergencies, the system may be stopped by pressing S2: this not only incapacitates the control program, but it also removes the power from the rails. If desired, a number of these stop switches may be installed in series along the track.

Switch S3 is the system reset control, which normally will not be used. Only if the system does not appear to react to any other control or if D34 unexpectedly lights, should this switch be used.

NEW PRODUCTS

TV Picture Cleaner

Say goodbye to disturbances in your TV Picture caused by tubelights, grinders, belnders, autorickshaws, scooters and low-flying aircraft. The TV Picture Cleaner, when connected to antenna cable, removes them electronically. The product can be easily connected to the antenna cable. Used throughout the world, this device has been designed and manufactured in India by Magnum Electric.



Magnum Electric Company Pvt. Limited • 2, Ramavaram Road • Manapakkam • Madras-600 089. Phone: 434547.

Microprocessor Controlled Charge Amplifier

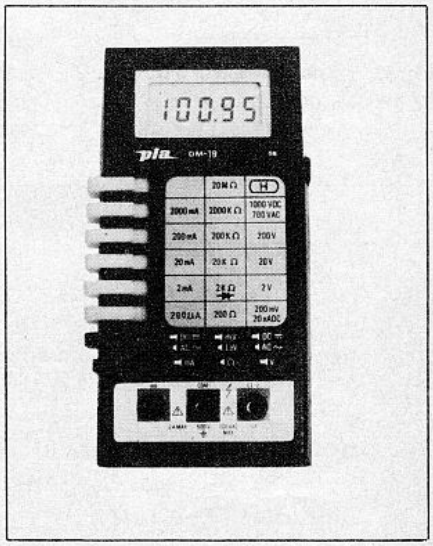
The mains operated, microprocessor controlled single channel; charge Amplifier Type 5011 from our Principals M/s. KISTLER INSTRUMENTE AG, SWITZERLAND, is a new concept in converting the charge yielded by Piezo Electric Transducers into a proportional

voltage signal. Main characteristics are continuous range setting from ± 10...999,000 pc and LCD parameter settings. The parameters remai set if mains failure occurs. Frequency range from 0-200 kHz, automatic zero offset correction, in built low pass filter with 8 selectable cut off frequencies, 3 selectable time constants. An IEEE-488 Interface enables the Charge Amplifier to operate via a Computer. Available against Actual Users Import Licence or Open General Licence as applicable.

M/s. Integrated Process Systems • 9, M.P. Avenue • Santhome • Madras-600 004.

Digital Multimeter

Pla has introduced a 4½ digit LCD digital multimeter. This accurately measures AC/DC voltage, current and a broad range of resistance. The instrument also features an In Circuit Low Voltage Tester. Other attributes include a Continuity Tester, Data hold facility, Diode Tester and add-Ons to measure high voltage upto 30 KV DC/20 KV AC. (HV Probe), Currents upto 20 A (Current Shunt), Frequencies upto 20 KHz (A.F. Probe) and 10 MHz.



Pla Electro Appliances Pvt. Ltd. • Thakor Estate • Kurla Kirl Road • Vidyavihar (West) • Bombay-400 086.

3½-DIGIT SMD VOLTMETER

T. Wigmore

This little circuit is simple to build, offers good accuracy and can be used in all applications requiring a small voltmeter with a clear LED read-out.

Much of today's electronic equipment requires a digital read-out to show system status or process variables. Such read-outs are usually compact voltmeter modules with an LC (liquid crystal) display. The present read-out is also a voltmeter, but uses displays with light- emitting diode (LED) segments. A LED indication was chosen for this application because it remains visible in the dark (this requirement would also have been met by an LCD with back-lighting). Also, the use of 7-segment LED displays in combination with a drive circuit built with SMA (surface-mount assembly) components allows a really compact voltmeter to be realized — see Fig. 1. This is particularly important if the meter is to be built into existing equipment.

One integrated circuit

The circuit (Fig. 2) is formed by a single integrated circuit Type ICL7107 from Intersil. This voltmeter IC is the LED version of the perhaps even more familiar ICL7106 for LCDs. The ICL7107 contains everything required for the analogue-to-digital conversion of the input signal, and the driving of a 3½-digit read-out. The chip is used in a more or less standard application circuit with some extra components to afford flexibility as regards the power supply.

Analogue-to-digital conversion

Analogue-to-digital (A-D) conversion can be accomplished in a number of ways. Fast converters almost invariably use

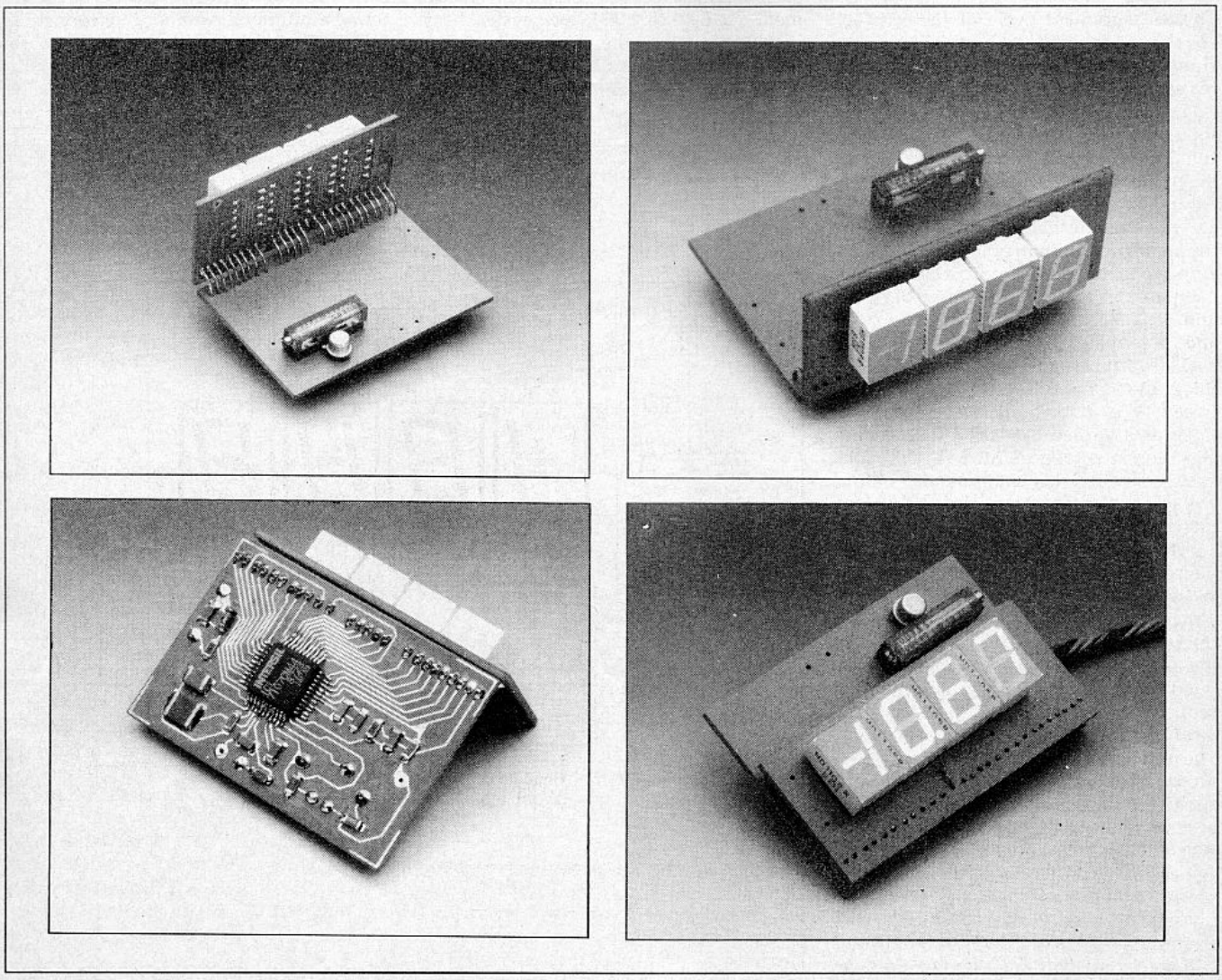


Fig. 1. The compact voltmeter module seen at different viewing angles.

flash ADC chips that are characterized by a large number of internal comparators. The other principle, successive approximation, is based on a resistor ladder network whose R-2R junctions are connected to counter outputs. The result of the D-A conversion is compared to the input signal. If a difference is detected, the clock oscillator with the counter is controlled accordingly until the output voltage of the internal D-A converter equals the externally applied voltage. In practice, the accuracy of this type of converter is that of the R-2R network, and the off-set voltage of the voltage comparator.

The ICL7107 and other ICs in its family work on yet another principle, which is entirely analogue and based on an integrator. Internal off-set voltages are compensated prior to any measurement cycle, so that a high accuracy is achieved even with small input voltages. Since the measurement principle is based on the comparison of an input voltage, U_i, with a reference voltage, U_{ref}, the display value is in fact U_i/U_{ref}. Interestingly, the reference voltage may be applied externally.

Three phases

The measurement cycle of the ICL7107 consists of 3 phases. Figure 3 shows the signal path in the analogue input circuit for each of these.

During the auto-zero phase (Fig. 3a), inputs IN LO and IN HI are disconnected. Internally, a closed loop is formed consisting of input buffer amplifier A_1, integrator A_2 and comparator A_3 (C_{int} is discharged as yet). The internal ground is formed by the analogue common potential. The auto-zero capacitor will charge to a voltage that compensates the off-set voltages of A_1, A_2 and A_3. Also, C_{ref} is charged to the reference potential.

The auto-zero phase is followed by the integration phase. The input voltage between IN LO and IN HI is applied to an integrator formed by A_2-R_{int}-C_{int}. The integration interval is defined as 1,000 clock cycles. During this interval, the output voltage of the integrator rises to a value directly proportional to the input voltage.

The last phase is the de-integration phase. The input voltage to the integrator is disconnected again and replaced by the voltage on C_{ref}. An internal circuit allows the reference voltage to be connected with the opposite polarity of the previously applied input voltage. This causes the integration process to be reversed, and the interval to be timed by the internal clock. The number of clock pulses is directly proportional to the ratio of the reference voltage to the input voltage. This principle is best understood by assuming the reference voltage to be equal to the input voltage, which results in a de-integration phase that is just as long as the integration phase. The length is 1,000 clock cycles, which is shown on the display. If the input voltage is only half the reference voltage, the de-integration process takes half the time of the integration process, and the display will read 500 to indicate that $U_{in} = 0.500 U_{ref}$.

The length of the de-integration phase depends on the input voltage. With relatively long de-integration phases, the auto-zero phase is automatically shortened so that the total measurement time — and with it the number of read-outs per second — remains constant. The integration phase always lasts 1,000 clock cycles, the de-integration phase 0 to 2,000 clock cycles, and the auto-zero phase 1,000 to 3,000 clock cycles. One complete measurement cycle takes 4,000 clock cycles, bearing in mind that the clock frequency is divided internally by 4. A clock frequency of 48 kHz gives an internal clock frequency of 12 kHz to allow 3 measurements per second.

Common mode

The dual slope measuring principle used by the ICL7107 has been discussed in some detail to show up the limitations of the common-mode arrangement.

Clearly, satisfactory measurements can be made only if the reference and input voltages lie within common mode range, V−(+1 V) to V+(−0.5 V), of the internal amplifiers. Another requirement is for the integrator output voltage to remain well below the positive supply voltage. During the integration phase, the

3½-DIGIT SMD VOLTMETER

• Read-out:	3½-digit LED display
• Sensitivy:	±200 mV; differential input with symmetrical supply
• Decimal point:	2 positions; indication 188.8 or 18.88
• Reference:	internal or external
• Supply voltage:	single 5 V (limited common-mode); 5 V with negative bias; symmetrical (±5 V)
• Current consumption:	max. 200 mA from positive (+5 V) supply; 300 µA from negative supply
• Size:	55×37×11 mm

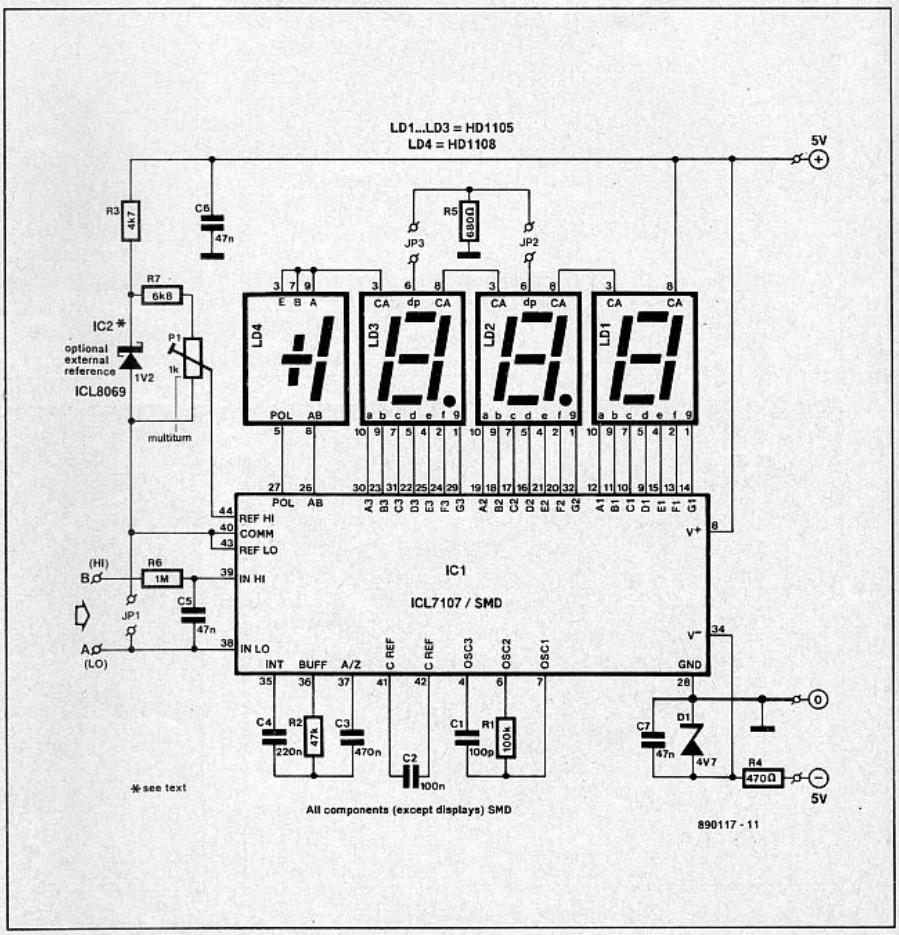


Fig. 2. Circuit diagram of the voltmeter.

voltages at IN LO and IN HI are connected to the inputs of the internal buffer amplifier and the integrator, and must, therefore, fall within the common-mode range. The reference voltage is never applied direct, but via the previously charged capacitor C_{ref}. This means that the common-mode voltage range (CMVR) of the reference voltage is the supply voltage, i.e., V+ to V–.

During the integration phase, the integrator uses the potential at IN LO as the reference. De-integration, however, is effected with respect to the 'common' potential. Consequently, any difference between the IN LO potential and the common potential causes a voltage jump at the integrator output during the switch-over from integration to de-integration (see Fig. 3b).

Displays

In the circuit diagram in Fig. 2, the oscillator frequency is set to 48 kHz by components C_1-R_1. This frequency results in 3 read-outs per second, and may be adapted to individual requirements by changing R_1-C_1 as appropriate, bearing in mind that the integrator time-constant, R_2-C_4, must be changed at the same time.

Input filter R_6-C_5 ensures a stable read-out.

The segment current capability of 5 to 8 mA of the ICL7107 obviates additional driver transistors and current limiting resistors. The read-out is composed of 3 common-anode 7-segment LED displays Type HD1105, and 1 common-cathode display Type HD1108. The latter is used because ½-digit, 12.7 mm-high, LED displays are difficult to obtain in common-anode versions. Fortunately, the cathode of the minus sign on the HD1108 is not connected to the A and B segment. Both the HD1105 and HD1108 are manufactured by Siemens.

Internal and external reference

The internal reference source of the ICL7106 and the ICL7107 may be used with a sufficiently high supply voltage (more than 6.5 V between V– and V+). The temperature characteristics of this reference may, however, cause problems with the SMA ICL7107 because this is a relatively small chip, and drives LEDs direct. For this reason an external reference, e.g., the ICL8069, may be used. Other reference devices may be used provided R_3 is modified accordingly to ensure optimum bias current (note that the voltage difference between REF LO and V+ is typically 2.8 V). Resistor R_7 has a value that allows multiturn preset P_1 to be adjusted to give a reference voltage of 100 mV between REF LO and REF HI.

Construction

The printed-circuit board (Fig. 5) accommodates the voltmeter circuit and the displays. The board is cut in two to enable the display section to be mounted either vertically or horizontally on to the voltmeter board.

All components, except the optional reference, IC_2, multiturn preset P_1 and the 4 displays, are surface mount assembly (SMA) types.

The values of R_3 and R_7 depend on whether or not IC_2 is used, while components R_4, C_7 and D_1 may be required only with certain power supplies as discussed below.

The two jumpers on the board allow the decimal point to be positioned either between the first and second digit (e.g., 100.0) or between the second and third digit (e.g., 10.00). The third option, 1.000, is not possible because the fourth digit is a common-cathode type.

Power supply

In most cases, the voltmeter will be incorporated into an existing piece of equip-

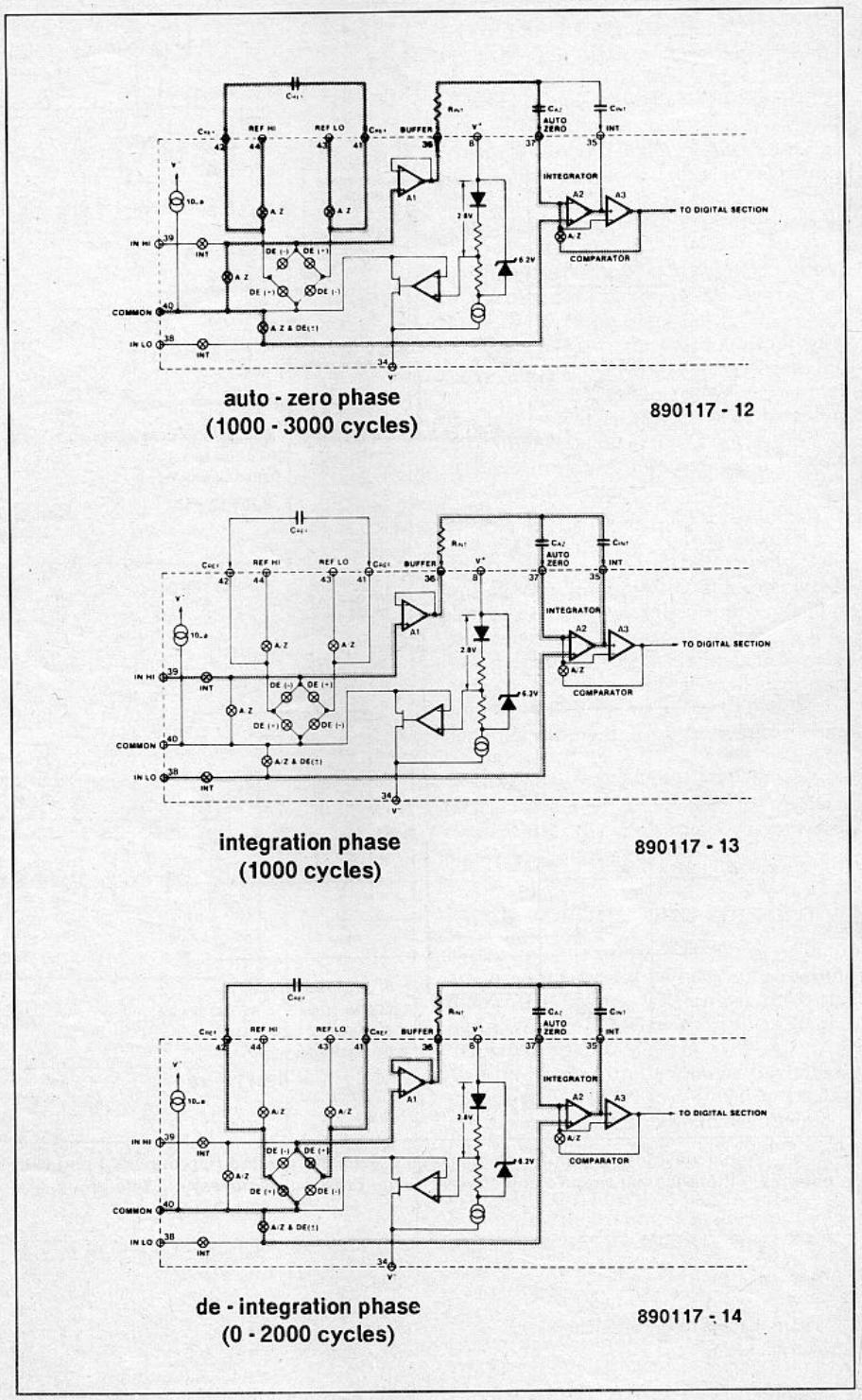
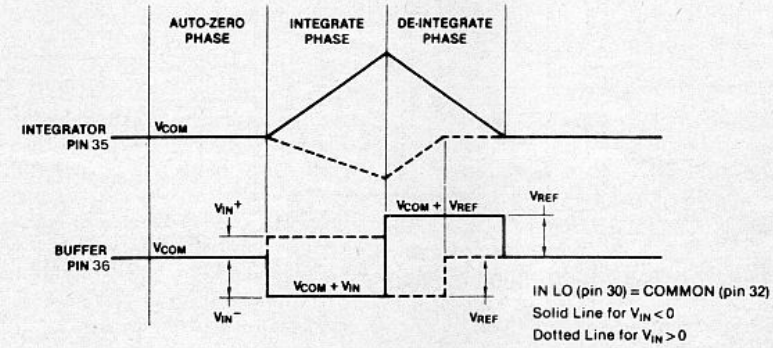


Fig. 3. Signal paths illustrating the basic three-phase operation of the analogue input stages of the ICL7107 voltmeter chip (*courtesy GE-Intersil*).



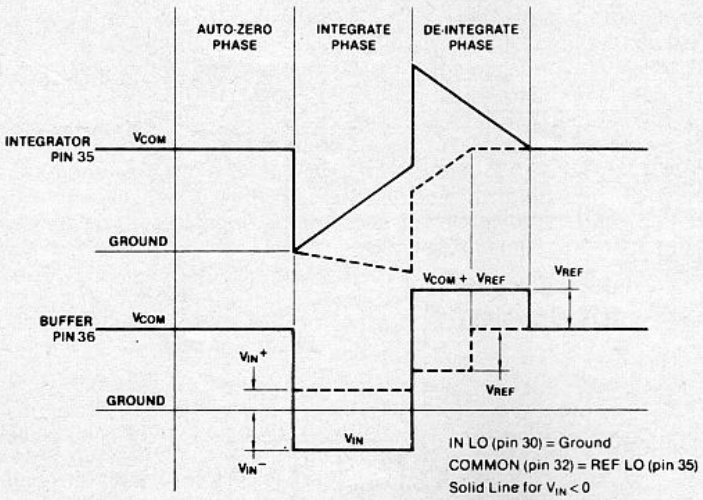


Fig. 4. Signal waveforms with terminals LO an COMMON connected (top drawing) and with a potential difference between LO and COMMON (lower drawing) (*courtesy GE-Intersil*).

Parts list

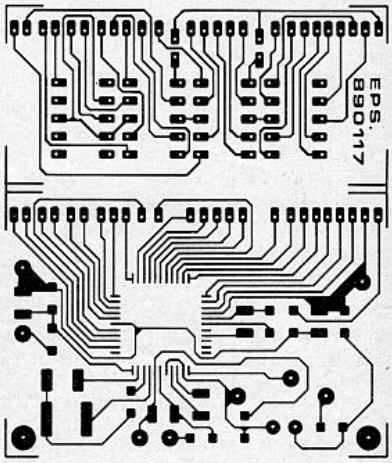
All parts surface-mount assembly except when marked +.

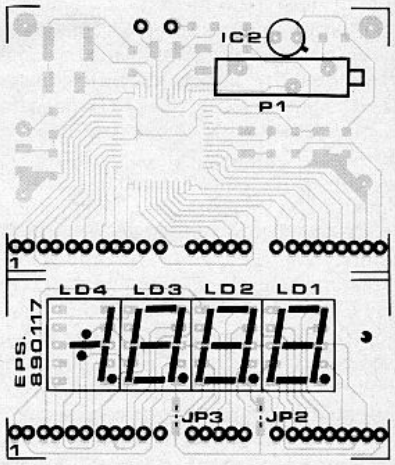
Resistors:
R1 = 100k
R2 = 47k
R3 = 4k7
R4 = 470Ω
R5 = 680Ω
R6 = 1M0
R7 = 6k8
P1 = 1k0 multiturn preset +

Capacitors:
C1 = 100p
C2 = 100n
C3 = 470n
C4 = 220n
C5;C6;C7 = 47n

Semiconductors:
D1 = zener diode 4V7; 400 mW
LD1;LD2;LD3 = HD1105R (Siemens) +
LD4 = HD1108R (Siemens) +
IC1 = ICL7107 (GE-Intersil)
IC2 = ICL8069 (GE-Intersil) +

Miscellaneous:
PCB Type 890117





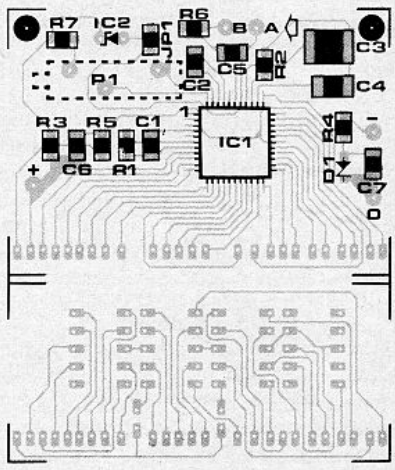
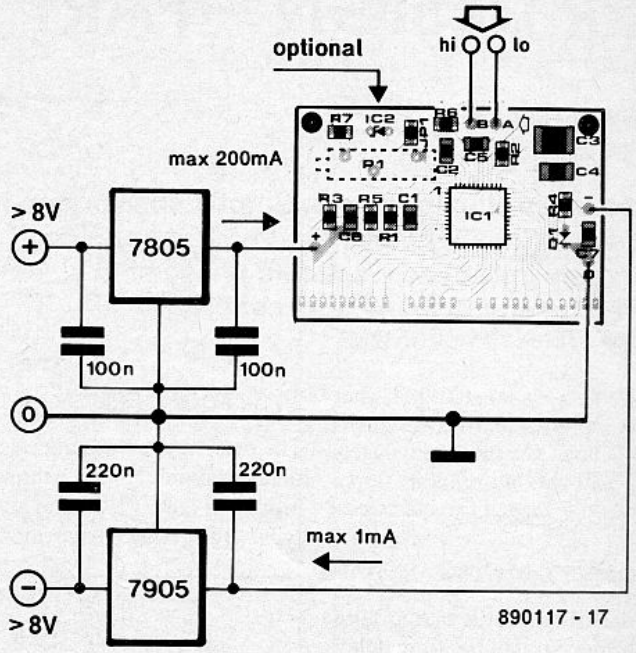
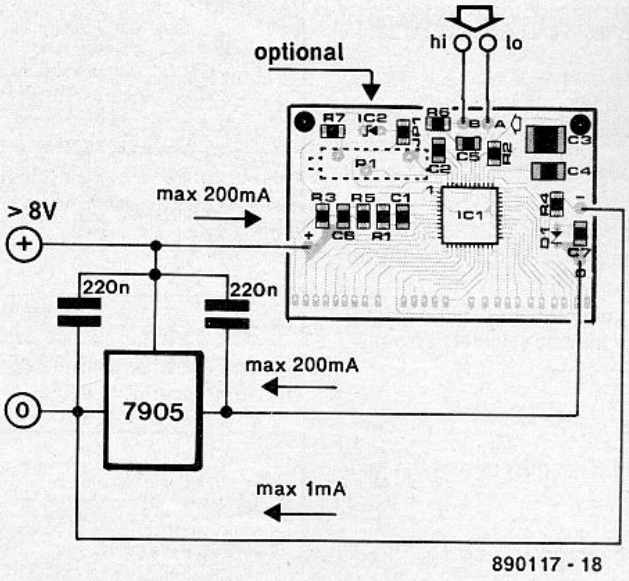


Fig. 5. Track layout and component mounting plan of the printed-circuit board.





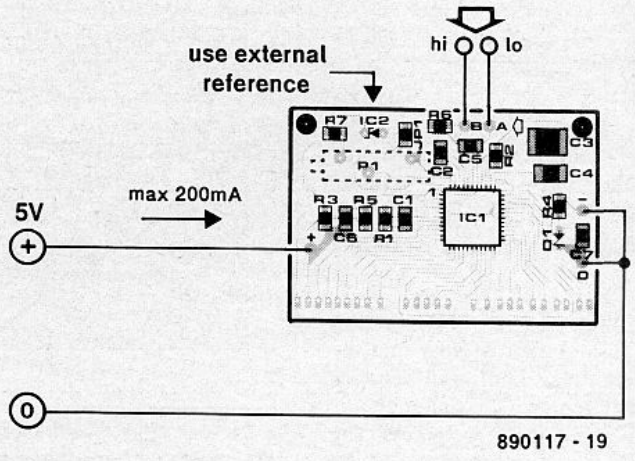


Fig. 6. Power supply configurations.

ment with an internal power supply.

Without displays, the voltmeter draws 1.5 mA at 6 V max. between V+ and ground, and –300 µA at 9 V max. between V– and ground. With displays, the current drawn from the positive supply lies between 70 mA and 200 mA, depending on the number of actuated display segments. The negative supply need not source more than 300 µA, and is not even required in some applications.

The positive supply voltage is limited to prevent the maximum dissipation of the ICL7107 being exceeded.

Figure 6 shows the various supply options. The first drawing, Fig. 6a, shows the most universal solution based on a symmetrical power supply. A 0 Ω or other low-value resistor is fitted in position R_4 (0 Ω resistors are quite common in surface-mount technology), and D_1 is *not* fitted.

The circuit of Fig. 6b may be used if a sufficiently high, regulated, supply voltage is available in the equipment. It should be noted that the input voltage is *not* measured with respect to ground.

Another possibility is shown in Fig. 6c. A single-rail power supply with an output voltage of 12 V or more may be used if the negative supply to IC_1 is limited by fitting D_1 and R_4.

In many cases, a single 5 V supply may be used as shown in Fig. 5d. This application requires the use of the external reference and the fitting of JP_1.

Input voltage and sensitivity

In deciding the range of the input voltage, due account should be taken of the common-mode voltage. Fit jumper JP_1 if the input voltage floats with respect to the display unit.

Non-floating input voltages must lie in the range V–(+1 V) to V+(–0.5 V). When the input voltage is close to V–, the readout, on going negative, may change suddenly to a large value, e.g., –005 instead of 000, –001 etc. This effect may be prevented by shifting the common-mode input voltage towards the middle of the supply voltage.

Set the sensitivity to 200 mV full-scale indication by adjusting P_1 for 100 mV between REF LO and REF HI (the reference voltage is half the full-scale indication). The preset allows small adjustments to be made as required for other sensitivities. If the meter is to be made less sensitive, either an external voltage divider must be fitted, or P_1 must be made larger. The latter solution, however, requires the integrator resistor to be increased accordingly to prevent clipping of the integrator.

PRACTICAL FILTER DESIGN – PART 10

by H. Baggott

This final part of the series discusses all-pass filters. Strictly speaking, these networks are not filters since (ideally) they have zero attenuation at all frequencies. However, they introduce a specific phase shift or time delay that is very useful in many applications.

Although all-pass networks have zero attenuation at all frequencies, they introduce a certain phase shift and act, therefore, as a sort of delay line. They may be used, for instance, to delay a signal in time or to modify the phase behaviour of an other filter.

A look at the complex field of these filters shows that their zeros of network function are mirror images of their poles. Since the poles are always located to the left of the y-axis (because of the required stability of the filter), the zeros must always be to the right of the ordinate. Thus, a first-order network is always a real pole-zero combination.

It is interesting to note that owing to the unique character of an all-pass network the introduced phase shift is always twice the value of that of a conventional filter. The maximum phase shift in a traditional first-order filter is 90°, while that in a first-order all-pass network is 180°.

First-order network

The transfer function of a first-order all-pass network is

$$T(j\omega) = \frac{j\omega - \alpha}{j\omega + \alpha}$$

where α indicates the location of the pole. The absolute value is

$$|T(j\omega)| = \frac{\sqrt{\omega^2 + \alpha^2}}{\sqrt{\omega^2 + \alpha^2}} = 1$$

It is seen that for every frequency the nominator and denominator have the same value. The associated phase shift is

$$\varphi = -2\arctan(\omega/\alpha)$$

The time delay, t, is also important in all-pass filters; it is calculated from

$$t = \frac{d\varphi}{d\omega} = \frac{2\alpha}{\omega^2 + \alpha^2}$$

The time delay in a first-order network is always maximal at very low frequencies and decreases gradually with increasing frequencies. The gradient of the increase depends on the value of α. When α is small, the time delay is large at 0 Hz, but decreases very rapidly with rising frequencies. When α is large, the time delay is relatively small at 0 Hz, but remains fairly constant over a wide range of frequencies.

Second-order network

A second-order filter affords rather more freedom in design, so that the time delay curve can be matched more accurately to the requirement.

The transfer function of this type of network is

$$T(j\omega) = \frac{(j\omega)^2 - j\omega\frac{\omega_r}{Q} + \omega_r^2}{(j\omega)^2 + j\omega\frac{\omega_r}{Q} + \omega_r^2}$$

The absolute value of this function is again 1. The presence of the resonant frequency ω_r is explained by the fact that this function concerns a resonant circuit. This frequency may be calculated from

$$\omega_r = \sqrt{\alpha^2 + \beta^2}$$

in which α and β are the poles of the function.

The Q factor is

$$Q = \omega_r / 2\alpha.$$

The phase shift of a second-order filter is

$$\varphi = -2\arctan\frac{\omega\omega_r}{Q(\omega_r^2 - \omega^2)}$$

while the time delay is calculated from

$$t = \frac{2\omega_r^2(\omega_r^2 + \omega^2)}{Q(\omega^2 - \omega_r^2) + \frac{\omega^2\omega_r^2}{Q}}$$

From these formulas, it is clear that the computations of a second-order network are not all that simple. The time delay is largest at the resonant frequency. The higher the Q, the more pronounced the peak in the time delay characteristic.

Practical passive networks

The design of a first-order delay network is fairly simple. Fig. 52 shows two possibilities: a ladder type and an asymmetric type. Both filters have identical output

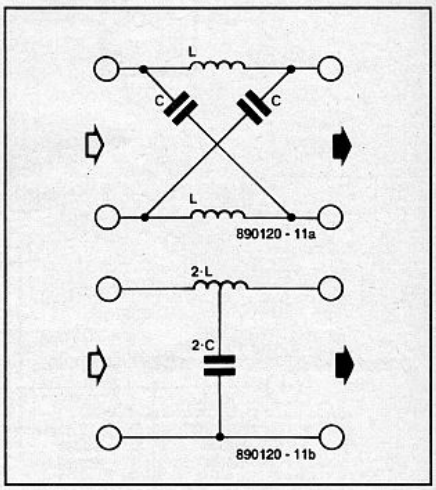


Fig. 52. First-order delay networks: (a) ladder type; (b) asymmetric type.

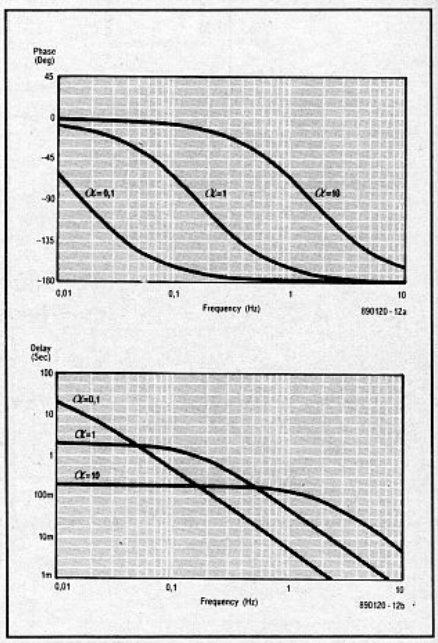


Fig. 53. Time delays of a first-order network at α-values of 0.1, 1.0 and 10 respectively. Fig. 2a shows the phase shift and 2b the time delay.

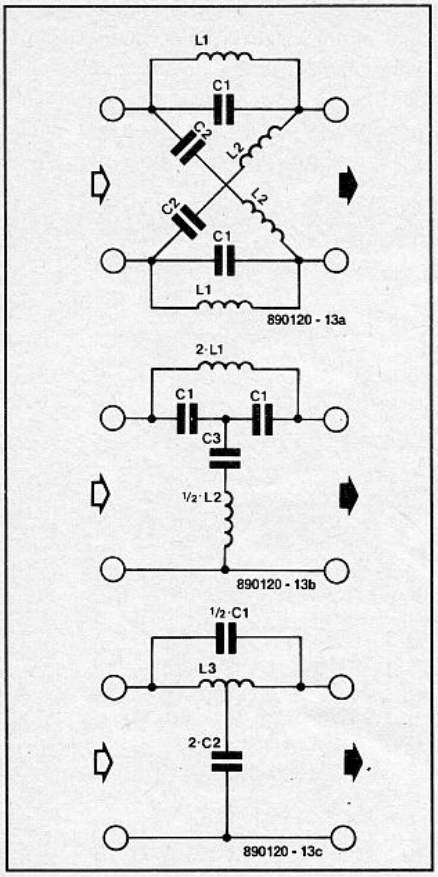


Fig. 54. Circuit diagrams of (a) a second-order ladder network; (b) an unbalanced network with a $Q > 1$; and (c) an unbalanced network with a $Q < 1$

impedances, so that they may be cascaded without any problems. The compuation of such a filter is quite easy:

$$L = R / \alpha$$

$$C = 1/\alpha R$$

where R is the desired output impedance.

The construction of the ladder network should not present any difficulties, but in building an asymmetric type it should be borne in mind that the inductor is centre-tapped: the magnetic coupling factor between the two halves must be 1.

The phase shift and time delay curves given in Fig. 53 are given for a-values of 0.1, 1.0 and 10. Note that the value of a may be chosen freely, dependent, of course, on the desired time delay curve.

Second-order networks are a little more complicated and may be designed for Q-values smaller and greater than 1. Several designs are shown in Fig. 54: in (a) a ladder network; in (b) an unbalanced filter for Q-values greater than 1 and in (c) an unbalanced filter for Q-values smaller than 1. The designs in (a) and (b) use standard components throughout, whereas that in (c) requires a centre-tapped inductor. The values of the various components are calculated as follows.

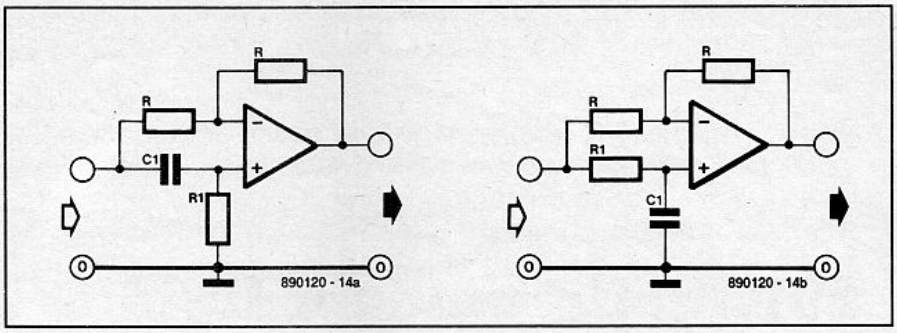


Fig. 55. Designs of active first-order networks: 55a shows a lagging network and 55b a leading one.

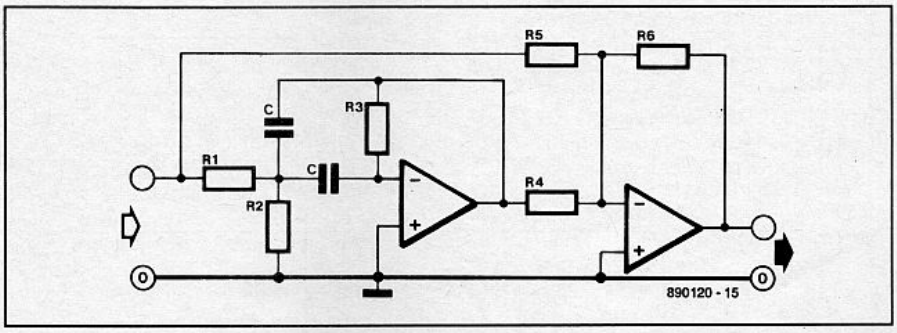


Fig. 56. An active second-order network; this design is suitable for Q-values from 0 to 20.

$$L_1 = \frac{2\alpha R}{\alpha^2 + \beta^2}$$

$$C_1 = \frac{1}{2\alpha R}$$

$$L_2 = \frac{R}{2\alpha}$$

$$C_2 = \frac{2\alpha}{R(\alpha^2 + \beta^2)}$$

$$L_3 = \frac{R}{\alpha} + \frac{4\alpha R}{\alpha^2 + \beta^2}$$

$$C_3 = \frac{4\alpha}{R(\beta^2 - 3\alpha^2)}$$

Active networks

There are even better possibilities of designing active all-pass networks than passive ones, but for clarity's sake they will be restricted to first- and second-order networks.

Good designs of a first-order filter are shown in Fig. 55: (a) is an inductive type and (b) a capacitive type. Furthermore, both circuits invert the input signal (which has nothing to do with the phase shift). Note that not a few people mix up the two circuits under the impression that the one in (b) is a lagging type.

The components in these circuits are calculated as follows.

$$\alpha = \frac{1}{R_1 C_1}$$

$$t_{DC} = 2R_1 C_1$$

$$t = \frac{2R_1 C_1}{(\omega R_1 C_1)^2 + 1}$$

$$\varphi = -2\arctan(\omega R_1 C_1)$$

The design of an active second-order network is shown in Fig. 56. It consists of a band-pass filter and a summing amplifier. The computation of the components is rather more complicated than with the first-order filter. First we assign a value to C and then:

$$R_1 = R_3/2$$

$$R_2 = \frac{R_1}{2Q^2 - 1}$$

$$R_3 = \frac{1}{\alpha C}$$

Next, $R5$ is given a suitable value, say, 22 kΩ. For unity gain, $R6 = R5$, but if amplification is required, $R6$ should be given a larger value.

For Q-values greater than 0.7, $R2$ is not required, while

$$R_1 = R_3/4Q^2$$

and

$$R_4 = R_5 Q^2$$

With the aid of second-order all-pass networks, it is possible to design delay lines that have a constant time delay over a given range of frequencies. The pole positions may be obtained from the tables given earlier in the series. The calculations are fairly complicated and will not be gone into here.

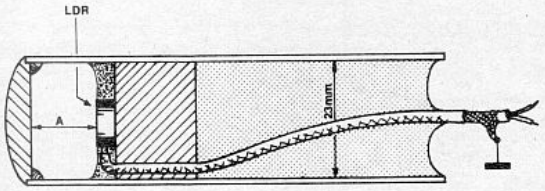
Although it is possible to design delay lines in this manner, the normally specific requirements of these devices make it difficult to to give general examples. The formulas given in this final part must, therefore, suffice.

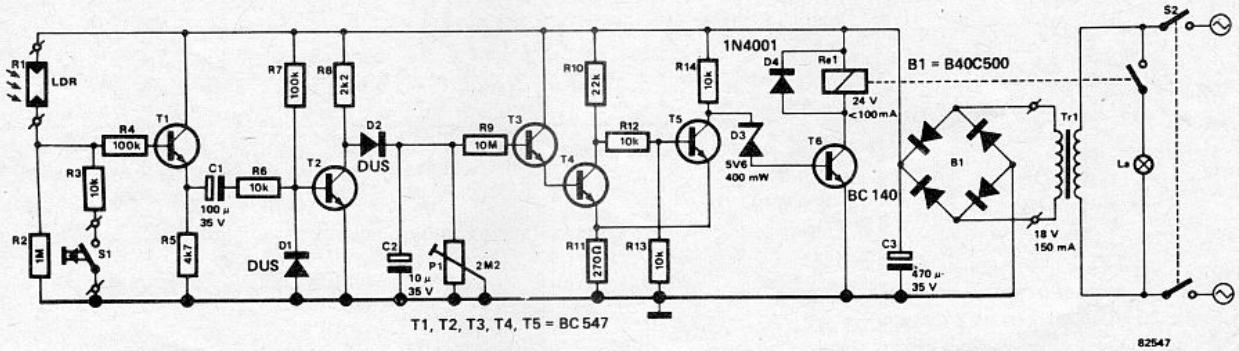
automatic outdoor light

shine a light on your door

J. Bodewes

The purpose of this circuit is to automatically switch on an outside light to illuminate your front door, when a visitor arrives.
The circuit uses a light detecting resistor (LDR) as the sensor. For the circuit to work an external light source such as a lamp post is required.





Needless to say this source needs to be close by. Please remember that the removal or repositioning of lamp posts needs the authority of the local council, so we do not recommend this circuit to anyone who has to extensively remodel the landscape.
The LDR is mounted into a tube, behind a lens, and aimed at the light source. This structure is positioned, so that the person approaching the front door, causes a shadow to fall onto the lens. Do not forget to ensure that the tube containing the LDR is water tight. Immediately the LDR is in shadow, its resistance will increase. This results in T1 applying a negative pulse to T2 via C1 and R6. T2 continues to conduct until this negative pulse arrives. As soon as T2 cuts-off, C2 starts to charge. When the voltage across C2 rises above 2 V, the schmitt-trigger formed by T3, T4, T5 (and their surrounding components), switches on transistor T6. T6 conducts and triggers the relay, which switches on the outside light. The rate at which C2 discharges is adjusted by P1. When the voltage across C2 falls below 1.5 V the schmitt-trigger returns to a quiescent state. T6 will cut-off switching off the relay and therefore the light.
The light will remain on for a maximum of one minute. Longer periods are possible, but then C2 will have to be substituted with a larger capacitor.
Switch S1 and R3 are connected in parallel to R2. S1 can be a make/break contact mounted on the front door. When the door is opened the light will switch on, going out immediately it is shut.
In order for the circuit to work effectively, the tube containing the LDR (and lens), must be positioned, relative to the light source, so that the voltage measured at the junction of R1, R2, is not less than 3 V, and not more than 20 V.

INTRUDER ALARM

In today's society, it makes good sense to provide some form of intruder alarm system in the home, if for no other reason than the family's peace of mind. Effective, reliable and simple to control, the intruder alarm system described in this month's article uses readily available low-cost components only.

E. Chicken, MBE, BSc, MSc, CEng, FIEE

Apart from its low current demand from a battery during non-alarm conditions, the alarm is also noteworthy for its system-test bleep on switching on and on leaving the house, its pulse drive of the external sounder to economize on battery power, and automatic time-out of the internal and external sounder to minimize social disturbance.

The block diagram given in Fig. 1 shows the various stages of the circuit, their interconnections and related signal routes. The way in which the stages interact in detail is explained below.

Circuit description

Power supply

As shown in the circuit diagram of Fig. 2, the alarm is powered by a small 12 V rechargeable battery that is trickle-charged by a mains adapter with d.c. output. In the quiescent condition, the current drain from the battery is less than 1 mA. Current consumption in the actuated condition is virtually that of the external sounders alone. Charging current for the rechargeable battery is limited to about 15 mA by R_7 in series with LED D_4, which, mounted on to the front-panel of the enclosure, serves as a charging indicator. The output voltage of the mains adapter must be measured and the value of R_7 chosen such that the maximum LED current of about 20 mA is not exceeded.

On/off control

Control of the alarm system is effected by a single-pole ON/OFF switch, S_1. Actually, the circuit is never switched off completely as long as the battery is connected, but the current drawn with the switch in the OFF position is negligible.

Closing S_1 to switch the system off connects R_2 to the negative supply rail, causing T_1 to conduct. Diode D_1 is forward-biased, and the resultant voltage drop of about 0.6 V maintains conduction of T_1 in the event of a reduction of the supply voltage. That conduction in turn maintains the off condition of the system, and so minimizes the possibility of false alarms.

When T_1 is switched on, D_3 ceases to conduct so that C_1 is charged to the supply voltage via R_5 and R_6. For convenience, low voltages from 0 to, say, +2 V will be referred to as logic 0, and the higher +12 V supply rail voltage as logic 1.

This voltage on C_1 forms a logic 1 that is inverted by NAND gate N_1 to present a 0 to one of the two control inputs of the bistable formed by N_2 and N_3. So long as pin 6 of N_2 remains at 0, the output of the bistable, pin 4 of N_2, is held at 1 to prevent the alarm sounders being actuated.

Switching the system off simultaneously takes the RESET pins of timers IC_2 and IC_3 low, which prevents the timers being inadvertently triggered into a false alarm sequence. As long as the system is switched off, D_2 is forward-biased via T_1 and R_{14}.

When the system is switched on, switch S_1 is in fact opened, so that T_1 ceases to conduct. This causes the collector voltage to drop to practically 0 V via R_4, so that D_3 is forward-biased via R_5 and R_4. As a result, C_3 discharges slowly via R_6, D_3 and R_4. The lowest voltage on C_3 is reached in about 15 seconds, determined by time constant $C_1(R_4+R_6)$.

The final voltage on C_1 as determined

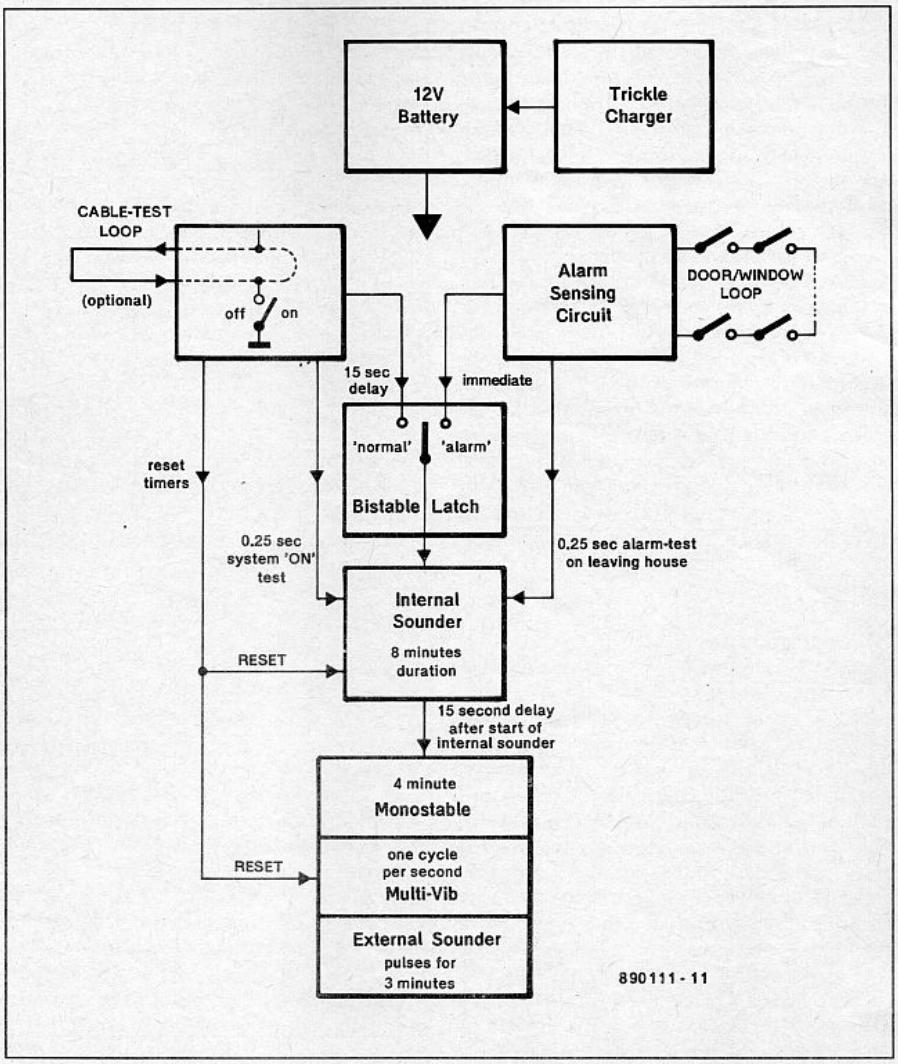


Fig. 1. Block schematic diagram showing the general structure of the intruder alarm.

by potential divider R_5-R_4 is about one tenth of the supply voltage, plus the forward drop of D_4. In total, this makes about +1.8 V, which represents a logic 0. The resultant logic 1 at the output of NAND gate N_1 causes bistable N_2-N_3 to toggle 15 seconds after switching the system on. The logic state at output pin 4 of the bistable becomes 1, and can be changed to 0 according to the logic level applied to the control input terminal, pin 1 of N_3.

Alarm sensing

When all doors and windows protected by the detector loop are closed, and assuming that the detector switches are of the normally-closed type, R_{13} is connected to the negative supply rail, causing T_2 to conduct via R_{12}-D_7-R_{13}. The function of D_7 is similar to that of D_1 as discussed earlier. With all detector switches closed and the loop unbroken, D_6 conducts via T_2 and R_{14}. Diode D_5 does not conduct because its cathode is connected to the positive supply rail via T_2, as is its anode via R_8.

Capacitor C_3 supplies a logic 1 to the second input of bistable N_2-N_3 after it has been charged via R_8 and R_9. The two logic 1s at the bistable inputs maintain a 1 at the output, pin 4 of N_2. As stated earlier, this 1 inhibits the sounding of an alarm.

Breaking the detector loop disconnects R_{13} from the negative supply rail, causing T_2 to stop conducting. Its collector potential drops to nearly 0 V, so that D_5 is forward-biased via R_8 and R_{10}. As a result, C_3 discharges in about 0.5 s via R_5, D_5 and R_{10}, its terminal voltage dropping to about +1.8 V, which represents a 0.

The 0.5 s delay produced by C_3-(R_9+R_{10}) assists in the prevention of false alarms by interference spikes and other transients in the loop circuit such as by doors shaking in the wind.

Control terminal pin 1 of the bistable accordingly changes from 1 to 0, so that the level at the output terminal changes from 1 to 0, where it will remain latched in the absence of an alarm condition until the other control terminal, pin 6 of N_2, changes state, i.e., until the system is switched off. The condition necessary for the generation of alarm signals is a 0 at the output of the bistable.

Sounder timing

The alarm system has provision for two sounders, one low-power internal alarm such as an active piezo-electric buzzer, and one high-volume external alarm such as a 12 V bell.

The circuit automatically switches off each of the alarm sounders after a reasonable period of time: 4 minutes for the external sounder, and 8 minutes for the internal sounder. The individual timing circuits may be altered, however, to suit personal preference.

Low-power CMOS timers Type 555 (IC_2) and 556 (IC_3) are used in the interest of battery economy. When the circuit is switched on, the timers are simultaneously released from the reset condition because their pins 4 are taken logic high.

Internal sounder

While the system is on, any break in the detector loop, such as by a protected door or window opening for longer than 0.5 s, initiates operation of the internal sounder. When the loop is broken, C_6 passes the 1-to-0 transition at the output of the bistable to pin 2 of IC_2, which is triggered into monostable operation for a period of about 8 minutes. Network C_6-R_{16} forms a differentiator to sharpen the trigger pulse.

On entering the premises, residents have about 15 s to switch off the system before the monostable switches on the internal sounder. Prior to the arrival of the trigger pulse at pin 2 of MMV IC_2, its output, pin 3, is normally at 0. This level keeps T_4 off via base resistor R_{19}. Immediately upon the arrival of the negative-going trigger pulse at pin 2 of IC_2, its output rises from 0 to 1. This level is maintained for about 8 minutes as determined by C_8-R_{17}. Transistor T_4 is switched on, and actuates the internal sounder in its collector circuit. When the 8-minute period has lapsed, the low level at pin 3 of IC_2 causes the internal sounder to be turned off by T_4.

For convenience of testing during the construction and installation stages, LED D_9 provides a visual indication of circuit operation without the internal sounder being connected. If actuated, the internal sounder is switched off simultaneously with the system.

External sounder

The operation of the external sounder circuit is slightly different from that of the

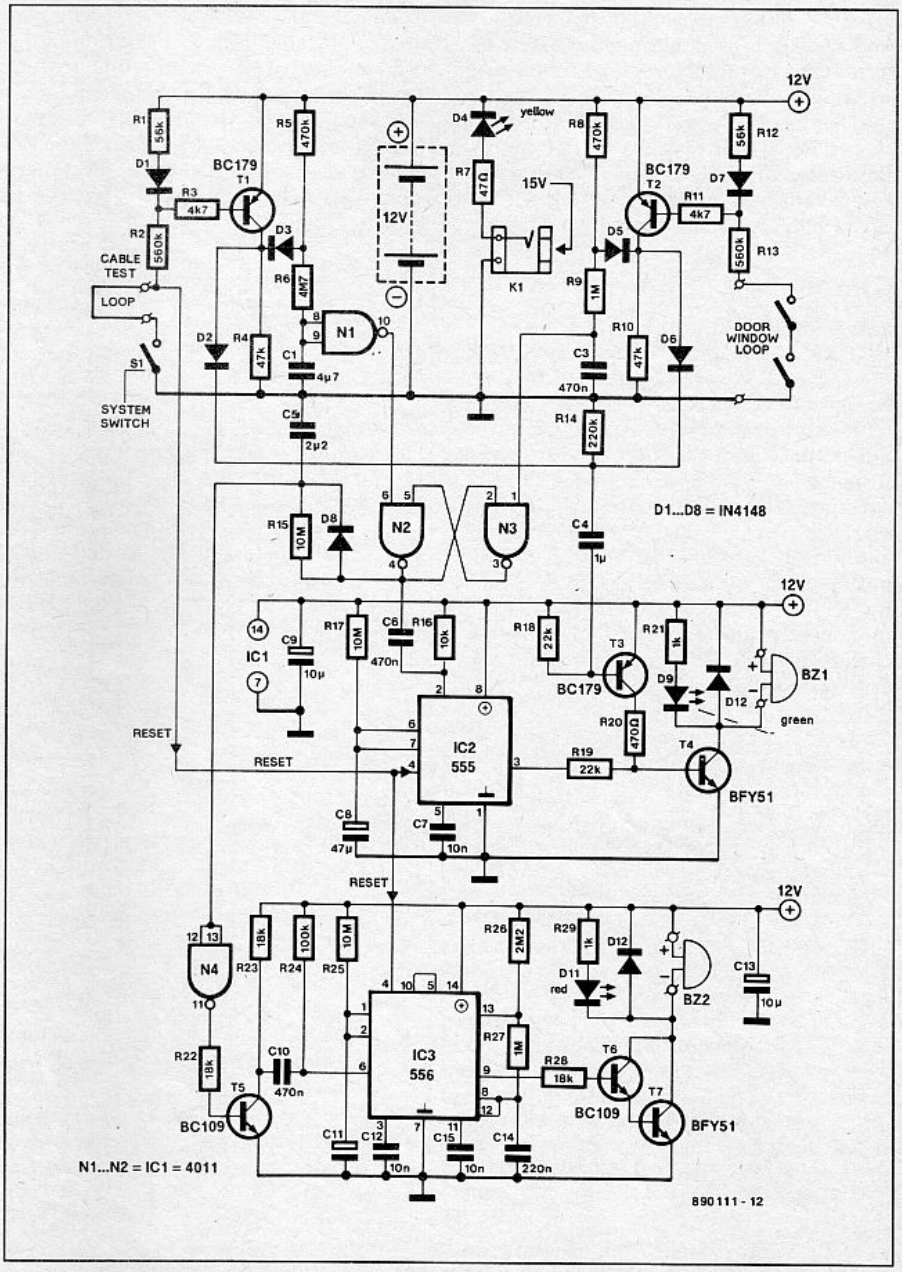


Fig. 2. Circuit diagram of the intruder alarm. Note that the timers, IC2 and IC3, must be low-power versions to ensure minimum current drain from the battery.

internal sounder. Assuming that the system is switched on and the detector loop not yet broken, the output of bistable N_2-N_3 is at 1. Capacitor C_5 charges rapidly via D_8, until its terminal voltage is also at 1. Subsequently, T_5 is turned off by the 0 supplied by inverter N_4. Timer IC_3 is not yet triggered into action, so its output terminal, pin 9, is at 0. Hence, darlington transistor T_6-T_7 is kept off in the absence of an alarm signal — external sounder Bz_2 is not actuated.

Circuit IC_3, a CMOS Type 556, contains two timers Type 555. Pin 4 of the first 555 in the chip is held logic high via R_2-D_1-R_1, so the timer is ready to be triggered. The instant the detector loop is broken, the 1-to-0 pulse transition at the output of bistable N_2-N_3 causes D_8 to block, enabling C_5 to discharge through R_{15}. The time constant formed by these two components introduces a delay of about 15 s in the transition from 1 to 0 at the input to inverter N_4. After this delay, the resultant transition from 0 to 1 at the base of T_5 causes the transistor to conduct. The collector voltage of T_5 drops from 1 to 0, and the negative-going pulse edge is differentiated by C_{10}-$R_{24}$to be passed as a sharpened trigger pulse to pin 6 of dual timer IC_3. The first timer in IC_3 is configured as a monostable with a 4-minute time period, the output of which is used to control the second timer circuit, which is configured as an astable multivibrator (AMV). This circuit can produce its 1-s on/off pulse rate only during the 4-minute period of operation set by C_{11}-R_{25} for the preceding monostable in the IC. The time period, t, in seconds can be calculated from

$$t = 1.1(C_{11}R_{25})$$

Output pin 5 of the first timer is normally at 0 until the arrival of an input trigger pulse, whereupon the output state changes abruptly from 0 to 1. Pin 5 is wired to the reset input, pin 10, of the second timer in the IC package. When taken high, this pin enables the AMV to oscillate at a rate of 1 Hz during the 4-minute period defined by the first timer. The period (in seconds) of the oscillator signal is calculated from

$$t = 0.7C_{14}(R_{26} + 2R_{27})$$

The square-wave oscillator signal drives darlington transistor pair T_6-T_7, so that the external sounder, Bz_2, is switched on and off at a rate of about 1 s until the 4-minute monostable period has lapsed. As with the internal sounder, a visual indication of external alarm activity is provided. Diode D_{12} protects T_7 from transient voltage spikes generated as the current through the inductance formed by Bz_2 is interrupted. Capacitors C_{12} and C_{15} are for decoupling and do not form part of the timing circuits.

System assurance bleep

Provision has been made for a system assurance bleep to indicate that the system is functional, prior to the resident's departure from the premises. Two assurance bleeps are generated: one before the end of the 15-s switch-on delay at the instant of switch-on, and one as the exit door is opened for departure.

While the system is switched off, C_4 has no voltage on it because T_1 conducts. Following switch-on, the 15-s delay before the system becomes 'live' allows time for the injection of a short control signal direct to the internal sounder control transistor, T_4, bypassing timer IC_2.

When the circuit is switched on, T_2 and D_2 become non-conductive so that C_4 is allowed to charge via R_{18} and R_{14} in about 0.25 s, which in effect momentarily causes the base of T_3 to be taken low via R_{14}. The upshot is that both T_3 and T_4 conduct just long enough to enable the internal sounder to produce a short bleep.

The same process occurs with T_2 and D_6 which, like D_2, is connected to the junction of C_4 and R_{14}, except that in this case the charging of C_4 is initiated by the breaking of the detector loop when a protected door or window is opened.

Construction

A convenient and low-cost method of construction is to use readily available copper SRBP stripboard with 0.1-inch hole spacing. The use of sockets for the ICs is recommended, but the layout of components is not at all critical.

Inter-component wiring is by thin insulated wire. If stranded wire is used, care must be taken to avoid unintended contacts by loose unsoldered strands.

The external wires are connected to terminal posts on the board. The two alarm-test LEDs are purposely located on the board for visual access during testing.

A separate box may be required to accommodate the battery, and possibly the mains adapter.

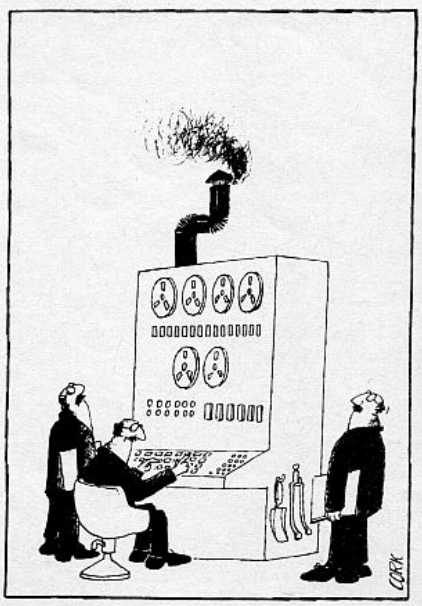
The ON/OFF switch is either a key-operated type, or a cheaper standard on/off miniature toggle switch. A reasonable compromise as regards safety might be to use a standard SPST toggle switch, and to conceal it from view either complete with the electronic assembly, or in a small separate enclosure.

Further practical considerations

The door and window switches are magnetically operated types that have the advantage of not drawing current from the battery. Constructors wishing to include a motion detector of some sort in the loop must bear in mind that such a device may well draw 20 mA or more whether actuated or not, which would have to be taken into consideration when choosing the battery and the associated charger. Also, the motion detector requires a separate cable to carry its supply voltage. One approach might be to replace the single-pole on/off switch with a double-pole (DPDT) type, the other pole of which is used to connect the +12 V to the motion detector only while the system is switched on, assuming that the battery is being recharged during the off condition.

The cable-test loop shown in the circuit diagram provides an indication in the event of the loop having been tampered with, for instance, cut by a prospective intruder who plans a return visit while the house is unoccupied. It would need to be a separate pair but within a two-pair cable; if both pairs are cut simultaneously, the system would be switched on, and the detector loop to be broken, so that the alarm is set off immediately. If such a situation is thought unlikely, the cable-test loop may be omitted, and a substitute wire link installed on the board. The detector loop would then need to be twin PVC insulated cable of, say, 7×0.2 mm running from the board to each detector in turn, and back to the board via the unbroken wire of the pair.

The choice of the external sounder is entirely up to the constructor, but care should be taken not to overload the transistor driver or the battery. The author used a weatherproofed sounder giving a choice of continuous or warbling tone at a sound level of 107 dBA for only 20 mA of current drain from the 12 V battery. It is standard practice to enclose the external sounder in a weatherproof enclosure, installed high up on the wall out of easy reach, and with its supply cable hidden behind the box as an anti-tamper precaution.



PROTECTING ASYNCHRONOUS MOTORS

by Mehrdad Rostami, University of Tehran, Iran

The circuit described here was designed for protecting heavy-duty asynchronous motors during the start-up period. As is well-known, without protection such motors may easily get damaged by poor starting. The circuit may also be used for other applications where a trip circuit needs to be triggered, such as, for instance, in the monitoring of liquid levels.

Every motor has a time-speed characteristic that shows how, or otherwise, it starts and reaches its normal speed. A number of such curves are illustrated in Fig. 1. If the characteristic of a particular motor is similar to the lower (bold) one, any attempt at starting the motor should be stopped immediately and the motor in-spected thoroughly. The dashed curve in-dicates the lower limits of acceptable motor performance, while the upper curve shows normal values of a properly functioning motor.

Circuit description

The circuit diagram in Fig. 4 consists of five identifiable blocks: (1) oscillator and time base—IC4, IC5 and IC6; (2) address unit and memory—IC7, IC8 and IC9; (3) shaft pulse receiver and counter—IC14 and IC15; (4)comparator—IC12 and IC13; and (5) automatic stop unit—FF1 and FF2.

The input to the circuit consists of pulses generated by a rotary encoder comprising an opto-coupler and perforated man-made fibre disk fitted securely on to the shaft of the motor as shown in Fig. 2. The pulses generated by the opto-coupler are applied to receiver/counter IC14 and then to counter IC15.

The 555 oscillator,. IC4, generates 50 Hz pulses that are divided by 5 in IC5. The output of this IC is taken to switch S1 and also applied to a second :5 divider, IC6.

The output of either divider may be selected by S1 and from there applied to cascaded circuits IC9 and IC10. The output of IC10 is used to reset the shaft pulse counters, IC14 and IC15, at the end of each period of 0.5 s or 0.1 s depending on the setting of S1, and also to clock the address unit, IC7 and IC8.

The EPROM must be loaded with the data of the appropriate motor curve. If, for instyance, the rotary encoder is supposed to send eight pulses in the first 0.5 s period (S1 set to 2 Hz)—which, of course, depends not only on the rotary speed of the shaft of the motor, but also on the number of perforations in the disk—the first memory cell of IC11 must be loaded with 00001000. The number of pulses is determined from the timing diagram of the relevant motor: a typical ttime vs rotary speed characteristic is shown in Fig. 3.

Similarly, if the pulse generator is supposed to send 12 pulses in the second 0.5 s period (S1 set to 2Hz), the second memory cell of the EPROM must be loaded with 00001100. This process must be repeated for each subsequent 0.5 s period (up to a total of 20 seconds, when a properly working motor will have started).

The outputs of the EPROM and the shaft pulse counters are applied to two Type 7485 comparators, IC12 and IC13.

At the end of each 0.5 s period, IC9 generates a pulse that is used to drive one of the inputs of AND gate N2 high. When the level at pin 7 of comparator IC13 is also high, the second input of N2 goes high.also. This results in the output of this gate becoming a logic 1, which is applied tots of AND gate N3.

The second input of N3 is supplied by AUTOSTOP unit FF1, a D-type bistable. This bistable is reset by AND gate N1 when address 00010100 is applied to the EPROM. Its $\overline{Q}$ output then goes high, which causes the second input, and thus the output, of gate N3 to go high. This causes a second D-type bistable, FF2, to be set. When that happens, the coil of a trip device in the starting circuit of the motor is energized so that the starting circuit is broken.

Circuits IC12 and IC13 compare the data input from the EPROM with that from counters IC14 and IC15. If these data streams are identical, pin 7 of IC13 re-mains low, preventing the operation of the automatic stop unit.

Schmitt triggers N4, N5 and N6 form an auto reset circuit for setting/resetting the bistables and returning the counters to their original state.

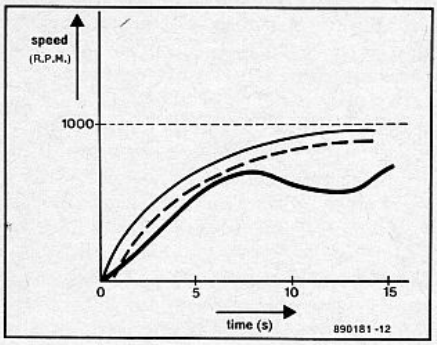


Fig. 1. Time-speed characteristics of a an asynchronous motor. The lower (bold) curve indicates a defect motor; the dashed curve indicates the lower limit of acceptable performance; and the upper curve is typical for a properly functioning motor.

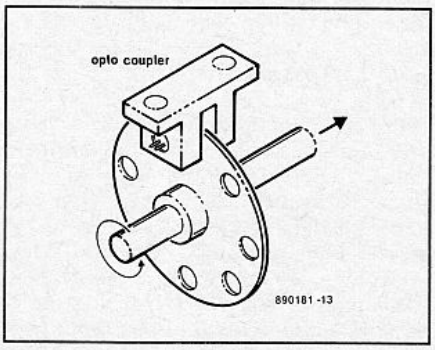


Fig. 2. The rotary encoder consists of an opto-coupler and a perforated man-made fibre disk fitted on to the shaft of the motor

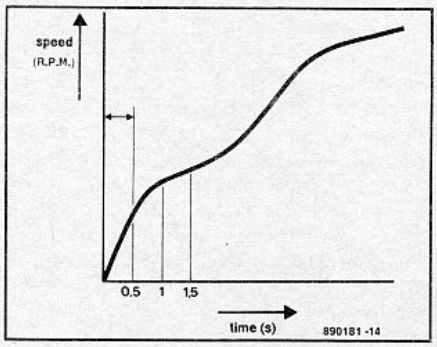


Fig. 3. Typical time vs rotary speed diagram of an asynchronous motor. A properly working motor should start within 20 seconds.

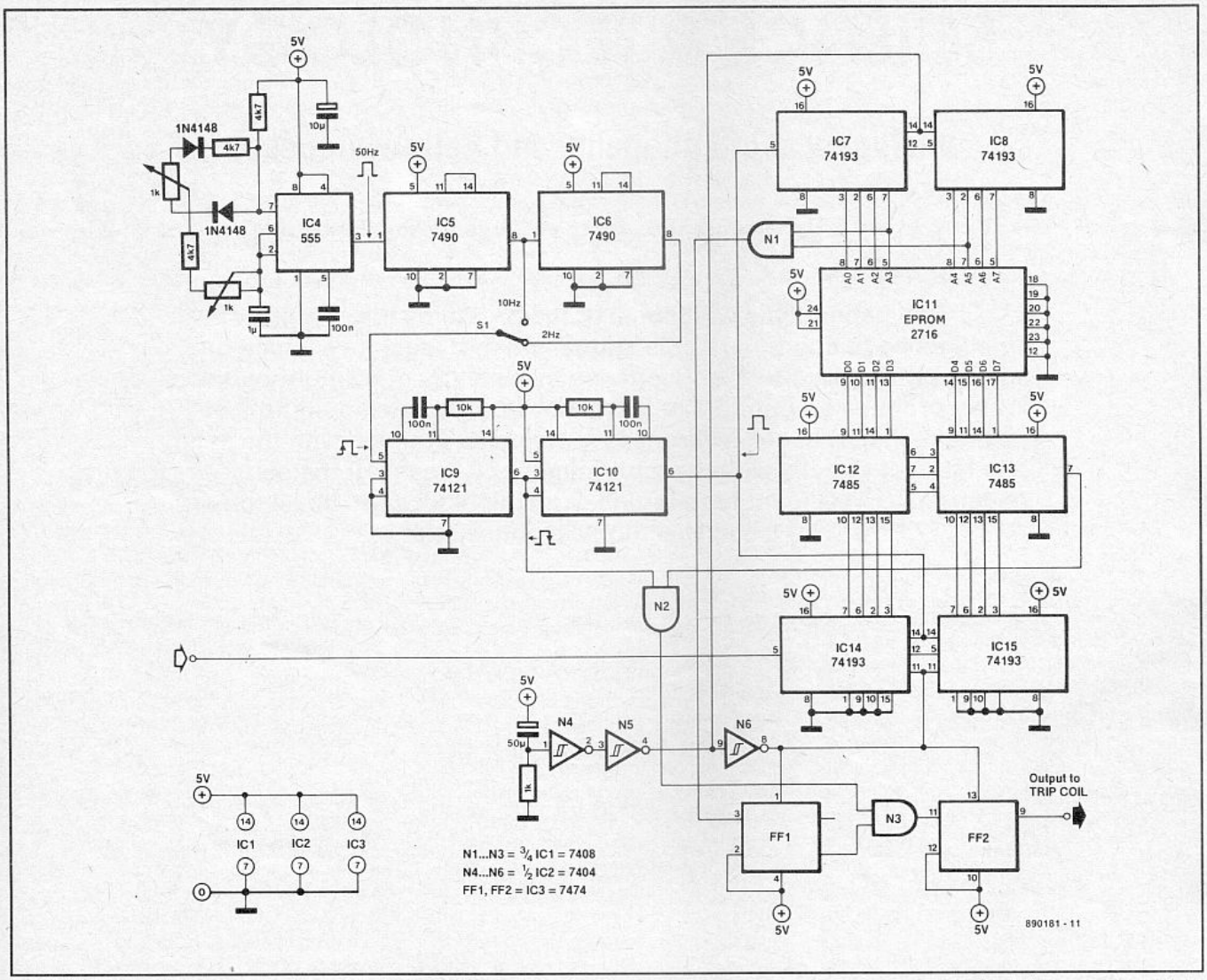


Fig. 4. Circuit diagram of the protection unit.

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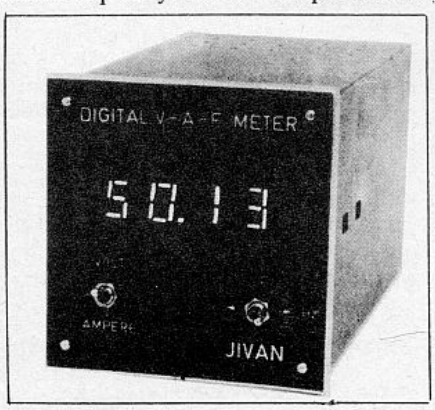

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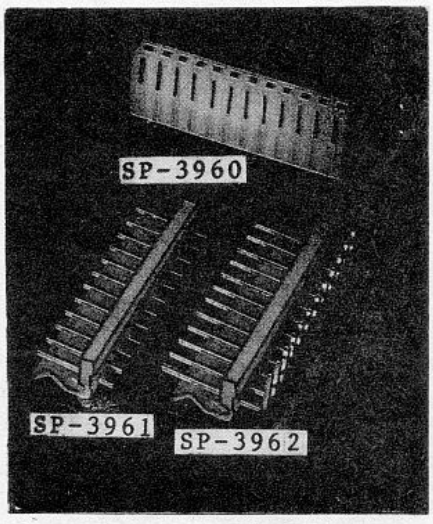

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SCIENCE & TECHNOLOGY

Intelligence, Intentionality and Self Awareness

by Dr T. Farrimond, University of Waikato, New Zealand

This paper deals with some of the problems in ascribing intelligence to computers. It is suggested that machines which only process the symbols of language are not intelligent even though they may produce an output similar to that from an intelligent human. It is maintained that self awareness in humans, coupled with the ability to interact directly with the environment by means of the senses, is central to intelligent functioning, which includes the development of a social/ecological conscience.

In his article "Artificial Intelligence", M. Seymour[1] provides an interesting and informative account of some of the problems met by computer designers in attempting to produce machines that exhibit artificial intelligence. The article discusses arguments for and against what constitutes artificial intelligence including the existence or otherwise of intentionality (Searle, 1984)[2]. The present paper examines some of the concepts from the point of view of a psychologist, who was a student at Manchester when Alan Turing was working on the theoretical aspects of information processing. The power of electronic devices has increased enormously since that time, but perhaps there has not been a similar growth in defining the terminology used to describe computer activities and brain activities.

At the simplest level there has been revival of anthropomorphism, a condemnatory appellation feared by biologists accused of reading human characteristics into the behaviour pattern of lower animals. However, equally imprecise use of language is exemplified by phrases such as 'computers talking to each other'. This is largely a matter of economy in the use of words, since it is easier to use concepts already in existence than to invent new ones, but there are dangers in over-extending the concepts to include things that are not justifiable. The problem is that with terms such as intentionality it is difficult to provide a definition that does not also include or imply the term intention, which then also has to be defined. In describing a spiral staircase, it is easier to make a visual representation by drawing one (or to wave one's arm to illustrate the concept) than it is to describe it verbally. If this is true for a concrete example such as this, then for abstract concepts the difficulties involved in using words to define them are enormous.

Is the term intentionality sufficient to cover those things the brain does that are different from a computer? How does one recognize intentionality? Can intentionality be proven and is it important to do so? The concept of intentionality is essential in dealing with human affairs, particularly when legal disputes arise and require resolution. We resort to a court of law where proof of intention may well determine the outcome of a case. Did the accused know what she was doing when she set fire to her husband's bed? Evidence may be produced to prove diminished responsibility; a person may be described as intellectually sub-normal and so not accountable for his/her actions. The implications in this case may be that the accused did not properly understand that the outcome of the action might be injury or death. Similar incapacity may also be ascribed to a person under the influence of drugs or suffering from some mental disorder. The question of responsibility is the key to determining whether the sentence should be 10 years or alternatively some form of medical treatment. In each case what is examined are the following.

(a) Could the individual predict the outcome of the act that caused the accident (is there an ability to follow a logical sequence of events on a probabilistic basis to a conclusion or variety of possible conclusions)?

(b) Did the person **intend** to set in train the causal events that resulted in harm? If a person accidentally backs into a lever that releases a winch carrying a load of iron, causing it to fall and kill someone it is not the ability to understand the causal relationships that determines guilt – but whether there was **intention** to do harm. In this example there was not.

(c) Was there an **awareness** on the part of the accused that he or she was carrying out the action?

Point (c) is relevant, for example, in the case of hypnosis. A woman under hypnosis may be persuaded to role-play the part of someone in authority and perform an act not normally acceptable to her simply because she regarded herself as another person during the period of hypnosis. In this case a **causal** sequence of events has occurred in which there is **intention** on the part of the subject to carry out an act, but because self awareness is absent, the individual would not be regarded as culpable in law. Even though her behaviour incorporates the two elements usually considered necessary for intelligent behaviour, i.e., it exhibits appreciation of **causality** and also **intentionality**, she is not seen as responsible for her behaviour. It may be argued that intelligent human behaviour involves these elements – causality, intention and self awareness and for a computer to be regarded as intelligent it also should exhibit the same properties.

It is this point of self awareness which I contend is different from intentionality and is possibly the central issue in determining whether behaviour is intelligent or not. It is assumed that the use of the term intelligence is a reference to human mental and behavioural processes since these are the only points of reference we have for what we mean by intelligent behaviour.

External behaviour

Would a machine designed to look and move exactly like a human being so that it would

be accepted at a barbecue (or even a social function!) really be intelligent? One could forgive the hostess for assuming that it is, since from the outside the machine does all the things normally expected of a human: it speaks, moves about, listens attentively and even laughs in the appropriate places.

It is tempting to argue that it is only the behaviour of the machine that is important, i.e., outside appearances and behaviour are all that matter. If these are indistinguishable from human behaviour, the machine should be regarded as human, and therefore intelligent. Indeed, this may be the effect on the hostess until it is demonstrated to her that a group of electronics enthusiasts have constructed the machine and are operating it remotely: one controlling locomotion, another speech, and so on. Thereafter, the hostess would no longer accept as fact that because someone (thing) exhibits intelligent human behaviour it is genuinely intelligent. This emphasizes the problem that without further knowledge about the controlling mechanisms it is difficult to prove that a behaviour pattern is intelligent or not. But is is obviously not safe to infer intelligence on behaviour alone. In the example given, the intelligence is elsewhere and is external to the machine.

A distinction should be made between the analogous behaviour and identical behaviour. Herein lies the distinction between machines at present and humans. The behaviour of a machine may be analogous to that of a human without necessarily being identical.

Although it may be the expressed aim of engineers to produce intelligent machines, it is doubtful whether they would want them to be intelligent in the human sense, since they may no longer wish to co-operate with the inventor – and may prefer to go on strike. Certainly, any organism (biological or mechanical) with self awareness would also be aware of its rights as a thinking being and its utility as a tool (that is, slave) would be reduced. An interesting prospect also opens up in the area of culpability for mistakes. If a machine is regarded as culpable and it transgresses, what should its punishment be?

Absence of need for programming

It has been envisaged that one day it may be possible to build a machine that can think, that is, need not be programmed to perform its functions. This statement as it stands perhaps needs elaboration before its implications can be considered. If the term 'thinks' refers to performing certain analytical functions, the similarity to human thinking is restricted to one level of activity. It would be necessary to define the term in other ways if it were to include intentionality and self awareness. The presence of one level of functioning does not automatically mean that the other levels are present. Terms such as intelligence, cognition, perception, etc., have evolved from attempts to categorize (by using symbols) certain aspects of human behaviour. The words are not specific but incorporate implied connections with all other aspects of human mental activity.

Gregory in his book *The Intelligent Eye* emphasizes the relationships that exist between the eye and the brain. The eye is an extension of the brain in a psychological as well as in an anatomical sense. The unitary nature of perception, cognition, intelligence, etc., makes it difficult to talk about simply one aspect of human behaviour without automatically including all the others. It would make little sense to examine human cognition without at the same time considering intelligence, memory store, and perceptual abilities, for cognition depends upon them all. Also, an individual's cognitive state is constantly changing, not only from new experiences, but by re-analysis of stored information from within, where models exist of the world (imagery) available to the individual for the process of thinking, researching and creating.

The capacity of the brain

In an attempt to duplicate the equivalent of a neural net system as found in the brain, experimenters have constructed electronic networks with a large number of interconnections. However, the human brain is not simply a neural network. The complex of 10 billion (10^9) interconnected brain cells confers only one part of the brain's processing power, for along with nerve cells there are over five times as many smaller **glia** cells. All these cells have numerous fine branches extending from them to form interconnections with other nerve cells: some individual cells may have several hundred connections, others several thousand and in the cerebellum certain cells may have one hundred thousand connections. The number of interconnections has been estimated to be of the order of 50 trillion (50×10^{18}). Nor is this the whole story. Memory storage in the brain seems to involve changes in the protein molecules associated with the nerve cells. Additionally, certain glia cells are not fixed relative to adjacent brain cells but may move into active areas of the brain, thus modifying the brain's structure in response to incoming stimuli. Glia cells, unlike larger brain cells, have the ability to subdivide as well as move, so that their number and distribution may change depending upon the activities of the brain.

What makes the human brain so interesting is that the owner is, to some extent, able to observe his/her mental states and decide upon a course of action thereby. This course of action is not unchangeable but open to modification. Even though humans have characteristic patterns of behaviour by which they may be recognized as individuals, it is still possible for a person to examine past behaviours and bring about a change for no other reason than that a change is regarded as desirable. This capacity makes human behaviour notoriously unpredictable even when we know a person very well. This is not the same as Turing's[3] suggested incorporation into a machine of a 'random element' consisting of a random number series which produces changes in the behaviour of the machine. In human terms, such a random element would be more characteristic of psychotic human behaviour, where there may be an absence of awareness of the behaviour on the part of the psychotic and little appreciation of its effect upon others. Self awareness is the ability that gives humans the capacity for controlled variability and includes intentionality and appreciation of causality.

The origin of self awareness

Although it is difficult to be specific on this point since we no longer remember what we experienced in the few months preceding our birth, it is possible to conjecture that our sense of 'self' begins to develop quite some time before birth. Acoustic images of developing foetuses show them yawning, moving, sucking their thumbs, etc., indicating the presence of kinaesthetic and tactile awareness. There seems little doubt that, like Tristram Shandy, we are responding to, and becoming aware of, our own bodies in relation to the environment surrounding us. In other words, we are developing self awareness.

Self awareness includes the development of body image, that is, the knowledge that our bodies are unique, yielding sensations that are related to each other. Visual and tactile investigation by a young baby of its body yields a complex integrated pattern of sensations that, in conjunction with kinaesthetic feedback from muscles and joints, gives the child a sense of personal identity that is different from all other objects in the environment: other objects are regarded as external to the self. To achieve this development of body image, the child must **move** relative to the environment, so that it experiences variations in the size of objects as distance changes and variations in shape as viewing angles change. Both the distance information gathering senses of vision and hearing are co-ordinated with the body senses of touch, pressure, pain, temperature and kinaesthetic feedback, to produce an organized pattern of information resulting in

self awareness.

The experiment by Held and Hein (1963)[4] with kittens indicates that visual ability requires integration of changing visual patterns (brought about by moving in the environment) with simultaneous stimulation of body senses and locomotor activity on the part of the animal. In this experiment, two kittens were kept in the dark until their eyes opened. Then they were placed at opposite ends of a bar pivoted at its centre so that it could rotate. Only one kitten, 'A', had its feet on the floor and so could walk around in a circle. It could also turn around on the spot because of the design of the apparatus. The other kitten, 'B', stood in a basket that prevented foot contact with the floor but, because of an interlinking system of gears and chains, it was moved whenever kitten A moved: it could not initiate movement itself. Both kittens therefore received similar visual stimulation. When the kittens were released after 30 hours, kitten A could make normal visual responses, such as avoiding a cliff, blinking to avoid an object approaching the eye and avoid obstacles. Kitten B was unable to do any of these tasks and only learned to see when allowed to walk.

It has been stated that "artifical intelligence is the study of computer programs" (Boden)[5]. In humans, it would perhaps be more accurate to say that intelligence is a function of the **body** and equates with sensitvity to external and internal stimuli. The new born baby has no program derived from outside sources, although it shows responses: exhibiting sensitivity to (and reflex movements away from) painful stimuli. Light and sound convey little meaning at this stage; learning is initially related to the body senses. For example, if the baby makes random movements of the hands, it may strike the side of the cot and receive a sensation in that hand. If the baby strikes its own face, it receives a sensation in the face as well as in the hand. This is a unique experience different from all other contacts with the world outside the individual's body. The baby soon associates these sensory inputs with the internally derived sensations from the muscles that are involved in making the movements, so from the beginning sensory information establishes a complex body image. This is later extended to include visual and auditory patterns and rapid learning occurs. It is worth noting that language need not be involved. A deaf child exhibits intelligent behaviour solely by observation of the environment: recognition of a person's facial expressions or gestures is an early form of communication. In humans, simple signals and signs later become more complex to include written and verbal symbolization so developing into language as used in the conventional sense. It is at this level of symbolization that it becomes possible to manipulate words or numbers as models of the environment. The usefulness of the scientific method has depended upon establishing an accurate correspondence between symbols and reality. When the symbols no longer do the job of predicting or explaining, one returns to the experiment as exemplified by Faraday[6].

There is a danger that the symbols may be regarded as the repository of intelligence, when in fact the symbols only exist because of the intelligence used to construct them initially. Mechanical manipulation of symbols according to the rules of language may bring benefits in solving problems, but the program responsible for the manipulation (itself a language) lacks the attributes of self awareness and sensitivity to the environment that characterize human intelligence.

Brain and machine translations

A machine may reproduce functions that may be similar to human ones, for instance, translating English into French. The process of translation is established by comparison of the two sets of visual symbols, since the languages follow very similar patterns. Languages describe the variables in our environment and these are, in most physical aspects, common to all societies. The same things are given different symbols (either auditory in the case of speech or visual in the case of written language). The dynamics of events in the environment are also constant: 'a girl runs', 'an object falls', 'a goat jumps', and so on. Therefore, translation involves matching two symbolic patterns, but to produce language, a perceptive organism must first observe the environment and establish a linguistic model of the 'real world', which may be used for interchange of ideas. In the case of a second language, some important similarities are established, for instance, finding what symbols in French stand for man, woman, girl, goat, etc., after which translation is relatively easy because of the communality of experience of the environment embodied in human languages. The translation of Egyptian hieroglyphics was not possible until the discovery of the Rosetta stone where the same message had been recorded in hieroglyphics, Greek and Coptic. The recognition of the name of Ptolemy, which occurred in all these versions, made it possible for Champollion to equate the unknown hieroglyphics with a known language and so produce a translation. Languages have contained within them a causal pattern echoing the environment from which the language was derived.

The interesting aspect of languages is that once they have been established, they may be processed in a variety of different ways because of the built-in degree of correspondence to our world, which makes them useful tools. However, language can not express unambiguously all aspects of the real world since linguistic concepts of language (including mathematics) relate to generalities and not specifics. Linguistic devices may be used to define a particular dog as spaniel, but specificity requires more descriptive information. We soon reach a point where language is no longer capable of conveying the information that a few seconds' direct contact with the dog would provide. State of health, condition of coat, friendly or not, does it like you, how old is it, how heavy, etc. Language is a substitute for reality, and this limitation extends to all descriptive applications.

The problem of ascribing intelligence to a device that solely processes language is revealed if a nonsense-language is used. The machine may produce 'solutions' to nonsense problems fed into it (following a set of rules), but these would be meaningless. The machine is no less capable than machines using real language, nor is its program less complex. The only difference between a nonsense machine and a language processing machine is the degree of correspondence of the symbols used to our environment and this is something that an external observer perceives. This is intelligence by implication, that is, the recognition that certain activities resemble (or differ from) human intelligence: in the case of language processing, intelligence is a function of neither the machine nor the program.

If a black box processes problems, it is tempting to regard the machine (or program) as intelligent since its behaviour resembles that of intelligent humans. If the black box is enlarged to make a room capable of housing hundreds of thousands of people, these may be arranged to process information in the same way as a machine. Chains of individuals handle the input, make available stored information and present an output as a machine does. In this case, where does the intelligence lie? The grouping of individuals is analogous to the circuitry of a machine, but no 'group intelligence' is generated simply by the use of a number of individuals. The instructions to the subjects are carried out by the occupants of the room, but each person is simply carrying out part-functions, the implications of which are not recognizable since their relation to other functions is not apparent. The program

represents the instructions that the workers are carrying out. Intelligent performance is recognizable only by observing the performance of the whole group. Intelligence then is not in the program itself, but in the way the program was designed. This suggests that it is possible to design a machine that performs according to its programming in an apparently intelligent way without it necessarily being intelligent. The machine would need to organize its behaviour by itself, monitor the environment and be responsive to it and be aware that it was doing so if its behaviour were to be equated with human intelligence.

Intelligence

A definition used by Alfred Binet involves at least four factors:

1. **Direction** – the ability to set up a goal and work toward it;
2. **Adaptability** – the ability to adapt onself to the problem and use appropriate means to solve it;
3. **Comprehension** – the ability to understand the problem;
4. **Self evaluation** – the ability to evaluate one's performance and to determine the correctness of approach.

Examples of intelligence in humans cover an enormous number of activities ranging from simple identification of objects to solving complex problems involving the practical manipulation of equipment and the development of theoretical models (based on the result of experimentation). This involves both language and mathematics.

In Binet's factor of self-evaluation, the concept of self awareness is implicit since to evaluate one's own performance requires that one must be aware of what the performance was, who the performer was and that the evaluator of the performance was the original performer. This type of self-analysis with its recognition of individual identity is a fundamental feature of human intelligent behaviour. Occasionally one finds in the literature reference to 'idiots savants'. Really, the term is self-contradictory since idiocy and sagacity are mutually incompatible. The term is used to describe those individuals who, while showing limited general intelligence, are somehow able to perform brilliantly in a specific area, for example, adding up large columns of figures, or working out the day on which a particular date falls in the calendar fifty years hence, etc. In human terms, they would not be regarded as intelligent but rather as having a processing facility for certain data. Wechsler[7] described intelligence as the purposeful and rational ability to deal with the environment. Human intelligence requires that an individual be able to interact with the environment, perceive relationships, predict events and be aware of the effect of his/her actions on others. This is an example of primary intelligence. Symbolic representations in the form of language and mathematics are evolved later as convenient tools for processing information derived from primary intelligence. As stated earlier, when symbolic systems have been constructed, these lend themselves to processing in a variety of different ways, but they are the outcome of intelligence rather than intelligence per se. Terms such as cognitive science or artifical intelligence as applied to the processing of symbols refer to aspects of human abilities and there is a danger in attributing too much to processing functions solely on the grounds that they reflect some aspects of human intelligence.

In the introduction to his book on intentionality, Searle has argued for the inclusion of mental activities when concepts such as intentionality are considered; he rejects "any form of behaviourism or functionalism, including Turing machine funactionalism, that ends up by denying the specifically mental properties of mental phenomena". My own thoughts from a psychological viewpoint also stress caution in reading too much into machine performance, since there is a danger of establishing a form of anthropomorphism that may militate against exploration of human brain functions by model making.

Systems of linguistic analysis and response are closed systems (at present). Once the rules are provided, behaviour is determined by the logic of the system, even though changes in patterns may be affected by the introduction of new data. Self awareness would represent a constant monitoring by the system of its performance in relation to the world outside and to itself. Some aspects of social self awareness are outlined by Duval and Wicklund (1972), Argyle (1969) and Fenigstein, Scheier and Buss (1975)[8].

Elements introduced by human self awareness are not necessarily logical or related to a predetermined goal of efficiency or accuracy. Departures from a logical path may be brought about by the recognition of similarity between the 'individual' and other individuals (which is the beginning of social intelligence and moral responsibility). Emotions such as pity, compassion, love, etc., may produce departures from a logical behaviour pattern since self awareness links all forms of behaviours with oneself. Ethical considerations involving feelings of empathy for others arise, involving both animals and humans. 'If I were a gorilla, would I like my habitat destroyed?', and so on. Introspection brings a new level of internal control of behaviours that may seem unintelligent (when in love, for instance), yet each behaviour is intelligent within the framework of the individual's perception of his/her feelings. The list of human attributes that may influence intelligent behaviour is enormous and includes, along with love, altruism, self-sacrifice, admiration, aesthetic appreciation, and so on. Without such sensitivity to environmental factors, it would be difficult to argue that intelligence was at work. The current conflict between developers and conservationists is an outcome of a wider intelligence coming into conflict with commercial intelligence. It would seem prudent from the outset that exploration into the areas of cognitive science and artificial intelligence should not be restricted to a narrow spectrum, but should attempt to deal with the wider issues involved in intelligent behaviour.

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DC-DC POWER CONVERTER

T. Wigmore

This high-efficiency step-up converter supplies up to 30 V at 75 W when powered from a 12 V car battery. The converter is ideal for many mobile and other out-of-doors applications: it functions as a power source for your DC-operated soldering iron, RF power amplifier, or NiCd battery charger for portable equipment such as a flasher or a video camera.

DC-DC converters for stepping up the car battery voltage are generally based on a switched-mode power supply (SMPSU) or a power multivibrator driving a transformer. The power converter described here is based on the first principle, and uses the Type TL497A integrated circuit from Texas Instruments. This device enables good voltage regulation with low output noise to be achieved fairly easily, and in addition guarantees a relatively high conversion efficiency.

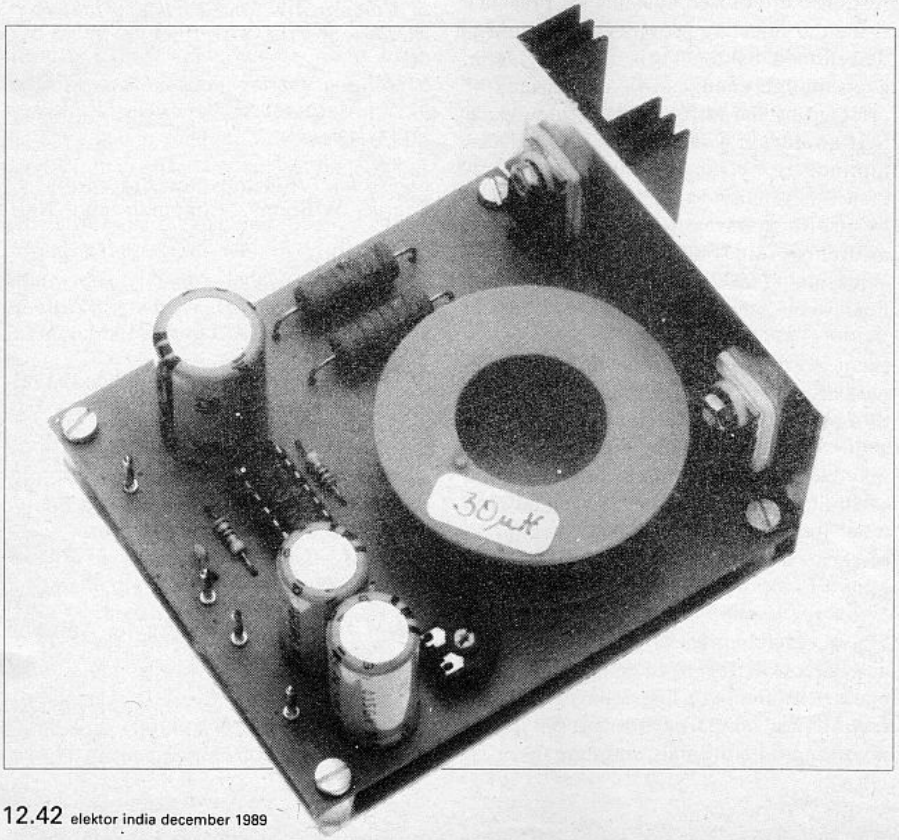
- Flyback-type step-up converter
- no special inductor required
- input voltage: 12 VDC
- output voltage adjustable between 20 and 30 V
- maximum output power: 75 W
- efficiency: 70%, independent of load current
- voltage reduction at load variation from zero to maximum: <200 mV
- ripple voltage: <500 mV_{pp}.

Design background

The converter described is of the flyback type. The flyback principle is the only practical way of generating a direct output voltage from a lower direct input voltage.

The central switching element in the converter is power SIPMOS transistor T_1 (see Fig. 1). When it conducts, the current through L_1 rises linearly with time. During the on-time, magnetic energy is stored in the inductor. The moment the transistor is turned off, the inductor functions as a source of magnetic energy, which is supplied as an electric current to the load via D_1. In this process, it is important that the transistor remains off during the time taken by the magnetic field to decay to zero. When this condition is not met, the current through the inductor rises to the saturation level. An avalanche effect then causes the current to increase very rapidly. The relative on-time, or duty factor, of the transistor control signal must, therefore, not be allowed to reach the value of one.

The highest permissible duty factor is dependent, among other factors, on the output voltage, because this determines the rate of decay of the magnetic field strength. The maximum output power that can be supplied by the converter is governed by the maximum permissible peak current through the inductor, and the frequency of the switching signal. The limiting factors here are mainly the saturation instant and the maximum tolerable ratings for the copper losses in the inductor, and the peak current through the switching transistor (remember that a 'burst' of a particular energy content is supplied to the output at each switching period).



TL497A

The operation of this integrated circuit is rather unconventional, so that a brief description is given below.

In contrast to widely used *fixed frequency, variable duty-factor* SMPSU controller ICs, the TL497A is qualified as a *fixed on-time, variable frequency* device. This means that the duty factor is controlled by means of frequency variation to maintain a constant output voltage. This method results in a fairly simple circuit, but has the disadvantage of the switching frequency reaching down into the audible range when the load current is low. In actual fact, the switching frequency becomes lower than 1 Hz when the converter is not loaded. The slow ticks heard as a result are the charge pulses applied to the output capacitors to maintain a constant output voltage. In the absence of a load, the output capacitors are, of course, slowly discharged by the voltage sensing resistors.

The on-time of the oscillator on board the TL497A is fixed, and determined by C_1. The oscillator may be disabled in three ways: first, if the voltage at pin 1 exceeds the reference voltage (1.2 V); second, if the current through the inductor exceeds a certain maximum; and third, via the in-

hibit input (this is not used here).

During normal operation, the oscillator causes T_1 to conduct so that the inductor current rises linearly. When T_1 is switched off, the magnetic energy stored in the inductor is used to charge the output capacitors. The output voltage, and with it the voltage at pin 1 of the TL497A, rises a little, so that the oscillator is disabled until the output voltage has dropped to a sufficiently low level. This process is repeated cyclically, at least, in theory.

In a configuration with real components, however, the voltage rise caused by the charging of the capacitors within one oscillator period is so small that the oscillator remains enabled until the inductor current reaches the maximum value defined with R_2 and R_3 (the voltage drop across R_2 and R_3 is 0.7 V at this stage). The current rises in steps as shown in Fig. 2b because the duty factor of the oscillator signal is greater than 0.5.

When the maximum current is reached, the oscillator is disabled, and the inductor is allowed to pass its energy to the capacitors. In this condition, the output voltage rises to a level high enough to keep the oscillator disabled via pin 1. The output voltage drops, and a new charge cycle commences.

Unfortunately, the switching operations outlined above are coupled to relatively high losses. In a practical application, this problem is resolved by making the on-time (i.e., C_1) large enough to ensure that the inductor current does reach the maximum within a single oscillator period (see Fig. 3). The solution in this case is the use of an air-cored inductor, which has a relatively low self-inductance.

Some waveforms

The timing diagrams in Fig. 3 show the signal waveforms at the main points in the circuit. The central oscillator in the TL497A operates at a low frequency (lower than 1 Hz if the converter is not loaded). The switch-on instant, shown as the rectangular pulse in Fig. 3a, is determined by capacitor C_1. The switch-off time is determined by the load current. During the on-time, T_1 conducts so that the inductor current rises (Fig. 3b). In the non-conductive period after the current pulse, the inductor functions as a current source. The TL497A compares the attenuated output voltage at pin 1 with its internal reference voltage of 1.2 V. If the measured voltage is smaller than the reference voltage, T_1 is driven hard again to enable the inductor to store energy.

The above charge and discharge cycles cause some ripple voltage on the output capacitors (Fig. 3c). The feedback arrangement enables the oscillator frequency to be adjusted for optimum compensation of voltage losses caused by the load current.

The timing diagram in Fig. 3d shows considerable swing of the drain voltage owing to the relatively high Q (quality)

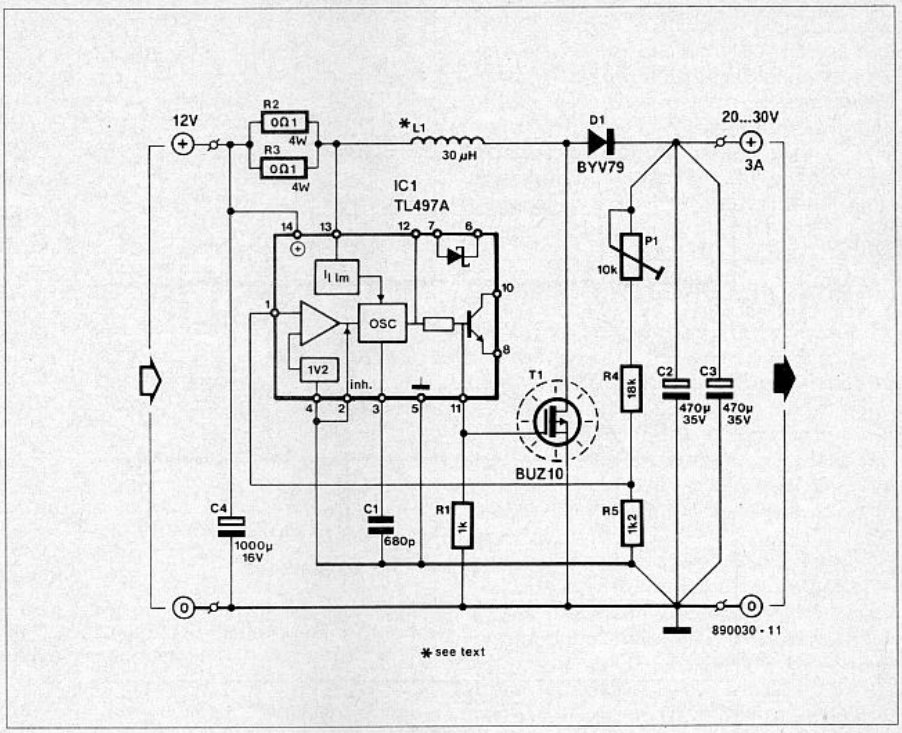


Fig. 1. Circuit diagram of the step-up converter.

factor of the inductor. Although the parasitic oscillations do not affect the normal operation of the power converter, they may be damped with the aid of a 1 kΩ resistor in parallel with the inductor.

From theory to practice

Naturally, a switch-mode power supply is designed for maximum rather than quiescent output current. High efficiency and a stable output voltage with little ripple are also prime design goals.

In general, the load regulation characteristics of a flyback type switch-mode power supply give little cause for concern. During every cycle, the on/off ratio is adjusted in accordance with the load current, so that the output voltage remains fairly stable in spite of large load current variations.

The situation looks a little different as far as the overall efficiency is concerned. A step-up converter of the flyback type typically generates relatively large current surges, which cause considerable power losses (remember that power rises exponentially with current). In practice, however, the proposed converter has a total efficiency higher than 70% at maximum output current, which is remarkable given the simplicity of the design.

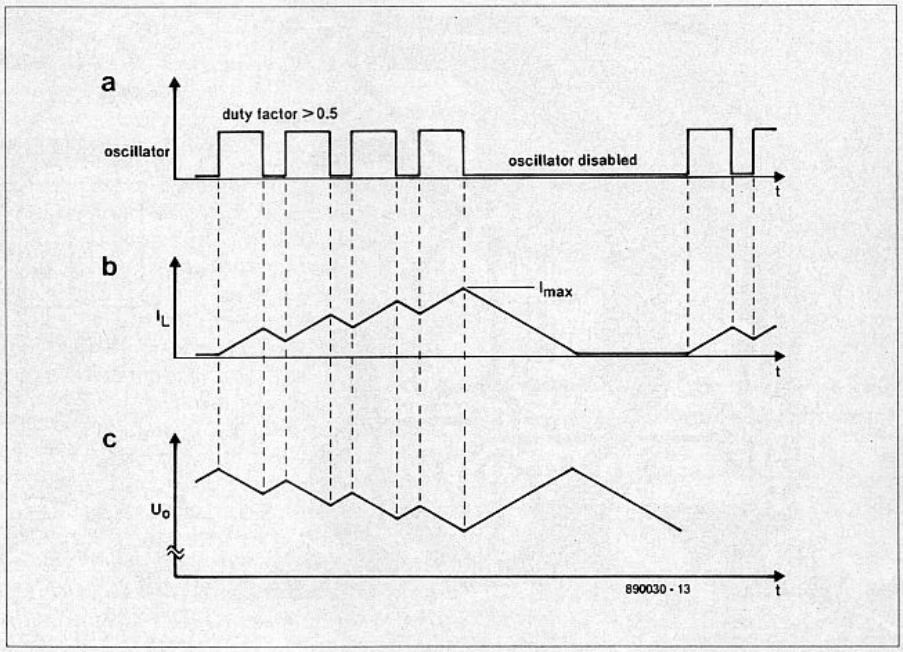


Fig. 2. Showing how the inductor energy is built up under the control of the oscillator signal.

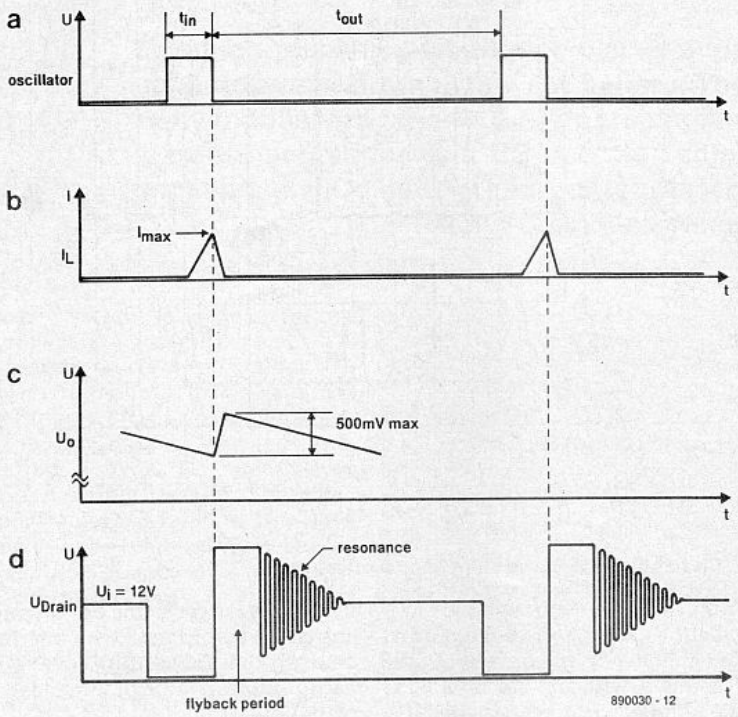


Fig. 3. Timing diagrams of the main signals in the circuit. The current reaches its maximum value within one period of the oscillator signal.

The switching frequency at maximum load is made as high as possible to allow the use of a relatively small self-inductance. The practical circuit is based on an air-cored inductor. Significant losses caused by a ferrite core are thus avoided.

A fast power-FET of the SIPMOS type is used to switch the inductor current. The Type BUZ10 or BUZ10A was chosen because of its short recovery time. To achieve acceptable efficiency, the transistor must be used as a switching element.

Parts list

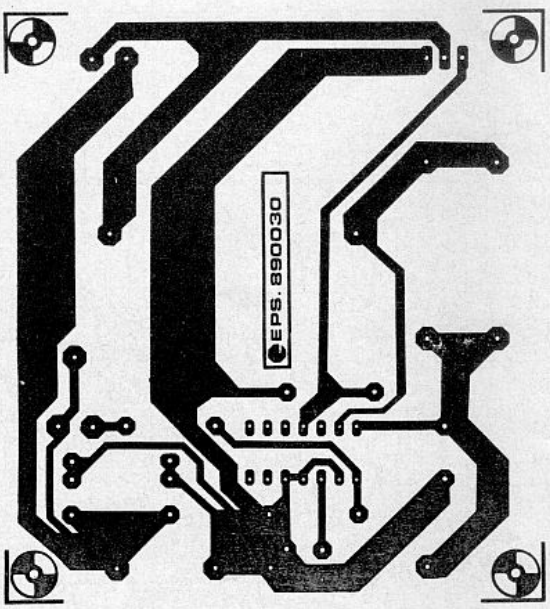
Resistors (±5%):
R1 = 1k0
R2;R3 = 0Ω1; 4 W
R4 = 18kΩ
R5 = 1k2
P1 = 10kΩ preset H

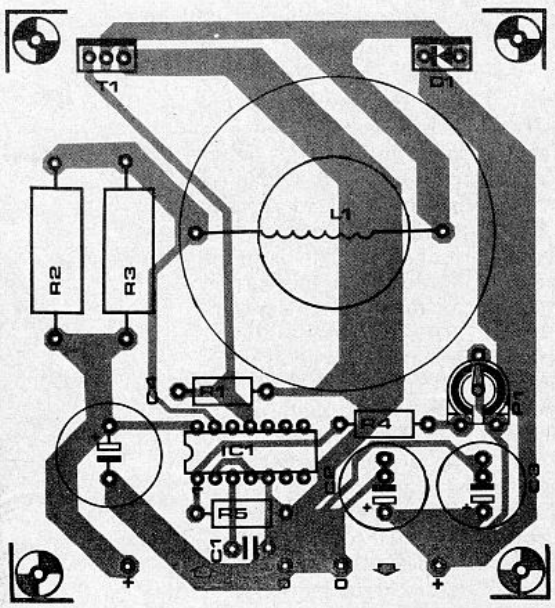
Capacitors:
C1 = 680p
C2;C3 = 470µ; 35 V; radial
C4 = 1000µ; 16 V; radial

Inductor:
L1 = 30 µH (home-made, see text)

Semiconductors:
D1 = BYV79
T1= BUZ10 or BUZ10A
IC1 = TL497A

Miscellaneous:
Heat-sink for T1.
PCB Type 890030





This, in turn, requires it to be driven into saturation, resulting in a relatively long turn-off time. Obviously, the longer it takes for the transistor to interrupt the inductor current, the lower the overall efficiency of the converter. Unconventionally, the BUZ10 is driven by the oscillator test-output of the TL497A (pin 11) rather than the internal output transistor.

Diode D_1 is another essential part in the circuit. The requirements for this device are an ability to withstand high current surges, and a low forward drop. The Type BYV79 meets these conditions, and must not be replaced with a general-purpose type.

Returning to the circuit diagram of Fig. 1, it should be borne in mind that current peaks of 15–20 A are not uncommon in the circuit. To prevent problems arising with batteries having a relatively high internal resistance, capacitor C_4 forms a buffer at the input of the converter. Since the converter charges the output capacitors with short, surge-like current pulses, two capacitors are connected in parallel to ensure that stray capacitance remains as low as possible.

The power converter is *not* short-circuit resistant. Short-circuiting the output terminals is the same as short-circuiting the battery via D_1 and L_1. The self-inductance of L_1 is not so high as to limit the current for the time required by a fuse to blow.

A home-made inductor

Inductor L_1 is wound from 33½ turns of enamelled copper wire. Figure 5 shows the dimensions. Most manufacturers supply enamelled copper wire on an ABS reel,

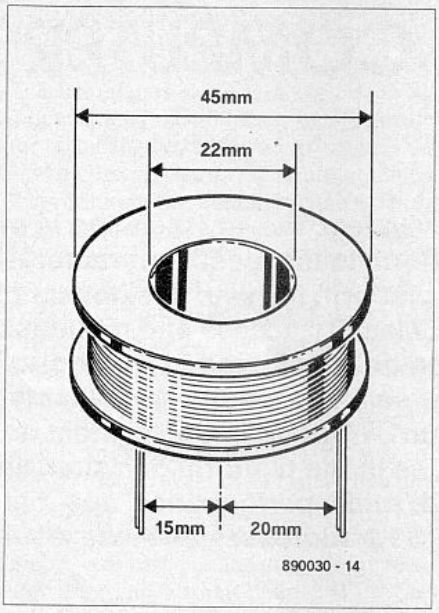


Fig. 5. Suggested construction of the inductor on an ABS reel.

which is suitable as the former for making the inductor. Drill two 2 mm holes in the lower rim to pass the inductor wires: one hole beside the cylinder and the other at the outside of the rim.

There is little point in using thick wire to wind the inductor, because the skin-effect, i.e., the displacement of charge carriers towards the outside of the wire, must be taken into account given the frequencies used in the converter. To ensure a low resistance at the required inductance, it is recommended to use two wires of 1 mm diameter, or even three or four wires of 0.8 mm diameter in parallel. Three 0.8 mm wires result in a total diameter that is roughly the same as that of two 1 mm wires, but has the advantage of resulting in a 20% larger effective surface.

The inductor is close-wound and may be encapsulated in a suitable resin or potting compound to limit the sound level (remember that the frequency of operation is within the audible range).

Construction and alignment

The printed-circuit board designed for the DC-DC converter is shown in Fig. 4. A number of constructional points require attention.

Resistors R_2 and R_3 run fairly hot and must, therefore, be mounted at a few millimeters above the board surface. The peak current through these resistors can be as high as 15 A. The power-FET also runs hot, and requires a medium-size heat-sink and the usual insulating material. The diode can do without cooling, although it is conveniently bolted on to the same heat-sink as the power-FET (do not forget to insulate it electrically). During normal operation, the inductor heats up.

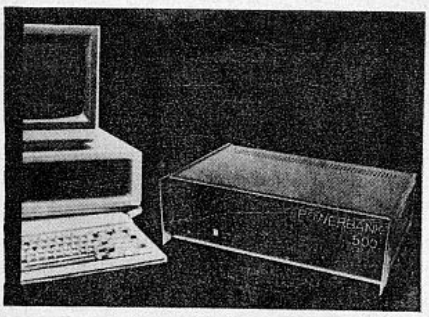
Heavy-duty terminals and wires must be used at the input and output of the converter. The battery is protected by a 16 A delayed action fuse inserted in the input supply line. Remember that the fuse does not protect the converter!

The circuit is simple to align: adjust P_1 for the desired output voltage between 20 and 30 V. The output voltage may be made lower, but not lower than the input voltage, by using a smaller resistor in position R_4. The maximum output current is about 3 A.

NEW PRODUCTS

9" Monochrome Monitors

9" Monochrome Monitors with composite video nad for ITL input are now available with reverse polarity protection for 12V DC input. The Monitor has Green Phospher Tube and has resolution of 800 x 35 video Amp. Bandwidth of 22 MHz.



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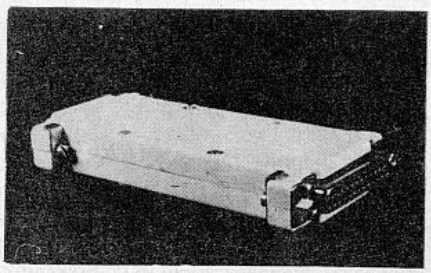
Hardware Locks

Real Time Systems have developed Hardware Lock which preents unauthorized copies of software. This has installation software. Once installed, the installed files can be freely copied but will not run without the device in the parallel part. The software contains its own loader which does the loading and hierarchial decision making structure to give maximum protection to software. Further no two units of installation software are same for added security. There is no limit to the number of files that can be installed with one device. In addition to this there is a data file protection unit DFP-1 which protects the program source code, letters, reports and



other data bases. Bothe thse units operate with IBM PC-DOS.

Real Time Systems • Plot No. 8, 4th Main Road Avenue • Dhandeeswarar Nagar • Velachery • Madras-600 042.

PERSONAL COMPUTER DECISIONS

by Linda Bishop*

In choosing a PC system, the key question is not so much which processor platform is the 'best', but rather which is the most appropriate platform for you. It is not simply a choice of speed either. Memory access and multitasking capability must also be considered in a platform decision. And then, of course, there's software. What type of applications will you run? What operating system do you need? In software, as in the platform decision, several criteria should be explored: price, performance, applications and the future. OS / 2 addresses all these issues.

OS / 2 allows multi-tasking, multi-user operation, breaks the 640 K barrier of DOS and supports the graphical user interface of presentation manager. This will make network communication easier, provide bigger databases, more complete and simple applications, and allow computers to do several things at the same time.

What makes OS / 2 unique is that it is the first full-fledged multi-tasking system for the 80286 microprocessor that can switch back and forth between protected mode and real mode to run the new programs designed for OS / 2 as well as most existing DOS programs.This will give DOS users a smooth upgrade path to OS / 2.

The built-in network support of OS / 2 allows multi-user operation: this facility of having several programs running at the same time is, of course, a most useful one. Moreover, OS / 2 permits distributed applications, that is, it allows the program in your PC to work (communicate) with programs in other PCs.

OS / 2 was written for the 80286 processor, taking advantage of the special protected mode feature. This feature is also provided by the 80386. OS / 2 was not written to take advantage of any of the new features of the 80386 and no performance advantages are obtained by running OS / 2 applications on an 80386.

The 80386 is no faster than an 80286 when running 16-bit software at the same clock speed. The primary reason for this is that the 80286 executes more 16-bit instructions in fewer clock cycles than the 80386 or 80386SX. Out of 190 existing 16-bit instructions, the 80286 is faster on 74, the 80386 is faster on 50 and the two devices are the same on 66 instructions. In fact, the only way the 80386 is able to run OS / 2 at all is by emulating the 80286.

The applications that are available today as well as those currently being developed will not take advantage of the 80386 until an OS / 386 specific version of the operating system is available some time next year: OS / 386 general applications are planned to become available sometime in 1991-92.

Once an 32-bit operating system is available for the 80386, the device will have an advantage over the 80286. But there is no guarantee that 80386, and especially 80386SX, personal computers available now have the configuration to run new 80386 32-bit software four years from now. After all, the first 80286-based PC sold several years ago at 6 MHz with 640 K of memory is hardly suitable for running 16-bit OS / 2 now. The same situation is likely to exist in four years' time for today's 80386 PC as far as running 32-bit 80386SX software is concerned.

What is important for the OS / 2 operating system then is not whether it is run on an 80286 or an 80386, but rather the speed of the processor. The bulk of the processor's work is multi-tasking, that is, the accomplishing of several things at the same time by dividing the computer's time into 'time slices' that last only a fraction of a second. These time slices are handled so fast that it appears as if programs are run simultaneously. Since the processor is actually carrying out all the tasks at separate intervals (time slices), the faster the processor, the quicker the multiple tasks will be completed. An adequately equipped 80286 system running at least 12–16 MHz with VGA (Video Graphics Array) graphics forms a very cost effective OS / 2 foundation .

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High-speed system pricing
80286 vs 80386

	286-20	386-20	Difference
Dell	$2,999	$4,099	37%
Zeos	$2,095	$2,995	43%
Northgate	$2,599	$3,699	42%
PC Brand	$2,379	$2,995	26%
Dataworld	$1,555	$1,995	28%
CompuAdd	$1,695	$2,295	35%

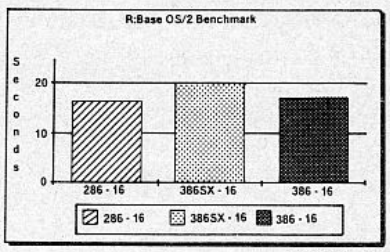

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Figure 1

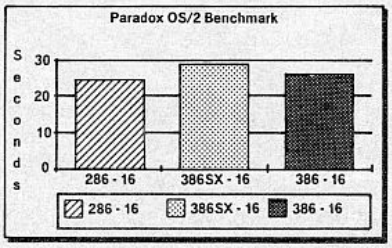

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Figure 2

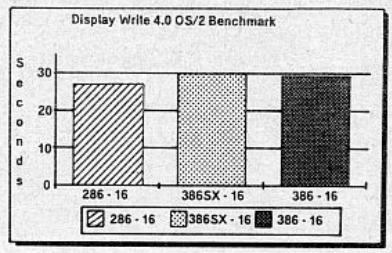

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Figure 3

The 80286 system offers everything for the needs of today's and tomorrow's user. Fast 80286 (16, 20 and 25 MHz) systems available now have the 16 Mbyte memory access capability and the protect mode for multiple applications required of OS / 2.

The 80286 is one of the best-selling processors on the market today and it is widely available. Moreover, its price is at an economical level for the system designer.

Owing to its die size, packaging and complex processing, the 80386 is more expensive. Moreover, systems built around this device require 32-bit peripherals: the design cost is, therefore, higher as well.

This leads to significant price differences between identically configured 80286-based and 80386-based personal computers. As shown in the table, an 80386-based system costs on average 35% more than an 80286-based system.

The 80286 and 80386SX PCs used in the tests to arrive at the comparison bar graphs in Fig. 1, 2 and 3 are Everex STEP models, while the 80386 is an IBM System 80. The 80386 PC uses page mode memory access for 0.8 average wait states with 80 ns DRAMs. Both the 80286 and the 80386SX run zero wait state with 60 ns DRAMs. The performance of these PCs is indicative of that of other PCs.

The benchmark in Fig. 1 is based on the R:Base database program. The source database used is PC Magazine's Index for Volume 4.0. First, a Grouping Select Query (SQL) was performed, followed by a category tally to count the number of occurrences in a category. Next, a calculation loop was performed on the first 100 records. The results are shown in seconds. The bar graphs show that the 80286 PC outperformed the 80386 PC by 4%, while the 80386SX was 24% slower.

The bar graphs in Fig. 2 are obtained from running the Paradox database program on the three computers. The source database is again PC Magazine's Index Volume 4.0. First, a Grouping Select Query was performed. Next, a report was run with the output sent to a file on RAM disk. The query results were then sorted and a conditional delete of the records in the query results was performed. The results are shown in seconds. As is seen, the 80286 PC was 18% faster than the 80386SX.

The comparative tests illustrated in Fig. 3 were based on the IBM word processor program Display Write 4.2. The benchmark started with a 100 K, 40-page document. A global search and replace was performed, changing one frequently used word for another. Next, the margins were narrowed, forcing a complete text rewrap. Lastly, the document was repaginated. The results are shown in seconds. Again, the 80286 PC was faster than the 80386 PC by 4%, while the 80386SX was 8% slower than the 80286 PC.

Comparative tests are influenced both by the processor and by the memory interface. In the PC systems used, the memory interfaces were relatively equal (0.8 wait states on the 80386 and 0 wait state on the 80286 and 80386SX machines). Thus, the performance difference measured between the 80286 and 80386SX was caused solely by the different processors with the former performing faster than the latter.

The performance difference between the 80286 and 80386 must take into account the different memory interface techniques. A 0.8 wait state system (as on the 80386 PC) has about a 9% performance degradation compared to a true zero wait state system (as on the 80286 PC). Taking this into account, the 80286 and 80386 systems performed essentially the same.

As OS / 2 software becomes more prevalent, PC performance will become more important. Performance is primarily a function of processor clock speed and memory interface in the PC. Clock speeds of 16 MHz and beyond will be needed to run multiple applications effectively. It should be borne in mind that there is little difference in performance between the 80286 and 80386 running at the same clock speed on OS / 2.

In addition to performance, price will also remain a major factor in personal computer decisions and it was seen that 80286-based PCs remain substantially cheaper than 80386-based systems. The 80286 has, moreover, a lot of life left for DOS, as well as OS / 2, systems and will continue the trend toward higher clock speeds.

According to Dataquest, the 80286 will increase its current market share of IBM and compatible PCs from 30% to 33% by 1992 and become the entry-level PC, replacing 8086/8088 based machines. Following a stable path to OS / 2, the 80286 is the best platform for cost vs performance.

ELECTRONICS SCENE

PICTURE-IN-PICTURE MINIBOARD FROM SIEMENS

The SDA 9088 Picture Insertion Processor from Siemens allows the picture-in-picture facility to be installed not only in digital TV sets, but also in analogue ones. The need for only two chips reduces time and material requirements and increases reliability. The SDA 9088, which is designed in Siemens 1 Mb it DRAM technology, also provides a much better picture quality than previous designs.

The SDA 9088 permits the insertion of a reduced-size picture into the main picture by using picture signals that may be based on completely different standards and synchronization principles. The combination of frame memory, control, digital signal processor and digital-to-analogue converters on a single chip enables equipment manufacturers to realize the picture-in-picture function in TV sets and video recorders on a high-performance and particularly cost-effective basis.

Although the picture-in-picture function has been in existence for some years, it has failed to become widely established in domestic video equipment owing to its high cost, incurred mainly by the expensive but indispensable frame memory and the peripherals required for the analogue-to-digital converters. Through the use of the most up-to-date semiconductor technology, it has now been possible to integrate all essential functions into a single circuit. The primary function of the PIP is to reduce the picture produced by the second picture signal and synchronize it with the main picture.

Two formats are available for the inserted picture: 1/9 and 1/16 the size of the main picture. The insert may be displayed in any of the four corners. A positioner for each corner permits adjustment to the particular set's geometry.

In contrast to previous designs, picture reduction is effected not by omitting the pixels that are not needed but by digital filtering of the horizontal and vertical signals to ensure that all the information is utilized.

The SDA 9088 handles all worldwide TV standards: a detector performs automatic transfer to the standard being received. It is also able to supply standard-converted picture signals at a line frequency of 32 kHz.

SPEEDING UP THE COMPUTER

by Pete Chown

The architecture of the computer

If you look at a modern micro, say, an 80386-based IBM compatible, you will discover that nearly all the memory bandwidth is used up. If faster memory were installed, it might be possible to increase the speed of the processor by several times, but that would be the limit for that particular architecture.

In an earlier article[1] I mentioned one way out of this dilemma: parallel processing. There are, however, many other ways of speeding up apparently sequential processors so that they can reach speeds of up to 600 MFlops (million floating point operations per second). At present, the Cray-3 represents the limit of that approach as far as commercial machines go. The Cray-2 is the fastest one that has been commercially released.

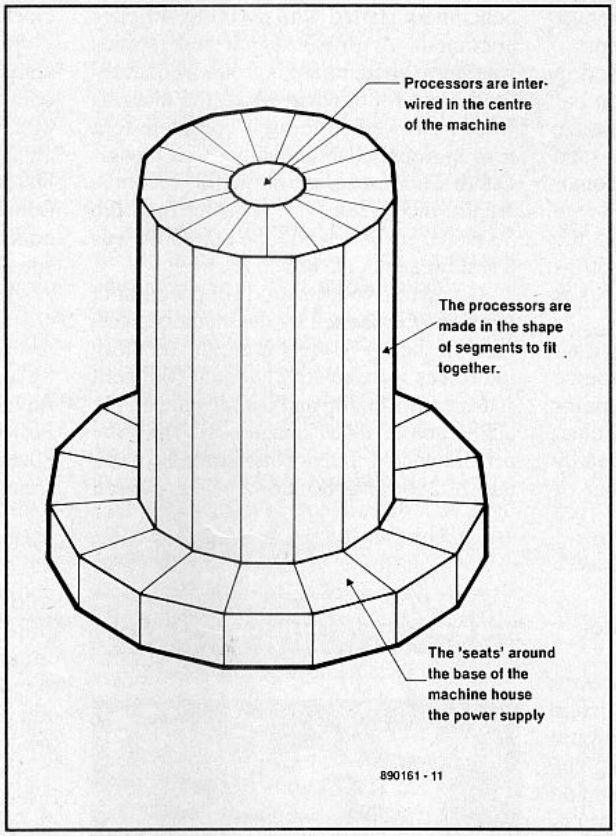
Cacheing

Cacheing is one of the simplest techniques that can be used to speed up a computer. Earlier, I mentioned that faster memory could allow the speed of most machines to be increased substantially. Unfortunately, fast memory costs a disproportionate amount more, and so manufacturers decided to use the fast memory only for instructions that are currently being executed. This means that the cache is loaded with the pages of main memory that are being used (normally in the opposite phase of the processor clock to that on which the processor reads the memory), and it is then available for use.

Using a cache has one other advantage. Memory protection – so that one process can not alter another's memory – is very hard to implement fast enough for the processor's request to access a particular word to be checked in time. On a large machine, only of the order of 100 ns would be available. If a cache is used, however, the system can verify that the process is allowed to use a particular page before it is ever loaded into the cache. A major cause of the inefficient use of caches is that each time the machine switches context (that is, changes the process it is executing) at least part of the cache has to be reloaded.

Multiple processors

Because large machines are generally used for time-sharing, it is quite acceptable for them to incorporate several processors. Generally, however, these share the same bus, so that problems are not encountered with lack of memory on one processor, or problems with an I/O device controlled by another processor. Caches are used to avoid continual conflicts for memory.



Construction of the Cray machines

This tends to be a not very efficient technique, because in practice a large number of conflicts for memory do occur. The best-known machine to use this system is the VAX 8900. It has four processors sharing a bus (each of which is the same as the single processor used in the 8700). Adding a fourth processor does, however, add only about 15% of the performance that the processor would generate on its own. The reason for this is that conflicts for memory mean that the processors are standing idle for much of the time.

The reason that DEC decided to use this technique is probably that it allowed them to keep the same architecture: a radical redesign would have meant changing the instruction set, and the major selling point of the VAX range is that programs for any VAX can be run on any other. The other advantage of this system is right at the top end of the computer market: the US Navy have produced a supercomputer using 16 largely independent processors, giving them the edge over single-processor equivalents.

Pipelining and vector processing

Pipelining and vector processing are other major ways in which manufacturers speed up their computers. They are, however, much more complex to implement than the other systems. The techniques are similar: some computers implement pipelines but not vector processors, but generally speaking the reverse is not true.

In pipelining, the processor, instead of starting on one instruction and executing it to completion, reads instructions continually. Once it has completed reading an instruction, the processor begins fetching the instruction's operands. At the same time, the next instruction will be read, the previous instruction will be executed, and the result of the instruction before that will be written to memory or registers.

In practice, things are not this simple. A pipeline tends to be longer than just indicated, because the aim is to keep the processor-memory interface busy for as much of the time as possible. Since not all instructions need their operands fetched, there would be a tendency for the interface to run out of information to fetch or store.

Problems with pipelines tend to be encountered with jumps. When the processor jumps, everything in the pipeline is useless because it no longer wants to execute those instructions. It is not possible to make the pipeline start taking instructions from the destination of the jump, because the jump might be conditional and the condition would not have been evaluated.

Another problem is when store locations change after the pipeline has been loaded. If one instruction uses the result of

the previous one, the old value that was present at that location in store would already have been loaded. There is no solution to this except the long one – with each and every instruction it must be checked that the operand being loaded is not going to be stored by an instruction already in the pipeline. This is particularly difficult with indirection, because care must be taken that the information about where the operand is coming from is available in time. If it is not, the processor must stop until it is, which leads to inefficiency.

As with caches, pipelines suffer when a processor switches context. Whereas with the cache some of it might be able to be preserved, the entire pipeline must be discarded since there is nowhere for it to be put until the processor returns to that process.

Vector processors take the idea of pipelining a stage further. With large machines providing a large variety of complex mathematical operations, the execution of an instruction is by far the longest step in the pipeline. Consequently, the information about where to find the operands is passed out to a lot of arithmetic processors. This saves the main processor from having to find out what the operands are, or to execute the instruction.

The problems with this are obvious. The difficulties with making sure that the operands of an instruction have not been modified since the instruction was loaded become much worse. Because some instructions complete faster than others, there is a danger of instructions being executed in the wrong order: tens of short instructions could have been executed in the time it takes for a complex floating point function to be evaluated and one of these short instructions might have wanted to use the result of the long one.

Another problem is memory bandwidth – the multiple processor problems are obviously much worse. This has, however, been almost completely solved. Memory, instead of being addressed over a single bus, is addressed on a chip-by-chip basis, so that as long as all the processors wish to access different chips, they can do so at the same time. This solution does, however, lead to another snag: the large amount of wire needed to connect each individual chip!

It is interesting to note that this architecture is based on parallel processing, even though the machines appear sequential to the user. The parallelism is on a very small scale, and so it has been described as 'fine' parallelism, whereas true parallel processing machines have been described as having 'coarse' parallelism.

As these computers get faster, the exact length of wire used to connect two points becomes significant in determining timing. Consequently, Cray Research decided to cut each piece of wire in their machines the same length! Unfortunately, these lengths have to be also as short as possible for the same reason and this led to the circular construction of the Cray machines as illustrated. It also led to the situation where the wires are almost impossible to get at, forming a three-dimensional web of cables that are tight enough for it to be difficult to reach a wire near the middle.

RISC processors

RISC processors are not really viable as a technique for building large machines. The reason is that you are faced with a choice of ways of improving performance – make each instruction do more or execute faster. Small machines had been tending to follow the former route despite the fact that there was not really enough processing power on a single chip to do it. A large increase in speed was therefore obtained when micros began to follow the latter route. Large machines have pipelines, caches and so on, and also aim to do a lot per instruction. Consequently, the Sun, Apollo and Hewlett Packard machines tend to set the limit for this type of technology.

There is now a move to provide a mainframe style processor on a chip, since this is becoming viable with greater reliability and packing density. This will effectively make the RISC processor obsolete in a few years' time, at least as far as the very fastest workstations are concerned.

This trend towards micros that are more like mainframe is actually another way of speeding up computers. We are approaching the limit as far as supercomputers go, but if workstations that only several people use get nearly that fast, they will effectively have a much more powerful machine because there are far fewer processes for it to run.

There will always be a place for the supercomputer, however, in performing single processes that are too complex for a workstation to do. It will, however, become increasingly wasteful to use a supercomputer for a lot of fairly small jobs.

One area of potential for RISC that has not received much attentional is that of arithmetic processing. It would be possible to build a RISC machine with, say, 256 bytes of RAM and several registers that would carry out operations between registers only and not RAM. It would thus be very simple and could, therefore, run at high speeds. It could then be programmed with short, repetitive calculations that could be done over and over again.

Managing a pipeline

I have already discussed some of the problems that arise from pipelining and vector processing. One of the easiest ways to understand the problems and how they are solved is, however, to look at how a vector processor would execute a certain sequence of instructions.

Since this is only for illustration, the instructions will be given in words – not in any form of mnemonic that would make it harder to follow. The instructions are to calculate the coordinates needed to draw a circle by trigonometry. Square brackets indicate indiscretion The label 'pointer' points to a location containing the address where the forty pairs of coordinates are to be placed.

1. Load register A with 0.
2. Load register B with 0.
3. Label:
4. Calculate cos(A), put in register C.
5. Calculate sin(A), put in register D.
6. Multiply C by [radius].
7. Multiply D by [radius].
8. Store register C at [pointer] + B.
9. Store register D at [pointer] + B + 1.
10. Add 2 to B.
11. Add pi/20 to A.
12. Jump to label if A < 2 * pi.

Let us now consider how a vector processor would execute this section of code. It would start by filling its pipeline from the beginning. No evaluation of operands would be necessary for instructions 1 and 2. When these got to be executed, they will be run at the same time because the processor would recognize that they did not refer to the same part of store.

Instructions 4 and 5 could not be executed until instructions 1 and 2 had been completed, because the values of the same registers are used. Once 1 and 2 had been completed, however, they would be executed together.

The same would be true of instructions 6 and 7, but here one of the advantages of a fast processor shows up. The processor has been instructed to look at a particular memory location in order to find the radius of the circle. There is no reason why this should wait to be evaluated until the rest of the instruction can be. Different processors would tackle it in different ways: those with just a pipeline and no vector processor would attempt to find time to evaluate it while the instruction is in the pipeline, while those with a vector processor would simply hand the pointer to one of the arithmetic units and instruct it to look at that place in store.

The two additions would take place concurrently, since they do not refer to each other in any way. The jump would then be encountered. The pipeline would have been unable to follow the jump to its conclusion to get subsequent instructions, because it is a conditional one. It is, there-

assume that the jump will not be taken, and it will have to abandon all the information it has built up about the instructions following the loop, except when the loop finally ends. Nothing has been lost compared to a conventional processor, however, because the bus would merely have been sitting idle. Once back at the start of the loop it might have kept the instructions because such an eventuality was likely or it might have to start building up its pipeline from scratch again.

Conclusions

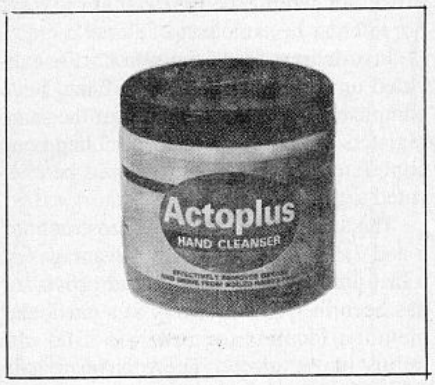
Because we are reaching the limits of semiconductor-based computers, the large computer of today is a far more complex thing than its predecessors. The normal rules of structured design have been abandoned in a search for the last megaflop, leading to such peculiarities as computers with all the wires the same length (normally, of course, no one would think of building a large system other than in standard 19 in. rack-mounted cases on a carefully constructed backplane). The techniques do, however, work and we have probably got computers an order of magnitude faster from them. It is, however, a tribute to the people who design them that they work at all.

Human nature being what it is, however, these techniques will probably be with us even when optical computers appear, and we will simply take our thousand times speed increase, and do exactly the same with optical fibres.

NEW PRODUCTS

Hand Cleanser

Advance Labs have introduced Actoplus Hand Cleanser. This remove grease, oil, smal particles of metal, dust, grime and dirt instantly when applied. A small quantity is applied in paste form and either washed away wth water or simply wiped clean with cotton waste or cloth. There are no side effects as it is absolutely safe.

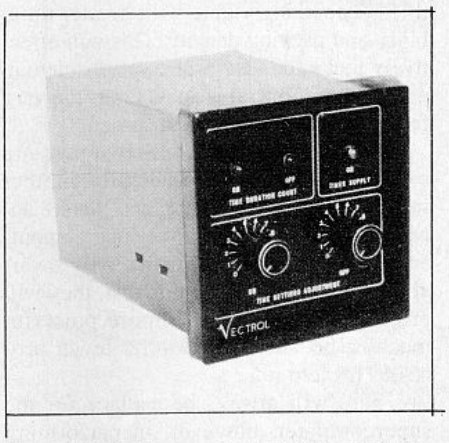


Advance Lab • 11, Below Shantidoot Hotel • Dr. Ambedkar Road • Dadar • Bombay-400 014.

Sequential Timers (Cyclic)

Vectrol Engineers introduces a solid state cyclic timers. These are available with two change over contacts. Timer switches a given device/load sequentially "ON-OFF" on giving signal/application of control supply and stops it when a soap signal/command is given. Timers can be supplied with 'ON' time count or 'OFF' time count start first on application of start command/signal/control supply to timer. Timer provides precise 'ON-OFF' sequence ratio with excellent repeat accuracy.

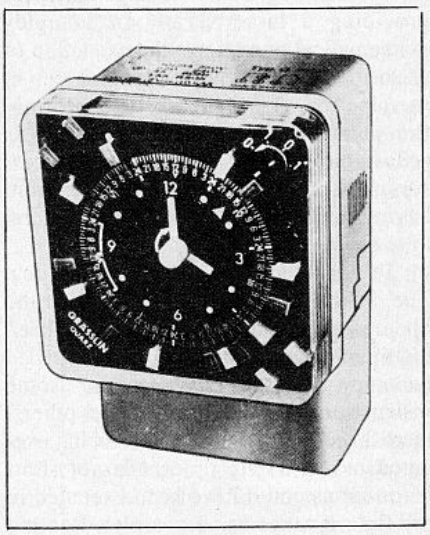
Cyclic timers are used in chemical/pharmaceutical and other allied industries, where device/load is required to repeat the operation automatically in succession, until the stop signal is given.



Vectrol Engineers • 4 A/32, Versova View Co-op. Hsg. Society • Four-Bunglow road • Andheri (W) • Bombay-400 058.

Grasslin Time Switch

The MIL 2008 Q series is fitted with a Quartz Electronic Drive Control and a step motor. The Quartz frequency is 14.9 million Hertz and the Quartz stabilization guarantees the exact running of the driving mechanism. These time switches are designed for the accurate and effortless control of oil heating installations, electric heaters, air conditioning plants, water processing plants, street lights, traffic signals, etc., etc.



MIL 2008 Q is available with contact rating of 16Amps. 250V AC and available with daily programme and weekly programme dial. Operates on mains supply and continue to run for 150 hrs. after power failure on a battery back-up.

M/s. Sai Electronics • (In association with Cupwud Arts) • Thakore Estate • Kurla Kirol Road • Vidyavihar (West) • Bombay-400 086. Ph: 5136601/5113094/5113095.

active loudspeaker–crossover filters

(2)

The first part of this article dealt with the design considerations concerning loudspeaker crossover filters in general, and active crossover filters in particular. This month a practical circuit is given, with details on how to modify it according to personal taste.

As explained last month, several decisions must be made before starting with the actual design of any loudspeaker crossover filter system. In chronological order:

- What type of filters: active only, hybrid or passive? This article only deals with filters that are active, at least in part.
- What type of system, three-way or two way? This decision will be based on such factors as desired cabinet size, available financial resources, desired frequency range – and personal taste.
- Which speakers? This depends in part on the answer to the previous question.
- What crossover frequencies, and how steep the filters? These decisions are both based on the answer to the previous question.
- Which amplifiers? This is a source of endless discussion, but the answer obviously depends in part on the type of system and the speakers used.

The points of interest in this article are the design decisions for the filter proper: two-way or three-way, what crossover frequency or frequencies, and how steep? These points are illustrated in figure 1f. If a two-way system is required, the crossover frequency is assumed to be f1–f2 can be ignored. For a three-way system, f1 is the lower crossover frequency and f2 is the higher. The filter slopes can be 6-, 12- or 18 dB / octave, and the 12- and 18 dB/octave slopes are numbered in figure 1f.

As an example, a three-way system with crossover frequencies of 400 Hz and 4 kHz and filter slopes of 12 dB/octave at the lower crossover point and 18 dB / octave at the higher frequency can now be defined briefly as 'f1 = 400 Hz, f2 = 4 kHz, filter slopes 1, 4, 6 and 7'. This shorthand notation will be used extensively in the tables given in this article.

The most complex circuit diagram is given in figure 5: a three-way system with all slopes 18 dB/octave. This corresponds to the figure 6 layouts for printed circuit board and parts.

When any less-complex set up is to be assembled it will only be necessary to complete the 'through paths' with wire links on the printed circuit board. This will be illustrated in detail further on.

For added convenience, all the circuits and parts-layouts have been duplicated several times – each time showing the simplified schemes and jumper wires needed for the less complex filters. The schemes we have chosen to illustrate are:

- Three-way system with 12 dB/octave slopes (figures 7 & 8).
- Two-way system with 18 dB/octave slopes (figures 9 & 10).
- Two-way system with 12 dB/octave slopes (figures 11 & 12).
- Two-way system with 6 dB/octave slopes (figures 13 & 14).

The frequency responses of the figure 5 filter set are plotted in figure 15. Figure 16 gives the plots for the figure 7 circuit. In both cases the frequencies chosen for illustration are 500 Hz (f1) and 5 kHz (f2).

Design procedure

The suggested procedure for finding the required design is as follows. First of all decide, using figure 1f or table 1, which set of filter characteristics is to be realised – and which crossover frequenties (values of f1 and f2) are to be taken. Table 2 may now be used as a kind of 'railway timetable' to determine which PC board positions are to be left open, which positions must be bridged by a jumper wire and which of the tables 3 . . . 8 is to be referred to for the component values. The examples given will illustrate this.

Loudspeaker connections

In just the same way as with passive filters it is important to connect the individual loudspeakers in the correct relative phases. The rules are as follows:

- When the filter provides a three-way symmetrical crossover with 12 dB/octave slopes, the midrange unit should be connected in opposite sense to the woofer and tweeter. Both systems of a stereo pair should of course be identically wired.

⊕	⊖	⊕
L	M	H
⊖	⊕	⊖

1f

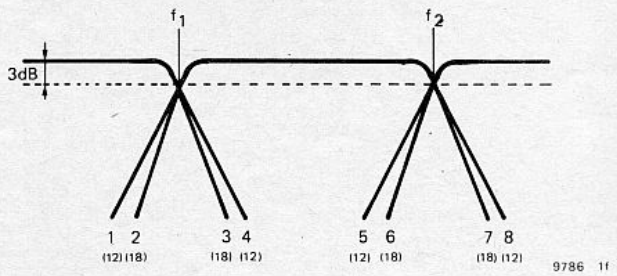
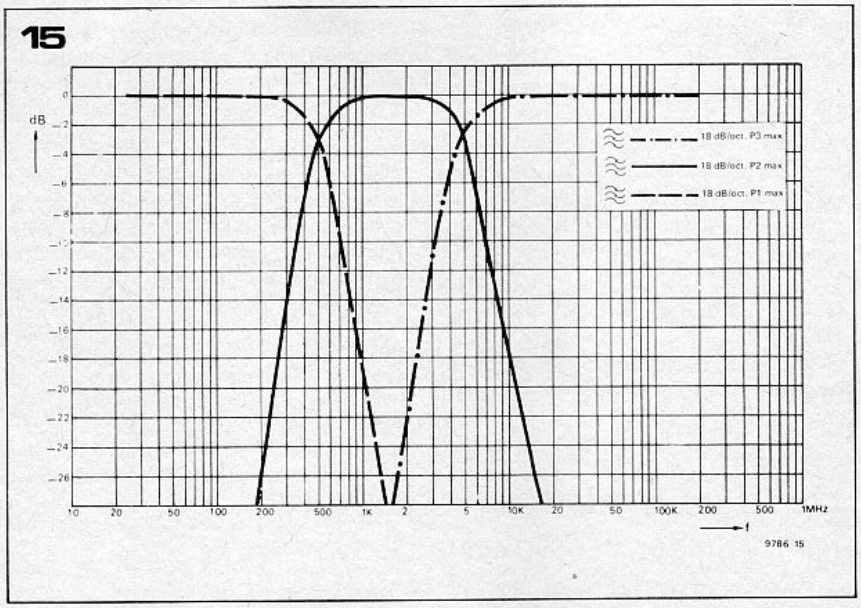
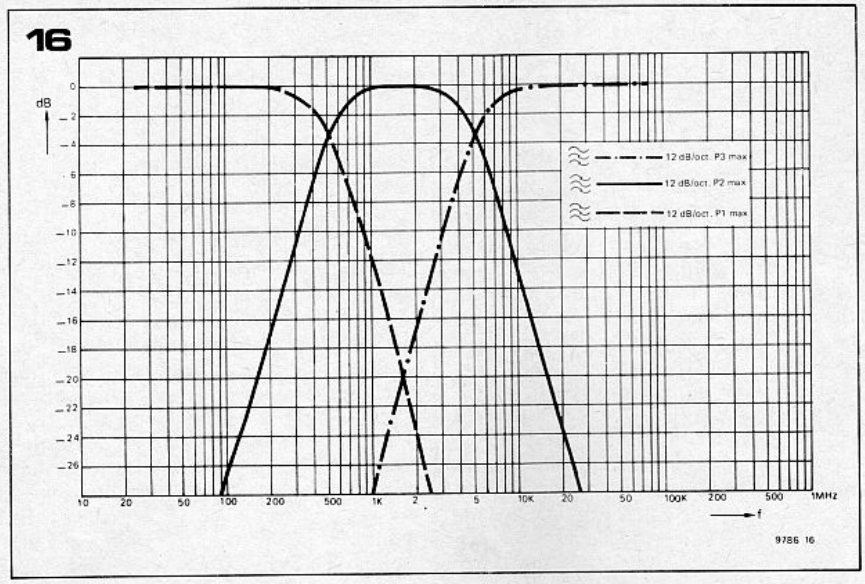


Figure 1f. A few frequency-response plots, with slopes of 12 and 18 dB/octave and one or two crossovers, as an aid to interpretation of table 1.





– When the filter provides a symmetrical two-way crossover with 12 dB/octave slopes, the tweeter should be connected in opposite sense to the woofer-midrange unit.

⊕ ⊖
L H
⊖ ⊕

– The problem is different with 18 dB/octave and 6 dB/octave slopes, where the phase shift in the filters at crossover totals 270° or 90°. It is convenient to connect all speakers in the same sense in these cases.

The loudspeaker-coupling electrolytic capacitors in the midrange and treble channels can in principle be given a smaller value than that in the woofer channel, thus saving space and cost. However, one must bear in mind that a smaller value component will have a lower alternating current ('ripple') rating. The smallest value that still has a current rating at least equal to the loudspeaker maximum RMS current will usually have a large enough capacitance too. In case of doubt ensure that the RC cutoff point of the capacitor with the loudspeaker's nominal impedance is 3 . . . 5 times *lower* than the high-pass crossover frequency in the channel concerned. The factor 3 . . . 5 should also be observed with the woofer! This results in the well-known rule of thumb:

$$C = \frac{10^5}{f_c} \quad (\mu F),$$

where f_c is the lower crossover frequency.

Nothing useful is gained (and there is a risk of too much phase shift or amplitude rolloff being caused) by also reducing the values of the input coupling capacitors of the midrange and treble amplifiers. C16 and C21 in the filter are 'unnecessarily large' for the same reason.

One final remark concerns the function of the presets P1, P2 and P3. These are *not* intended as tone control adjustments! They should be used only to compensate for possibly unequal sensitivities of the individual amplifier-speaker channels. Deliberate maladjustments of not more than 3 dB (tone controls after all!) may however occasionally be permissible.

Component list for figures 5 and 6.

Resistors:

R1,R2	= 220 k
R3,R8,R14, R19[1],R24[1]	= 5k6
R4,R9,R15, R20[1],R25[1]	= 2k2
R5[2]	see table 3
R6[3]	see table 3 or 5
R7	see table 3, 5 or 7
R10[4]	see table 4
R11[5]	see table 4 or 6
R12,R13	see table 4, 6 or 8
R16[2,6]	see table 3
R17[3,6],R18[1]	see table 3 or 5
R21[1,4]	see table 4
R22[1],R23[1],R26[1]	see table 4 or 6
P1,P2,P3[1]	10 k preset

Capacitors:

C1	= 470 n
C2,C6,C11, C15[1],C20[1]	= 4n7
C3[4]	see table 3
C4[5]	see table 3 or 5
C5	see table 3, 5 or 7
C7,C16,C21[1]	= 10 µ/25 V
C8[2]	see table 4
C9[3]	see table 4 or 6
C10	see table 4, 6 or 8
C12[1,4]	see table 3
C13[6],C14[1]	see table 3 or 5
C17[1,2]	see table 4
C18[1],C19[1]	see table 4 or 6
C22	= 100 µ/40 V
C23,C24,C25, C26[1],C27[1]	= 100 n

Semiconductors:

T1,T3,T5,T7[1], T9[1]	BC107 B, BC547 B or equivalent
T2,T4,T6,T8[1], T10[1]	BC177 B, BC557 B or equivalent

Footnotes

[1] means: omit part for two-way filter set
[2] means: replace by wire link for 12 dB/oct and 6 dB/oct.
[3] means: replace by wire link for 6 dB/oct.
[4] means: omit this part for 12 dB/oct or 6 dB/oct.
[5] means: omit this part for 6 dB/oct.
[6] means: replace by wire link for two-way filter set.

NB. The 6 dB/octave slopes are only useful in a very limited number of two-way system designs– the tables therefore do not give values for three-way design.

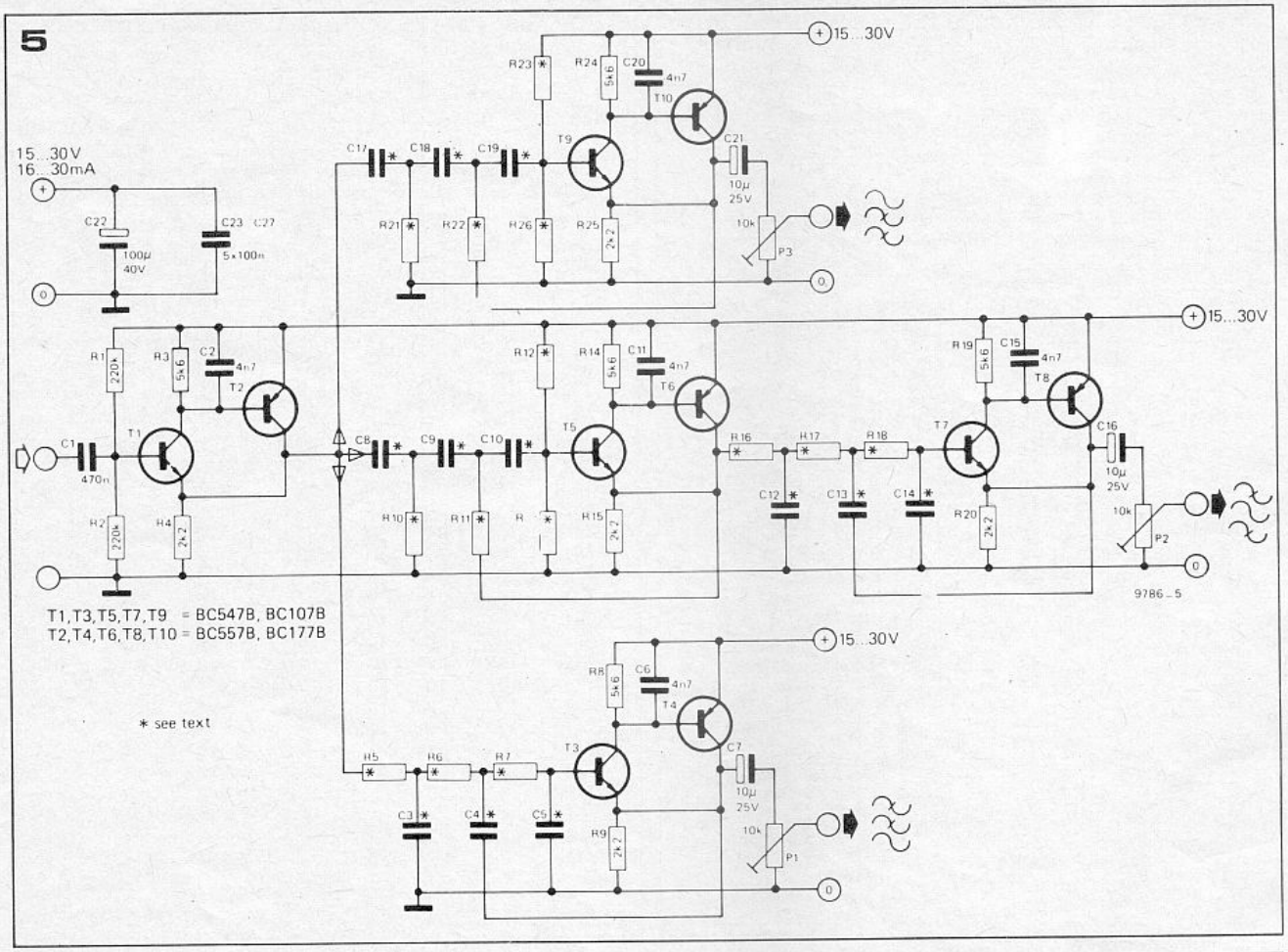
Figure 15. Frequency response of the figure 5 circuit, as measured with f1 set at 500 Hz and f2 at 5 kHz.

Figure 16. Frequency response of the figure 7 circuit with the same crossover points as figure 15.

Figure 5. Complete circuit diagram of an active filter set for two symmetrical 18 dB/octave crossovers (three-way).

Figure 6. Component layout and p.c. board copper-side plan for the figure 5 circuit. (EPS 9786)

5


15...30V
16...30mA
15...30V
15...30V
15...30V
T1,T3,T5,T7,T9 = BC547B, BC107B
T2,T4,T6,T8,T10 = BC557B, BC177B
* see text
9786-5

6

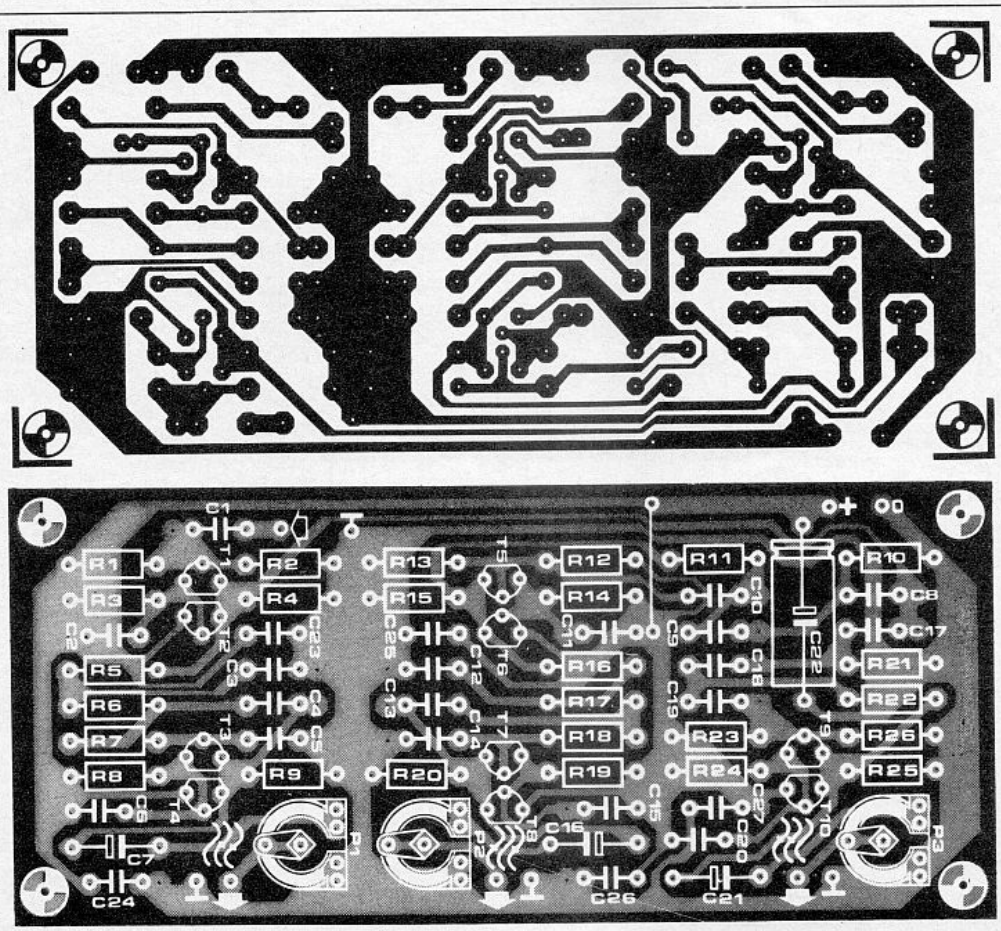


Table 1.

The different possible combinations of symmetrical or asymmetrical crossovers and 12 or 18 dB/octave slopes.

filters slopes at f_1 to be		filters slopes at f_2 to be		combine from figure 1f	refer to figures
18	12	18	18	2, 4, 6 & 7	
18	12	12	12	2, 4, 5 & 8	
18	12	18	12	2, 4, 6 & 8	
18	12	12	18	2, 4, 5 & 7	
12	18	18	18	1, 3, 6 & 7	
12	18	12	12	1, 3, 5 & 8	
12	18	18	12	1, 3, 6 & 8	
12	18	12	18	1, 3, 5 & 7	
18	18	18	18	2, 3, 6 & 7	5 & 6
18	18	12	12	2, 3, 5 & 8	
18	18	18	12	2, 3, 6 & 8	
18	18	12	18	2, 3, 5 & 7	
12	12	18	18	1, 4, 6 & 7	
12	12	12	12	1, 4, 5 & 8	7 & 8
12	12	18	12	1, 4, 6 & 8	
12	12	12	18	1, 4, 5 & 7	
18	18	–		2 & 3	9 & 10
12	12	–		1 & 4	11 & 12
12	18	–		1 & 3	
18	12	–		2 & 4	

Table 2.

response (see figure 1f)	1	2	3	4	5	6	7	8	9	10
component										
R5			t3	wl					wl	
R6			t3	t5					wl	
R7			t3	t5					t7	
C3			t3	–					–	
C4			t3	t5					–	
C5			t3	t5					t7	
C8	wl	t4								wl
C9	t6	t4								wl
C10	t6	t4								t8
R10	–	t4								–
R11	t6	t4								–
R12	t6	t4								t8
R13	t6	t4								t8
R16							t3	wl		
R17							t3	t5		
R18							t3	t5		
C12							t3	–		
C13							t3	t5		
C14							t3	t5		
C17					wl	t4				
C18					t6	t4				
C19					t6	t4				
R21					–	t4				
R22					t6	t4				
R23					t6	t4				
R26					t6	t4				
see figure	3b	2b	2a	3a	3b	2b	2a	3a	4a	4b

Cross-reference table of frequency-determining components, starting from the 'available response curves' of figure 1f. The components are numbered as in the complete circuit and layout diagrams (figures 5 & 6); t3 . . . t8 are the value-table references, 'wl' means 'wire link' and '–' means 'omit'.

Table 3.

The 18 dB/octave low-pass filter, having the response given in figure 2a, with the nominal crossover frequencies obtainable using E12 series component values.

f (Hz)	R (kΩ)			C_a (nF)	C_b (nF)	C_c (nF)
f1	R5	R6	R7	C3	C4	C5
f2	R16	R17	R18	C12	C13	C14
97	10	10	10	220	560	33
119	10	10	10	180	470	27
146	10	10	10	150	390	22
179	10	10	10	120	330	18
214	10	10	10	100	270	15
268	10	10	10	82	220	12
322	10	10	10	68	180	10
392	10	10	10	56	150	8.2
472	10	10	10	47	120	6.8
574	10	10	10	39	100	5.6
684	10	10	10	33	82	4.7
824	10	10	10	27	68	3.9
974	10	10	10	22	56	3.3
1191	10	10	10	18	47	2.7
1461	10	10	10	15	39	2.2
1786	10	10	10	12	33	1.8
2143	10	10	10	10	27	1.5
2679	10	10	10	8.2	22	1.2
3215	10	10	10	6.8	18	1
3921	8.2	8.2	8.2	6.8	18	1
4728	6.8	6.8	6.8	6.8	18	1
5742	5.6	5.6	5.6	6.8	18	1
6841	4.7	4.7	4.7	6.8	18	1
8244	3.9	3.9	3.9	6.8	18	1
9743	3.3	3.3	3.3	6.8	18	1

Table 4.

The 18 dB/octave high-pass filter, having the response given in figure 2b, with the nominal crossover frequencies obtainable using E12 series component values.

f (Hz)	R_a (kΩ)	R_b (kΩ)	R_c (kΩ)	C (nF)
f1	R10	R11	R12 = R13	C8 = C9 = C10
f2	R21	R22	R23 = R26	C17 = C18 = C19
114	10	3.9	150	100
139	10	3.9	150	82
168	10	3.9	150	68
204	10	3.9	150	56
243	10	3.9	150	47
293	10	3.9	150	39
346	10	3.9	150	33
423	10	3.9	150	27
519	10	3.9	150	22
635	10	3.9	150	18
762	10	3.9	150	15
952	10	3.9	150	12
1140	10	3.9	150	10
1390	10	3.9	150	8.2
1680	10	3.9	150	6.8
2040	10	3.9	150	5.6
2430	10	3.9	150	4.7
2930	10	3.9	150	3.9
3460	10	3.9	150	3.3
4230	10	3.9	150	2.7
5190	10	3.9	150	2.2
6350	10	3.9	150	1.8
7620	10	3.9	150	1.5
9520	10	3.9	150	1.2
11400	10	3.9	150	1

How to use the tables.

- Decide on the type of filter required, and refer to figure 1f and/or table 1 for the 'shorthand notation'. Note that responses 9 and 10 are 6 dB/oct low-pass and high-pass, respectively; these are not shown in figure 1f.
- Proceed to table 2. Under each of the (two or four) chosen response curves, further information is given regarding a group of frequency-determining components. This can be either 'wl' (wire link), '–' (omit) or reference to one of the tables 3 . . . 8 (e.g. 't3' means 'refer to table 3').
- Proceed to the tables referred to. As an example, assume that slope 3 is required at a lower crossover frequency f1 = 400 Hz. Under response 3, table 2 refers to table 3 for R5 . . . R7 and C3 . . . C5. Proceeding to table 3, the nearest frequency to the desired 400 Hz is 392 Hz. For this frequency, the values of R5 . . . R7 are shown as 10 kΩ, C3 = 56 n, C4 = 150 n and C5 = 8n2.

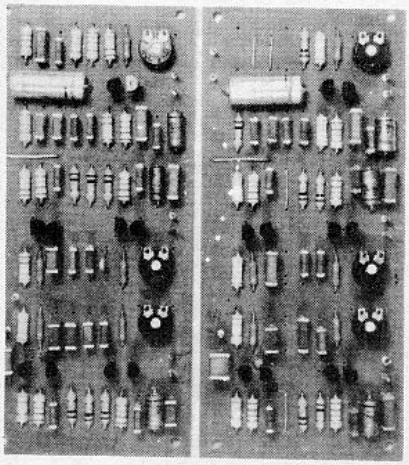


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Table 5.

The 12 dB/octave low-pass filter, having the response given in figure 3a, with the nominal crossover frequencies obtainable using E12 series component values.

f (Hz)	R (kΩ)	C_b (nF)	C_c (nF)
f1	R6 = R7	C4	C5
f2	R17 = R18	C13	C14
102	22	100	47
125	18	100	47
150	15	100	47
188	12	100	47
225	10	100	47
274	10	82	39
331	10	68	33
402	10	56	27
479	10	47	22
577	39	10	4.7
682	33	10	4.7
834	27	10	4.7
1020	22	10	4.7
1250	18	10	4.7
1500	15	10	4.7
1880	12	10	4.7
2250	10	10	4.7
2740	10	8.2	3.9
3310	10	6.8	3.3
4020	10	5.6	2.7
4790	10	4.7	2.2
5840	8.2	4.7	2.2
7040	6.8	4.7	2.2
8550	5.6	4.7	2.2
10190	4.7	4.7	2.2

Table 6.

The 12 dB/octave high-pass filter, having the response given in figure 3b, with the nominal crossover frequencies obtainable using E12 series component values.

f (Hz)	C (nF)	R_b (kΩ)	R_c (kΩ)
f1	C9 = C10	R11	R12 = R13
f2	C18 = C19	R22	R23 = R26
113	100	10	39
137	82	10	39
165	68	10	39
201	56	10	39
239	47	10	39
289	39	10	39
341	33	10	39
417	27	10	39
511	22	10	39
625	18	10	39
750	15	10	39
938	12	10	39
1130	10	10	39
1370	8.2	10	39
1650	6.8	10	39
2010	5.6	10	39
2390	4.7	10	39
2890	3.9	10	39
3410	3.3	10	39
4170	2.7	10	39
5110	2.2	10	39
6250	1.8	10	39
7500	1.5	10	39
9380	1.2	10	39
11300	1	10	39

Table 7.

The 6 dB/octave low-pass filter, having the response given in figure 4a, with the nominal crossover frequencies obtainable using E12 series component values.

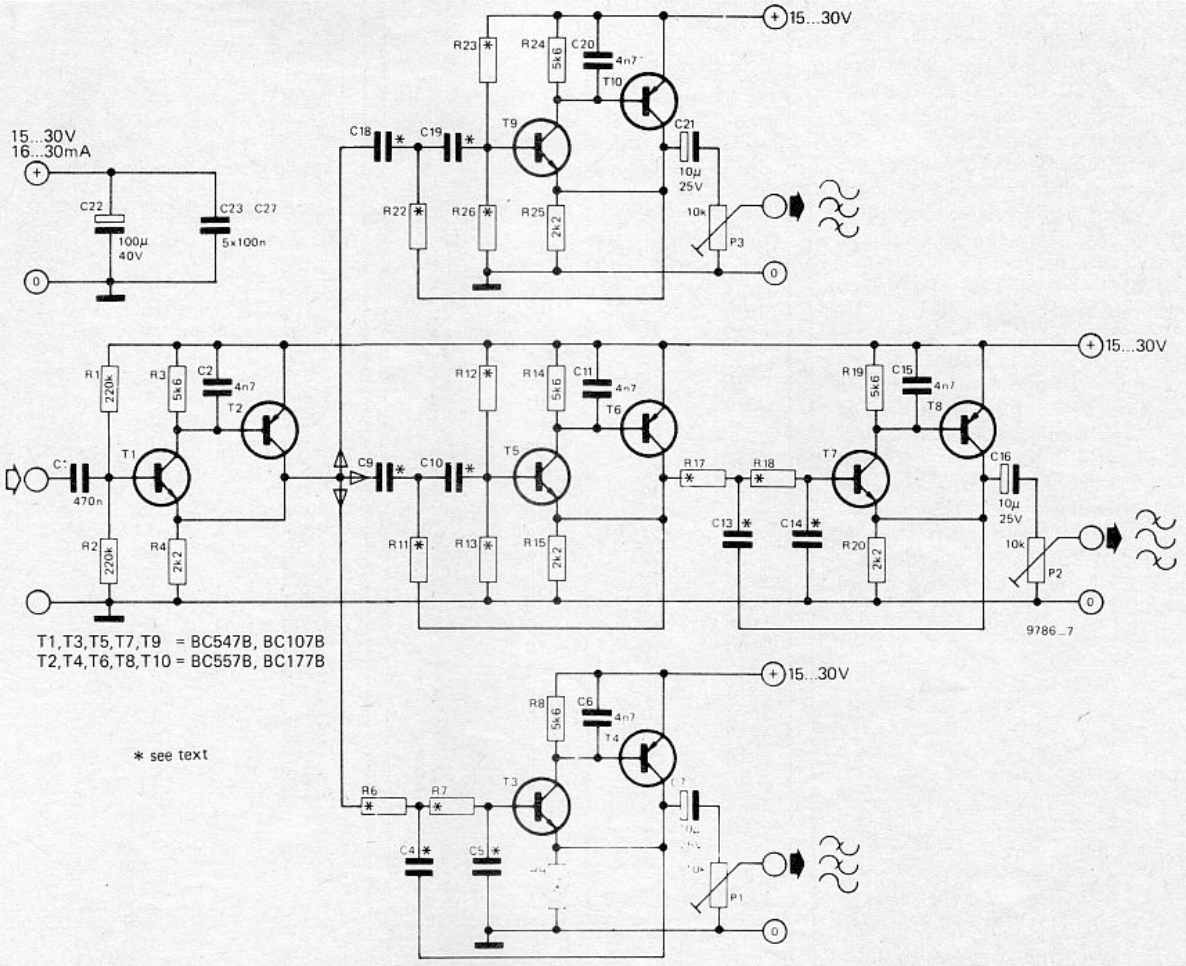
f (Hz)	R (kΩ)	C_c (nF)
f1	R7	C5
106	10	150
133	10	120
159	10	100
194	10	82
234	10	68
284	10	56
339	10	47
408	10	39
482	10	33
589	10	27
723	10	22
884	10	18
1060	10	15
1330	10	12
1590	10	10
1940	10	8.2
2340	10	6.8
2840	10	5.6
3390	10	4.7
4080	10	3.9
4820	10	3.3
5890	10	2.7
7230	10	2.2
8840	10	1.8
10600	10	1.5

Table 8.

The 6 dB/octave high-pass filter, having the response given in figure 4b, with the nominal crossover frequencies obtainable using E12 series component values.

f (Hz)	R_c (kΩ)	C(nF)
f1	R12 = R13	C19
106	22	150
133	22	120
159	22	100
194	22	82
234	22	68
284	22	56
339	22	47
408	22	39
482	22	33
589	22	27
723	22	22
884	22	18
1060	22	15
1330	22	12
1590	22	10
1940	22	8 2
2340	22	6.8
2840	22	5.6
3390	22	4.7
4080	22	3.9
4820	22	3.3
5890	22	2.7
7230	22	2.2
8840	22	1.8
10600	22	1.5

7



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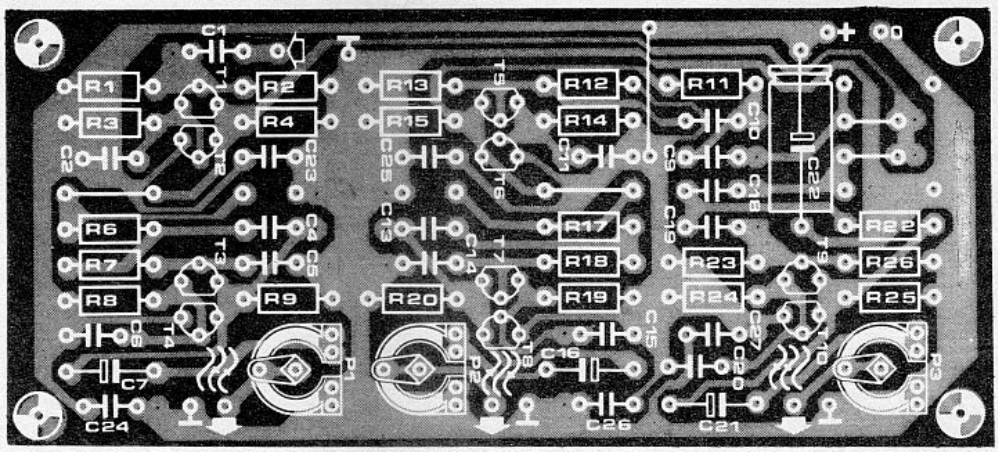


3 - way, 12 dB/oct.

As an example, assume that a three-way 12 dB/oct. filter system is required (slopes 1, 4, 5 and 8 in figure 1f) with crossover frequencies f1 = 400 Hz and f2 = 3 kHz.

Referring to table 2: for slope 1, C8 = wire link; R10 = omitted; C9, C10, R11 . . . R13 are to be found from table 6. In the latter table, the nearest frequency to the desired f1 is 417 Hz. The corresponding component values are given as C9 = C10 = 27 n; R11 = 10 k; R12 = R13 = 39 k.

Back to table 2: for slope 4, R5 = wire link; C3 = omitted; R6, R7, C4 and C5 are to be found from table 5. Proceeding to this table, the component values corresponding to f1 = 402 Hz are shown as R6 = R7 = 10 k; C4 = 56 n and C5 = 27 n.

Back to table 2: for slope 5, C17 = wire link; R21 = omitted; C18, C19, R22, R23 and R26 are to be found from table 6. For f2 = 2890 Hz (the closest to the desired 3 kHz), this table gives the component values: C18 = C19 = 3n9; R22 = 10 k; R23 = R26 = 39 k.

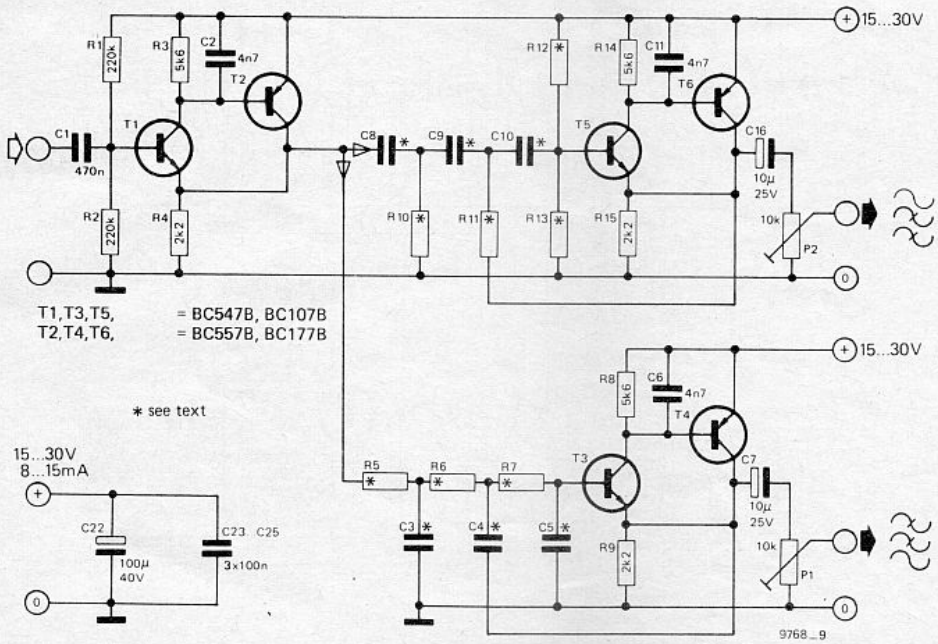
Now table 2 again: for slope 8, R16 = wire link; C12 = omitted; R17, R18, C13 and C14 are to be found from table 5. For f2 = 2740 Hz, this results in R17 = R18 = 10 k; C13 = 8n2; C14 = 3n9.

Finally, referring to the parts list for figure 6 gives all other component values. Note that the footnotes 2 and 4 are valid in this case (12 dB/oct); however, we had already found these wire links and omitted parts from table 2.

Figure 7. Circuit diagram of an active three-way filter with symmetrical 12 dB/octave crossovers.

Figure 8. Parts layout modified for the figure 7 circuit.

9



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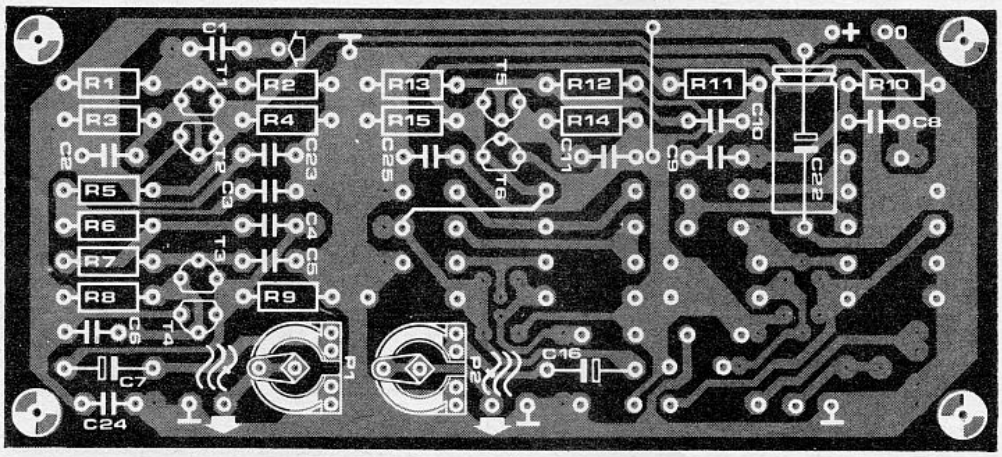


2-way, 18 dB/oct.

The two-way filter is assembled on the same board. In this case T6 collector has to be linked with the 'hot' side of C16– no matter which filter slopes are chosen – and the gain of the 'high' channel is preset by P2.

Correct use of the tables should produce this result automatically. As an example, assume that slopes 2 and 3 are required at a crossover frequency f1 = 500 Hz. For slope 2, table 2 refers to table 4 for the following components: C8 . . . C10 and R10 . . . R13. For slope 3, the table refers to table 3 for R5 . . . R7 and C3 . . . C5.

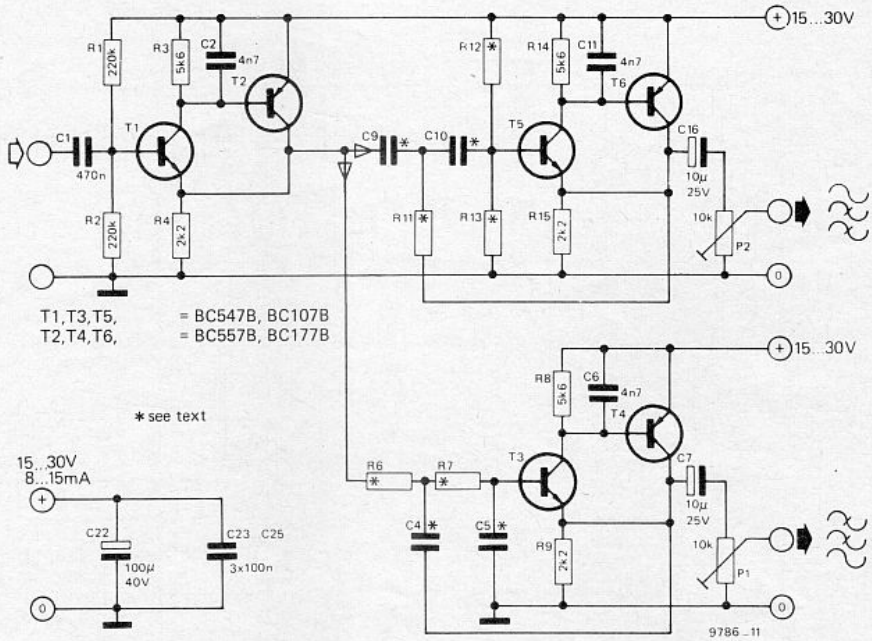
Proceeding first to table 4, the component values for f1 = 519 Hz are found to be: R10 = 10 k, R11 = 3k9, R12=R13=150k,C8 = C9 = C10 = 22n. Referring now to table 3, the component values for f1 = 472 Hz are found to be: R5 = R6 = R7 = 10 k; C3 = 47 n; C4 = 120 n; C5 = 6n8.

Finally, the parts list for figure 6 gives all other components. Footnote 1 is valid in this case: 'omit this part for two-way filter set'. This turns out to mean that T9 and T10 (figure 5) are omitted, with all associated components; T7 and T8 are also omitted, with all associated components. Furthermore, footnote 6 is valid: 'replace by wire link for two-way filter set'. This refers to R16, R17 and C13, giving the required through path from T6 to C16. Note however that on the component layout a single wire link is shown, direct from one end of R16 to one end of C13. This will also work of course . . .

Figure 9. Two-way circuit with symmetrical 18 dB/octave crossover.

Figure 10. Parts layout modified for the figure 9 circuit.

11



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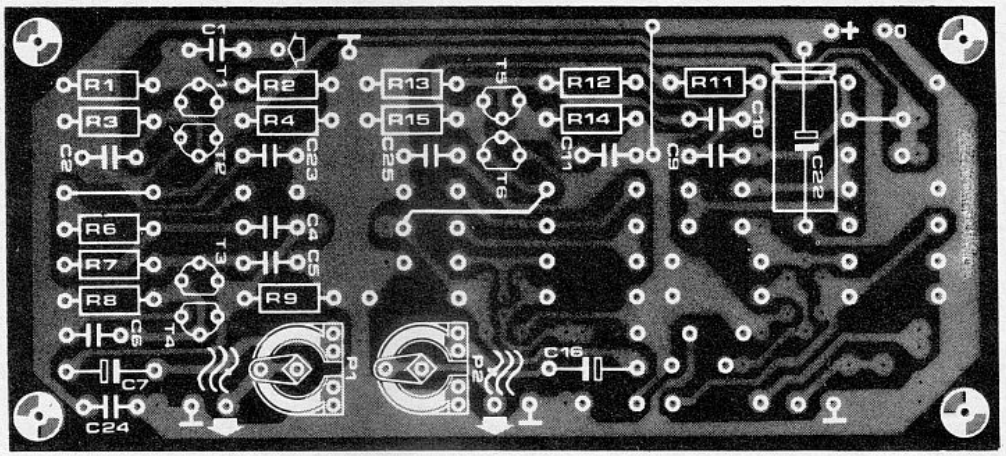


2-way, 12 dB/oct.

In figure 1f, the required slopes are numbered 1 and 4. Assume that the crossover frequency is to be f1 = 1 kHz.

As before, the first table to look at is table 2. For slopes 1 and 4, C8 and R5 both have to be replaced by wire links; R10 and C3 are omitted; the values for C9, C10 and R11 . . . R13 are to be found from table 6; the values for R6, R7, C4 and C5 are to be found from table 5.

First table 6. For f1 = 938 Hz, the component values are given as follows: C9 = C10 = 12 n; R11 = 10 k; R12 = R13 = 39 k.

Now table 5. Here the nearest frequency given is f1 = 1020 Hz. The corresponding component values are: R6 = R7 = 22 k; C4 = 10 n; C5 = 4n7.

Finally, check the parts list. In this case, footnotes 1, 2, 4 and 6 are all valid. In other words, components marked either [1] or [4] are to be omitted and components marked either [2] or [6] are to be replaced by wire links.

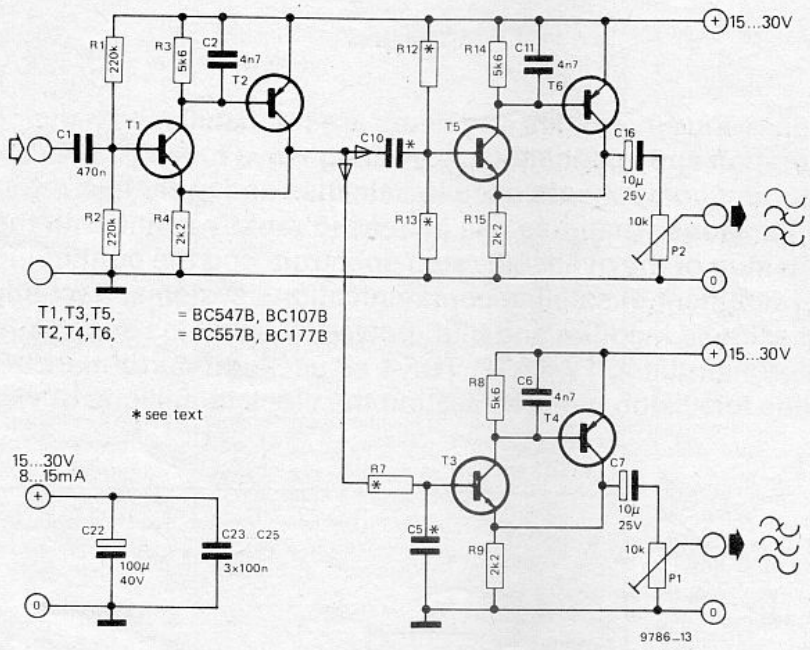
To sum it up, the complete parts list for this example would be:

Resistors:
R1,R2 = 220 k
R3,R8,R14 = 5k6
R4,R9,R15 = 2k2
R5 = wire link
R6,R7 = 22 k
R11 = 10 k
R12,R13 = 39 k
R16,R17 = wire link
P1,P2 = 10 k preset

Capacitors:
C1 = 470 n
C2,C6,C11 = 4n7
C4 = 10 n
C5 = 4n7
C7,C16 = 10 µ/25 V
C8 = wire link
C9,C10 = 12 n
C13 = wire link
C22 = 100 µ/40 V
C23,C24,C25 = 100 n

Semiconductors:
T1,T3,T5 = BC107 B or equivalent
T2,T4,T6 = BC177 B or equivalent

13



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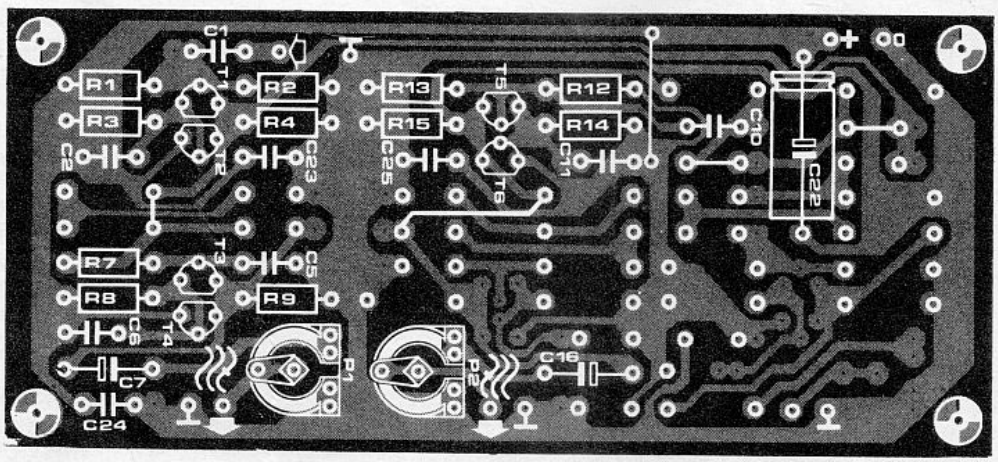

Figure 11. Two-way circuit with symmetrical 12 dB/octave crossover.

Figure 12. Parts layout modified for the figure 11 circuit.

Figure 13. 6 dB/octave two-way circuit diagram.

Figure 14. Parts layout modified for the figure 13 circuit.

2-way, 6 dB/oct.

Before going any further, it should be stated clearly that 6 dB/oct slopes are only useful in a very limited number of applications. They should be used with caution, since there is always a danger of destroying the high-range loudspeaker.

However, for completeness' sake an example is given here: two-way, 6 dB/oct (slopes 9 and 10, not shown in figure 1f), with a crossover frequency f1 = 4 kHz.

Table 2 specifies a wire link for R5, R6, C8 and C9; C3, C4, R10 and R11 are to be omitted. The values for R7 and C5 are to be taken from table 7; the values for C10, R12 and R13 are to be taken from table 8.

For f1 = 4080 Hz, table 7 specifies R7 = 10 k and C5 = 3n9.

For f1 = 4080 Hz, table 8 specifies R12 = R13 = 22 k and C19 = 3n9.

In this case, all 6 footnotes in the parts list are valid . . . Since footnotes 1, 4 and 5 are valid, the following components should be omitted: R10, R11, R18 . . . R26; P3; C3, C4, C12, C14, C15, C17 . . . C21, C26, C27; T7 . . . T10. Furthermore, since footnotes 2, 3 and 6 are valid, the following components are to be replaced by wire links: R5, R6, R16, R17; C8, C9, C13. Note that C17 has already been eliminated by footnote 1, and is therefore not replaced by a wire link when we get to footnote 2!

TRAVELLING-WAVE TUBES

B. Higgins

Although many electronics engineers are not familiar with their basic operation and applications, travelling-wave tubes (TWTs) are important components used in satellites and other microwave applications. Their use has increased rapidly in line with the widening of the available radio spectrum and the continuing development of satellite communications systems. Recently commissioned medium and high-power TV satellites such as Astra 1A, DFS Kopernikus, TV-SAT2, TDF-1 all use high-performance TWTs to provide television pictures around the clock to millions of viewers.

A travelling-wave tube is an electronic amplifier for microwave radio signals. It is not, strictly speaking, a thermionic tube, but rather a complete wideband RF power amplifier in a vacuum envelope. Originally developed in the mid 1940s, TWTs have been improved considerably since then. In particular, their power efficiency has gone up over the years from a modest 10 to 20% to nearly 50% for the latest types used in direct-broadcasting TV satellites.

The radio signals produced by TWTs are normally in the frequency range from 2 GHz to 22 GHz, spanning the S, C, X, Ku and Ka bands. Table 1 lists the 10 different TWTs operating at frequencies spread across these radio bands.

The outstanding feature of the TWT is its high power gain of 30 dB to 55 dB. This means that an input power of less than 1 mW is sufficient to achieve an output power of tens of watts across a wide frequency range. Disadvantages of the TWT are its size and weight, relatively low efficiency, and high-voltage power supply requirement.

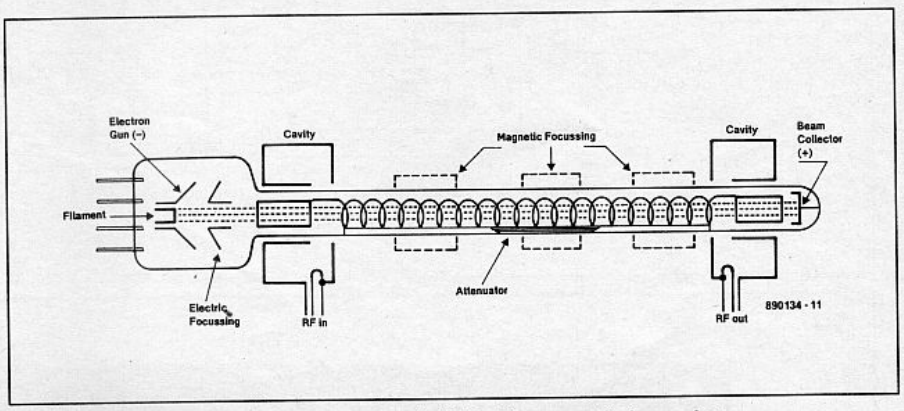

Fig. 1. Basic helix travelling-wave tube (TWT) with magnetic focussing.

How it works

The principle of operation is illustrated in Fig. 1. The electron beam produced by a filament, cathode and associated gun structure travels along the axis of the TWT, before being collected by one or more electrodes (collectors). The helical circuit spaced closely around the beam axis has a structure that causes it to propagate an RF wave that is slow with respect to the speed of light. The helix propagation velocity depends on the power rating of the TWT, and is typically 10–30% of the speed of light. An input cavity is provided to couple the RF signal to the 'slow' wave structure. The amplified RF output signal is similarly taken from a cavity.

The collector voltage and filament emission are accurately controlled so that the velocity of the electron stream is approximately the same as the axial phase velocity of the RF input wave on the circuit. If the helix is properly proportioned, its phase velocity is almost independent of frequency over a wide range. It is, therefore, not uncommon for a TWT to have a bandwidth of more than an octave.

The electron stream is density-modulated because the longitudinal component of the field generated by the 'slow' wave interacts with the electrons travelling in approximate synchronism with it. The result of the modulation is that the electron stream induces additional waves on the helix. Thus, along the length of the tube, a portion of the direct-current energy of the

Frequency Range (GHz)	Output power (W)	Mass (kg)	Type number	Manufacturer	Radio band
2.5 to 8	500	4.5	500CW	Teledyne	S
3.5 to 12	30	0.68	QKW5004	Raytheon	S
3.7 to 4.2	10	0.68	TL4010	AEG	S
4.5 to 10	1.5	0.9	N1078	EEV	C
7.9 to 8.4	60	–	N10025	EEV	C
6 to 18	40	0.68	QKW5005	Raytheon	X
8 to 18	2	0.7	N10024	EEV	X
12 to 12.8	20	0.7	TL12019	AEG	Ku
14 to 14.5	200	3.2	Ku200W	Teledyne	Ku
29 to 31	12	1	TL30011	AEG	Ka

Table 1. Across the spectrum spread: listing of ten TWTs capable of working at different bands in the radio frequency spectrum.

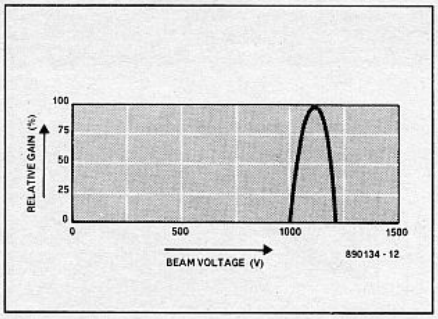

Fig. 2. Typical relative TWT power gain as a function of accellerating voltage.

electron stream is transferred to the circuit as RF energy, resulting in amplification of the RF input wave.

The all-important synchronism between the electron beam and the RF requires accurate control of the accelerating voltage, which is by no means simple to implement in a spacecraft. The graph in Fig. 2 shows the typical dependency of the RF power gain on the beam accelerating voltage.

Magnetic focusing

In order to control the physical size of the electron beam in a TWT a focusing field is required, providing a strength that enables the charge forces to be compensated that would otherwise cause excessive beam divergence. The need of weight and size reductions in satellites have forced the development of permanent-magnet focussing structures in which the field is reversing periodically. Owing to various technical limitations, electrostatic focusing has not (yet) proved a viable alternative to magnetic focusing.

A carbon-based attenuator structure is often fitted along the beam axis to enhance the stability of the TWT (at gains of more than 50 dB, oscillation is a real hazard).

THEORETICAL BACKGROUND TO TRAVELLING-WAVE TUBES

The electron velocity, v, in cm/s is a function of the accelerating voltage, V, as expressed in

$$v = 5.93 \times 10^7 V^{1/2}$$

The approximate power gain, G, in decibels, of a TWT may be calculated from

$$G = A + BCN$$

where
A is the initial mode establishing loss on the helix. Typical values are –6 dB to –9 dB;
B is a gain coefficient representing circuit attenuation and space charge;
C is a gain parameter determined by the impedances of the circuit and the electron stream;
N = the number of active wavelengths in the tube.
Factor C is accounted for by

$$C = \sqrt[3]{\frac{E^2}{(\omega/v)^2} P \times \left(\frac{I_0}{8 V_0}\right)}$$

and N by

$$N = (l/\lambda_0)(c/v)$$

where
I_0 = beam current
V_0 = beam voltage
l = axial length of the helix
λ_0 = free-space wavelength
v = phase velocity of wave along tube
c = speed of light.

Voltages and currents

To obtain maximum efficiency from a TWT, its operating voltages are all-important. There are 3 main voltages to consider: the collector voltages, the helix voltage, and the heater voltage. Table 2 list the voltage and current specifications of a number of TWTs.

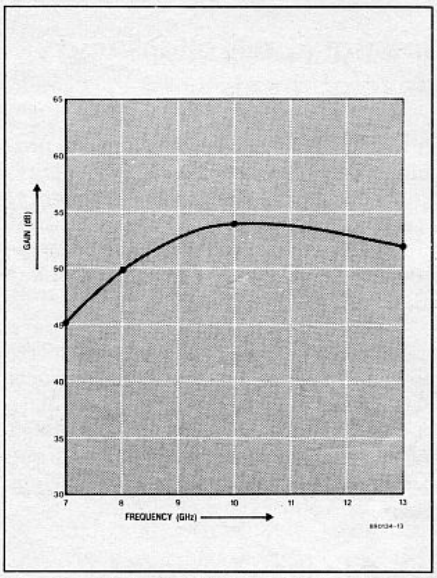

Fig. 3. Typical TWT small-signal gain characteristics.

Collector voltages are usually of the order of 2 kV, although the current trend is towards voltages below 1 kV. Collector current is typically between 20 mA and 1 A. Voltage regulation to within 10% is required for reasons outlined above. Multiple collectors can help to increase efficiency.

Helix voltages are typically between 2 kV and 10 kV, and currents between 10 mA and 500 mA.

The heater voltage, finally, is between 3.5 V and 6.3 V at a current demand of 0.5 A to 2.5 A. The filament heats up the cathode to a temperature of about 650 °C to enable electron emission to take place.

Type	Voltage (kV)				Current (mA)					
	Collector 1	Collector 2	Helix	Heater (V)	Cathode	Collector	Helix	Heater (A)	Efficiency (%)	Gain (dB)
500CW	4.2	2.2		6.3	650		65	3.4		
QKW5004	1.45		2.5	6.3		135				55
TL4010			1.55		37				40	
N1078	2		2		25					37
N10025	2.1				49				34	28
QKW5005	1.8		3.8	6.3		135	12	0.5		40
N1024	2.5		2.5			22				
TL12019			4.2		44				37	
Ku200W	8.6			6.3	215		3	1.4		
TL30011			5		38				29	

Table 2. Electrical characteristics of a selection of TWTs.

Special applications and developments

Pulsed TWTs have been developed to produce a short coherent burst of RF energy, for radar applications. The frequency, bandwidth and peak-power specifications of these special TWTs have been optimized to meet the demands of radar users.

Modern metallurgical processes have enabled TWTs to be produced with a low mass and special alloy focusing magnets that give accurate beam control. Low mass of the TWT and, of course, its associated multi-voltage power supply, are prime considerations to keep the payload weight of launch vehicles to a minimum.

What to look forward to

Recent history has seen industry commitment for delivery of amplifiers that cover the frequency range of 10.7 GHz to 12.7 GHz, mainly as a result of the increasing use of satellite-TV in the communications and direct-broadcasting segments of the X and Ku radio bands. Tube designs that can address this whole bandwidth are in the inventory of a number of major TWT manufacturers including Telefunken, Varian Associates, T-CSF and Hughes EDD. It is important, however, to recognize that new circuit technologies based on 2-stage collectors are showing promise of efficiencies previously associated only with 4-stage collector designs. In addition, these 2-stage collector designs are expected to yield substantially improved phase linearity over 'classic' designs and could, to a large extent, help to remove, or at least relax the requirements of, linearization devices from future TWT systems.

Research has shown that a typical Ku-band satellite-TV TWT with a bandwidth of 2 GHz and a 2-stage collector may be expected to exhibit greater than 50% efficiency with a 4-stage depressed collector. The previously mentioned developments in TWT technology, however, allow devices to be produced that provide efficiencies up to 54% with 2-stage collectors. In these new TWTs, the 2-stage collector has not been modified. The circuit improvement, which primarily involves optimization of velocity taper techniques, produces beam efficiencies of the order of 27–30%, which is significant at X and Ku-band frequencies. In addition, these new circuits further reduce phase distortion with typical AM-PM conversion at 2 to 4 dB. Also, third-order intermodulation (IM) products are significantly reduced. At saturation, the two-carrier third-order IM product is not less than 14 dB down from single-carrier saturation.

In conclusion, it is interesting to project the performance, and in particular the efficiency, of TWTs that utilize these new techniques with 3 or 4-stage collectors. Conservative estimates would place minimum TWT efficiency at 58 to 60% for the next generation of low-mass devices.

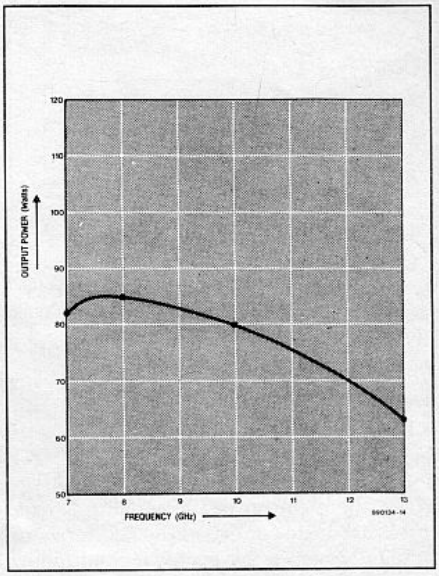

Fig. 4. Typical TWT saturated power output as a function of RF input frequency.

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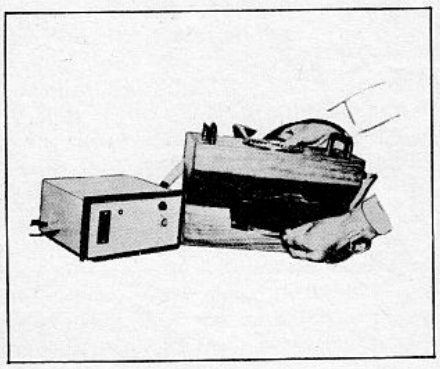

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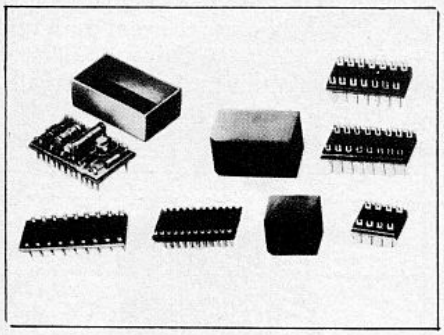

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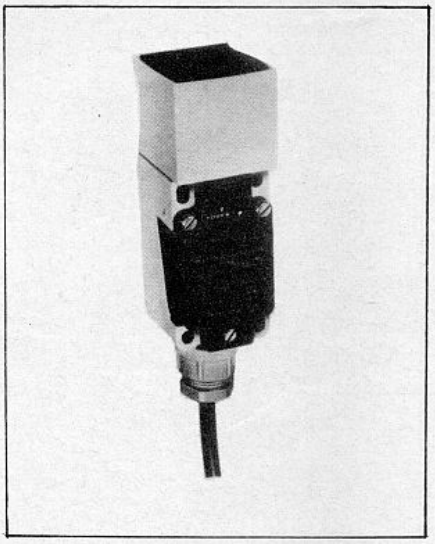

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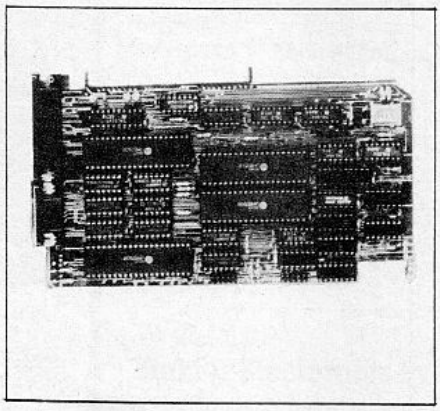

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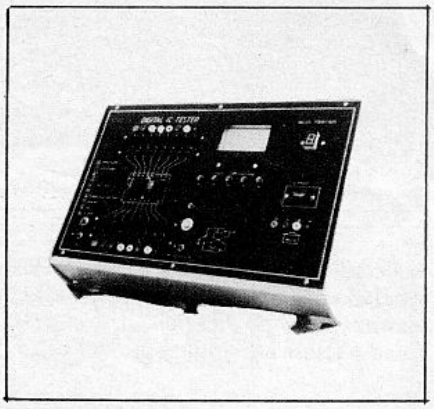

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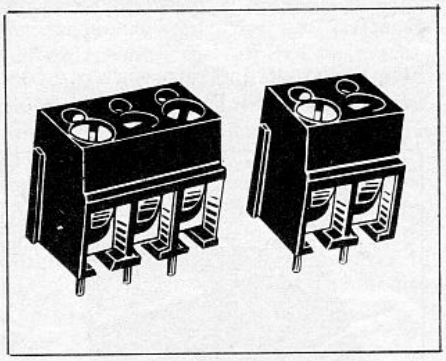

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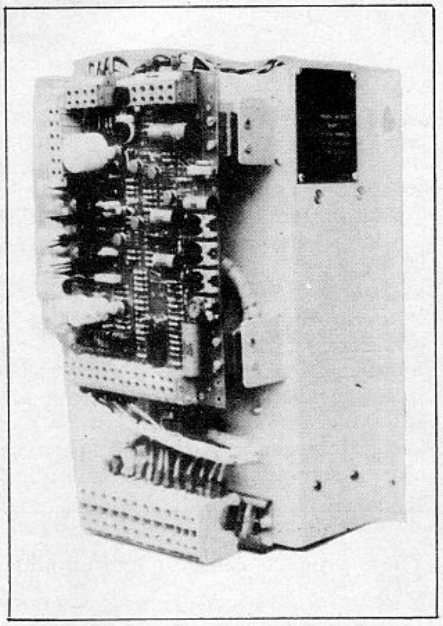
Static Power Systems offers Megacorp Single Phase Powerpacks, manufactured with technology using Thyristor Control, these power packs are primarily used for speed control of DC Motors provided in Plastic extruders, Printing, Rubber and Type Machineries, Welding equipments, Packaging machines etc. Single phase powerpacks are available up to 5 H.P. (3.7 KW) Ratings and can also be used as basic convertor in manufacturing battery chargers, Electroplating rectifiers, Power Control units for ovens, Regulated DC power supplies etc.

Megacorp Power Packs are also available in three phase versions up to 200 KW Ratings and are made of Expoxy coated chasis which can be readily mounted by various OEM's in the main panels of their machines.



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SOLID STATE RELAYS

Satronix have introduced PCB/Chassis Mount solid state relays of 2A, and Amps output current relays. AC input models can accept AC signals ranging from 90 to 280 Volts AC. The DC input signals can be operated from 3 to 32 Volts making them easy to interface to the microprocessors and other logic level devices. Output voltage can be selected from 40 to 280 Volts AC. All relays in the series benefit from zero-voltage turn on as well as the zero current turn-off. Solid-State design without mechanical contacts and associated arcing virtually eliminates electro magnetic interference and transients.

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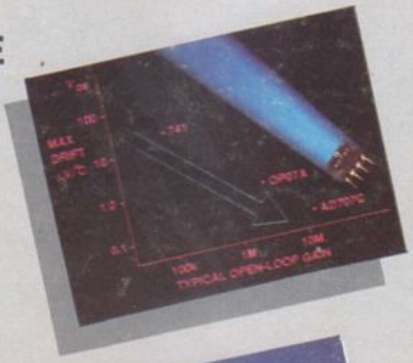
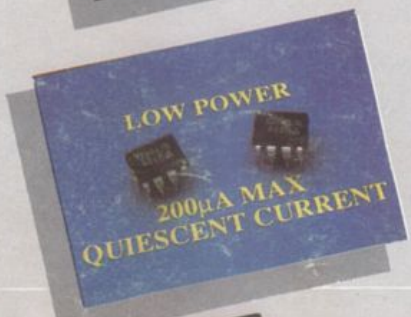


AD 707 JN



AD 548 / 648

PRECISION

The AD 707 features the best d.c. accuracy specification available in a non-chopper stabilized design. It features a maximum input offset voltage of 15 μV (C Grade) & input offset voltage drift of 0.1 μV/°C (C Grade)

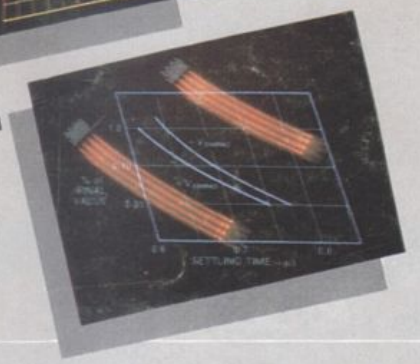
The AD 548/648 features ultra low input bias current-down to 10 p A.

The AD 707/548/648 are available in the plastic MINI-DIP, CERDIP & TO-99 metal can. The AD 707 is also available in an 8 pin plastic small outline (SO) package.

	AD 707 JN	AD 548 JN (Single)	AD 648 JN (Dual)
input bias current	2.5nA	20pA	20pA
input offset voltage	90μV	2mV	2mV
input offset voltage drift	1 μV/°C	20 μV/°C	20 μV/°C
input voltage Noise P-P	0.6 μV	2 μV	2 μV
Price (100's)	$1.37	$0.82	$1.37

Whether it is Precision or speed you can count on the leader – Analog Devices Inc

AD 744 JN



AD 711 / 712 JN

SPEED

The AD 744 is fast settling BIFET op-amp. it can settle to 0.01% (for 10V step) in 500 n sec. (K grade) and to 0.0025% (for 10V step) in 1.5 μ sec (K grade). It also has a slew rate of 75 V/μsec.

The AD 711/712 combines good speed and bias current specifications.

The AD 744/711/712 are available in the plastic MINI-DIP, CERDIP, and TO-99 metal can.

	AD 744 JN	AD 711 JN (Single)	AD 712 JN (Dual)
input bias current	100 pA	50 pA	75 pA
input offset voltage	1 mV	2 mV	3 mV
Setting Time to 0.01%	0.9 μs	1 μs	1 μs
Typical slew rate	75V/μs	20V/μs	20V/μs
Price (100's)	$2.47	$0.88	$1.37

For more details contact your nearest Analog Devices representative in India

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