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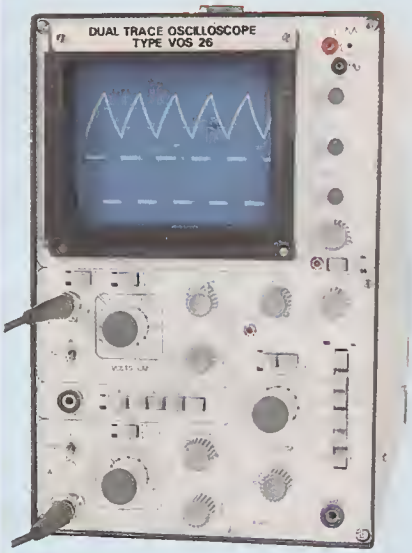

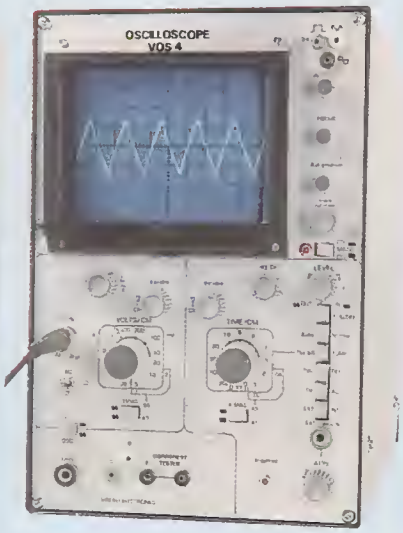

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Front cover

Although the Digital Audio Taperecording system, introduced in Japan earlier this year, has run into difficulties with the combined might of the western world's records producers and composers' and music writers' organizations, it appears that it is here to stay. But, in the absence of prerecarded tapes, the impossibility of recarding from CD players, and a relatively high price, it is probable that it will take a long time before it will make its presence felt on the market.

THE BIRTH OF SATELLITE COMMUNICATIONS

Twenty-five years ago worldwide communications entered a new era. Telstar, the world's first commercial communications satellite, was launched on July 10, 1962, and the first live television signals via satellite were received by British Telecom's Goonhilly earth station in the early hours of the following morning.

In October 1945, the magazine *Wireless World* published an article by Artur C. Clarke, today probably better known as the autor of *2001—A space Odyssey*, entitled *Extra-terrestrial relays—can rocket stations give worldwide radio coverage?*
Arthur C. Clarke commented in his article: "Many may consider the solution proposed in this discussion too farfetched to be taken very seriously." Yet his idea was to prove the blue-print for today's satellite communications network.
He accurately predicted the orbital velocity that a rocket would need to become an artificial satellite, or second moon, circling the world with no expenditure of power. He also predicted that a satellite circling the earth above the equator at a certain height would appear to be stationary to the earth and that three such satellites could give global radio coverage.
He further predicted that development of rocket technology, started by the Germans during the second world war, would soon make it possible to place a satellite in orbit.
Today, reality has caught up with science fiction as British Telecom International-BTI-handles more than three million minutes of telephone calls, television pictures, data, facsimile, and telex, every day through Goonhilly and its other intercontinental links.
About 90 per cent of the world's telephones—some 600 million of them—in 173 countries can be dialled direct from the UK. Telephone services are provided to more than 200 countries and each day more than 500,000 calls are connected from the UK to the other countries.

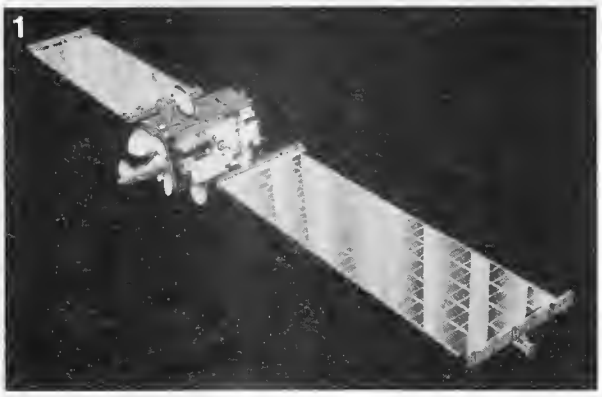


Fig. 1. The Olympus satellite is one of the largest and most powerful in the world. *Photograph courtesey of British Aerospace.*

The early Telstar demonstrations and tests

In the Spring of 1961 it was jointly announced in the United Kingdom, the USA and France that the US National Aeronautics and Space Administration (NASA), the French Centre for Telecommunications Studies and British Telecom, as its predecessor Post Office Telecommunications, would co-operate in a programme for transatlantic testing of communications satellites.
At the same time it was announced that satellite earth stations would be built in England and France "for the reception and transmission of telephone, telegraph and television signals across the Atlantic using satellites to be launched by NASA during 1962 and 1963."
Work began shortly afterwards to build the UK's first satellite station at Goonhilly Downs in Cornwall. The site was chosen because it was as far west as possible to obtain the maximum period of visibility to the United States via the satellite, to be remote from sources of electrical interference, and to provide an onobscured view to the horizon for the longest possible contact with the satellite.
In less than a year from gaining access to the site the station was ready. A massive, steerable dish antenna, weighing 870 tonnes with a 25.9m dish had been built. All of the equipment on the station was of British design and manufacture, with the exception of one American transmitting klystron valve.
The British design was the odd-man-out among the three earth stations to be used for the tests. Both the American station at Andover, Maine, and the French station at Pleumeur Bodou in Britanny were equipped with horn antennas housed in radomes. The British station had cost around £800,000 to complete, about a quarter of the cost of the American and the French stations.
In early July 1962 it was announced that Telstar would be launched from Cape Canaveral on either July 10 or 11.
The successful launch took place at 8.35 GMT on Tuesday, July 10, and the desired orbit was achieved. With Telstar circling the earth at heights varying between 590 and 3500 miles, it was possible to achieve three or four periods during each 24 hours when mutual visibility between Goonhilly and Andover lasted for 30 to 40 minutes.
During these periods the antenna at Goonhilly had to be accurately manoeuvred to follow the satellite from the moment it rose above the horizon until it again disappeared from view. The signal transmitted from the antenna to the satellite was con-

Fig. 2. A small section of Goonhilly Downs Earth Station: in the foreground Aerial No. 7. *Photograph courtesy of British Telecom.*

centrated into a narrow beam, one-fifth of a degree in width, so absolute precision was necessary. To maintain this accuracy in high wind meant that the antenna had to be massive and sturdy. In order to move the antenna so accurately it was equipped with electric motors of some 100 horse power. However, the engineering design resulted in such good balance and smooth movement of the antenna that normaly less than two horse power was required under reasonable weather conditions.

The primary purpose of the Telstar satellite tests was to acquire data on which to base the future design of satellite systems for commercial operation. However, during the period from July 10 to July 27 a number of demonstrations were carried out which illustrated the potentialities of satellite systems for world-wide telecommunications.

In the early hours of July 11 the first usable orbits were the sixth and seventh and the first attempt at television reception was made. Reception was decidedly poor. Some experts were quick to blame Goonhilly's unique antenna design, and *The Times* described the experiment as "an almost total failure". Some experts said the antenna was too heavy and cumbersome to accurately track the satellite, others blamed the driving mechanism. The problem proved to be that one component had been fitted the wrong way round and it was a twenty-minute job to correct it. The effect of the incorrect fitting had been to reverse the direction of the wave polarization of the antenna, relative to that of the satellite, introducing a serious weakening of the strength of signals received. The problem arose because of an ambiguity in the accepted definition of the sense of rotation of radio waves; a difficulty which had been encountered both in the USA and the UK in the period just before the tests. With the correction made, excellent pictures were received on orbit 15 during the evening of July 11, and during orbit 16 the first live television transmission between Europe and the USA was made from Goonhilly to Andover. The pictures and sound received at Andover were reported to be of excellent quality and were broadcast as received throughout the USA.

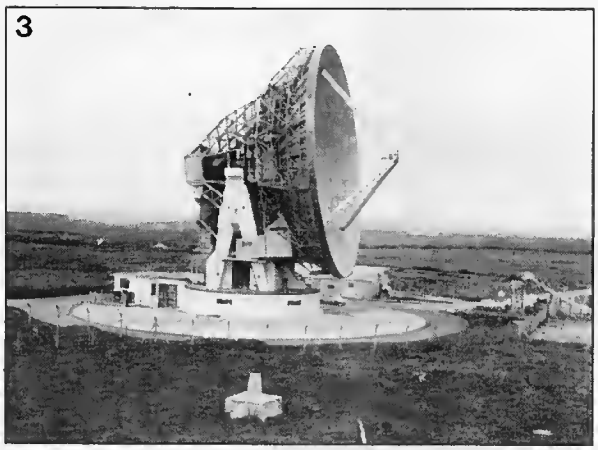


Fig. 3. The first of the dish antennas to be installed at Goonhilly Downs. *Photograph courtesy of British Telecom.*

Fig. 4. Aerial 6 is Goonhily's largest dish with a diamter of 32 m. It was also the first "dual frequency" antenna, able to transmit and receive on two different frequencies simultaneously. *Photograph courtesy of British Telecom.*

Fig. 5. The latest of the antennas (No. 10) to be installed at Goonhilly Downs. *Photograph courtesey of British Telecom.*

On July 12 the first two-way transatlantic telephony tests were made, showing that good-quality, stable telephone circuits with low noise levels had been achieved. These tests were to be followed two days later by the first transatlantic telephone call and photo-telegraphy (facsimile) transmission via satellite.

On July 14 during orbit 34, the director general of the Post Office, Sir Ronald German, spoke from his home in London to the president of American Telephone and Telegraph Co (AT&T), Mr. Eugene McNeely, in New York. Simultaneously, one pair of channels was used to send facsimile pictures between London and New York.

On July 15 tests to assess the ability of a communications satellite to carry large numbers of telephone circuits were carried out during orbit 43. These demonstrated that at least 600 first-grade international circuits should be possible by satellite.

The first transmissions of colour television signals by satellite were made from Goonhilly during orbits 60 and 61 on July 16. With the co-operation of the BBC's research and designs department, who provided a colour slide scanner and monitor equipment, the signals, on 525-line NTSC standards, comprised captions, test cards and still pictures to assess colour quality. The transmissions were initially made from Goonhilly to the satellite and back to Goonhilly but were also received in Andover. Andover reported: "Colour—good; picture quality—excellent".

During orbit 87 on July 19 satellite communications were opened up to the press. Twenty-four calls were made by the British press from Fleet Building in London, to the American press in New York.

On July 23 during orbit 125 an 18-minute long programme from the European Broadcasting Union was transmitted from Goonhilly to Andover. The programme consisted of scenes from many European countries and was transmitted by the Eurovision link to Goonhilly, from Goonhilly to the satellite, and was received at Andover and broadcast throughout the USA.

During orbit 151 on July 26, the Telstar link between Goonhilly and Andover was used to provide telephone circuits for the US Information Agency involving conversations between "notable persons" in 20 pairs of cities in the USA and Europe for the Agency's "People-to-People" programme. The circuits were reported as excellent.

The Telstar tests confirmed that communications satellites could provide high-quality, stable circuits for television and multi-channel telephony. The performance of Goonhilly earth station was reported as excellent in every respect, and the equipment, almost all of which was of a unique new design, had worked well. In fact, Goonhilly's antenna design was to prove, as had Arthur C. Clarke's idea, to be the blue-print for the future.

A brief history of Goonhilly satellite earth station

The choice of Goonhilly Downs, on the Lizard Peninsula in Cornwall, as the site of the United Kingdom's first satellite earth station, was made for exactly the same reasons that Guglielmo Marconi chose the Lizard for his pioneering work in maritime and international "wireless" telegraphy. The Lizard offers an uninterrupted view across the Atlantic and little electrical interference.

The first transatlantic wireless message was sent from the Lizard on December 12, 1901. Three faint but discernible "dots" of the Morse letter "S" were sent from Marconi's transmitter at Poldhu and received by him in Newfoundland, Canada. A year later Poldhu sent a signal to the vessel *Philadelphia* more than 2000 miles away in the ocean. Long-distance telecommunications had been born.

Sixty years later the advance of technology had made satellite communications, first proposed by the author and scientist Arthur C. Clarke in 1945, a realistic possibility. The United Kingdom, the USA and France announced in 1961 that they would co-operate in a programme for the transatlantic testing of communications satellites.

The search for a suitable site in the UK for the station that would receive the signals from the satellites, ended in the Lizard, on the flat expanse of Goonhilly Downs.

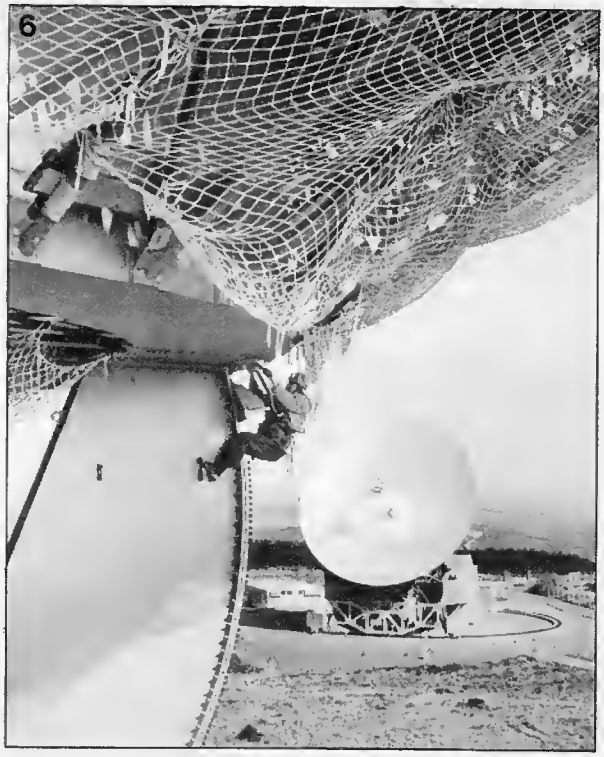


Fig. 6. A British Telecom rigger examines the steelwork of Goonhilly Eart Station's antenna No. 6. *Photograph courtesey of British Telecom.*

The Lizard offered an unimpaired view of the Atlantic horizon, giving the longest possible contact with the low-orbiting satellites then being used. It suffered from little electrical and radio interference; was well placed to connect with inland communications, power supplies and transport links; and had a climate with moderate rainfall, little seasonal variation in temperature and only occasional snow.

Equally important was the geology of the area. The serpentine bedrock reaching a thousand feet deep would give vital support to the massive weight of the antennas.

Within a year of obtaining possession of the site, the first antenna, the control room and its associated equipment were installed and ready for the first tests which would use the Telstar satellite, to be launched by the US National Aeronautics and Space Administration (NASA) on July 10, 1962.

Fig. 7. A section of the control area at Goonhilly Downs. *Photograph courtesey of British Telecom.*

Those tests confirmed that satellites could have a commercial future in international communications. During a period of 16 days several world-firsts went into the record books—the first live television transmission between Europe and the USA, and the first telephone calls, facsimile transmission and transmission of colour television by satellite.

Because of the low orbit of Telstar—between 590 and 3500 miles above earth—the satellite was only usable for three or four 30-to-40 minute periods in each 24 hours. As the satellite raced across the sky from horizon to horizon, the antenna had to be nimble enough to follow the satellite to one-fifth of a degree's accuracy during each of these brief visits.

Aerial 1 at Goonhilly was a unique design - an 870 tonnes "dish" antenna, compared to the French and American horn antennas enclosed in radomes. Some initial problems during the first usable orbits of Telstar caused experts to blame the design of the British antenna, but a small problem with a component which had been fitted faultily proved to be a twenty-minute job to correct and the antenna then went on to establish its world-firsts.

Goonhilly Station had cost around £800,000 to complete, about a quarter of the costs of the American and French stations, and it was the unique design of the British dish antenna which was to go on to become the norm for satellite communications throughout the world. The dish design is now used generally by nearly 700 satellite stations in more than 150 countries.

Following the successful tests with Telstar an international satellite organisation was set up in August 1964 - INTELSAT. Interim agreements were signed by 11 member nations - the USA, UK, Canada, Denmark, France, Italy, Japan, the Netherlands, Spain, the Vatican City State and Australia. Today INTELSAT is owned by more than 100 member countries.

INTELSAT launched its first satellite into orbit in April 1965. The satellite, INTELSAT 1, known as *Early Bird*, was a

high-orbiting satellite in "geostationary orbit".

Arthur C. Clarke had proposed in his 1945 paper that satellites, circling the earth above the equator at a certain height, would appear to be stationary to the earth's surface—their period of orbit would exactly match that of the earth's natural rotation. That distance was 22,300 miles above the equator. After INTELSAT I's successful launch to this height, commercial service opened in June 1965.

Arthur C. Clarke had also proposed that three satellites in geostationary orbit could give world-wide radio coverage.

A second satellite—INTELSAT II—was launched in December 1966, and at the same time, Aerial 1 at Goonhilly, which now no longer needed to track low-orbiting satellites across the sky, had an extra reflecting surface added, pushing its weight up to 1100 tonnes.

Satellite communications had now truly entered commercial operation. As the demand for transatlantic TV and telephone transmission grew, so did Goonhilly with the addition of Aerial 2 in 1968.

By 1969 three geostationary satellites were in orbit, fulfilling Arthur C. Clarke's prophesy of global communications. INTELSAT III was positioned above the Indian Ocean and demand for satellite communications with the Far East grew. To meet this need Aerial 3 was brought into service in 1972.

Aerial 4 was added in 1978, to meet an ever-increasing demand for communications across the Atlantic. This was also one of the first antennas in the world to use the 11/14 GHz frequency as soon as it became available for business satellite communications.

Demand for satellite communications grew by 20 per cent a year during the 1970s and early 1980s. Further satellites were put into orbit and in October 1978 a second earth station was brought into service by British Telecom at Madley in Herefordshire.

Demand for specialist sevices also grew during this period and in 1983 Aerial 5 at Goonhilly was completed to provide satellite services to ships at sea.

At the same time Aerial 6 was being built to provide further capacity on the busy transatlantic route. Aerial 6 is Goonhilly's largest dish with a diameter of 32m. It was also the first "dual-frequency" antenna, able to both transmit and receive on two frequencies simultaneously—doubling potential capacity. It entered service in September 1985.

Fig. 8. Children from a nearby primary school being shown a model of the Intelsat V satellite. *Photograph courtesy of British Telecom.*

While aerial 6 was being built, Aerial 7 was also being brought into service to provide leased TV services to North America. With continuing growth in demand for satellite communications, British Telecom announced plans in August 1983 to built a third earth station in London's Docklands, primarily for satellite TV distribution and specialised business services. The London Teleport, in North Woolwich, opened for operation in February the next year—less than six months after site clearance began.

Aerial 7 at Goonhilly, initially used for TV circuits, is now being used for the trial of *Skyphone*—a telephone service to aircraft in flight—which is due to start by the end of this year.

Fig. 9. The antennas are painted regularly: each ona takes a 1000 gallons of marine paint and two full seasons' painting. *Photograph courtesy of British Telecom.*

Meanwhile Aerials 8, 9 and 10 have been built. These are small-dish antennas below 14m in diameter. They are used for research and development, and to provide monitoring and control facilities on the more than 130 satellites currently in use.

Today, development at Goonhilly continues. Aerial 6, the biggest antenna, has been equipped to operate to the latest development in satellite communications—Time Division Multiple Access/Digital Speech Interpolation (TDMA/DSI). TDMA/DSI means that signals from the station are grouped and sent by time rather than frequency, so that, on the principle that during the average telephone conversation either party is only speaking for one third of the time of the call, other groups of signals can be sent along the same channels during the lapses of conversation

While British Telecom's earth station at Goonhilly provides vital links for today and tomorrow, it has not forgotten its past—a past that goes back far beyond Marconi's early experiments.

The Lizard Peninsula is designated as an Area of Outstanding Natural Beauty and Goonhilly Downs was Cornwall's first National Nature Reserve. In developing the earth station, British Telecom spent £200,000 landscaping the scheme to form natural-looking mounds, or bunds, inside and outside the station's boundaries. Local heathers, gorse and willow were planted in the station, in keeping with the natural character of the Downs. With little intrusion from the public, amidst the silent giants of Goonhilly's antennas, the local flora and fauna have been able to flourish, making Goonhilly not only a pioneer in high-technology but also a botanist's paradise.

BASIC COMPUTER

At the heart of this versatile and simple to build computer for process control and automation applications is Intel's Type 8052AH-BASIC microcontroller.

As already noted in reference [1], the Type 8052AH-BASIC V1.1 is a single-chip microcontroller tailored to data manipulation in intelligent instrumentation, measurement and control systems. Not surprisingly, therefore, the 8052AH-BASIC features an extensive and powerful set of input/output and timekeeping functions.

By virtue of its compactness and ease of programming, the BASIC computer described here is suitable for a wide range of domestic as well as industrial applications. Although not every programmer will applaud the use of BASIC, it can be argued that this is still the most widely known, and often first apprehended, programming language. Moreover, the BASIC interpreter of the 8052AH-BASIC is an advanced version offering instructions like DO-WHILE and DO-UNTIL which enable better structuring of programs than the GOTO statement. Also, variables can be stored and retrieved by means of instructions PUSH and POP. The BASIC interpreter is reasonably fast as compared with competetive 8 and 16 bit systems. In conclusion, the 8052AH-BASIC couples the power and versatility of the 8051 to the qualities of a well-written, reasonably fast, BASIC interpreter.

The computer described is suitable for experimental as well as stand-alone applications. Programs can be written, tested, and debugged by anyone with a reasonable command of BASIC. The microcontroller used is not cheap, probably because of its specialist nature, and the fact that it has hitherto found applications mainly in industrial control systems. None the less, the cost of the 8052AH-BASIC is justifiable considering its impressive potential.

To aid programmers in writing efficient programs, Intel supplies the indipensable *MCS BASIC-52 USERS MANUAL*, which carries reference number 270010-003.

It is important to note that ready-made programs for the BASIC computer are not available. The proposed system is intended primarily for applications where the BASIC programs are not an end in themselves, but where the hardware-software link is readily accessible to enable developing and testing computer controlled systems of a wide variety. Once a program is debugged and known to function satisfactorily, the computer can act as a reliable stand-alone controller.

1

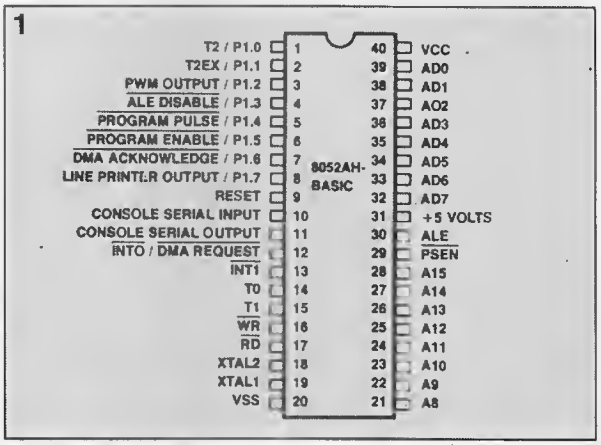


Fig. 1 Pinning of the microcontroller Type 8052AH-BASIC from Intel.

Features

The computer described features an on-board EPROM programmer, which is controlled direct by the 8052AH-BASIC CPU. This means that the processor can store its own programs in EPROM after debugging and testing. Once it is EPROM resident, the BASIC program is available for direct

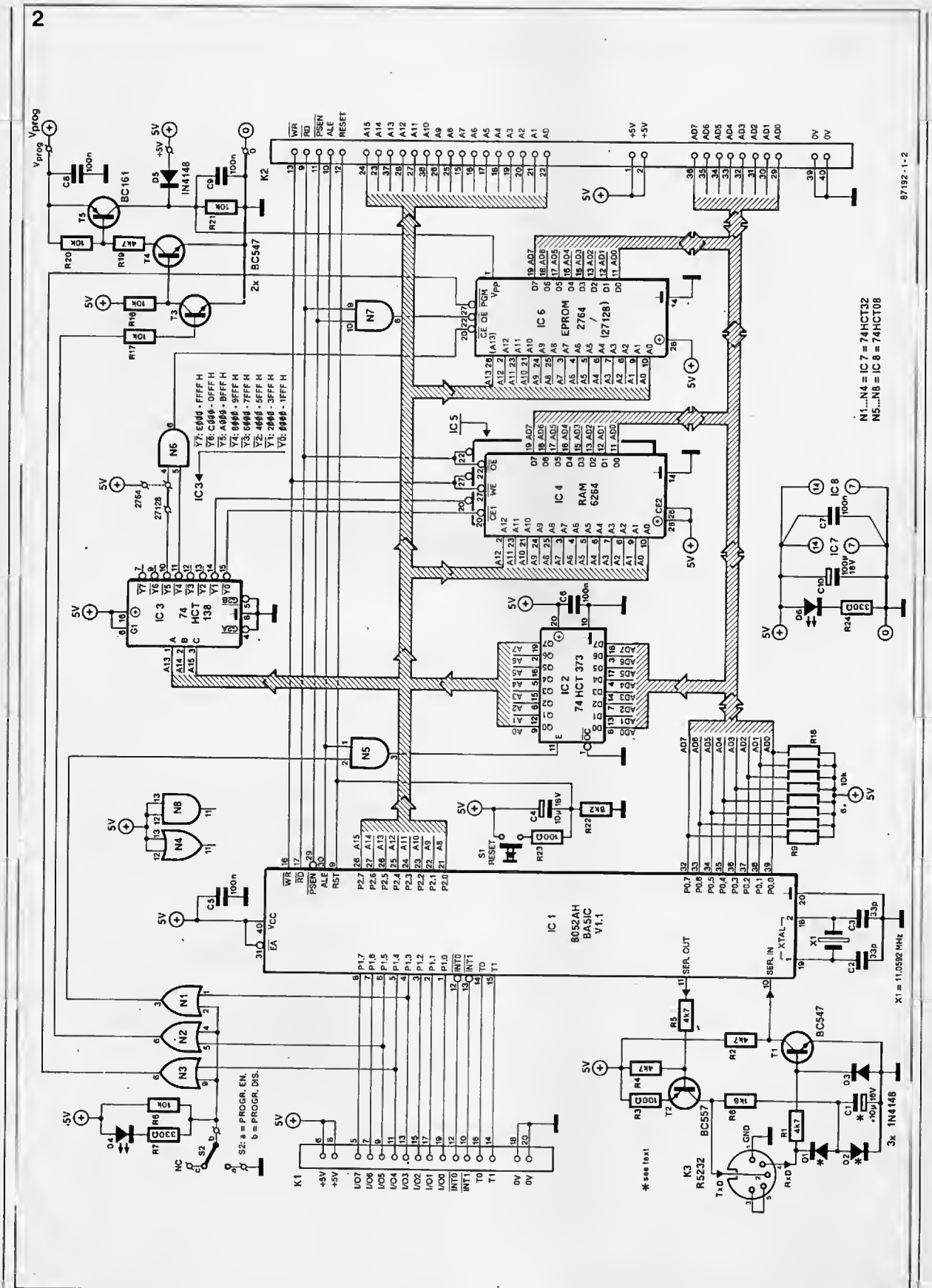


Fig. 2 Circuit diagram of the BASIC computer.

and autonomous execution by the processor. The EPROM contents form the token program listing rather than machine code obtained by a compiling process. The programming of EPROMs on the board is straightforward, and fully supported by BASIC instructions. A single EPROM can hold a number of programs, which can even call each other when necessary.

It should be noted that the BASIC computer has no keyboard and screen of itself. These communication functions are taken over by an external console (terminal), connected to the computer's bidirectional, serial I/O port.

As to the hardware configuration of the proposed BASIC computer, this is characterized by a high degree of flexibility, allowing the user to readily add, say, a UART (*universal asynchronous receiver/transmitter*), an ACIA (*asynchronous communications interface adapter*), a number of PIAs (*peripheral interface adapter*), or other peripheral circuitry such as an alphanumerical display, a sound generator, or a keyboard encoder. The pinning of the 8052AH-BASIC is given in Fig. 1.

The 8052AH-BASIC has a number of powerful timing instructions which, in conjunction with the interrupt statements, special registers, and instruction counters, afford excellent control of time critical I/O applications. A real time clock is also available in the form of function TIME, which offers a resolution of about 5 ms.

The Type 8052AH-BASIC is an 8 bit *microcontroller*, which means that it combines the functions of central processing unit (CPU), and peripheral circuits (I/O; DMA). The chip has an accumulator A, a register B, a status register PSW (*program status word*), an 8 bit stack pointer, a 16 or 2×8 bit data pointer DPTR, 4 8 bit ports for use as an I/O and/or address, data, or command bus, a double serial communication register SBUF, 3 register pairs TH0-TL0, TH1-TL1 and TH2-TL2, which together form the 3 16 bit timers T0, T1 and T2, an intermediate storage register pair RCAP2H-RCAP2L for a number of functions of timer 2, and, finally, an array of registers for various command functions: IP (*interrupt priority*), IE (*interrupt enable*), TMOD, TCON & T2CON for the timers, SCON (*serial control*) and PCON (*power control*).

Circuit description

The circuit diagram of the BASIC computer is given in Fig. 2. The 8 Kbyte BASIC interpreter is internal to the microcontroller, IC1. EPROM IC6 holds the user's BASIC programs. The minimum amount of RAM for the 8052AH-BASIC is 1 Kbyte starting at address 0000. In the present application, the RAM area is either 8 Kbyte (0000—1FFF) or 16 Kbyte (0000—3FFF), depending on whether 1 or 2 RAMs Type 6264 are fitted (IC4; IC5). Write and read operations are controlled direct by signals $\overline{WR}$ and $\overline{RD}$ respectively.

The memory structure of the 8052AH-BASIC is not in accordance with von Neumann's model: the program memory is distinct from the data memory, which explains the logic combination of signal $\overline{PSEN}$ (*program store enable*: control of read operations in an external program memory) with $\overline{RD}$ in gate N7 to select the ROM memory area (2764 = 8 Kbyte from 8000 to 9FFF; 27128 = 16 Kbyte from 8000 to BFFF). This does not exhaust all the possible memory configurations for the 8052AH-BASIC, but forms a practical as well as efficient combination—see Fig. 3. In the EPROM programming mode, the microcontroller addresses EPROMs in the memory area starting at address 8000.

Decoder IC3 divides the memory area in blocks of 8 Kbyte. AND gate N6 makes it possible to combine 2 block select signals when the EPROM used is a Type 27128. Normally, octal latch IC2 demultiplexes the data and lower address bytes with the aid of signal ALE (*address latch enable*). In the EPROM programming mode, however, the LS address byte is kept latched much longer than during normal bus cycles.

This also goes for the MS address byte and the dataword—the normal duration of a programming cycle is of the order of 50 ms. The software has no direct control over the length of the ALE pulse, and this is, therefore, inhibited with the aid of N1, N5 and the logic low level on CPU output P1.3.

When port 0 is used in the I/O mode, pull-up resistors are required on the open drain outputs. Normally, this port functions as the data & address bus, but operates as an I/O port in the EPROM programming mode.

The TTL levels at the serial output, P3.1, of the microcontroller are converted into the corresponding positive and negative levels for the terminal. Rectifier D1-D2-C1 is connected to the terminal's TXD line to provide the negative supply for TXD driver T2. Components D1 and D2 can be omitted, and C1 replaced by a wire link, when the terminal accepts and sends pulses with TTL levels.

The connections on the serial I/O connector, K3, are given in the circuit diagram.

Table 1 shows the pin assignment on connector K1, which carries the 8 lines of peripheral port P1, interrupt inputs $\overline{INT0}$ and $\overline{INT1}$, and lines T0 and T1, which form the external inputs of the respective timers. Line pairs $\overline{WR}$ and $\overline{RD}$, RxD and TxD, $\overline{INT0}$ and $\overline{INT1}$, and T0 and T1 together form port P3 of the 8052AH-BASIC. Apart from their normal use as I/O lines, the lines on port P1 may be used for special purposes. For example, P1.0 and P1.1 can provide trigger as well as clock pulses for timer T2. This is a standard function of the 8052, and not a particular feature of the BASIC interpreter. Lines P1.3, P1.4 and P1.5 are used for programming the majority of currently available EPROM and EEPROMs Type 2764 and 27128.

Output P1.6 is connected to input INT0 for ready implementation of a DMA (*direct memory access*) mechanism. Output P1.7 can act as a direct serial channel for driving, say, a printer, controlled with the aid of commands LIST# and PRINT#. There are more BASIC instructions for port 1: PWM, for example, offers control of the pulsewidth on output P1.2,

3

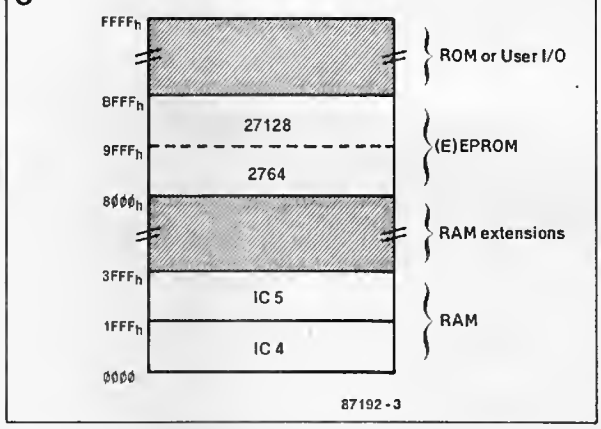


Fig. 3 Memory structure of the 8052AH-BASIC.

Table 1.

Connector K1:		Connector K2:			
Pin	Pin	Pin	Pin	Pin	Pin
1 NC	2 NC	1 +5 V	11 $\overline{PSEN}$	21 A1	31 D2
3 NC	4 NC	2 +5 V	12 RESET	22 A0	32 D3
5 I/O7	6 +5 V	3 NC	13 $\overline{WR}$	23 A14	33 D4
7 I/O6	8 +5 V	4 NC	14 NC	24 A15	34 D5
9 I/O5	10 $\overline{INT1}$	5 NC	15 A7	25 A8	35 D6
11 I/O4	12 $\overline{INT0}$	6 NC	16 A6	26 A9	36 D7
13 I/O3	14 T1	7 NC	17 A5	27 A11	37 A13
15 I/O2	16 T0	8 NC	18 A4	28 A12	38 A10
17 I/O1	18 ⊥	9 $\overline{RD}$	19 A3	29 D0	39 ⊥
19 I/O0	20 ⊥	10 ALE	20 A2	30 D1	40 ⊥

Table 1 Pinning of connectors K1 and K2.

while instruction PORT1 enables direct read/write access.

The signal assignment on connector K_2 is shown in Table 1. This connector carries lines AD0...AD7, A0...A15, and the command bus, and so enables ready connection of peripheral extension, or DMA, circuitry. It is possible to halt the processor in the *idle* mode, and so arrange for an external processor or microcontroller to temporarily gain access to the memory in the BASIC computer. The *idle* mode is initiated with the aid of the corresponding BASIC statement, and can be used for switching the microcontroller to the non-active state when no action on its part is required.

The clock oscillator is internal to the 8052AH-BASIC, and merely requires a quartz crystal and 2 capacitors. The indicated crystal frequency of 11.0592 MHz is required to ensure the correct timing for the serial channel, the real time clock, and the EPROM programming pulses. When it is intended to use, say, a 12 MHz crystal, the processor should be informed of this by declaring XTAL=I2000000. It should be noted that any oscillator frequency other than 11.0592 MHz may result in reduced accuracy of the counter operations.

The computer is reset and initialized on power up either automatically (R_{22}-C_4) or manually (S_1). Input $\overline{EA}$ (*external address*) is made permanently logic high because the BASIC interpreter is an *internal* memory area.

Programming EPROMs

The (E)EPROM programming facility of the present BASIC computer is, without doubt, one of its most attractive features. It is important to note that the computer is not just an EPROM programmer, but a data handling and storage system that can be customized as required for the application in question. While communicating with the user via the terminal, the 8052AH-BASIC can store edited, debugged and tested BASIC (sub)routines in EPROM to facilitate calling these as "tools" at any time. Before programming is effected, the microsoftware in the 8052AH-BASIC takes care of all the tokenizing of the object program to ensure compact storage. Depending on the programming mode, certain parameters are stored along with the program, and are instantly available when this is loaded and run. These program parameters include the baud rate, variable MTOP, an autoexecute flag, and a flag that enables skipping the memory initialization routine at power-on—this is particularly useful when the RAM is battery powered.

Finally, it is possible to use BASIC for loading an EPROM with an assembler program that is executed automatically after a RESET pulse.

With reference to the circuit diagram, when line P1.5 goes low, transistors T_3, T_4 and T_5 ensure that the programming voltage reaches the Vpp terminal of the EPROM. The programming voltages for a number of EPROMs are listed in Table 2. The microcontroller places the LS address byte onto lines AD0...AD7, then disables ALE by making P1.3 logic low. The address byte remains latched in IC_2 during the remainder of the programming cycle. The MS address byte is placed onto lines A8...A15, and the databyte onto lines D0...D7 of the EPROM to be programmed. Then, output P1.4 is made logic low, and the byte is programmed in the EPROM because $\overline{PGM}$ goes low while Vpp is applied. Instructions PROG and FPROG select a duration of the programming cycle of 50 and 1 ms, respectively. FPROG uses the intelligent programming algorithm, and may require raising the EPROM supply voltage from 5 to 6 V, which is *not* supported by the proposed circuit. Details on the intelligent programming algorithm can be found in reference [2]. In all cases, the duration of the $\overline{PGM}$ pulse is determined by the clock frequency of the microcontroller, and operator XTAL should be defined as as discussed previously. Switch S_2 enables blocking the 3 programming signals. This is done for reasons of security because port P1 can be used for purposes other than programming EPROMs.

Up to 255 BASIC modules can be held in a single EPROM, and each of these can call any of the others. The 8052AH-BASIC automatically assigns a number to each BASIC program before storing this in EPROM. The number is sent to the terminal for the programmer's reference. Loading and running a particular BASIC module is effected with the aid of commands ROM X followed by RUN. Variable X is the number of the relevant module. Modules can be copied from EPROM to RAM by means of command XFER.

The programmer has direct access to an extensive library of routines in the BASIC interpreter. Also, BASIC allows calling external machine code subroutines provided by the user. It should be noted, though, that writing (fast) machine code requires an 8051 assembler, and, of course, considerable experience in working at the assembly code level.

Table 2.

Manufacturer	Type	memory organization	Vpp
AMD	AM2764	8K × 8	21 V
	AM2764A	8K × 8	12.5 V
	AM27128	16K × 8	21 V
	AM27128A	16K × 8	12.5 V
Fujitsu	M8M2764	8K × 8	21 V
	M8M27C64	8K × 8	21 V
	M8M27128	16K × 8	21 V
Hitachi	HN482764	8K × 8	21 V
	HN27C64	8K × 8	21 V
	HN482764P	8K × 8	21 V
	HN4827128	16K × 8	21 V
	HN27128P	16K × 8	21 V
Intel	2764	8K × 8	21 V
	P2764	8K × 8	21 V
	2764A	8K × 8	12.5 V
	27C64	8K × 8	12.5 V
	P2764A	8K × 8	12.5 V
	27128	16K × 8	21 V
	27128A	16K × 8	12.5 V
	P27128A	16K × 8	12.5 V
Mitsubishi	M5L2764	8K × 8	21 V
	M5L27128	16K × 8	21 V
National Semiconductor	NMC27C64	8K × 8	12.5 V
	NMC27CP128	16K × 8	12.5 V
NEC	μPD2764	8K × 8	21 V
	μPD27C64	8K × 8	21 V
	μPD2764C	8K × 8	21 V
	μPD27C64C	8K × 8	21 V
	μPD27128	16K × 8	21 V
	μPD27128C	16K × 8	21 V
Rockwell	R87C64	8K × 8	21 V
	R27C64P	8K × 8	21 V
SEEQ	2764	8K × 8	21 V
	27128	16K × 8	21 V
SGS/ATES	M2764	8K × 8	21 V
Texas Instruments	TMS2564	8K × 8	25 V
	TMS2764	8K × 8	21 V
	TMS27128	16K × 8	21 V
Thomson-CSF	ET2764	8K × 8	21 V
Toshiba	TMM2764	8K × 8	21 V
	TMM2764DI	8K × 8	21 V
	TMM27128	16K × 8	21 V

The type indications as given may be followed by an access time specification.

Table 2 Programming voltages for a number of EPROM types that can be loaded by the BASIC computer.

The practical use and operation of the EPROM programming facility is extremely straightforward. All that is required is to fit an EPROM in the socket for IC_6, apply the correct programming voltage, switch S_2 to PROG. EN, load the BASIC file in RAM, and issue command PROG. The other programming commands,
(F)PROG1...(F)PROG6 enable storing auxiliary program information, including the baud rate indicator, and the autoexecute flag. The available options are described in the previously mentioned programming manual from Intel.

Construction

It should be reiterated that the computer described is intended mainly as an aid in developing software and hardware for automated processes and stand-alone, intelligent, controllers or data loggers, where timekeeping is an essential requirement.
The printed circuit board for the BASIC computer is double-sided and through-plated. The component mounting plan is given in Fig. 4.
It is recommended to fit good quality sockets for all ICs. The socket for EPROM IC_6 can be a type with turned pins, although a ZIF (*zero insertion force*) socket mounted as shown in the photograph of the prototype is probably the best solution. Be sure to purchase a microcontroller Type **8052AH-BASIC V1.1**. Connectors K_1 and K_2 are intended for extensions, and need not be fitted as yet. Initially, a single RAM, IC_4, is sufficient, since it offers a memory area of about 7 Kbyte for BASIC programs. Resistors R_9...R_{16} incl. form an 8-way SIL network, but it is also possible to use 8 ordinary resistors, mounted vertically and commoned by a short length of wire connected to +5 V as shown in Fig. 5. The function of the LEDs, D_4 and D_6, is evident from the circuit diagram. The supply and programming voltage are applied to the circuit via soldering pins and mating sockets, insulated with the aid of heat shrink sleeving. *Do not confuse the Vcc and Vpp connections.* The PROG. EN switch, S_2, and the EPROM selector, S_3, may each be replaced by 3 pins and a mating jumper if it is not intended to frequently program EPROMs, or change between a 2764 and a 27128.
EPROM IC_6 is not required to make the circuit function. It is not fitted until it can be pro-

4

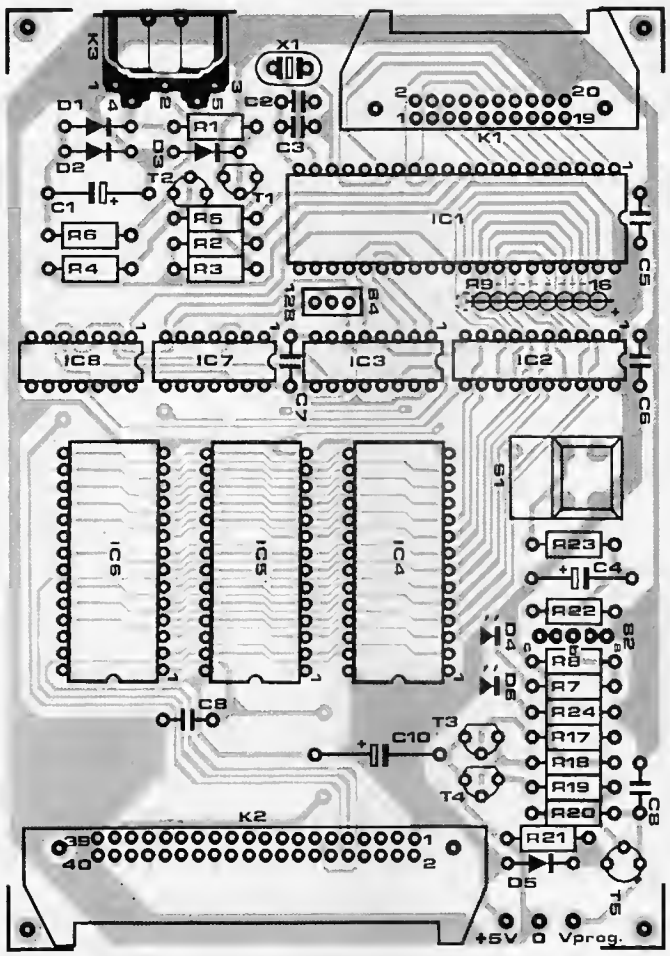


Fig. 4 Component mounting plan for the BASIC computer. The circuit board is available ready-made through the Readers Services.

Parts list

Resistors (±5%):
R_1;R_2;R_4;R_5;R_{19} = 4K7
R_3;R_{23} = 100R
R_8 = 1K8
R_7;R_{24} = 330R
R_8;R_{17};R_{18};R_{20};R_{21} = 10K
R_9...R_{16} = 8-way 10K SIL network, or 8 10K resistors
R_{22} = 8K2

Capacitors:
C_1;C_4 = 10μ; 16 V
C_2;C_3 = 33p ceramic
C_5...C_9 incl. = 100n
C_{10} = 100μ; 16 V

Semiconductors:
D_1;D_2;D_3;D_5 = 1N4148
D_4 = green LED
D_8 = red LED
T_1;T_3;T_4 = BC547
T_2 = BC557
T_5 = BC161
IC_1 = 8052AH-8ASIC VERSION 1.1*

IC_2 = 74HCT373
IC_3 = 74HCT138
IC_4;IC_5 = 6264 8Kx8 static CMOS RAM
IC_6 = 2764 or 27128 (see text)
IC_7 = 74HCT32
IC_8 = 74HCT08

Miscellaneous:
S_1 = Digitast SPST push button.
S_2 = miniature SPST switch.
K_1 = 20-way right angled IDC header with side latches.
K_2 = 40-way right angled IDC header with side latches.
K_3 = 5-way DIN socket for PC8 edge mounting.
X_1 = 11.0592 or 11.059 MHz, HC18 enclosure.
28-way ZIF socket.
Jumpers and soldering pins as required.
PC8 Type 87192 (available through the Readers Services).
Suitable A8S or metal enclosure.
Suitable power supply.

It is regretted that a ready-made front panel for this project is not available.

* Intel distrubutors ere listed on InfoCard 505 in the March 1987 issue of *Elektor Electronics*.

The chip is also available from Universal Semiconductor Devices Limited • 17 Granville Court • Granville Road • Hornsey • London N4 4EP. Telephone: (01 384) 9420. Telex: 25157 usdco g. Fax: 01 348 9425.

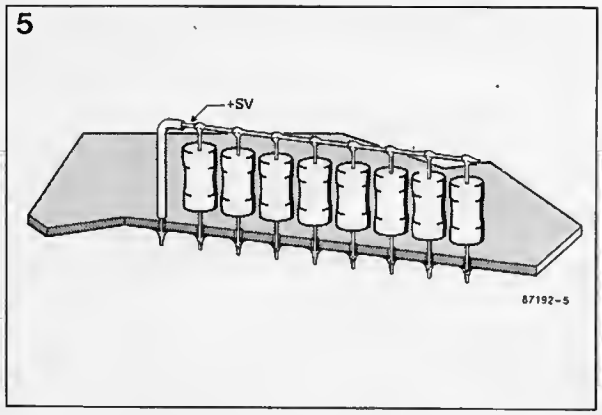


Fig. 5 Showing the use of 8 ordinary resistors instead of a SIL network.

grammed with BASIC modules, and only when the computer is turned off.
The power supply for the BASIC computer can be a simple type with regulated outputs for 5 V (500 mA), and the programming voltage(s).
Initially, the CPU and the memory chips are not fitted while the completed board is fed with Vcc and Vpp. Consult the circuit diagram and carefully check the presence of the supply voltage at all the relevant points. Make sure that there is no short circuit around pin 28 of ICs, since the programming voltage is carried nearby. Switch off the power, carefully fit the CPU and the RAM(s) with the correct orientation, and switch the power on again.

Communication: the terminal

The serial data format for the BASIC computer is:

8 data bits, no parity, 1 stop bit.

Most terminals, consoles, or terminal emulation programs for computers can support this format.
The 3-wire connection between the BASIC computer and the terminal is shown in Fig. 6. At the terminal side, it may be necessary to hard wire a number of RS232 hanshaking lines—consult the relevant documentation. A solution that works in most cases is to connect the following pins in the 25-way RS232 connector:
4—5—8 and
6—20 (sometimes 6—20—22).
Where — denotes the connection.

The BASIC computer has an internal baud rate timing routine. Press RESET, wait a second or so, and press the space bar on the terminal. The message

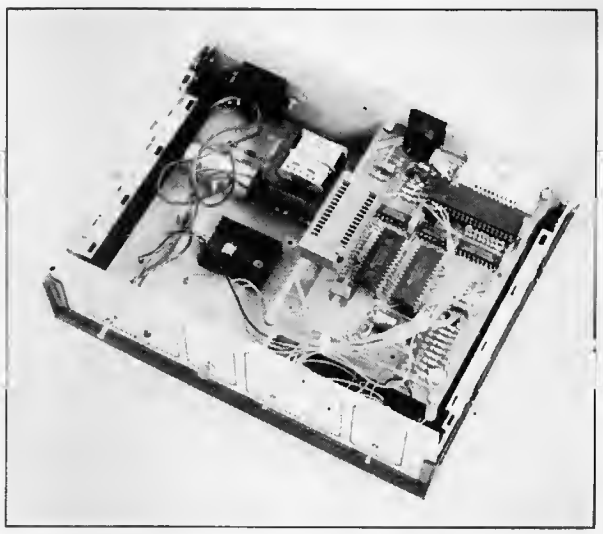
```
*MCS-51(tm) BASIC V1.1
READY
>
```

is displayed on the terminal screen, and the BASIC computer is ready to accept commands.
After RESET is pressed, the CPU initializes its internal RAM, and a number of pointers and registers. It then tests, initializes, and determines the size of the external memory area (IC_4 and IC_8). Next, the memory size is stored with the aid of operator MTOP (*memory top*), operator XTAL is defined (default: 11059200), and, finally, the CPU reads the data at address 8000 to check for a valid baud rate definition, programmed in EPROM IC_6. When a baud rate byte is found, it is stored in register T2CON. The computer then skips its automatic baud rate timing routine and operates at the preprogrammed serial speed, obviating the need for the terminal operator to press the space bar after actuating RESET on the BASIC computer.
The maximum baud rate is 38.4 Kbit/s, and timing characters other than 20_H (space) are not accepted.

To verify the correct operation of the system, type

PRINT XTAL,TMOD,TCON, T2CON <CR>

to which the computer replies



Inside view of a prototype of the BASIC computer.

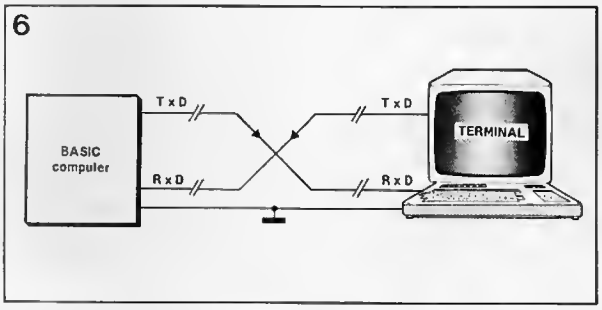


Fig. 6 The 3-wire connection between the BASIC computer and the terminal.

```
11059200 16 244 52
```

The system prompt > is displayed to indicate that the computer is ready to accept commands, which are not executed until <CR> is received. Actually, the 8052AH-BASIC starts tokenizing and storing the BASIC commands after receiving a carriage return (OD_H). Depending on the length of the line, and the complexity of the command(s), this takes some time, and *new characters must not be sent* until the CPU responds with the prompt, indicating completion of the storage process.

The BASIC computer is probably best programmed and controlled with the aid of a personal micro sporting an RS232 port. As to software, a terminal emulation or communication program in conjunction with a wordprocessor enables efficient editing and downloading of BASIC files. A general flowchart of a serial I/O routine to support the above

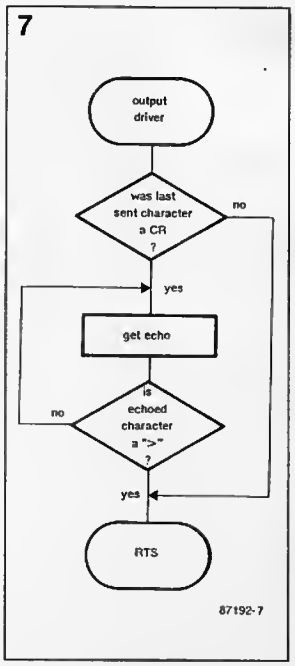


Fig. 7 The sending computer must wait for the > prompt from the BASIC computer before sending a new line of commands.

handshaking procedure is shown in Fig. 7.

Table 4 is a hex dump of a simple filehandler for IBM PCs and compatibles. The program is called SENDBAS.COM, and was written by H Peters. It loads (ASCII) BASIC files from disk, and sends these to the BASIC computer via serial port COM1:, in accordance with the previously mentioned prompt-based handshaking arrangement.

The program is loaded and written onto disk with the aid of DEBUG, which can be found on the DOS disk (use version 3.1 or later). Format a new disk, and copy DEBUG.COM onto it. Select the relevant drive, e.g. B:. Follow this instruction if you are unfamiliar with the operation of DEBUG:

DEBUG<CR>

Fill a 256 byte block with nulls:

F 0100 01FF 00<CR>

Name the program:

NSENDBAS.COM<CR>

Ready for entering the 256 bytes:

E 100<CR>

Enter the bytes (*not the addresses*) in Table 4, starting with B4. The first 2-byte address on each line is irrelevant in this case. Use the hyphen for corrections, and the space bar to proceed to the next byte. Type <CR> when the block is complete, and check the screen against the data in Table 4. If necessary, consult the chapter on DEBUG in your DOS manual.

Call up the block pointers:

RCX<CR>

and type

00FF<CR>

after the colon. Do the same with

RBX<CR>

and again

00FF<CR>

Write the .COM file to disk:

W<CR>

Leave DEBUG:

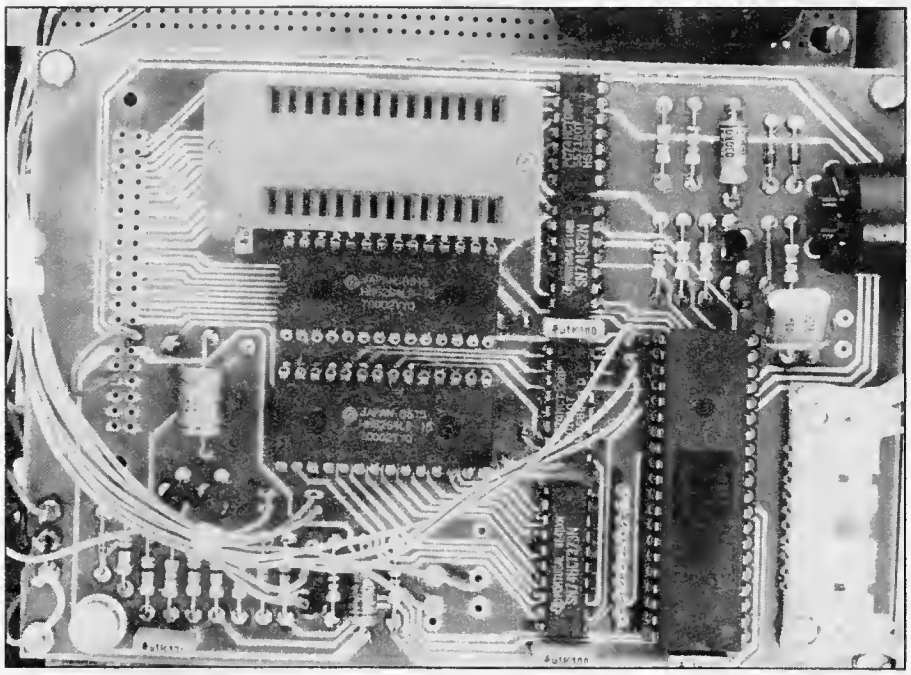
Q<CR>

The PC filehandler is now available on disk, and can be called with command SENDBAS. Test the program: the screen is cleared, and the text **ENTER FILENAME:** is displayed. Type <CR> to return to the DOS command prompt.

Table 3.

COMMANDS	STATEMENTS		OPERATORS	
RUN	BAUD	ONTIME	ADD (+)	DBY( )
CONT	CALL	PRINT	DIVIDE (/)	XBY( )
LIST	CLEAR	PRINT#	EXPONENTIATION (^)	GET
LIST#	CLEAR(S&I)	PRINT@ (V1.1)	MULTIPLY (*)	IE
LIST@ (V1.1)	CLOCK(1&0)	PH0.	SUBTRACT (-)	IP
NEW	DATA	PH0.#	LOGICAL AND (.AND.)	PORT1
NULL	READ	PH0 @ (V1.1)	LOGICAL OR (.OR.)	PCON
RAM	RESTORE	PH1.	LOGICAL X-OR (.XOR.)	RCAP2
ROM	DIM	PH1.#	LOGICAL NOT (.OR.)	T2CON
XFER	DO-WHILE	PH1.@ (V1.1)	ABS( )	TCON
PROG	DO-UNTIL	PGM (V1.1)	INT( )	TMOD
PROG1	END	PUSH	SGN( )	TIME
PROG2	FOR-TO-STEP	POP	SQR( )	TIMER0
PROG3 (V1.1)	NEXT	PWM	RND	TIMER1
PROG4 (V1.1)	GOSUB	REM	LOG( )	TIMER2
PROG5 (V1.1)	RETURN	RETI	EXP( )	XTAL
PROG6 (V1.1)	GOTO	STOP	SIN( )	MTOP
FPROG	ON-GOTO	STRING	COS( )	LEN
FPROG1	ON-GOSUB	UI(1&0)	TAN( )	FREE
FPROG2	IF-THEN-ELSE	UO(1&0)	ATN( )	PI
FPROG3 (V1.1)	INPUT	LD@ (V1.1)	=, >, >=, <, <=, <>	
FPROG4 (V1.1)	LET	ST@ (V1.1)	ASC( )	
FPROG5 (V1.1)	ONERR	IDLE (V1.1)	CHR( )	
FPROG6 (V1.1)	ONEX1	RROM (V1.1)	CBY( )	

Table 3 Overview of the instructions supported by the 8052AH-BASIC.



A close look at the component side of the populated board (prototype version)

Table 4.

```
A>DEBUG SENDBAS.COM
-D 0100 01FF
1E4B:0100  B4 00 B0 02 CD 10 BC CB-05 10 00 BE DB BB ED 00   ................
1E4B:0110  53 EB 3B 00 7A 26 E9 94-00 5B 8A 07 43 53 3C 1A   S.;.z&...[..CS<.
1E4B:0120  74 F4 3C 0A 74 16 B4 01-BA 00 00 CD 14 B4 02 BA   t.<.t...........
1E4B:0130  00 00 CD 14 B4 02 BA D0-CD 21 EB DD B4 02 BA 00   .........!......
1E4B:0140  00 CD 14 8A D0 B4 02 CD-21 3C 3E 75 EF EB CA B4   ........!<>u....
1E4B:0150  09 BA B0 00 CD 21 B4 0A-BA CB 00 CD 21 BB CC 00   .....!......!...
1E4B:0160  BA 07 3C 00 75 03 EB 45-90 BB CD 00 B9 1E 00 BA   ..<.u..E........
1E4B:0170  07 3C 0D 74 06 43 E2 F7-EB 05 90 B0 00 BB 07 B4   .<.t.C..........
1E4B:01B0  3D BA CD 00 B0 00 CD 21-BB DB B4 3F B9 FF FF BA   =......!...?....
1E4B:0190  ED 00 CD 21 BB DB B4 3E-CD 21 B0 20 B4 01 BA 00   ...!...>.!. ....
1E4B:01A0  00 CD 14 B0 0D B4 01 BA-00 00 CD 14 C3 5B CD 20   .............[.
1E4B:01B0  0D 0A 0A 0A 0A 20 20 20-20 20 45 4E 54 45 52 20   .....      ENTER
1E4B:01C0  46 49 4C 45 4E 41 4D 45-3A 20 24 1E 00 00 00 00   FILENAME: $.....
1E4B:01D0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
1E4B:01E0  00 00 00 00 00 00 00 00-00 00 00 00 00 1A 26 00   ..............&.
1E4B:01F0  74 09 EB 40 E1 EB 1B F1-EB BC E1 A1 D6 26 A3 04   t..@.........&..
-
                                                        87192-T4
```

Table 4 Hexdump of SENDBAS.COM, the filehandler for PCs and compatibles.

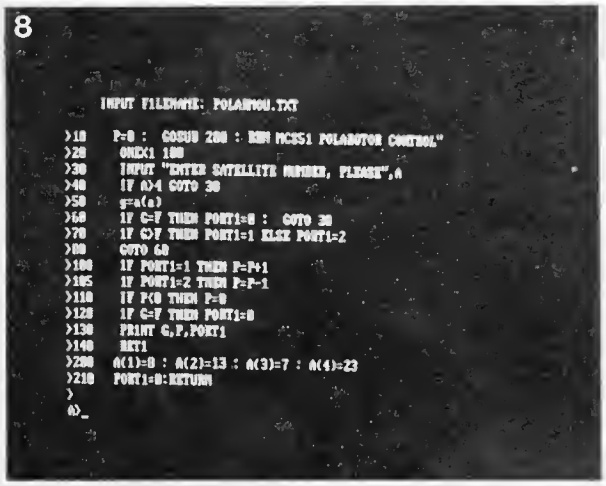


Fig. 8 SENDBAS.COM has completed sending a program to the BASIC computer via the COM1: port on a PC turbo XT. The baud rate is 1200.

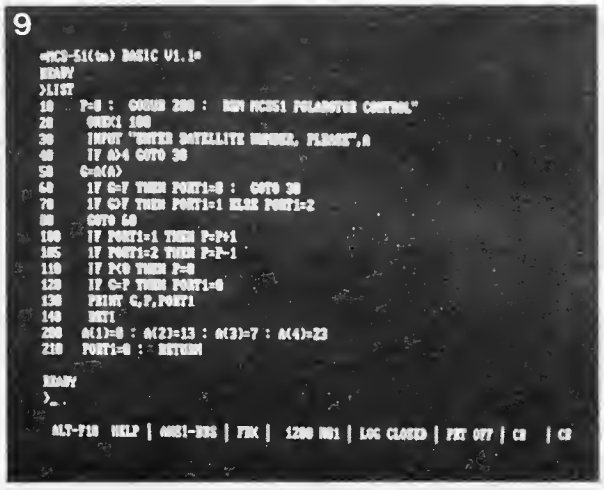


Fig. 9 The BASIC computer is on line again, and has received a program for controlling a polarmount satellite dish position system. Note the system's welcome message at the top of the screen, and the status line of PROCOMM® at the bottom.

SENDBAS.COM was tested in conjunction with PROCOMM® 2.4.2, a versatile communication program for PCs and compatibles. BASIC text files were prepared and stored onto disk in DOS text format using the wordprocessor WORDPERFECT 4.2. Other combinations of communication program and wordprocessor should also work, as long a the files for sending to the BASIC computer are written in DOS text (ASCII) format, i.e., without all the control codes specific to the wordprocessor used. As to the communication program, it is very practical if this offers a SHELL or DOS Gateway command to temporarily switch to DOS, start SENDBAS for loading the updated file, and return to the BASIC computer by means of EXIT. SENDBAS takes over the set baud rate, and awaits the > prompt from the computer before it sends a new line via COM1:. The writing of the file can be seen on the screen. After sending a file using SENDBAS, and EXITing DOS to return to the comms program, type a <CR> when the BASIC computer displays

READY
>

Type LIST to check the contents of the new program, and run it... The use of SENDBAS.COM on a PC-XT turbo is illustrated in Figs. 8 and 9.

A simple filehandler for the BBC micro is listed in Table 5. This program works in conjunction with the well-known wordprocessor VIEW, the micro's serial outlet and the communication program COMMUNICATOR, set up for VT52 emulation, XON/OFF, and, say, 9600 baud I/O. It is assumed here that the user is thoroughly familiar with these programs, and the way they are called up and exited. Test the communication between the BBC micro and the BASIC computer by pressing RESET and then the space bar as outlined above. Owners of a MASTER micro can avail themselves of the built-in terminal, obviating the need to purchase a separate communication program.

Leave COMMUNICATOR, run BASIC, and enter the listing of Table 5. Run the program. It creates a small machine code routine called PRDR-52 (*printer driver* for 8052AH-BASIC), which is automatically saved onto disk. Select the computer's serial output channel by typing **FX5,2**. Call up VIEW (*W), and load or write the program (i.e. text file) for the BASIC computer. Install PRDR-52 on the serial port by typing **PRINTER PRDR-52** at the command level. The VIEW file is now sent to the BASIC computer at the specified baud rate. The fact that VIEW can not send but complete pages is of no consequence. Leave VIEW and run the terminal emulation program to control the BASIC computer direct. *Th*

Table 5.

```
LIST
 10 MODE 7
 20 FOR ADDRESS=&4200 TO &426B
 30  READ BYTE
 40  ?ADDRESS=BYTE
 50 NEXT ADDRESS
 60 *SAVE PRDR-52 4200 4300 0400 0400
 70 END
 80 DATA &4C,&40,&04,&4C,&0F,&04,&4C,&26,&04,&4C,&3C,&04,&4C,&30,&04
 90 DATA &48,&8A,&48,&98,&48,&A9,&02,&20,&EE,&FF,&A9,&02,&A2,&01,&20
100 DATA &F4,&FF,&68,&A8,&68,&AA,&68,&60,&48,&8A,&48,&98,&48,&A9,&03
110 DATA &20,&EE,&FF,&A9,&02,&A2,&00,&20,&F4,&FF,&68,&A8,&68,&AA,&68
120 DATA &60,&A0,&00,&60,&8D,&FE,&04,&48,&8A,&48,&98,&48,&A0,&FE,&04
130 DATA &C9,&0D,&F0,&09,&20,&EE,&FF,&68,&A8,&68,&AA,&68,&60,&20,&E7
140 DATA &FF,&20,&E0,&FF,&C9,&0A,&D0,&F9,&20,&E0,&FF,&C9,&3E,&D0,&F2
150 DATA &4C,&52,&04
```

87192-T5

Table 5 This program creates PRDR-52, the filehandler for the BBC micro running VIEW and COMMUNICATOR.

References:

(1) *Single-chip microcontrollers. Elektor India*, October 1987.

(2) *MSX extensions — 5: EPROM programmer (2). Elektor India*, May 1987.

Procomm® is a registered trademark of Datastorm Technologies, Inc. • PO Box 1471 • Columbia MO 62205 • USA. BBS: (314) 449-9401 (24 h.).

MCS-51® is a registered trademark of Intel Corporation.

THE DIGITAL AUDIO TAPERECORDER

Earlier this year, a number of Japanese manufacturers introduced a new type of personal taperecording system, which has become known as Digital Audio Taperecorder–DAT. Although this system ran into immediate problems with the combined might of the western world's record makers and composers' and music writers' organizations (which at the time of writing have still not been wholly resolved), it appears that it is here to stay.

There is as yet no standard for the DAT or the tape cassettes, although proposals have been submitted to the International Electrotechnical Commission. Data, standards, and specifications referred to in this article are as contained in those proposals.

Cassette

The information carrier is a magnetic tape of 3.81 mm width rolled on flangeless hubs installed in a cassette with a slider and a lid protecting the tape from accidental damages. The tape is a metal powder type or its equivalent.

Information is recorded on oblique tracks formed by helically scanning magnetic heads and can be erased by overwriting. Information is read by magnetic heads that follow the tracks with the aid of Automatic Track Finding—ATF.

The external dimensions of the cassette are 73 x 54 x 10.5 mm: it is thus somewhat smaller than the compact audio cassette.

Recorder mechanism

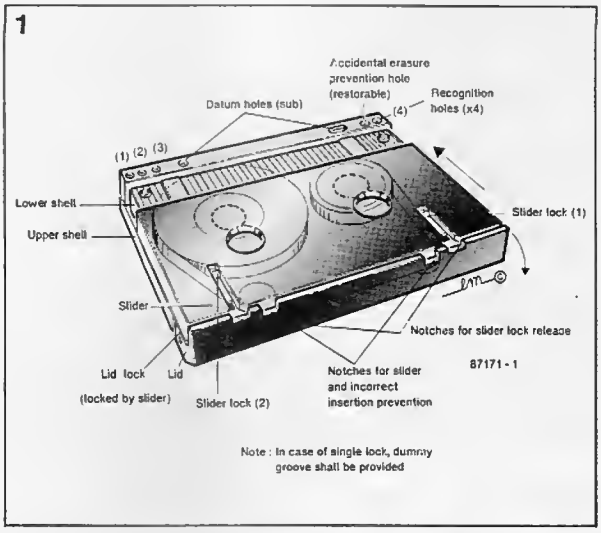
The mechanism of the recorder resembles that of a video cassette recorder—VCR—but it is somewhat smaller (roughly the same size as the mechanism of a Video-8 machine).

The rotary head drum has a diameter of 300 mm and rotates at a velocity of 2000 rev/min. The angle at which the tape lies around the drum is 90°. The normal tape speed is low: only 8.150 mm/sec. The resulting relative tape speed is, therefore, 3.130 m/sec (the tape speed in a VHS video recorder is 4.85 m/sec). Other tape speeds are: 4.075 mm/sec (half speed) and 12.225 mm/sec (wide track).

The track pitch is 13.591 μm in normal track mode and 20.410 μm in wide track mode. The track length is 23.501 mm (normal mode) and 23.471 mm (wide track mode).

The track angle (tape running) is 6°22'59.5" in the normal mode and 6°23'29.4" in the wide track mode. The azimuth angle of the two heads is $\pm 20° \pm 15'$ (see Fig. 3).

The above, and some other, data are summarized in Table 1. Since there are only two heads and the tape runs along only a quarter of the drum diameter



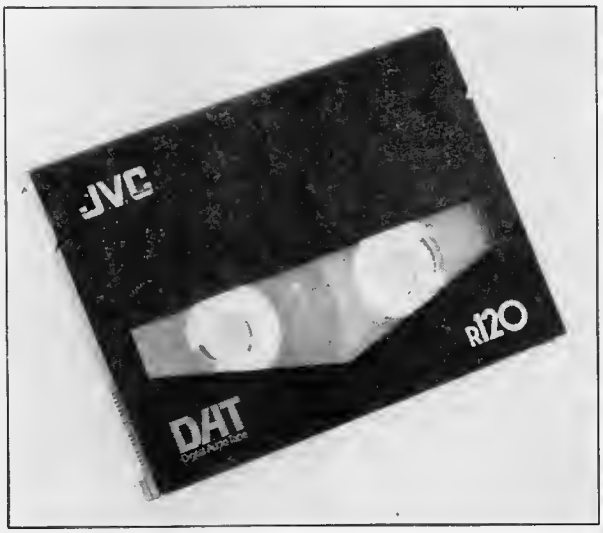


Fig. 1. The digital audio tape cassette is somewhat smaller than the compact audio cassette.

Table 1

Tape width	3.810 mm
Recording width	2.613 mm
Track centre	1.905 mm
Tape speed (normal)	8.150 mm/s
(half speed)	4.075 mm/s
(wide track)	12.225 mm/s
Track length	23.501 mm
Track pitch (normal)	13.591 μm
(wide track)	20.410 μm
Trank angle (normal)	6°22'59.5"
(wide track)	6°23'29.4"
Head azimuth	$\pm 20° \pm 15'$
Optional track 1	0.5 mm
Optional track 2	0.5 mm

Table 1. Tape specifications (normal mode).

(see Fig. 3), the heads will scan the tape for only half the total usable time. This means that the data have to be stored on the tape in time-compressed form: during reading they have to be expanded again. The output signal of the heads is shown in Fig. 4.

The small angle between the tape and the head drum gives the advantage that pull on the tape is small, and also that even during fast forward or rewind operation the tape can remain in contact with the drum. This is essential to facilitate finding a specific passage on the tape quickly (at 200 times normal tape speed). The pull on the tape is then about the same as that on normal video tape.

Recording parameters

Recording parameters are summarized in Table 2. Information is recorded on a main data area as well as on a sub data area, exactly as on a compact disc. However, the sub data area is about 4.5 times as large as that on a CD.

The composition of a single track is shown in Table 3. It is seen that the largest part of the available space is occupied by modulation and subcodes, but the track also contains synchronization data and Automatic Track Following—ATF—zones. These zones enable automatic tracking of the heads. The individual function blocks are separated by the Inter Block Gaps-IBG. This separation is necessary to enable writing in the sub data area without affecting the modulation data. In principle, only the main data and sub data areas are of importance to the user, because these are the parts that are audible to him.

From analogue to PCM

It is seen from Table 2 that the normal recording and playback sampling frequency is 48 kHz (the other sampling frequencies will be reverted to later). Sampling is carried out at a resolution of 16 bits. This means that every 21 μs a portion of the analogue input signal is translated into a 16-bit code. This happens simultaneously for the left-hand and right-hand channels. The digital data are subsequently processed in serial form. The data stream consists, therefore, of $48 \times 10^3 \times 16 \times 2 = 1.536$ Mbit/s.

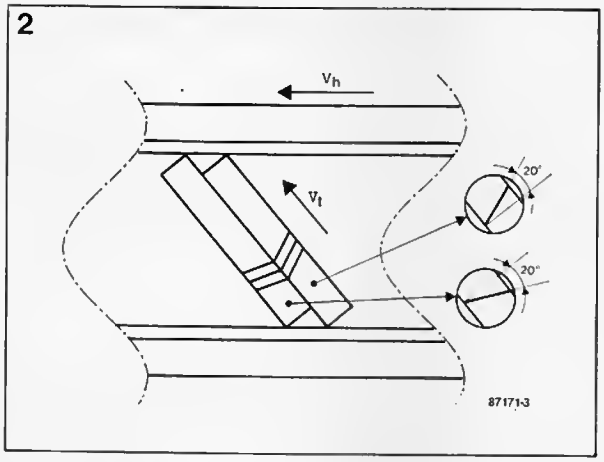


Fig. 2. Arrangement of the tracks on the tape.

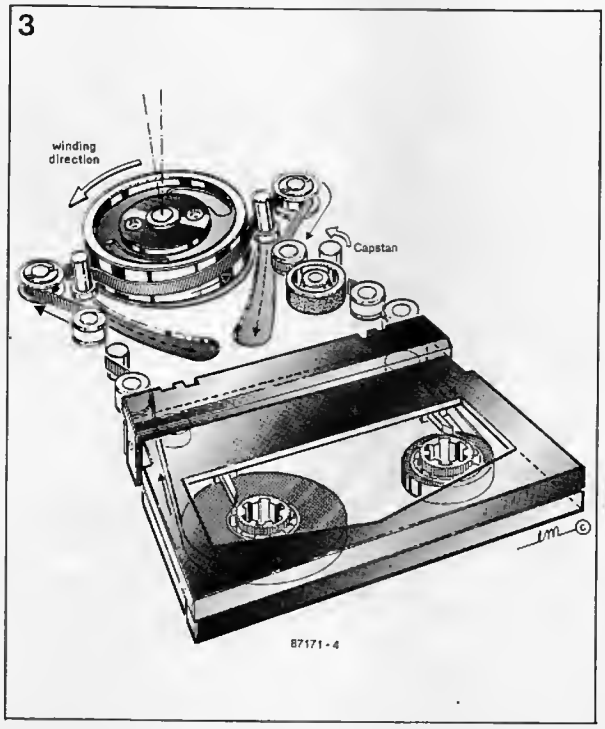


Fig. 3. Exploded view of a digital audio tape cassette.

Table 2

Number of channels	2 (optionally 4)
Sampling frequencies	48 kHz; 44.1 kHz; 32 kHz
Quantization	16 bits linear (optionally 12 non-linear)
Encoding	2 complement
Error correction	double Reed-Solomon code
Sub code	273.1 kbit/s
PCM capacity (each track)	4 kbit
ID codes	68.3 kbit/s
ID capacity (each track)	1 kbit
Transfer speed	2.46 Mbit/s
Information density	114 Mbit/in²

Table 2. Technical parameters of the DAT system.

Processing of PCM data

The PCM data are encoded according to the Reed-Solomon code, which is also used in CD technology. However, in contrast to the CD process, the DAT technique uses the product code of two Reed-Solom codes, which results in an inner and an outer code. The inner code contains the data bits and the parity bits derived from these according to a certain pattern. This encoded block is surrounded by the outer code, which forms its own parity bits form data contained in the inner code. After this, the data are interleaved, i.e., shifted in time, to enable reconstruction of a possibly lost data bit.

The Reed-Solomon coding and interleaving result in a data redundancy of about 37%, which causes the data stream rate to increase to some 2.45 Mbit/s. Added to this are the sub data information, such as the sampling frequency, the number of channels, copy protection, and so on, which finally gives a data stream rate of 2.77 Mbit/s.

The data thus composed are divided into blocks of 288 bits. The modulation zone of a track can contain 128 of these blocks, each comprising 32 bytes: a total of 4096 bytes. Of these, only 2912 bytes are real data: the remainder serve for error correction.

To increase the reliability even further, the data are divided into blocks, each of which contains the even samples of one channel and the odd ones of the other channel. These blocks are cross-interleaved onto the $\pm$ azimuth tracks as shown in Fig. 6. In this way, even when a complete track is lost, or a head malfunctions, reconstruction is possible by interpolation of the adjoining tracks.

Since the heads are in contact with the tape for only 50% of the time, the data can not be read or written in real time. The PCM data are, therefore, stored in a 2×64 kbit auxiliary memory at the sampling frequency, then read at a higher clock frequency, and subsequently writ-

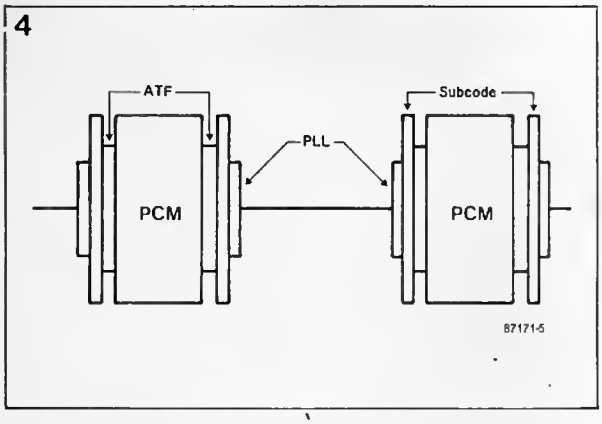


Fig. 4. The output signal of the heads consists of a series of bursts.

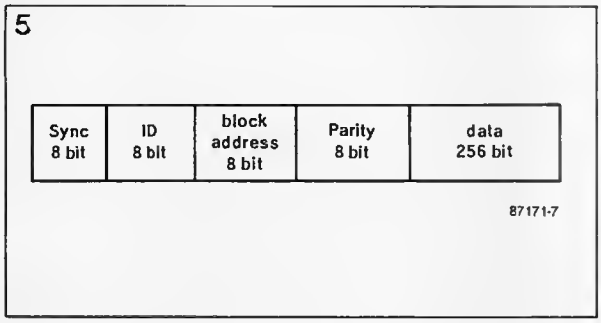


Fig. 5. The composition of the main data area in Table 3.

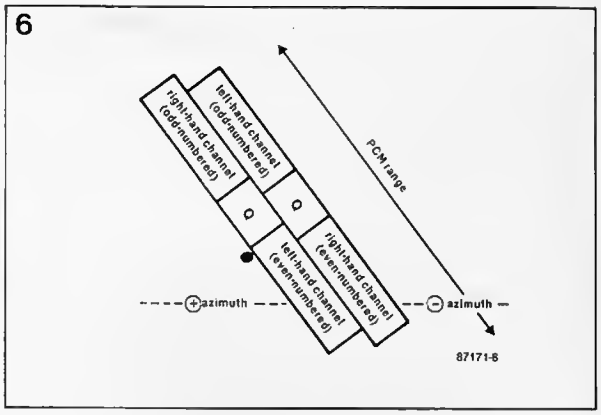


Fig. 6. Illustrating the cross-interleaving of the channels in the modulation range. Areas Q are separation zones between the data areas.

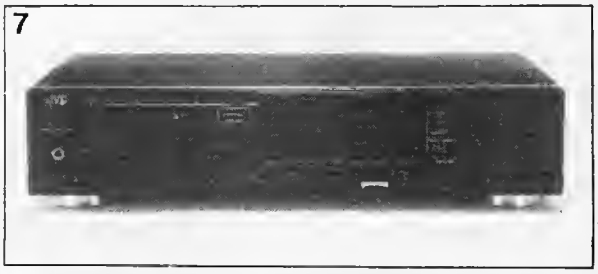


Fig. 7. The JVC Digital Audio Taparacorder.

ten onto the tape. In this manner, the rate of the original 2.46 Mbit/s data stream is increased to 7.5 Mbit/s.

Modulation of data

When writing the data onto the tape, they are not truly modulated, but subjected to an 8-to-10 conversion. Because of the consequent Non Return to Zero—NRZ—a signal edge is only generated if the bit is 1. In this way, the frequency spectrum on the tape is reduced, which is necessary in view of certain properties of the heads and the tape.

Playback

During playback, the operations of the recording process are carried out in reverse order. First, the clock frequency is extracted from the HF signal produced by the heads, after which the signal is reconverted from 10 to 8 bits. Subsequently, the cross-interleaving of the data has to be negated, for which the same 2 x 64 bit auxiliary memory is used. Here, the data are first written and then read again in the correct order. The sub data are separated from the remainder of the information and fed to the system control circuits.

Next, an error correction is carried out with the aid of the double-coded Reed-Solomon code. After this, digital sound data are available which can be processed in a manner similar to those in a CD player. These data are controlled by a digital-to-analogue converter, which may operate with twice or four times oversampling to avoid the necessity of steep-skirted analogue filters.

Sampling frequencies

So far, it has been assumed that the input signal is analogue, for which the sampling frequency is 48 kHz. This frequency is also used for the copying of other DAT tapes (but

Table 3

Araas	Contents	Number of blocks
Marginal area	Margin 1	11
Sub araa 1	Pre-amble 1	2
	Sub data area 1	8
	Post amble 1	1
ATF area 1	IBG 1	3 (2)
	ATF 1	5 (7.5)
	IBG 2	3 (1.5)
Main area	Pre-ambla 2	2
	Main data area	128
ATF araa 2	IBG 3	3 (2)
	ATF 2	5 (7.5)
	IBG 4	3 (1.5)
Sub araa 2	Pre-amble 3	2
	Sub data area 2	8
	Post amble 2	1
Marginal area	Margin 2	11

Note: The number in perentheses is for wida track mode.

Table 3. Tha format of a track (signel allocation) is in accordance with this table.

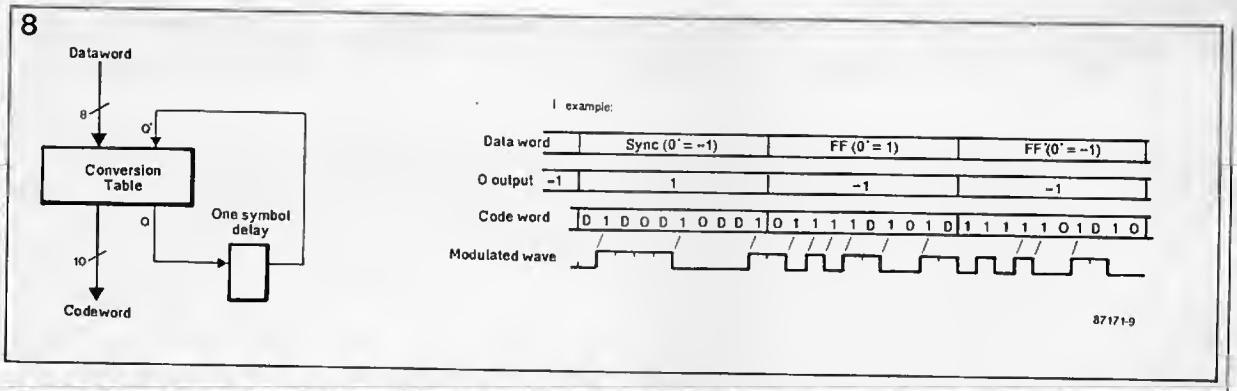


Fig. 8. In the NRZ process a signal edge is generated for each logic high bit.

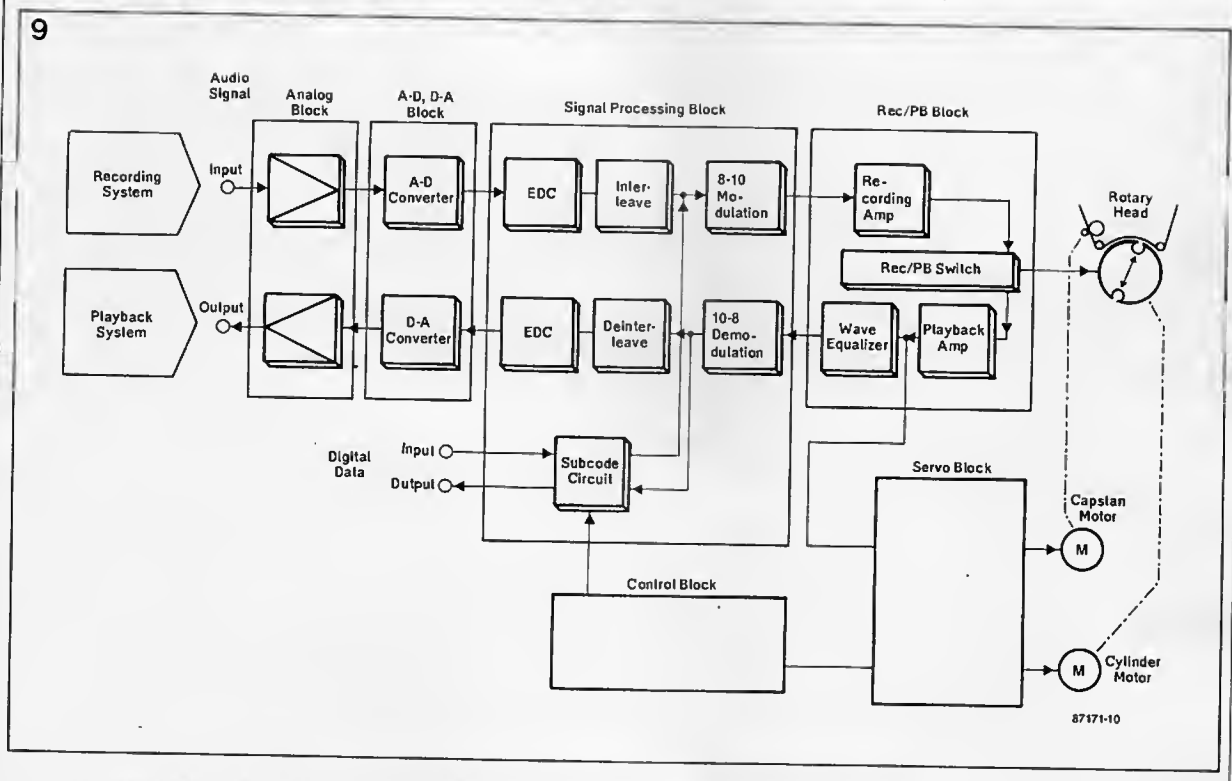


Fig. 9. Block schematic of a typical digital audio taperecorder.

not proprietary pre-recorded ones—see under).

The 32 kHz sampling frequency is used for 4-channel recording of analogue input signals. It is also intended for future recording of digital satellite channels. With this low sampling frequency, the frequency range is limited to 15 kHz.

The sampling frequency of 44.1 kHz (the same as that of compact discs) is provided for the playback of proprietary pre-recorded tapes. This enables makers of these tapes and CDs to use the same mother tape in the production process.

The DAT has a copy protection circuit that prevents the direct recording from compact discs. This is incorporated at the in-

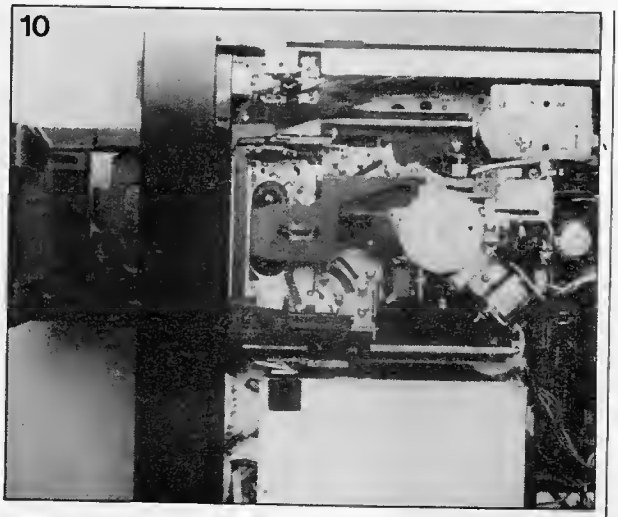


Fig. 10. Typical DAT recorder mechanism.

sistence of the record industry in the western world, backed by their respective governments. In view of the regrettable failure by governments to protect these industries against the nefarious copying of gramophone records, this decision must be welcomed by any sensible person. None the less, there have already been rumours that some DAT manufacturers are threatening to market DATs without copy protection. Fortunately, many governments have already countered these by prohibiting the manufacture or import of such recorders in their countries. It must be hoped that all western countries will be united in this determination.

THE UNIX OPERATING SYSTEM

Now that the US and the EEC are endorsing the UNIX operating system, and the X/Open Group of European and American computer manufacturers are basing their common standards on UNIX, it seems timely to have closer look at this system.

To begin with, it is useful to state that UNIX is no more and no less than a computer operating system, that is, a program that enables users to *operate* the computer according to an agreed set of commands and utilities. Therefore, UNIX

- is not the latest programming language;
- has essentially nothing to do with graphics assisted programming;
- has provisions for manipulating the computer memory, whether resident as hardware, or in the form of a magnetic storage device (tape; hard disk).
- forms the lowest command level for loading and running higher language interpreters and compilers (C; Cobol; Fortran).

UNIX in its most elementary form is fairly crude, and has none of the user friendly features offered by currently available PC operating systems as, say, PC Boss, GEM, POWER, or MS Windows. It is an operating system intended mainly for minicomputers and mainframes that communicate with a number of users via terminals. The system is, therefore, said to have *multi-tasking* and *multi-user* capabilities, and the operating speed of the computer depends on the *processor load* caused by the users accessing and manipulating various data fields, utilities and programs in the memory. One of the most important points about UNIX is its portability, which means that it can be installed on any (big) computer running the C programming language—more about this later. The recently introduced fast PC ATs, hard disks, 80286 and 80386 based PCs, RISC (reduced instruction set) computers, transputers, and the absence as yet of a supporting disk operating system (DOS) from MicroSoft, have furthered the interest in UNIX, which, in its most rudimentary form, has long been the exclusive domain of academic and scientific institutions. Whence, then, the interest in a fairly primitive operating system when existing DOS versions support full-screen command editors, turn-key and ready-programmed utilities for complex file operations, and computer control direct from a keyboard? Surely, these are preferable to a terminal and a serial link to and from the computer? The answer to this is, paradoxically, another question: if the latest computers are so fast, and come with so much memory at affordable cost, why not share their capabilities between several users?

The story of UNIX

The evolution of UNIX is shown simplified in Fig. 1. In 1969, two programmers at the Bell Laboratories, K Thomson and D Ritchie, decided to develop a time sharing system for the PDP-7 computer. The program was written in assembler code, and named MULTICS. Some years later, the higher programming language C was developed, and applied to MULTICS to make this portable to other systems. The resultant operating system was called UNIX, and Bell Labs distributed it to many non-profit institutions, including the University of California, Berkeley. Due to various political and economic reasons, UNIX was further developed in numerous other, mainly academic, institutions, and all standards seemed to be lost for a time. Reseachers at UC Berkeley, however, once more applied the latest version of C to UNIX, and came up with the so-called *C shell*, which gave greater flexibility than the

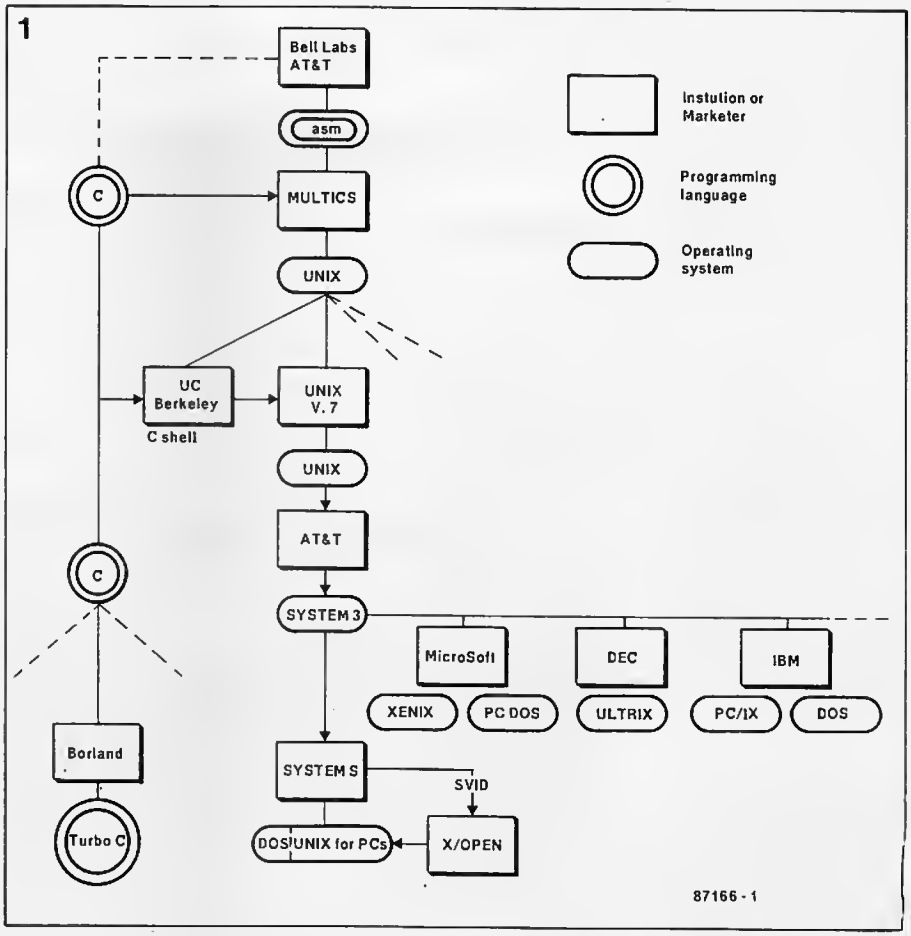


Fig. 1 The history of UNIX is one of many derivatives, licence holders and marketers.

earlier Bourne shell in implementing the system on a mainframe. The shell of UNIX is the part of the software that translates the user's commands into workable code for the *kernel*, which forms the system's "brain". The programs that run under UNIX have direct access to the kernel. Programmers at AT&T reworked UNIX using the C shell, and eventually released SYSTEM 3. They also agreed to support licence holders for this product, and worked on further improvements as to compatibility with previous releases. Microsoft, DEC and IBM were among the many marketeers to use UNIX as the basis for a new operating system. While DEC and IBM worked on software and hardware for mainframes, or, in any case, large computers, Microsoft came up with a version of UNIX that could be implemented on 8086 and 8088 based machines, in other words, the (IBM compatible) personal computer. XENIX is a fairly large operating system, requiring at least 512 Kbytes of RAM, and a 10 MB hard disk. It is a multi-user and multi-tasking system that runs PC DOS as a subset or concurrently. Obviously, the speed of XENIX is not up to that of a mainframe, even if the processor load is relatively light.

PC/IX is marketed by IBM, and is not a true version of UNIX in that it supports but one user. It can, however, run multiple tasks, and supports the DOS functions. Contrary to XENIX, PC/IX uses the Bourne shell.

With the arrival of the previously mentioned new generation of fast PCs, the need arose for a single, standardized, version of UNIX, which at that time existed in a multitude of derivatives. For the first time since the development of MULTICS, written in assembler code, the hardware configuration of the computer running UNIX became a major issue—remember that UNIX in the form of a C file required compiling and adapting certain "modules", particularly in the shell, to suit the particular hardware used; this was all for the sake of portability, which enabled programs written in higher languages, such as Fortran or Cobol, to be loaded and run on many types of computer. It can be argued, therefore, that UNIX owes some of its popularity in the professional fields to the programming language C, which has, meanwhile, developed into many different versions, the best known of which is probably Borland's Turbo C.

Three years ago, a number of computer hardware manufacturers teamed up to form the X/Open Group, which includes Bull, Ericsson, Nixdorf, Olivetti, ICL, Philips, DEC, Unisys, Hewlett Packard, and Siemens. Recently, AT&T also became a member, while Gould and Honeywell are bidding for acceptance in the group.

The aim of the X/Open group is to set the hardware standard for the UNIX operating system, and, possibly, to arrive at a complete integration of UNIX and DOS. The starting point for the Group's proposals is UNIX System 5, and the associated *System V Interface Definition* (SVID) from AT&T. The new version of UNIX will be called POSIX (*portable* UNIX).

Working with UNIX

The scope of this introductory article does not allow detailing every aspect of the UNIX operating system. None the less, some idea will be given how a user communicates with the computer through UNIX, or, more precisely, the UNIX shell. Via the terminal, console or PC, the user must first log into the system and state a valid password to gain access to the files and/or programs in (sub)directories he is authorized to work with. Some of the simpler utilities in UNIX are resident, i.e., always available irrespective of the file or directory currently opened. As an example, Fig. 2 shows the directories available to user Henry2, who operates one of the terminals in the system. Henry2 has access to files in the directories set up for Fortran, Wordprocessing, Desktop Publishing (DTP), and Computer Assisted Design (CAD), but not to Accounting. Each of the directories shown is divided in a number of subdirectories, and files can be transported between them. So far, the system looks very similar to a DOS tree structure. In principle, there is no limit on the number of directories, provided there is enough space on the hard disk. Several users may access the same file simultaneously, and programming tasks may be carrried out in the background, that is, the user starts the relevant command sequence, and the computer determines the appropriate moment for dealing with it and presenting the output. So-called *pipes* and *filters* can be set up to feed the output of one command to the input of the next. Using command **tee**, it is even possible to specify the location of a tee fitting in pipe. This enables feeding data in parallel to two files or command sequences simultaneously.

UNIX has a number of built-in editors, which are all much more powerful than the well-known DOS line editor, EDLIN. Depending on the data involved, and the type of terminal, the user selects the line editor (**ed** or **ex**), the screen editor (**vi**), or the stream editor (**sed**) before calling up a file or running an application program. UNIX has commands and utilities for scanning, concatenating, deleting, copying, dating, sorting, comparing, locking, filtering, encrypting and copying files. If a particular file operation is expected to cause a considerable processor load, it can be carried out in the background, or even in the absence of the operator. In most UNIX based systems, there is a central system controller who assigns the priority levels to the users, and determines whether or not they have access to certain directories. Usually, the controller's own terminal has the highest priority, and is located near the computer. The controller's task is to monitor the processor load, and, if necessary, redirect commands to the background level.

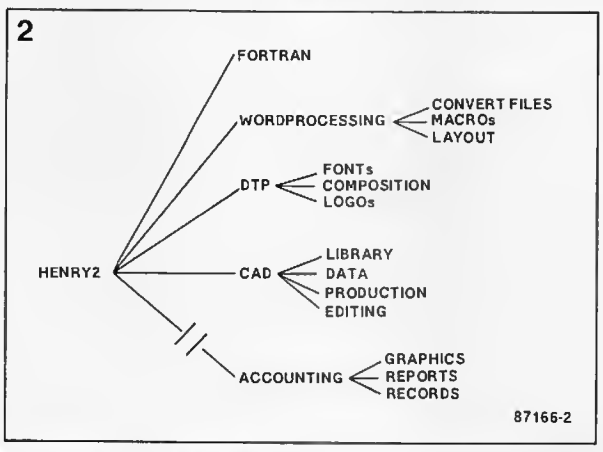


Fig. 2 Example of directories and subdirectories that can be accessed by a user in a UNIX system.

Unix and MS-DOS: competition or integration?

It is interesting to note that the term DOS has become a synonym for *computer operating system*, whereas, strictly speaking, it is only a *disk* operating system. UNIX is a computer operating system in the true sense of the word, and DOS, therefore, forms a part of it.

As already stated, the new 32-bit microcomputers are definitely fast and powerful enough to carry a "heavyweight" operating system such as UNIX, if this is supported by the hardware standards proposed by the X/Open Group. But what is the future of such a standard if IBM is not a member of the group? Every PC user knows that there exists a massive amount of software running under MS-DOS, and fears may arise that this is incompatible with the PC version of UNIX that will eventuallye volve from the Group's activities. Fortunately, IBM considers it "consistent to support Posix as a standard as well as enhancements to it", to quote the company's market development manager, Mr Art Goldberg. IBM, in co-operation with Interactive Systems, has already introduced a UNIX computer for professsional applications: the Type 6150 PC RT UNIX. For 80386 applications, the companies have developed

a virtual machine monitor called VP/ix. This makes it possible to support multiple DOS users under UNIX. Recently, AT&T licensed Microsoft to develop a 80386 based version of UNIX, as a follow up of XENIX.
The Model 80 in the recently launced Personal Series 2 computers from IBM can run the proprietary Operating System 2 (OS2) as well as DOS version 3.3. OS2 is similar to UNIX and XENIX in that it allows running programs in the background. Nevertheless, IBM have tentatively announced their own version of UNIX for the Model 80.

A lot is happening in the current computer scene, and the announcements of major computer manufacturers and software houses concerning UNIX follow in rapid succession. It will take some time, though, before UNIX will be available to the user of a personal computer that is not part of a network. Meanwhile, the development of suitable LANs (local area networks) is an important aspect in the discussion on software for multi-user systems. It is not unlikely that the work of the X/Open Group will provide a strong impulse for the standardization of networks with, say, to 16 users.
As usual in the computer business, the users are after standardization and cost effectiveness, and the manufacturers after increasing their sales. Numerous events in the past have shown that these interests are at best...incompatible.

```
UNIX(r) VAX11/750
#
login:_ henry2
password:_intime
%_who

William tty03 Nov 5 08:15
Anita console Nov 5 08:31
Steve   tty13 Nov 5 09:12

%_write william
pascal programs ready for testing on tty30
o
yes send as \bin file please
oo

%_cd reports
%_ed newdoc
?newdoc
```

.87166

A typical programming or file editing session under UNIX starts with the login procedure.

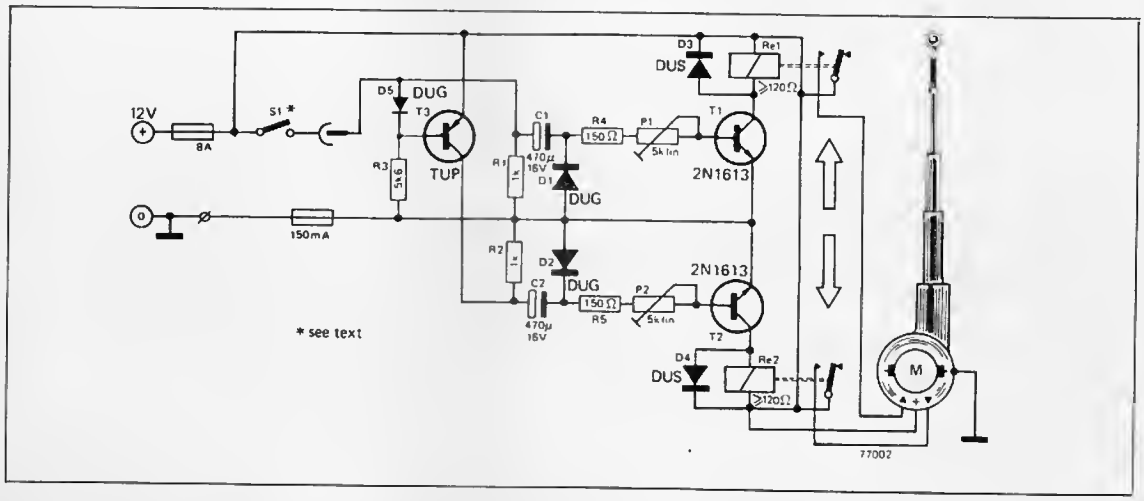
For further reading:

Unix on the IBM PC, by William B Twitty. Glentop Publishers, ISBN 1 85181 061 7.

automatic car aerial

Many motorised car aerials are not fully automatic in operation but are provided with a manual dashboard switch. This has a biased centre off position, and to raise the aerial it is necessary to hold the switch over to one side until the aerial is fully extended. To lower the aerial the switch is held over to the other side until the aerial is fully retracted. It is quite easy to forget to lower the aerial when leaving the car, thus losing the vandal-resistant advantage of a motorised aerial.

The circuit described here will raise the aerial automatically when the car radio is switched on and lower it when the radio is switched off. S1 can be the special switch contact provided for this purpose in some car radios, or an extra lead may be taken from the normal on-off switch, since little extra current is drawn through this contact.
T3 is normally turned on. When the radio is switched on (S1 closed) T3 is turned off. Current flows from S1, charging up C1 through R4, P1 and the base of T1. T1 turns on, energising Re1 and causing the aerial to extend. The time for which the aerial motor runs can be adjusted to the correct value by P1. When the radio is turned off T3 turns on and C2 charges through T3, R5, P2 and the base of T2. T2 turns on, Re2 is energised and the aerial retracts. The time can again be adjusted (by P2).



THE INMOS TRANSPUTER AND OCCAM

A brief introduction to the higher programming language tailored to supporting the transputer's concepts of concurrency and parallel processing.

Traditionally a computer is set up according to John von Neumannn's model: a central processor fetches instructions from a memory, and manipulates data accordingly. Whatever its speed and internal architecture, the processor can only handle a single instruction at a time. This is even true in multi-user and multi-tasking systems such as UNIX and concurrent MS-DOS, where the processor is apparently engaged in several tasks at a time, but in reality assigns time slots to portions of the relevant task(s). Obviously, the faster the processor, the less users are aware of the time sharing process.

The transputer is a radical departure from the von Neumannn concept. Transputers are optimized for true concurrency. Parallel processing of data and instructions is achieved by synchronized, very fast point-to-point communication channels between processes as well as individual transputer modules. There is, in principle, no limit on the number of transputer modules that can be connected to form a computer. In contrast to other processors, transputers enable defining the speed of the system simply by adding as many modules as required. Currently, the IMS T800 transputer from Inmos is the fastest single chip microcomputer available. In the so-called Whetstone benchmark test, the 20 MHz version outperforms all of its 32 bit competitors, including the Fairchild Clipper, the National Semiconductor NS32332—32081 and Motorola's MC68020—68881. Note that the latter 2 are combinations of a microprocessor and a floating point arithmetic co-processor; the transputer has both of these on a single chip. The calculation performance of the IMS T800 is equal to that of the VAX 8600 scientific computer from DEC, while a network of 10 IMS T800 modules offers the speed and processing power of the Cyber 205 supercomputer from Control Data Corporation. Clearly, the hardware concept of true parallel processing implemented in the transputer guarantees a yet unheard of computing power, but at the same time calls for supporting software that exploits the concurrency, and so enables gaining most benefit from the transputer architecture. The answer was given by Inmos themselves in the form of the higher programming language Occam.

Concurrency in software

Before introducing the higher programming language Occam, it is useful to note that a transputer can also run existing scientific programming languages including C, Fortran and Pascal thanks to the availability of suitable compilers. Interestingly, some software houses have applied the parallel programming constructs available in Occam to implementations of existing higher programming languages, with the aim of optimizing speed and performance.

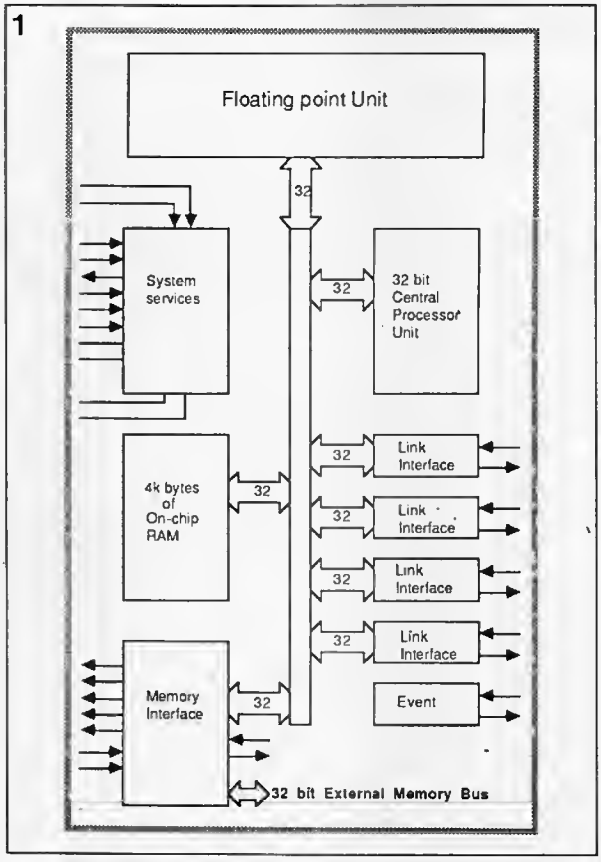


Fig. 1 Block diagram of the IMS T800 transputer module from Inmos.

Occam is not just a new programming language, it is the framework for designing concurrent, transputer-based, systems. As such, it is similar to Boolean algebra as the framework for designing with logic gates. Abstract logic functions can be realized, i.e., built using the actual gates, while the function of a number of these can be analysed in turn by the corresponding Boolean notations. Similarly, a process in a computer can be thought of as a black box, with inputs and outputs. Processes can be connected together by channels to build more complex, concurrently operating, systems. A collection of processes is in itself a larger process with internal and external concurrency. The transputer has a scheduler which enables any number of concurrent processes to be executed together, sharing the processing time. Occam has provisions for supporting this hardware concurrency, and is stated to be as efficient as hand coding, obviating the need for an assembly language. The central processor in the transputer is so fast that procedure calls, process switching and interrupt latency all have a duration in the sub microsecond region. Processes waiting for communication or a timer function do not consume CPU time. The floating point unit in the IMS T800 is a 64-bit type to ANSI-IEEE 754-185, operating fully concurrent with the processor at more than 1.5 MFLOPs. Data between processes is transferred via links, which are either unidirectional or bidirectional. The 4 available links are synchronized DMA block transfer mechanisms operating at a speed of 20 Mbit/sec, with 10 and 5 Mbit/s also allowed for compatibility with other Inmos transputers (IMS T212, IMS T414). The internal 4 Kbyte

memory can be accessed at 120 Mbytes/s, and the IMS T800-30 can directly address an external memory area of 4 Gbytes at a rate of 40 Mbytes/s. The block diagram of the IMS T800 transputer is given in Fig. 1.

There exists a remarkable architectural relationship between Occam and the transputer. With the introduction of Occam, Inmos, like no other semiconductor manufacturer, have succeeded in gearing software to hardware, and vice versa.

In Occam, there are 3 primitive processes, namely input, output, and assignment. Each of these can be performed in 3 ways: sequentially, in parallel, or alternatively. The latter term simply means that whichever data is first available is first processed. Parallel processes are set up by defining channels through which the data is routed. At first sight, Occam programs look very similar to, say, C or even Forth. This is because the writing down of instructions on paper is in fact a sequential process: we can not express concurrency by writing 2 or more instructions over another, since this would make the text illegible. Thus, although the program is still made up of lines of instructions, these are not necessarily executed in the indicated order, or in the order indicated by the instructions themselves (as is the case with, for example, GOSUB, ONERR, or GOTO in BASIC). Also note the complete absence of line numbers.

The structure of an Occam program reflects the hardware concept of parallelism, but the programmer need not bother where and how the actual processes are executed in the transputer. Concurrent programs are by no means easy to write and debug. And yet, Occam is readily learnt once its formal description is known.

The principles

Two brief examples will be given of hypothetical Occam programs reproduced from reference [1]. The first is given in Fig. 2. The protocol of channels comm1 and comm2 is defined as integer transfer with the aid of statement **CHAN OF INT**. **PAR** defines parallel processing. i.e.. the data obtained from the communication process first finished is first dealt with by the processor. The communication processes themselves are defined as sequential by instruction **SEQ**. Variables **x** and **y** are integers. Notice the indentation levels that indicate which statements belong to **SEQ** and to **PAR**. The program shown illustrates the central principle of Occam programming; the **PAR** statement defines that the written order of the component processes is irrelevant, as they are all performed at the same time, i.e, *concurrently*. The idea of several things happening simultaneously in computer programs may be new to many programmers. **PAR** causes component processes to start at the same time, and the programmer need not bother which of these is completed first.

The exclamation mark **!** denotes output, and the question mark **?** input on a channel. It is seen that integer 2 is first output on comm1, before comm2 is allowed to receive variable **x**. At the same time, however, comm1 receives variable **y** before comm2 is allowed lowed to send integer 3. The effect is that each process sends a value to the other: **x** becomes **3**, and **y 2**. Note that the order of the **!** and **?** in each **SEQ** process is important to prevent them waiting for each other's output indefinitely.

The next example is a program for digital volume control on an amplifier. It is assumed that there are 3 buttons, called **louder**, **softer** and **off**, which are arranged to pass their current status to an Occam channel. A fourth channel, **amplifier**, transmits the required value to the volume control chip.

The program of Fig. 3 is fairly easy to read and understand. First, the minimum and maximum value of the volume setting are declared as 0 and 100 respectively. Variables **volume** and **any** are defined as integers. The **ALT** statement indicates alternative processing as long as the WHILE statement is true. In this example, each of the processes that belong under **ALT** are "scanned" for activity, i.e., there is immediate action on part of the program and the transputer hardware when either **louder**, **softer**, or **off** is actuated. For instance, if the **softer** button is pressed, the *sequential* process of decreasing the value assigned to **volume** is started, but this does not mean that the other **ALT** processes are not continuously interrogated for activity. The program terminates when the **off** button is pressed, since this ends the validity of the WHILE statement.

Conclusion

The previously discussed programs illustrate only a few of the many instructions and statements available in Occam. It is beyond doubt that Occam is currently the only language that enables profiting from the concept of parallel processing in a network of transputers.

Inmos have a vast range of products to aid in learning to work with transputers. As to hardware, there are, for instance, memory extension modules, a chip with a very fast colour lookup table (CLUT), link switch and adaptor modules, and, most importantly, development and evaluation systems. These are available for various computers, including the VAX/VMS, and the IBM PC XT/AT. Also available are complete evaluation modules composed of a rack, a busboard, a power supply, and cards with an option for fitting a number of IMS T414 or IMS T800 transputer modules. Clearly, Inmos, in contrast to many of its (would-be ?) competitors, deserves credit for presenting hardware **and** supporting software for a computer concept that is both completely new and close to real life, since it is based on concurrent rather than sequential processing. *Bu*

Reference:

[1] *A tutorial introduction to OCCAM programming*, by Dick Pountain.

More information on transputers and Occam can be found in:

The transputer family: Product Information.
Inmos Spectrum.
IMS T800 Architecture.

All publications are available from Inmos Limited • 1000 Aztec West • Almondsbury • Bristol BS12 4 SQ. Telephone: (0454) 616616. Telex: 444723.

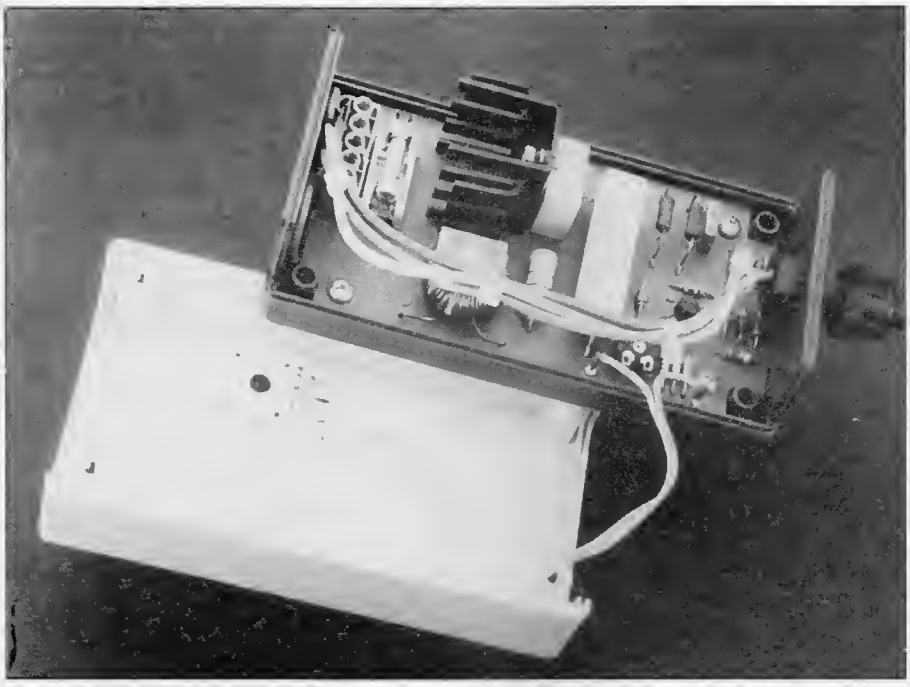
2
```
CHAN OF INT comm1, comm2:
PAR
  INT x:
  SEQ
    comm1 ! 2
    comm2 ? x
  INT y:
  SEQ
    comm1 ? y
    comm2 ! 3
```

Fig. 2 Illustrating how Occam makes the distinction between parallel and sequential constructs.

3
```
VAL maximum IS 100 :
VAL minimum IS 0 :
BOOL active :
INT volume, any :
SEQ
  active := TRUE
  volume := minimum
  amplifier ! volume
  WHILE active
    ALT
      (volume < maximum) & louder ? any
        SEQ
          volume := volume + 1
          amplifier ! volume
      (volume > minimum) & softer ? any
        SEQ
          volume := volume - 1
          amplifier ! volume
      off ? any
        active := FALSE
```

Fig. 3 This Occam program controls the digital volume input on a hypothetical AF amplifier.

DIMMER FOR INDUCTIVE LOADS



A simple circuit overcomes the well-known difficulty in maintaining the triggered condition of a silicon controlled rectifier when this is used for regulating inductive loads.

The vast majority of dimmer circuits is only suitable for regulating resistive (*non-reactive*) loads, i.e., when there is no phase difference between the mains voltage and the load current. This means that the trigger pulses can be kept relatively short, since the load current is in phase with the mains voltage immediately after triggering has taken place. Normally, the load current is greater than the holding current, so that the triac or thyristor is triggered immediately, and remains on.

When the load is mainly inductive (e.g. a transformer, or a choke for a fluorescent lamp) the load current lags the voltage, and may either not have reached, or exceeded, the holding level. The SCR then conducts briefly, but is switched off at the end of the trigger pulse. This unwanted effect can be kept within limits by means of stretching of the trigger pulse, triggering by pulse trains, or the use of an R-C network. The first approach calls for a control circuit with appropriate drive power. The pulse duration requires exact controlling to prevent pulses occurring after the zero crossing of the mains voltage, causing erroneous triggering. Suitable circuits to accomplish this are, understandably, relatively complex.

A simpler way out is the R-C network, which in essence raises the current to the holding threshold, so that the SCR remains on when the trigger pulse is inactive. Although SCR manufacturers usually provide the relevant design data for this application, it is still fairly difficult to dimension the circuit for optimum and reliable triggering. In most cases, therefore, trial and error adjustments are required, as well as signal analysis with the aid of an oscilloscope.

Triggering by pulse train

The circuit described here is based on gate triggering by a pulse train, yet is composed of discrete components only.

Figure 1 shows 3 ways of controlling a triac.

Figure 1a illustrates a phase angle control circuit for the load Z_L. It is composed of a triac T, a diac D, and a timing network *R-C*, where *R* is (P), connected in parallel with D-A_2, and *C* is connected in parallel with D-A_1. In this circuit, the triggering is load dependent, in other words, synchronization is by the voltage across the triac, and this is a function of the load current. The circuit is, therefore, unsuitable for regulating highly inductive loads requiring a small conduction angle. Also, there exists a strong tendency to asymetrical operation, which can be dangerous in view of saturation of the inductance due to the relatively high direct current.

Figure 1b shows a basic circuit for triggering the triac by the mains voltage. Here, timing resistor (P) is connected to the neutral line instead of parallel to D-A_2. The trigger pulses occur with a fixed phase difference of 180°, irrespective of the load current. Although this circuit offers more accurate control of the load than the previous one, its operation becomes completely asymmetrical if the gate angle is smaller than the angle representing the current lag in the load. Another disadvantage is the requirement for connection to the phase and neutral lines as shown in the diagram.

Figure 1c shows a slightly more complex triac control circuit. Following the trigger pulse, additional pulses are generated up to the next zero crossing of the mains voltage. The operation of the circuit is illustrated in timing diagram Fig. 2. Assuming a phase difference, φ, of 85° between the mains voltage and the load current, and a gate angle, Φ, of 60°, the triac is triggered after the trigger delay has lapsed (A), and remains on up to about 240° (B) thanks to the pulse train. It is blocked at point B, but is immediately retriggered by the next repetitive gate pulse. The operation is slightly asymtrical during the first half periods, but the duration of conduction gradually becomes more balanced, as shown by the dotted curve.

The practical circuit

The circuit diagram of the dimmer for inductive loads is given

in Fig. 3. A small, sensitive, auxiliary triac, Tri_2, generates the pulse train necessary for maintaining the gate control signal for Tri_1. Capacitor C_1, compensation resistor R_5 and potentiometer P_2 define the gate angle Φ. Preset P_1 enables setting the minimum conduction angle, so ensuring reliable triggering of Tri_1 even when the load current is fairly low.

Capacitor C_1 is charged from 0 V, and diac Di_1 triggers as soon as its breakover voltage is reached. The set conduction angle is equal for both half periods.

A first pulse is applied to the gate of TRi_1, and the voltage surge on R_8 triggers Tri_2. Once this is on, it bypasses resistance $(R_4+P_2 \,//\, R_3+P_1)$, so that the remaining charge cycles of C_1 have a much shorter period $(R_5+R_6)C_1$. After this delay, Tri_2 is triggered, starting a new cycle. A succession of pulses is applied to the gate of the main triac, Tri_1, until the mains voltage reaches the zero crossing. Triac Tri_2 is then blocked, so that the charging of C_1 during the following half period is determined by the time constant set by the resistance $(R_4+P_2 \,//\, R_3+P_1)$. Once more consult the timing diagram of Fig. 2 for further details on the operation of the circuit.

Zener diodes $D_5 \ldots D_8$ incl. afford protection against overvoltage, and at the same time ensure a stable supply voltage for the trigger circuit, eliminating instability due to fluctuations on the mains. Diodes $D_1 \ldots D_4$ incl. and resistors R_1 and R_2 ensure that C_1 is completely discharged during the zero crossings, so that the hysteresis remains within acceptable limits. Damping network C_2-R_7 has a stabilizing effect on the control circuitry because it suppresses needle pulses originating from the inductive load when this draws less than the holding current of the main triac.

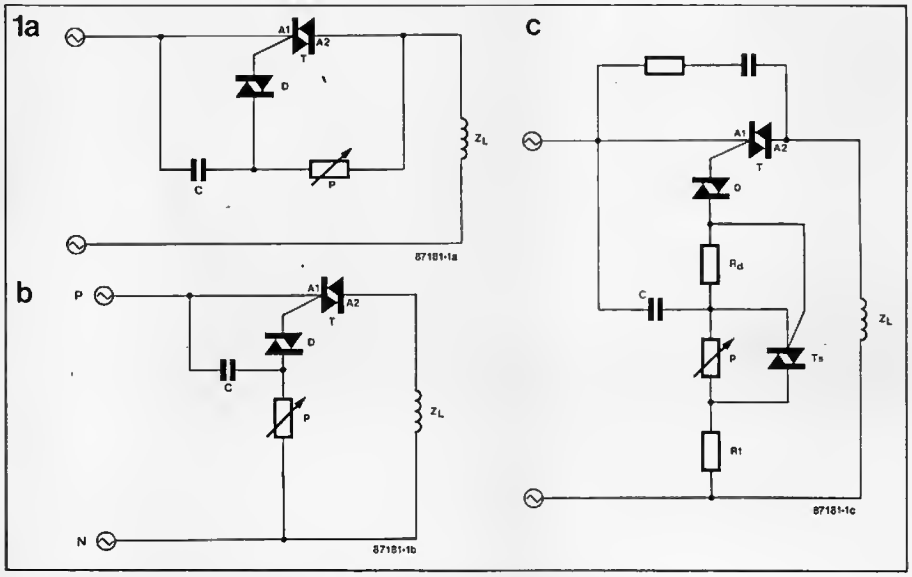


Fig. 1 Three ways of controlling the gate angle in a triac based dimmer.

Construction: safety first

The dimmer is constructed on the printed circuit board shown in Fig. 4. Power resistor R_5 should be fitted slightly off the board to allow for its dissipated heat. Inductor L_1 is a common triac suppressor choke, which is not strictly required for in-

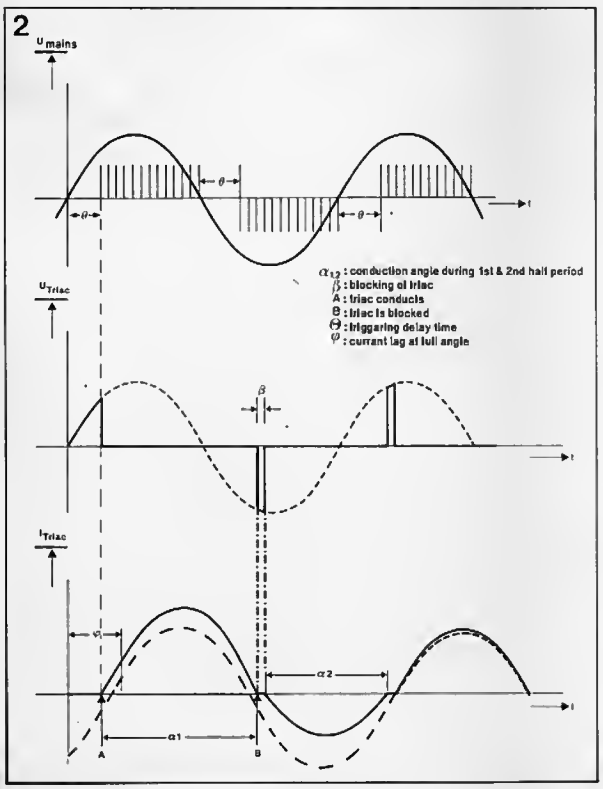


Fig. 2 Triggering by a pulse train synchronized with the mains voltage.

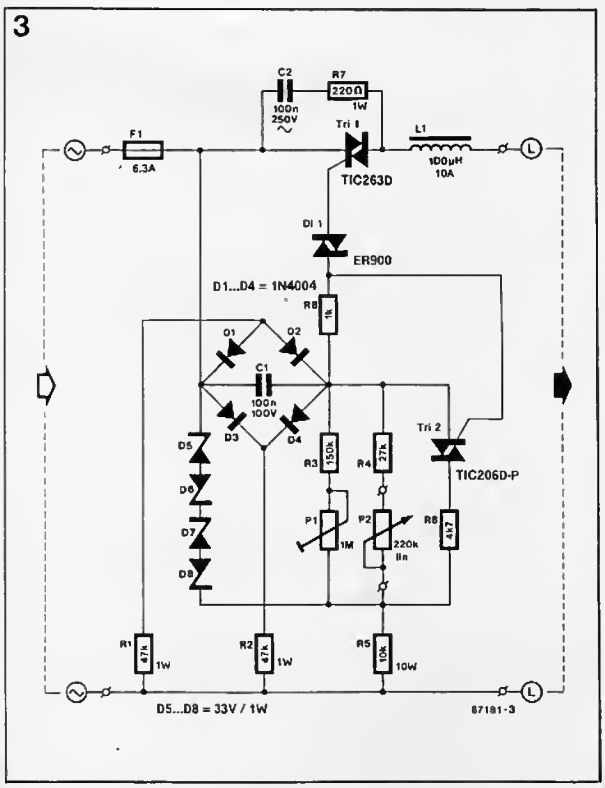


Fig. 3 Circuit diagram of the dimmer for inductive loads.

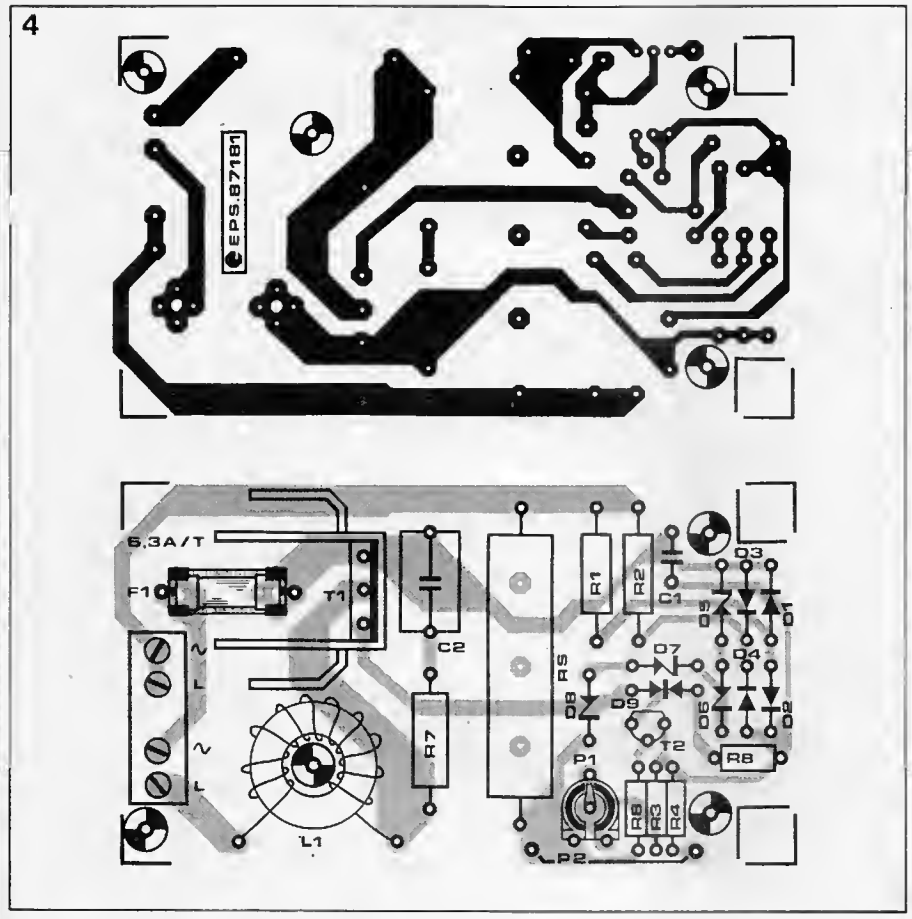


Fig. 4 Track layout and component mounting plan for the dimmer PCB.

ductive loads. For resistive loads, however, it should not be omitted because it limits the switch current surges. The inductance and current rating of L_1 are as required by the load; the indicated values of 100 μH and 10 A are only required when the dimmer is used for regulating loads of the order of 750 W and more. The size of the heat-sink for Tri_1 is mainly determined by the available space in the ABS enclosure. A few holes should be drilled in the lid to ensure sufficient cooling of R_5 and Tri_1. Make sure that the whole unit is rugged and properly insulated. If used, the input and output cable should be fed through a grommet, and secured by a suitable strain relief. Be sure to use a potentiometer with a plastic shaft.

VARIOUS PARTS IN THE DIMMER CARRY THE MAINS VOLTAGE AND ARE, THEREFORE, DANGEROUS TO TOUCH WHEN THE UNIT IS OPERATIONAL.

Finally, the circuit described offers good accuracy of control without the need for an additional supply. It enables virtualy complete variation of power on inductive loads rated up to approximately 1,000 W.*Sv*

Source:

Triac Applications, Thomson Semiconductors.

Perts list

Resistors (±5%):
R_1;R_2 = 47K; 1 W
R_3 = 150K
R_4 = 27K
R_5 = 10K; 10 W
R_6 = 4K7
R_7 = 220R; 1 W
R_8 = 1K0
P_1 = 1M0
P_2 = 220K or 250K linear potentiometer with insuleted shaft.

Capacitors:
C_1 = 100n; 100 VAC
C_2 = 100n; 250 VAC

Inductor:
L_1 = dimmer suppression choke e.g. 47μH; 10 A *

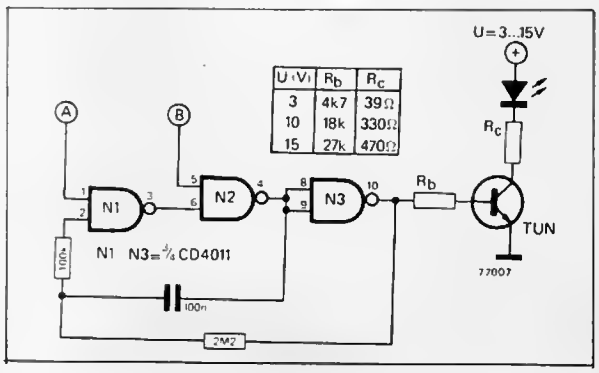
Semiconductors:
D_1 . . . D_4 incl. = 1N4004
D_5 . . . D_8 incl. = 33 V; 1 W zener diode
Di_1 = general purpose 32 V diac, e.g. ER900, ST2, D132AC, or BR100-03*.
Tri_1 = TIC263D*
Tri_2 = TIC206D-P

Miscellaneous:
F_1 = 6.3 A fuse with PCB mount holder.
Suitable ABS enclosure.
Grommet and strain relief for mains wire.
5-way screw terminal block for PCB edge mounting.
TO220-style heet-sink for Tri_1.
PCB Type 87181 (available through the Readers Services).

* Available from Omni Electronics • 174 Dalkeith Road • Edinburgh EH16 5DX. Telephone: (031 667) 2611.

LED logic flasher

The condition of the LED is determined by the logic states of the two inputs A and B. If A is low and B is high then the LED will be lit continuously. If B is low then the LED will be extinguished, irrespective of the state of A. If A and B are both high then the astable multivibrator comprising N1, N2 and N3 will start to oscillate and the LED will flash at about 3.5 Hz. Component values are given for supply voltages of 3, 10 and 15 V. At the maximum supply voltage of 15 V the current consumption is less than 25 mA.
Source: RCA CMOS Application and design ideas.



PRECISE MOTOR SPEED REGULATOR

by Arturo Wolfsgruber *

By virtue of an innovative dual control loop scheme, the TDA7272 motor speed regulator chip achieves both fast response and long-term stability without speed sensors.

The speed of small DC motors is usually controlled either by regulating the current or with a velocity feedback loop using a tacho generator or speed sensor. But both of these systems have disadvantages. Current control offers a fast response to transients but poor long term stability, while velocity feedback schemes need a costly tacho generator and only provide an adequate transient response if a high-frequency AC tacho is used.

A new motor speed regulator chip, the SGS TDA7272 (Fig. 1), combines the best features of the two techniques, having a current control loop to guarantee fast transient response, plus a velocity feedback loop to guarantee long term stability. Unlike conventional velocity feedback controllers, the TDA7272 needs no tacho generator or speed sensor; it determines the motor rotation speed exactly by sensing the motor's commutation spikes.

H-bridge output delivers 1 A

Originally designed for autoreverse cassette tape players, the TDA7272 includes a H-bridge output stage capable of driving a DC motor in both directions with a single supply and delivering up to 1 A peak output current.

Two logic inputs select the direction of rotation—clockwise or counterclockwise—and fast braking (with the motor short-circuited by the device's output stage), or the standby/free-running mode where all four transistors in the bridge are turned off.

By means of external resistors or control signals the rotation speed may be set independently for each direction. In a typical μC-controlled autoreverse car cassette player the two speed control inputs are commoned and connected to ground via a resistor which sets the play speed and is shorted by an open-collector output to select the fast forward/rewind speed.

The TDA7272 operates on a 5-18 V supply and includes protection against load dump transients, output short circuits and thermal overload.

The device is assembled in a special high power DIP package called Powerdip 16+2+2. This 20-lead package has a thick copper leadframe and uses the four center pins to conduct heat from the die to the printed circuit board copper. Suitable for automatic insertion, this package is ideal for applications where space is limited.

Senses motor commutation spikes

One of the most interesting features of the TDA7272 is its ability to determine the true motor rotation speed by sensing the commutation spikes across the motor terminals.

Figure 2a shows the current waveform in a typical three-phase miniature DC motor. In the TDA7272 this waveform, converted into the corresponding voltage waveform by a sensing resistor, is differentiated and clipped to obtain a feedback signal consisting of six pulses per rotation (Figs. 2b & 2c). A hysteresis of 10 mV and 20 mV bias in the clipping comparator assure sufficient noise immunity to make this scheme reliable in practice.

In a typical cassette player the motor runs at about 2000 rpm so the tacho pulse signal will be roughly 200 Hz.

These pulses are then integrated to provide a voltage proportional to the motor speed. This voltage is compared with a reference voltage—derived from the speed-setting inputs—in the error amplifier.

However, the integration capacitor must be large to minimize ripple, which explains why pure tacho feedback schemes suffer from a poor transient response.

This is where the TDA7272's

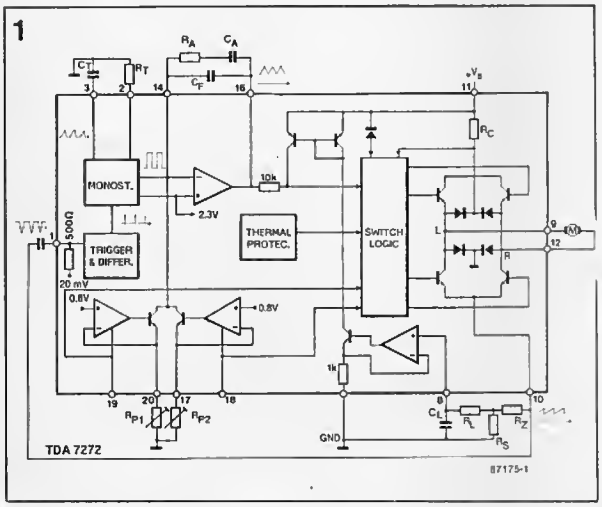


Fig. 1. Internal diagram of the TDA7272 motor speed regulator chip.

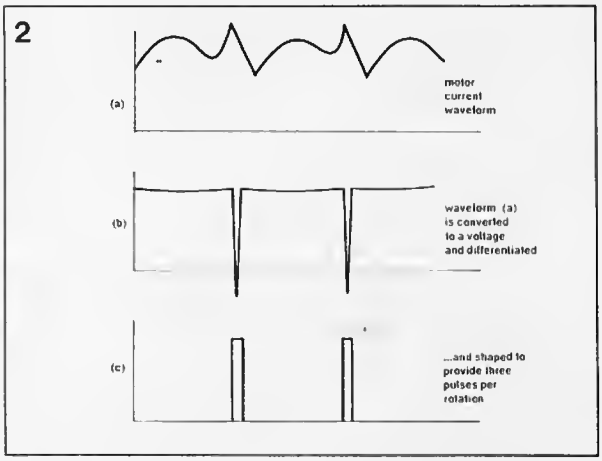


Fig. 2. To obtain a tacho signal without a tacho, the TDA7272 amplifies the commutation spike waveform across the motor terminals, differentiates it, and clips it to provide six pulses par rotation (from a typical three phase motor).

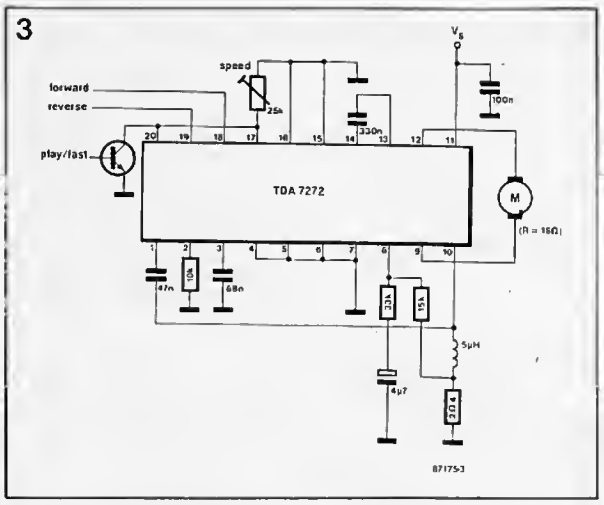


Fig. 3. In a typical autoreverse car-cassette application, the TDA7272 speed controller drives a bidirectional motor and both feedback loops are active. Rewind speed is selected by shorting the resistor on pins 17 & 20.

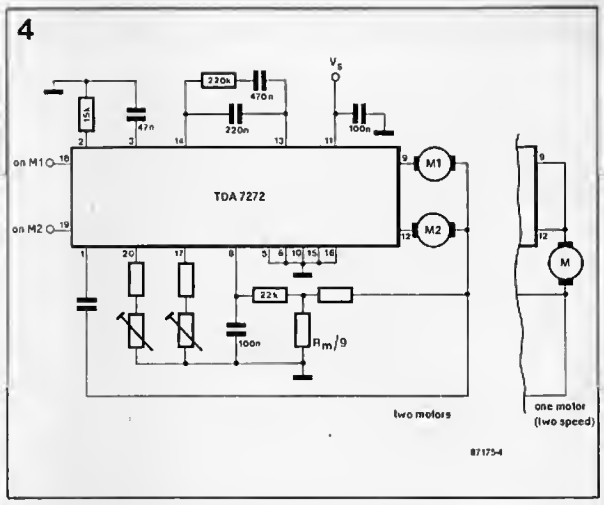


Fig. 4. The TDA7272 may also be used to drive two one-way-only motors running at different speeds, or one motor running at two speeds.

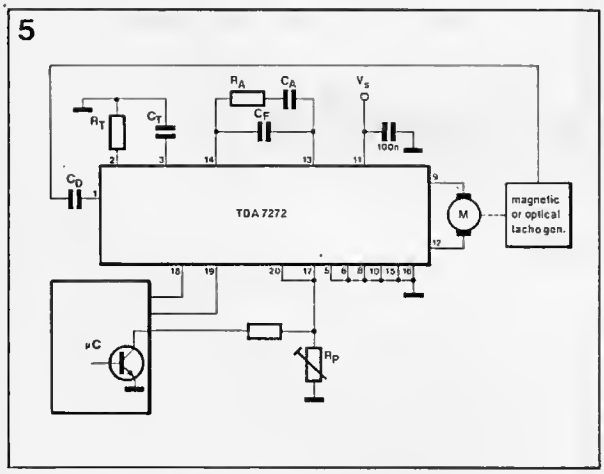


Fig. 5. A tacho generator can be added where greater noise immunity is needed. If the tacho frequency is above 2 kHz the current loop is unnecessary, allowing a saving in external components.

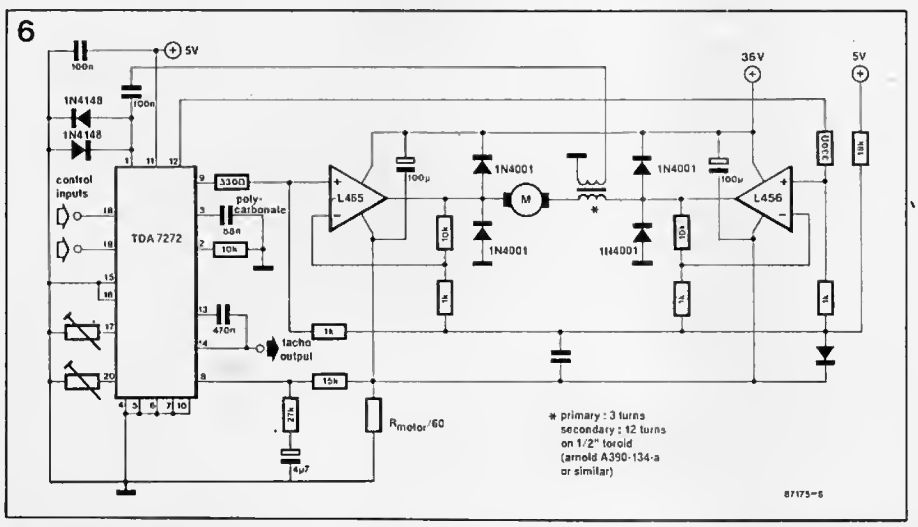


Fig. 6. Where the TDA7272's 1 A output capability is insufficient, power opamp boosters can be added as shown here.

second control loop comes in. Current feedback from the motor is summed with the output of the error amplifier. Consequently, large transient speed changes are compensated immediately by the current loop, leaving only a small error for the velocity loop to correct in order to maintain a precisely controlled speed.

An external resistor sets the amount of V/I 'preregulation' superimposed on the tacho control loop. This resistor is chosen to provide the optimal balance between transient response and speed precision for each application. The current control loop can even be inhibited completely to save components in applications where both the motor's load and supply voltage are sufficiently constant to obviate the need for fast transient response.

Useful in many applications

The TDA7272 motor speed controller is useful in many applications where precise (±1/1000) speed control of small DC motors is required.

Figure 3 illustrates how the device is used in an autoreverse car-cassette player or tape recorder, driving a single bidirectional motor. In this application both control loops are used. The effective speed control provided by the TDA7272 is important in tape players since it affects directly the audio quality, minimizing wow, flutter and pitch errors.

Note how an open-collector output of the µC chip selects either play or rewind speed by shorting the speed setting resistor.

The TDA7272 can be used equally well in applications where the motor never reverses. Alternatively, a single device can drive two motors operating at different speeds, or a single two-speed motor as shown in Fig. 4.

Though the device was designed for use without tacho generators, it can easily be used with one, or with a digital-type speed sensor. This can be useful when, for example, greater noise immunity is required, or where a motor/tacho combination is already

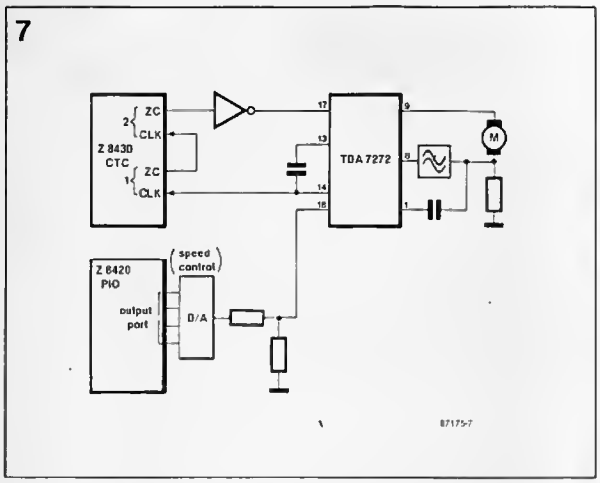


Fig. 7. The tacho signal derived by the TDA7272 from the motor commutation spikes can be useful to count the number of revolutions. Two 8-bit counters cascaded in the Z8430 CTC count up to 10923 revolutions.

available. Moreover, if the tacho frequency is high enough—at least 2 kHz—the current feedback loop is not necessary, permitting a saving in external components, as shown in Fig. 5. For applications where the TDA7272's 1 A output capability is insufficient, high power opamp boosters such as the SGS L465 may be added as shown in Fig. 6. This circuit delivers up to 4 A with a motor supply of 40 V. High power speed control circuits like this are useful in the industrial and electromedical fields.

Another useful feature of the TDA7272 is that a TTL-compatible tacho signal—derived from the commutation pulses—is available on pin 14; there are 6 pulses per rotation. This output can be used, for example, to count the revolutions for applications such as measuring the flow rate of a pump, or the travel of a servomechanism. The pin 14 tacho output may be connected to a presettable up/down counter, or to a counter/timer peripheral such as the Z8430 (Fig. 7). Using an 8-bit counter in the Z8430 it is possible to count up to 42.5 revolutions; 2 cascaded 8-bit counters can count up to 10923 revolutions. In the circuit of Fig. 7, a Z8420 parallel I/O peripheral controls the motor speed through a D/A converter.

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COMPUTER SCIENCE'S HOLY GRAIL

The art of computing gave birth to its own science, which, since it is abstract and mathematical, is a mystery to most people. This is a pity because computer science explores the limits of tomorrow's computers. The next three pages examine its practitioners' current obsession: "P=NP?"

Suppose you have 10,000 numbers and want to find out quickly whether any group of them adds up to 17. This sounds a straightforward enough job for a computer. Alas, this is not the case. Take the problem to a computer programmer and he will shake his head sadly and say that he does not know any practical way to do it. This is strange, because computers do all sorts of complicated things in a trice. And the 10,000-number problem is, after all, so simple that it can be stated in one short sentence. You have stumbled on a member of a class of problems known as NP. In fact you have hit a problem in this class that is in some ways the most difficult of all (computer scientists call it an NP-complete problem). NP has had computer scientists tied up in knots for the last 15 years. Nobody has found a way of making these problems easy, but nobody has shown that there is no way to do so.

It is more than idle curiosity that drives theoretical computer scientists to search for an answer one way or the other. It would be useful to have fast solutions to some of the problems in NP. The travelling-salesman problem, a mathematicians' old chestnut, is an example. It seeks the cheapest route for a salesman who must visit several cities on a sales trip. No fast way to solve it is known, but nobody has shown that there is no way. NP-problems are in limbo: are they different from the class of problems with fast solutions (called P) or are they one and the same? This question, usually put as "P=NP?" in shorthand, has become the Holy Grail of theoretical computer science.

Remember that our number problem was said not to have a practical solution by computer. What exactly does it mean for a problem to have a practical computer solution? Suppose you work for a telephone company and need to produce the local telephone book. At some point you have to sort through the list of everybody who has a telephone line. Since, for some cities, this can involve millions of names, you need to make sure it can be done quickly. And you not only have to consider how well the computer sorts this year's names, you also have to worry about next year. You need a program that does not take too much additional time as the number of names increases. The best measure of the efficiency of such a program is an indication of how the computation time needed to perform the task rises with the number of names. The relation between the running time and the size of the input (here, the number of names) is called the time complexity of a program.

Computer theorists say a problem has a practical computational solution if there is a program with polynomial time complexity that solves it (or, alternatively, that it can be solved "in polytime"). This means that the time needed to solve it depends directly on the size of the input, or on the size of the input multiplied by itself, or on the size of the input multiplied by itself twice, or thrice, or four times, and so on.

Such problems are said to be in the class P (for polynomial time). Like all theorists, computer theorists tend to be a little unrealistic at times: actually, despite this definition, not all P-problems have genuinely practical solutions. Most programs that run in a time that is any larger than the size of the input cubed (ie, multiplied by itself twice) are probably going to be impractical. This is because the greater the power of the polynomial (the more times you multiply the size of the input by itself) the longer the program will take as the input size increases.

Towards exponential blow-up

NP is the class of problems with solutions that can be checked in polynomial time. For example, in the "subset-sum problem" considered at the beginning of this article: if you want to convince somebody that there is a group of numbers whose sum is 17, all you need do is provide a group that does add up to 17. A computer takes practically no time at all to add up a given group of numbers and check whether or not the result is 17. Note that this implies nothing about how hard it is to find a solution, only that if somebody thinks they have a solution, a computer can easily check it. The trouble with problems such as subset-sum is that however hard computer scientists try, they can come up with little better than a program that inspects every possible group of numbers from the 10,000 provided and checks to see if the sum is 17. With a few tricks, it is possible to get the number of combinations to be inspected down to just over one thousand billion billion billion. Given that the fastest computers operate at a rate of mere millions of instructions per second, solving the problem is a lost cause.

This obstacle is known as exponential blow-up. All the known programs for problems such as subset-sum and the travelling salesmen suffer from the fact that when you add just one more element to the input (such as one more city in the case of the travelling salesman) the amount if computation time required is multiplied by some number. Such a program is said to have exponential time complexity. This quickly makes the computation time extremely large. Imagine a chessboard with a penny on the first square, two on the second square, and so on, with the number of pennies doubling on each square. On the last square, there will be enough pennies to buy around ten billion tons of gold.

When computer scientists defined the class P in 1964, NP was not even a dot on the horizon. But they were turning up problem after problem that exhibited the troublesome features of subset-sum: easy to check a solution if you have one, difficult to find the solution in the first place. Scheduling the operation of different bits of machinery at a factory to get the most efficient production is another such problem, for which no polynomial-time program has yet been found. Current programs use rough and ready rules of thumb to get an answer that is good, but probably not the best.

During the 1960s, scientists noticed that some NP problems could be reduced to other NP problems, which turns out to be a helpful start. For instance, a travelling-salesman problem can be converted into an instance of the subset-sum problem with the help of a conversion program that runs in polynomial time. At the moment, this does not help much because subset-sum problems are just as difficult to solve as travelling-salesman problems. But if you could find a polynomial time solution to subset-sum problems, you could automatically get a polynomial solution to travelling salesman problems by tacking the program to solve the subset-sum problem on to the conversion program. This is because the running time for the two-part program would be the sum of the times for its constituent programs, and adding two polynomials gives you another polynomial. Suddenly, solving many problems became as easy—or as difficult—as solving one of them.

The main breakthough came in 1971 when Dr Stephen Cook, a computer scientist at the University of Toronto, proved a remarkable theorem. He showed that all NP problems could be reduced to a single NP problem in logic called satisfiability (or SAT). If SAT has a fast solution, every NP problem has a fast solution. SAT is therefore said to be an NP-complete problem. It became, in one sense, the most difficult problem in NP. In 1982, Dr Cook got a Turing award—computer science's equivalent of the Nobel prize.

Hard on Dr Cook's heels came Dr Richard Karp from the University of California at Berkeley. Dr Karp reduced SAT to a raft of other NP-problems. At first, this sounds an odd thing to do because Dr Cook had already shown that everything in NP can be reduced to SAT. But the fact that SAT itself can be reduced to subset-sum, and to a handful of other NP-problems, as Dr Karp showed, means that SAT cannot be harder to solve than subset-sum. Dr Cook's reduction of everything in NP to SAT showed, in effect, that nothing in NP was harder than SAT, so—taking Dr Cook's and Dr Karp's results together—it follows that nothing in NP is harder than subset-sum. Subset-sum, like SAT, is NP-complete. Dr Karp, who gave the question "P=NP?" its present form in a paper published in 1972, won the Turing award in 1985.

Dr Leonid Levin, a Russian mathematician now at Boston University (there are quite a few emigré Russian mathematicians working in computer science in America) developed the concept of NP-completeness independently, if a litte later than Dr Cook and Dr Karp. The concept of completeness is crucial to a problem such as "P=NP?". Either you show that P=NP is true or you show that it is false. To show that it is true, you must show that every NP-problem is in P. But there are infinitely many NP-problems. On the other hand, showing that P=NP is false would mean producing an NP-problem that cannot under any circumstances be solved by a polynomial time program. Which problem from NP do you select? You may choose one only to find that it does belong in P, which still leaves you in the dark about all the other (infinitely many) problems in NP.

The concept of NP-complete problems helps you here, because it tells you which problems in NP to look at. The NP-complete problems are the hardest ones in NP. If any NP-complete problem can be shown to be in P, then all of NP is in P. Likewise, if you are working on the assumption that NP is different from P, your best bet is to show that some NP-complete problem is not in P, because if any problem in NP is not in P it will be the hardest one. Cook's theorem allowed computer scientists to confine their attention to the complete problems, and ignore the rest.

Can oracles help?

Even so, and despite their best efforts, computer scientists have got nowhere with the problem in the 15 years since Dr Karp first brought it to their attention. Perhaps surprisingly, there are three possible answers to "P=NP?": yes, no, and indeterminable. Although each has its champions, most computer theorists believe that the answer is no—largely because people have been trying to find polynomial time programs for NP-problems for a long time, and have failed miserably.

Not only have computer scientists failed to prove that P is not equal to NP, they have managed to show (worse luck) that one of the traditional methods for distinguishing classes of problems can work in the case of NP. This emerged from work on some strange computers called oracle machines.

Imagine an ordinary computer that is attached to a black box. In the black box lives an elf, who is an expert on a certain problem—call it A—but doesn't know about anything else. If a programmer asks the elf true-or-false questions about A, the elf answers instantaneously. Now it is possible to define two classes of problems, P^A and NP^A in the same way that P and NP were defined: P^A is all problems that can be solved in polytime by the computer with the aid of the elf, while NP^A is all problems that have solutions that can be checked in polytime. The computer now has the extra power of this elf, or oracle. With this extra power the computer can solve problems in far less time than before. Suppose, for example, that the elf knows all about subset-sum. Then the oracle computer can compute any NP-problem in polynomial time, since it need only convert the NP-problem to subset-sum

(which takes polynomial time) and ask the oracle the answer (which it gives instantaneously). Such oracle computers are unrealistic, so what does imagining them prove? Imagining one oracle did not achieve much, but imagining two let computer scientists discover something new. It is possible to work out the details of two different oracles, called A and B, such that $P^A=NP^A$ is true, but $P^B=NP^B$ is false. This is a depressing result for computer scientists. Computer theorists have some tried and tested methods of showing that two classes of problems are different. But all these methods work independently of the presence of an oracle. This means that if the methods were to show that P=NP is false, then $P^A=NP^A$ would be false for every oracle A. But there is a particular oracle B for which $P^B=NP^B$ is true. Thus none of the traditional methods can ever show that P=NP is false.

Another attempt at the problem uses random oracles. In a random oracle the black box contains a little elf with a coin. When asked any true-or-false question the elf simply flips his coin, answering true if he gets heads, and false if he gets tails—unless he is asked a question he has already answered, in which case he gives the same answer as before. For complicated reasons, considering random oracles turns out to be a way of considering all possible oracles at once. Computer scientists found that, for almost all oracle machines, P and NP were not the same. What they wanted to show was that if something was overwhelmingly likely for a random oracle machine, it must be true for machines without oracles. Unfortunately this turned out to be wrong.

Back to the wiring

At the moment, most of the work on the "P=NP?" problem concentrates on circuits, which is ironic. Computer science developed by abstracting computation away from its material basis in electronics and other hardware in order to consider it mathematically. Now computer scientists are turning back to circuits to answer the questions raised by those mathematical abstractions.

The idea is to consider all the digital circuits that can solve a certain problem. The problem is encoded using 0s and 1s and fed into the inputs of the circuit, which yields the answer (1 or 0). A circuit is made up of simple components called gates. The link between circuits and the "P=NP?" question lies in the number of gates required by a circuit to solve a particular problem. If the circuit for a given problem needs more than a polynomial number of gates, that problem cannot be in P. So computer scientists try to show that, for example, SAT cannot be solved by a circuit with only a polynomial number of gates. If it cannot, P=NP must be false.

One of the leading computer scientists now working on circuits is Dr Michael Sipser at the Massachusetts Institute of Technology (MIT). Dr Sipser and his colleagues concentrate on much easier problems than NP-complete ones. Thet have spent a lot of time on the circuit for a problem called parity, which works out whether there is an odd or an even number of 1s in a string of 0s and 1s. The problem of parity is a straightforward one that is definitely in P, but studying satisfiability without looking at simpler problems first would be just too difficult. One technique is to handicap the circuit in some way. For instance, computer scientists might restrict the type of gate used. If they can sort out the simpler restricted cases, they may be able to apply the principles they learn there to the general case.

Plenty of work on circuits has already been done by scientists in the Sovjet Union, as a group of graduate students at the University of California at Berkely accidentally discovered last year. The students had come up with what they and most others thought was a novel result about the minimum number of gates needed to solve the parity problem. To their chagrin, they learned from a paper in an obscure Soviet journal that it had already been done several years earlier. Dr Alexander Razbarov from the Steklov Institute in Moscow seems to be the leading researcher. Dr Sipser collars the occasional Russian graduate student at MIT to translate for him when the latest paper from Dr Razbarov arrives.

Circuit analysis of this sort is not of interest only to theorists. The makers of semiconductors would like to know just how few gates they can get away with using on their chips.

It it were proved that P=NP is false, computer scientists would know for sure that there are no fast ways of solving problems such as the travelling salesman. Some people would be happy to hear it. For a long time, so-called "unbreakable" codes were designed by making up codes, giving them to mathematicians, and letting the mathematicians chew on them for a while. It they could not break them after concentrated effort, then the code was deemed to be usable. The problem with this approach is that a code might turn out to be crackable after just a teeny bit more effort—say one day after it has been passed as uncrackable. If P and NP are not the same, then there are some problems whose solutions are easy to check but difficult to obtain. Much of modern cryptography—at least the part of it that is publicly known—works on this assumption. Some cryptographers would be quite happy to learn that P=NP is false.

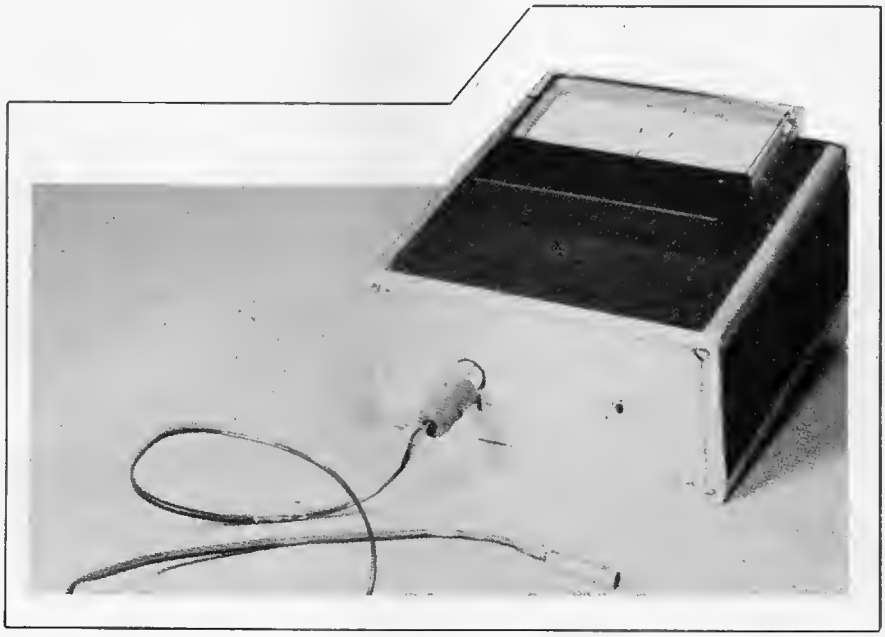
There are still some researchers who believe that P=NP. Many of them are not taken very seriously because they produce endless numbers of flawed papers that purport to show that P=NP. One problem with such papers is their length. Since all the obvious ways of making a fast program from NP-complete problems have been tried, any new attempt is going to be fairly devious. On the other hand, bad proofs purporting to show that NP is different from P are not unknown, either. Dr David Johnson at AT&T's Bell Laboratories in New Jersey has a modest (and almost serious) proposal to stem the tide of bad papers. He proposes that anybody who wants their proof published in a reputable journal should post a $1,000 bond. If the proof turned out to be rubbish, they would forfeit the bond. As an added incentive, forfeited money would go into a pot that would be given to the first verified proof.

If "P=NP?" turned out to have no answer, everybody would lose their money. Before the second world war, a Viennese mathematician, Kurt Gödel, and others proved that some questions in mathematics can never be answered. It is possible that "P=NP?" is one of them. Possible, but inherently unlikely, according to most mathematicians. After all, either there is a program that does subset-sum in polynomial time or there is not. Computer scientists tend to invoke Gödel late at night when they are tired and frustrated.

The smart money is on NP as a separate class, but nobody expects to have an easy time proving it. Dr Cook and Dr Johnson think that the whole field needs an overhaul before the status of NP can be established one way or the other. This is no cause for despair. Computer science is still a young field compared with physics and mathematics. There are ancient unsolved problems in mathematics, such as Fermat's Last Theorem, which get chipped down piece by piece over the years. P=NP has many more implications than Fermat's Last Theorem, an unsolved chestnut about polynomials that has taxed mathematicians for over 300 years. Pure mathematicians are being drawn into the field and computer science problems are being solved by using branches of mathematics, such as geometry, which seemed at first unrelated to computer science.

Everyone concedes that it is difficult to prove even the simplest results in computer science. Even proofs that are easy to understand seem extraordinarily hard to think up, and they may prove unexpected things. This summer Dr Neil Immerman of Yale University settled a question, known as "NL=co-NP?", which is even older though less significant than "P=NP?". A relatively straightforward two-page proof showed that Dr Immerman's answer to the question was yes—the opposite of what most computer scientists expected. Many computer scientists were amazed at how easy the proof was. As one graduate student in computer science put it: "a bunch of complexity theorists are all kicking themselves", which sums up the present atmosphere in a curiously tricky field.

THERMOMETER



When we use a mercury thermometer, the most irritating thing is to find the correct angle at which we must hold it, so that we can see the mercury column properly. Fortunately, this frustration is now over. The good old mercury thermometer is now a thing of the past. The electronic thermometer can convert the temperature to an equivalent voltage which can be directly read on the scale of a meter. Another advantage of the electronic thermometer is the range of temperature which can be read with it. The circuit presented here can read temperatures from -20°C upto about 100°C quite accurately.

Temperature Sensors.

There are many types of temperature sensors which can be used to convert the temperature to a voltage signal; either directly or indirectly.

The simplest type of such sensors is the thermistor - or temperatue dependent resistors. The resistance of a thermister changes with the temperature. This change in resistance can be converted to a change in voltage if we pass a constant current through the thermister and measure the voltage across it.

There are two ways in which a thermister can change its resistance with temperature - either increase with temperature or decrease with increasing temperature. The first type is called PTC-Thermister, the one with a positive temperature coefficient. The other is the NTC-Thermister, the one with a negative temperature coefficient. The thermister is the simplest form of temperature sensor, however, it has a disadvantage of being non linear. The change in resistance is not directly proportional to change in temperature, and due to this, the calibration of the meter scale becomes a complex task.

To avoid this problem, we have used a silicon diode as the temperature sensor in our circuit of the thermometer. An unwanted feature of the diode has been used here to an advantage. We already know that, when a diode is forward biased, the voltage drop across the junction is about 0.7 Volts. When we are using the diode as a diode, we would desire that this 0.7V remains constant, bu in reality it doesn't. It varies with the ambient temperature. This happens due to the temperature sensitivity of the semiconductor materials. Generally the data specified by the manufacturers is valid at an ambient temperature of 25°C. Thus, the forward voltage drop of a diode is also valid at 25°C, and is about 0.7V. With change in ambient temperature this voltage reduces by about 2mV per degree centigrade rise. This change in voltage is constant over a wide range of temperatures. As the change in voltage is linearly proportional to change in temperature, our scale calibration problem would be totally eliminated. This is a great advantage over the NTC or PTC thermisters.

The graphs for NTC, PTC, thermisters are shown in figure 1 a, and the graph of forward voltage drop acrss a diode versus temperature is shown in figure 1 b.

The Circuit

The heart of our thermometer circuit is an IC which contains four Op amps. these four Op amps are shown in the circuit of figure 2 as A1 to A4. They have the following functions to perform A1 produces a reference voltage. Az. functions as a tempeature to voltage converter; A3 works as a differential amplifier and A4 with P3 determines the null point on the measuring scale - which which corresponds to 0°C, or the freezing point.

P1 is used for zero adjustment during calibration and P2 is used for calibrating the full scale reading at 100°C.

This gives just a brief idea of the functioning of the circuit. More details will follow in the course of the further discussion.

The thermometer circuit can be powered from a 9V

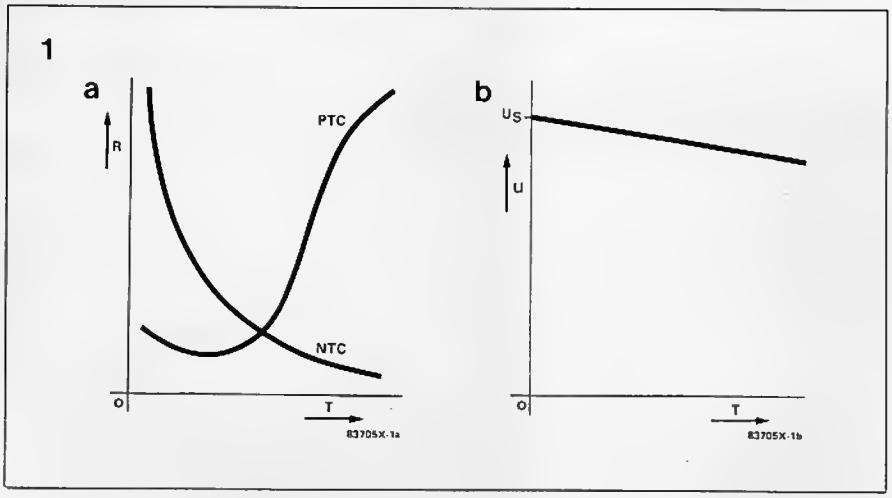


Figure 1:
The thermisters have a disadvantage that they are not linear in nature. The variation in resistance with respect to temperature is shown in figure 1 a.

In contrast to this, the semiconductor materials also exhibit a temperature dependance and have an advantage that the variation with temperature is linear. Figure 1 b shows the variation in threshold voltage of a forward biased silicon diode. With increasing ambient temperature, the voltage falls by 2mV/°C.

Figure 2 :
The thermometer circuit consists mainly of the Op amp IC LM 324, which has four Op amps. The voltage values shown on the diagram are referred to the power supply ground. (Pin 3 of IC1)

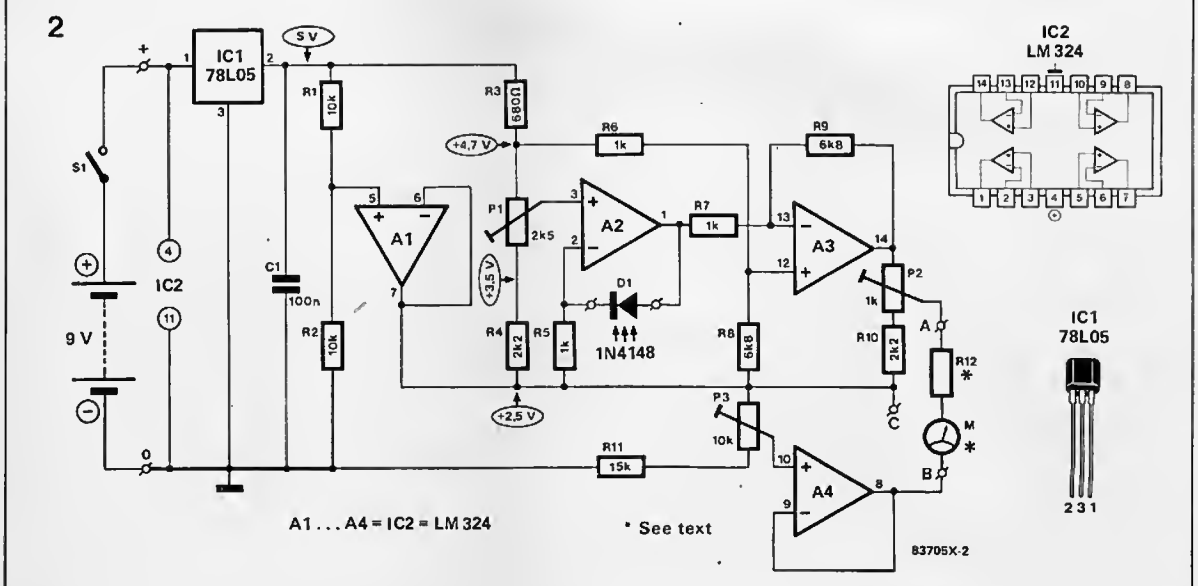
battery if it is not meant for continuous operation. In case of continuous or long duration operation, the circuit must be supplied from the battery eliminator shown in figure 3, with which we are already familliar.

The circuit draws about 5 mA current, and continuous operation on battery will exhaust the batteries too quickly.

Even though the power supply of figure 3 produces an output voltage of 15.5V and the battery gives just 9V, the functioning of the thermometer circuit is not affected because there is a regulator IC (78 LO5) incorporated in the circuit which generates a stable output voltage of 5V at its output terminal. IC1 can accept any voltage between 7V and 20V at its input and generates a constant output voltage level of 5V.

The circuit is some what different from most other circuits we have so far studied in SELEX. The ground line connection is not continuous from the power supply, directly to the output as usual. In this circuit only five components are directly connected to the power supply ground; IC1, IC2 R2, C1 and R11. The resistancs R4, R5, R8, R10 and P3 are all connected with point C, the voltage of which is +2.5V with respect to the powersupply ground.

If we consider the point C



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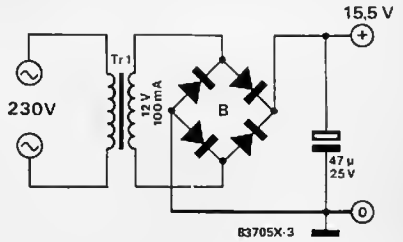

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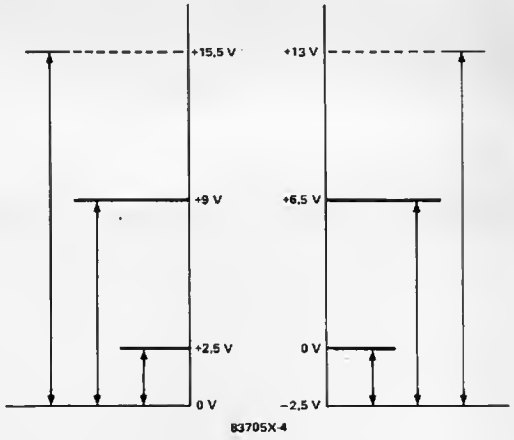

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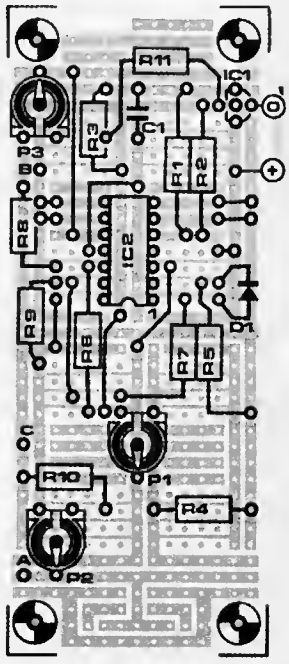


as the ground for this part of the circuit, the power supply + line become a + 2.5V line, and the power supply ground line becomes a - 2.5V line.

This is not the case, however, for IC2 as it is connected directly across the input power supply, which is 9V in case of battery and 15.5 in case of the eliminator. Thus, with respect to C as the ground, the IC2 has a positive supply of either 6.5 or 13, and a negative supply of - -2.5V. This comparison is shown in figure 4. Point C is called the virtual ground of the circuit. The sole purpose of shifting the earthing point to the virtual ground is that the IC2 with four Op amps neds a dual power supply. This also enables us to measure the temperatures below zero, upto -20°C. Op amp A1 is responsible for generating this virtual ground reference, with the help of R1/R2 combination. A1 is connected as a voltage follower. A voltage follower is an amplifier with unity gain. Thus the voltage at pin 7 and pin 5 of A1 must be same. This is a fixed at 2.5 V by the input voltage divider made by R1/R2. The output of 2.5V from A1 is used as the virtual ground reference.

Figure 3:
Battery eliminator circuit for use with the thermometer, if it is to be continuously operated. Operating continuously with batteries would be less sensible.

Figure 4:
The comparison of voltages referred to the power supply ground, as well as the virtual ground. This shows the importance of shifting the ground reference level.

Figure 5:
Component layout of the thermometer circuit on a 40 x 100 mm SELEX PCB only the power supply, meter and the diode are connected externally. The diode is connected with long flexible wires to act as temperature probe.

Component List

R1, R2 = 10KΩ
R3 = 680Ω
R4, R10 = 2.2 KΩ
R5, R6, R7 = 1 KΩ
R8, R9 = 6.8 KΩ
R11 = 15 KΩ
R12 = 8.2 K Ω or 6.8 KΩ

P 1 = 2.5 KΩ Trimpot
P 1 = 1 KΩ Trimpot
P 1 = 10 KΩ Trimpot

C 1 = 100 ηF

D1 = 1N 4148 (Silicon diode)
IC1 = 78L05
IC = 2 LM 324

Other parts :

40 x 100 mm SELEX PCB
14 pin IC socket
100 µA or 100-0-100 µA meter
Power supply/Battery

Casing :
Connecting wires etc.

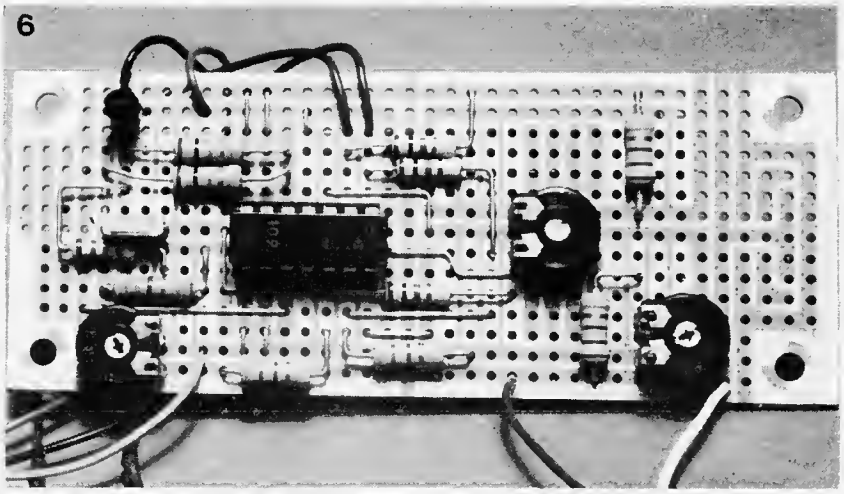


Figure 6 :
The assembled PCB of the thermometer circuit, with two ICs, one diode, one capacitor, three trimpots and a few resistors. It is all that is needed for the thermometer circuit.

Op amp A2 works as temperature to voltage converter. The voltage divider made of R3, P1, R4 decides the input voltage at pin 3 of A2 and is fixed between 3.5V and 4.7V depending on the position of the slider contact of the potentiometer P1. (with reference to the power supply ground). The diode D1 forms the feedback branch of the circuit around A2. This decides the difference between the input voltage on pin 2 and the output voltage on pin 1.

As the voltage input at pin 3 is fixed by the voltage divider, the output of Op amp A2 directly depends on the voltage across diode D1, which in turn depends on the temperature.

The 2mV/°C change in the voltage acrss the diode is very small to drive a moving coil meter and must be amplified. this task is managed by Op amp A3 which operates as an amplifier with a gain of 6.8. The gain is decided by R9 and R7.

The potentiometer P2 is adjusted in such a manner that a voltage change of 2mV on the inverting input (Pin 13) of A3 causes an increase of 10 mV at the output of A3 (Pin 14).

The slider contact of P2 is connected to point A which then feeds the moving coil meter. Point B is connected to the output of Op amp A4, which is more negative than the point C (virtual ground,) itself. This ensures that we can measure temperatures even below the freezing point at 0°C.

A multimeter with a 1V DC or 2V DC range can be used in place of the moving coil meter shown in the circuit. If you can have a separate meter for our thermometer, the best suited one will be a 100μA DC meter or a 100-0-100 μA DC meter. R1 will be 8.2 KΩ for a 100 μA meter and 6.8KΩ for a 100-0-100 uA meter.

Construction

The complete circuit of the thermometer fits onto a 40 x 100 mm SELEX PCB. The component layout is shown in figure 5. The meter and the powder supply, of course, cannot be accomodated on the PCB. The temperature sensor diode D1 will naturally be connected externally with long flexible wires to act as a temperature probe.

As usual the construction begins with soldering all jumper wires, then resistors, trim pots, capacitors and then the ICs. IC1 is a 3 pin device and the pin connections are as shown in figure 2, IC2 should preferably have a socket, Be careful with the Pin 1 marking of the IC2 while inserting it into the IC socket.

The diode is soldered to the flexible connecting wires, with its terminals fully insulated upto the glass body. The diode can be properly insulated using an adhesive which can withstand 100°C.

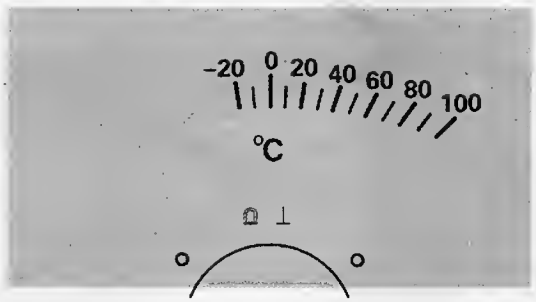
This will be all the more important when measuring liquid temperatures. A photograph of the assembled board is shown in figure 6.

The meter scale will have to be marked with temperature values. This has been shown in figure 7, for a 0-100 uA meter. Figure 8 shows a scale suitable for 1 a 100-0-100 uA meter. If you can obtain a meter which has the dial of this size, the printed scale of figure 7 or 8 can be cut out and directly pasted on the dial.

A 0-100 uA meter will be connected across terminals A and B of the circuit diagram in figure 2. A meter with 100-0-100 uA

7

8



movement must be connected across terminals A and C. In this case, op amp A4 is not used. Also resistor R11 and trim pot P3 is superfluous in this case.

In both the cases, the +ve terminal of the meter must be connected to terminal A of the thermometer circuit.

Calibration

If a 0-100 uA meter is used, all three trimpots P1, P2, P3 are required for calibration. In this case the needle of the instrument has its rest position at the leftmost end of the scale, which corresponds to -20°C. To adjust the 0°C reading, the meter is first connected between B and C. (+ve terminal of meter should be on C.) The trimpot P3 is now adjusted so that the needle comes to 0°C reading. The meter is now connected across terminals A and B, and the temperature probe immersed in the freezing point mixture. The needle may not show 0°C at first, which should be adjusted by trimpot P1 to indicate exactly 0°C. This completes the 0°C calibration. The upper end calibration at 100°C. can be done using boiling water and adjusting the reading to 100°C by trimpot P2. If a good calibrated reference thermometer is available, the upper end calibration can be done at temperatures lower than 100°C also.

In case a meter with 100-0-100 uA movement is used, The calibration is a bit simpler. The meter is connected between A and C. 0°C calibration is done with ice water using trimpot P1 and 100°C calibration is done with boiling water, using trimpot P2. Trimpot P3 is not in the picture at all.

The thermometer can be housed in a small enclosure as shown in the photograph at the begining of this article.

Figure 7:
A suitable scale for the thermometer, when a 0-100 uA meter movement is used.

Figure 8:
A suitable scale for 100-0-100 uA meter movement for the thermometer.

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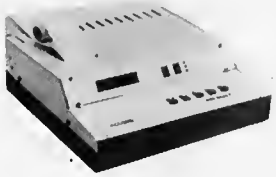

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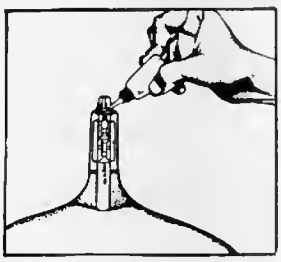

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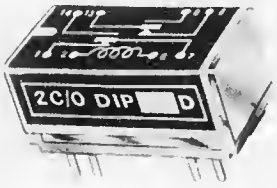

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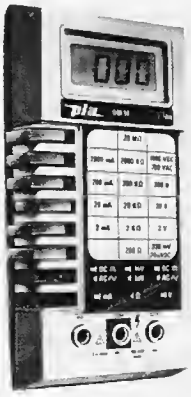

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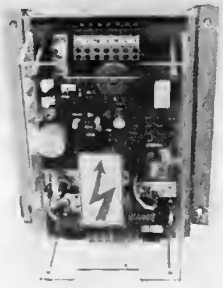

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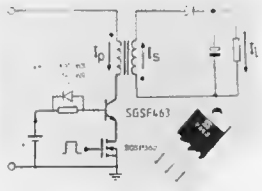

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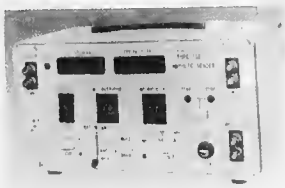

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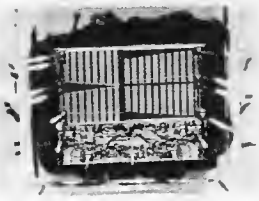

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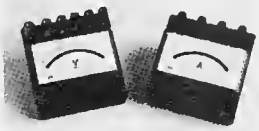

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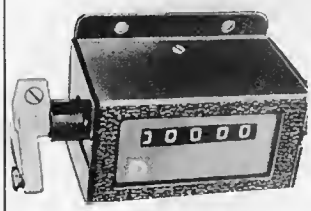

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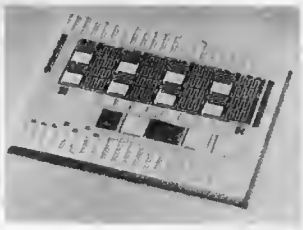

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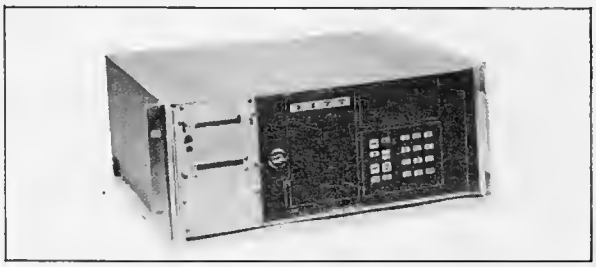

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CORRECTIONS

Stream encryption

October 1987 p. 10-28

Equations [24], [26] and [27] should be amended as follows:

$K'_j =$
$(K_j + 4K_{j+1} + \overline{K}_{j+2} + 3K_{j+2} + K_j) \bmod 2$

$X_j = (AX_{j-1} + B) \bmod M$ [26]

$K_j = X_j \bmod 2$ [27]

The number sequenca and the binary sequence in the section $X^2 \bmod PQ$ generator should be modified to read

$X_j = X^2_{j-1} \bmod N$ and

$K_j = X_j \bmod 2$ respectively.

Active phase-linear cross-over network

October 1987 p. 10.48

The parts list should be modified to read:

$T_1; T_2 =$ BD139.

Digital sine-wave generator

March 1987 p. 3.21

When the unit is fed from a supply voltage lower than ±10 V, as suggested in the article, it is recommended to change R_{10} from 2K2 to 3K9, and R_{11} from 3K9 to 8K2.

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