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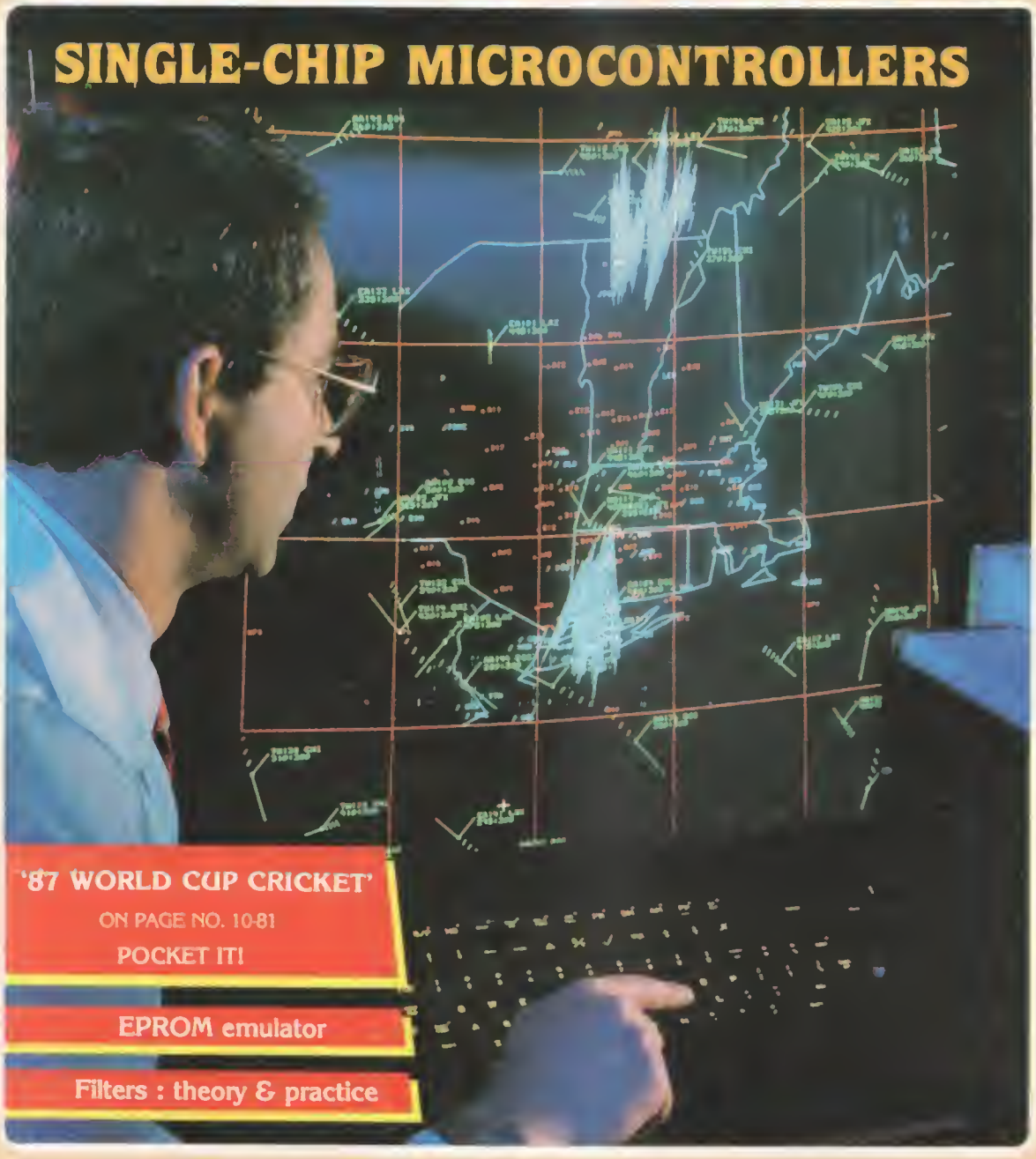

SINGLE-CHIP MICROCONTROLLERS

'87 WORLD CUP CRICKET'

ON PAGE NO. 10-81

POCKET IT!

EPROM emulator

Filters : theory & practice

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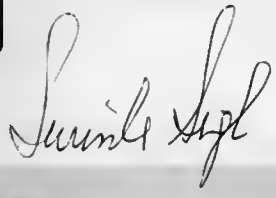

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FIRST COMPUTERIZED BUREAU SYSTEM FOR SATELLITE TRUCK

Texas Television Station WFAA has become the first news station to equip its satellite truck with the Bureau System produced by BASYS' International, a subsidiary of Independent Television News—ITN.

The installation gives WFAA remote newsroom capabilities directly tied to the news production system by linking the station's DalSat electronic news gathering (ENG) truck to the BASYS system at headquarters.
BASYS systems are already used by over 100 radio and television newsrooms worldwide, including Cable News Network, the National Broadcasting Corporation, the American Broadcasting Company, the British Broadcasting Corporation, and ITN, but WFAA is the first to implement the remote newsroom system. (LPS)

NEWSROOM SYSTEM FOR SWISS RADIO INTERNATIONAL

BASYS International has received an order from Swiss Radio International for the supply of a newsroom computer system capable of dealing with the many languages used by SRI.
The system will allow SRI journalists to view the four different languages in which they take copy, write in all the Roman alphabet languages they use, and also print them.
BASYS has also developed a method by which material generated in the main newsroom can be downloaded to separate personal computers, allowing Arabic journalists and translators a bi-character environment.
This means that virtually all SRI's 24-hour-a-day broadcasts in seven major languages (English, French, German, Italian, Portuguese, Spanish, and Arabic) plus either Romansch or Esperanto, can be computerized.
Similar BASYS systems are already being used by YLE in Finland and by the BBC. (LPS)

Hi-fi VCR from Mitsubishi

Mitsubishi Electric Corporation recently put on the market a new hi-fi VCR whose picture quality almost matches that of one-inch professional equipment. The new unit retails at Y218,000 (about $1,450). The company plans to produce 5,000 units per month.

SATELLITE COMMUNICATIONS FOR THE CONSUMER MOVES CLOSER

The International Maritime Satellite Organization (INMARSAT) has issued final specifications for its Standard-C satellite communications system.
INMARSAT is the 48-country international consortium that operates a system of nine satellites worldwide for the provision of maritime and other mobile communications services.
Main features of the Standard-C system are that it uses very small earth stations weighing only a few kilograms to transmit and receive telex, electronics mail or data to or from practically anywhere in the world, regardless of distance or weather and independent of existing communications facilities. The "C" in Standard-C could stand for consumer because, for the first time, it will give the consumer access to the quality and reliability of satellite communications.
Demonstrations of the Standard-C system would begin during the latter part of this year; sea trials would be held in early 1988, and full service should be available through some coast earth stations during the second half of next year. (LPS)

NEW LIFE-SAVING RESCUEPAGERS FOR RNLI

The Royal National Lifeboat Institution—RNLI—the charity which operates rescue services around the British coastline, is to have a tailor-made communications system that will mean faster call-out for its lifeboats.
The Rescuepage system has been devised by British Telecom Mobile Communications (BTMC) and will replace such traditional call-out devices as explosive flares.
The first batch of 1000—out of a total of 2000—specially adapted Radiopagers is already being delivered to lifeboat stations that at present are hampered by poor communications or cumbersome call-out procedures.
The new procedure will enable an entire crew to be called out through a single telephone call which alerts all their BT Tone Radiopagers. (LPS)

EURO CELLULAR RADIO

Now that France and Federal Germany have agreed to the narrow-band standard for a Pan-European cellular radio system set by the Conference of European Posts and Telecommunications earlier this year, the Department of Trade and Industry has given the go-ahead for a £1 million cellular radio project.
The project, involving British Telecom, Racal, GEC, and Plessey, is expected to produce results by the end of the year.
Two operators, Cellnet and Racal-Vodafone, have been allocated space in the prototype spectrum for testing prototype Pan-European radio equipment and systems.
In the wake of all this activity, Plessey and Racal announced the setting up of Orbitel Mobile Communications, owned equally by them, who will develop infrastructure equipment and mobile radiotelephones for the European system.
The new company, whose workforce is expected to reach 300 by the end of the year, will be headed by Mike Pinches, until his appointment technical director of Racal Telecommunications. (LPS)

TELETEXT SPREADS ITS WINGS FURTHER STILL

Logica has won a further contract from the Swiss Teletext Corporation to extend its Pavane teletext editorial system at Biel. Believed to be already the largest system of its kind in the world, Pavane provides a full teletext and subtitling service in French, German and Italian.
This will be the second Logica teletext system for the Swiss Teletext Corporation. The first accepts data from Telekurs, a financial services information provider.
Logica's work on teletext began ten years ago in conjunction with the BBC's CEEFAX service. Since then, Logica has supplied teletext systems to Australia, Austria, Canada, Finland, Germany, Italy, New Zealand, Singapore, Switzerland, and the United States.(LPS)

Life saving communications system

Cut down the time between receiving an alarm call and taking emergency action: that is the requirement of a new alarm centre communication system now under test in Sweden. After only a short period of (test) use, the system has already shown that the time between the alarm call and consequent action can be reduced appreciably.
The system, called Coordcom, integrates and co-ordinates information support and communications handling for alarm centre operators. It has been developed by a subsidiary of Swedish Telecom and will be shown at Telecom '87 in Geneva from 20 to 27 October.

DOUBLE FIRST FOR RACAL AVIONICS

Alaska Airlines of Seattle is the first US air carrier to purchase the Racal Avionics advanced RNS5000 navigation management system. Racal will provide 19 of the systems for Alaska's Boeing 727 fleet at a cost of £750,000.
The contract is a double first for the British company because, for the first time, the RNS5000 will be used with an inertial reference system (IRS) and a head-up guidance system (HGS).
The secret of the RNS5000's high navigational accuracy lies in its ability to process data simultaneously from a number of different navigation sensors, any of which may be selected to "steer by". More accurate airways by flying on precise go-direct guidance lead to an overall reduction in route mileage with a corresponding saving in operating costs.

ESTEC contract for Signal Processors

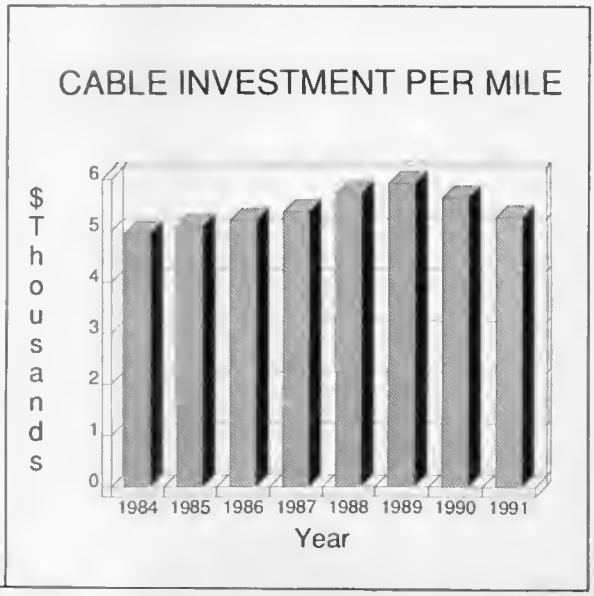
The European Satellite Technology Centre—ESTEC—has awarded a contract to Signal Processors of Cambridge for a study on the application of a novel technique invented by SPL to improve sensitivity of ground receivers used to track satellites.
The work will be carried out in collaboration with the SERC's Rutherford Appleton Laboratory which funded the initial work by SPL to validate the new technical approach. Its first application is likely to be in experiments by the European Space Agency with the Olympus satellite, due for launch in 1989, which will operate at much higher frequencies than are employed in current satellite communications.
SPL's approach avoids the use of phase-locked loop signal recovery methods in the receivers. Instead, it exploits digital signal processing by the use of fast Fourier Transform techniques. This is expected to have the additional benefit of lower manufacturing costs.

BOOST FOR CITY TELECOMMUNICATIONS

British Telecom is to spend a further £40 million on optical fibre links for its business customers in the City of London.
In a major step towards completion of the new system, STC Telecommunications, with Plessey as sub-contractor, has been awarded the contract for the second phase of British Telecom's City Fibre Network (CFN), enabling customers to channel all their services through a single "pipeline".
The first phase of the project, announced last December, is nearing completion. Under this £30 million contract, more than 60,000 km of fibre has already been installed, representing the bulk of the CFN cabling.

CABLE TECHNOLOGY FIGHTING BACK

According to *Cable Hardware & Technology Market in the U.S.* (#1653), a study just published completed by Frost & Sullivan, the VCR has been entirely responsible for the drop in cable operator's revenues from pay services. The report notes that the very effective competition of the VCR has forced operators to increase experiments with pay-as-you-view programming, suggesting major growth areas in addressable home converters and in computer systems for billing, tracking, and servicing customers.
Overall, the study says, capital expenditure by the cable operators should grow about 5% a year through 1990, from the $1.5 billion that was spent on equipment in 1986.
About 6,500 cable systems now serve 40 million subscribers; F&S believes the 71,100 miles of plant construction done in 1986 will stand at 74,500 miles in 1990. However, the proportions of new vs replacement plant construction will shift dramatically: new wiring was 55% of the 1986 mileage put in, but will be little more than a tenth of the 1990 figure.



RIBBON INDUSTRY

Computers and electronic typewriters may have varying market but the market for typewriter ribbons is constantly growing. According to conservative estimates, there were 40,000 computers and 20,000 electronic typewriters in India by the end of 1986 and in 1987, another 25,000 computers and 20,000 electronic typewriters are expected to be added.

Assuming a consumption of two ribbons per installation per month, the annual market for ribbons is estimated at Rs.50 crores and this is likely to grow to Rs.150 crores per annum by 1990.

Different cassette manufacturers have different designs for the same model. The length of the fabric specified by manufacturers is different depending on the design. The internal mechanism also differs from type to type. Different printers produce different impacts and a proper combination of ink and fabric is essential to achieve the same darkness of print. Often the thickness and width of fabric may be same for two different ribbons but the ink formulation in them will be different. This aspect is often ignored by customers.

Most of the computer ribbons currently in use are endless type with a joint in the fabric. The joint should be strong and smooth, as the rough joint will damage the print mechanism. Ultrasonic weld process is widely used all over the world for this joint but results of joints by this process are not satisfactory.

The Japanese have eliminated the joint in some of the new ribbons by using a woven circular loop. In India, Ink-Link India Private Ltd., New Delhi, is said to have developed an indigenous thermochemical technology to make this joint and some foreign ribbon manufacturers have also shown interest in purchasing this technology.

Lack of proper standards for ribbons is affecting the quality. The Indian Standards Institution has not yet evolved any specifications for computer ribbons and consequently, testing of the ribbons is done by users on a subjective basis. The ribbon industry in India needs support from some government institutions in testing and quality control aspects.

As per the import policy of the Government of India, ribbons for electronic typewriters are allowed for stock and sale but the imports for computer ribbons are allowed only for "actual users". Imported ribbons are, however, openly sold.

MARK READERS

Optical Mark Readers, the computerised scanning systems which read information with the aid of light waves are used extensively abroad but they have not yet found place in India, primarily because computer usage in the country is still not high enough. Further, the equipment could meet with resistance as a number of jobs would be lost and the cost might become high. Accurate data analysis, high speed data scanning, automated data input, reduced paper work, low costs and high flexibility are some of the advantages of OMRs. Unlike in the past, OMRs do not require costly mini or mainframe computers as they can be now interfaced with supermicro and microcomputers.

Major real life applications of OMR include test and grading applications, attendance and record keeping, payroll preparations, continuing engineering and commercial data tabulation, inventory management and others. The average scanning speed of an OMR is 13 inches per second.

NON-STOP SYSTEMS

Fault Tolerant Computing, FTC, has become a new branch of computer science which goes by different names like non-stop systems, fail proof computers and zero defect machines. An international workshop on FTC was held in Bangalore recently.

Fault avoidance and fault tolerance are two approaches in FTC. In the first approach, a higher reliability is achieved by prior elimination or reduction of causes of failures. This approach does not completely eliminate the possibilities of failures. Even with the most careful system design and fabrication, faults can still occur. The second approach, on the other hand, accepts the inevitability of failures and counteracts the effect of failure through some form of redundancy.

Fault tolerant systems are also attractive for unattended facilities where nobody is on hand for repairs or restart. One may think of providing redundancy by hooking up two or more computers but in practice, fault tolerant computer design is more complex. The challenge is to meet these requirements in the face of real-life constraints on synchronous operation of redundant systems, cost, throughput, weight, volume, power consumption and the length design cycle.

There is no universal, clear cut solution to the problem of fault tolerance as the decision on the technique to be used, the level at which it is to be adopted and the degree of fault tolerance needed depend on a number of factors like application, price paid and the risk one is willing to take. Aircraft flight control systems, landing systems, rapid transport systems, chemical and continuous process industries, telecommunication, banking and most of the defence applications require FTC.

TANDON ON VIRAAT

Tandon computers have joined the Indian Navy. They are on board the newly acquired aircraft carrier, INS Viraat. The 750 feet long aircraft carrier is equipped with seven Tandon computers. Six PCA20s and PCA70 fileserver, networked together by 500 metre cables running between eight decks, connect the flight control, operations, briefing, aircraft maintenance control, management system and store rooms.

Networking specialist, Next Computer Ltd., Tandon dealer in the UK, was selected by the Indian Navy to supply and install the system. Running under the Novell software, the network will be used to computerised maintenance management, inventory and stock control, personnel, accounting and undisclosed military procedures.

As with most of the military applications, this is a harsh environment for a computer system. It will have to cope with the roll and tilt caused by stormy seas and the vibration of aircraft taking off and landing.

SOFTWARE FACTORY

Following the example of Texas Instruments, a software factory is being set up in India with a satellite link to the business partner in Italy. Modi Rubber Ltd. and the Olivetti of Italy have signed a collaboration deal. Agreements are also in the offing with Logica of UK and

Continental Gummi Werke of West Germany for exports of specialised software.

The software unit will be set up at Modinagar in Uttar Pradesh. An earth station will provide direct communication link to Italy and the UK by satellite. The system will also be used for transmission of software packages to customers abroad. The computer systems will be supplied by olivetti. The unit is expected to begin software export by mid-1988 and the estimated turnover in the next two years is about Rs.10 crores.

The Modi group has already joined hands with Xerox for making the copiers. The group recently tied up with Olivetti for a Rs.28 crore project for manufacturing computers.

LCA COMPUTERS

A separate, high technology corporation may be set up by the government of India to manufacture and supply mission computers needed for Light Combat Aircraft programme, according to Dr. Kota Harinarayana, director of the LCA project.

As a part of the efforts to produce components, subsystems and equipment for the LCA within the country, a mission computer research facility will be set up, first to develop the computers and then to manufacture them. This research facility may cost over Rs.60 crores.

Not more than one-third of the entire LCA budget would be spent on imports. Out of Rs.1000 crore, earmarked for the LCA development programme, already Rs.150 crores had been spent. For the management of the project, 600 work packages have been evolved to handle different aspects. A high-level Indian defence team has concluded negotiations with the United States which has agreed in principle to assist India in the LCA project.

LASER VIDEO

A team of French researchers has developed a new system that helps obtain high resolution images having the quality of 35 mm cinematographic images through a laser video-projector. These images can be directly transmitted for TV broadcasting through satellites, cable networks, or viewed directly on large screens.

The images are of 1,200 lines of 2,000 dots for a 16/9 or 5/3 frame size. The image contrast obtained is more than 40 per cent while in a TV it hardly crosses 10 per cent. At present, the images are monochromatic and there is no technical difficulty in having the transmission in colour.

The Opto-acousto-electronic laboratory of the Universite de Valenciennes and Hainault-Cambresis, run by Prof. Edouard Bridoux have accomplished this, gaining advantage over several foreign laboratories.

This laboratory set up a laser video projector in 1985 using the acousto-optical effect to transfer video information on light beam emitted by a laser.

The importance of video images is that shots can be reviewed immediately after filming to verify their quality.

TV SCENARIO

Eighteen years after the introduction of television in India and five years after the colour TV made its entry, the TV market in the country is still struggling to become fully indigenous. The promise of a colour TV for Rs.5000 is yet to be fulfilled.

The future market for TV is theoretically very big. Against TV transmission coverage of 70 per cent of the population now, the actual coverage is only 15 per cent. To bring the actual coverage to at least 50 per cent of the population we need another 60 million sets, taking an average of five viewers per set.

In 1986, approximately 800,000 colour TV sets were manufactured in the country as against 90,000 in 1982. The most important component of a CTV is the picture tube.

In January, 1987, JCT Electronics Ltd. in technical collaboration with Hitachi of Japan gave the first colour picture tube made in India. Subsequently, Uptron and Samtel, joined the CTV tube production in collaboration with Toshiba and Mitsubishi, respectively.

The colour picture tube constitutes 30 per cent of the overall cost of a TV set and indigenous production could help in saving foreign exchange. The licenses capacity for CTV tubes is 1.5 million pieces per annum.

JCT proposes to introduce non-glare picture tubes and 14-inch colour tubes. Uptron intends to manufacture colour tubes with 22.5 mm mini neck. Samtel colour picture tubes would be flat square tubes which calls for a substantial change in the production technology and demands additional investment. The picture tubes would also be costlier.

The TV industry feels that the government should treat TV as a medium of communication and not a luxury item. As the consumer price of a TV has 50 per cent in the form of levies like excise, sales tax and octroi, the government reduce the taxes on TV.

NEURAL NETS

The main task for scientists engaged Artifical Intelligence has been to find out the nature of the symbols and rules which the human mind uses. The conventional assumption has been that once the mind's symbols and rules are known neuroscientists can then figure out how the brain pnysically produced them. Those who build neural networks now are challenging this assumption. John Hopfield and his colleagues at California Institute of Technology have been building a computing machine that operates on an entirely different principle than the conventional, step by step symbol processing. The new machine would be modelled after the brain, a vast network of neuron-like units that operate on data all at once.

Scientists have succeeded in simulating such "neural nets" on powerful conventional computers. It represents a radical shift in designing computers that think and possibly, it may change our thoughts about the process of thinking.

NETalk is one machine that can learn through algorithms and this 200-unit neural net has learned to read aloud.

Neural nets are still in the experimental stage and many cognitive scientists are sceptical about their potential. Yet many others feel that neural nets will enhance our understanding of how the brain works and help us build better AI systems.

SINGLE-CHIP MICROCONTROLLERS

Single-chip microcontrollers, such as Intel's MCS-51 series described in this article, are currently finding their way in more and more industrial control systems. They offer a remarkably low chip-count as well as ease of programming when the computer is assigned a single task.

For many applications, the use of a dedicated microcontroller has obvious advantages over a standard microprocessor like the 6502 or Z80. This is mainly due to the microcontroller being tailored to perform only the necessary functions. Input/output lines, for instance, are available direct on the chip, obviating the need for a complex set-up with individual I/O chips, interfaces, buffers, and all the necessary hardware for address and data decoding. Often, the microcontroller holds a programmable timer/counter also, and has an extensive instruction set for bit manipulation.

The Types 8051 and 8052 are single-chip microcontrollers from Intel's extensive MCS-51 series. Over the past years, they have found an increasing number of applications in industrial processing systems. This introduction aims at familiarizing you with the 8051, 8052 and 8052AH-BASIC, which are versatile and powerful controllers that enable designing and building compact, microprocessor-based, equipment for a wide range of applications.

MCS-51 Microcontrollers.

Technical features:

- 8-bit CPU optimized for control applications.
- Extensive Boolean processing (single-bit logic).
- 32 bidirectional and individually addressable I/O lines.
- 128 or 256 bytes of on-chip data RAM.
- 2 or 3 16-bit timer/counters.
- Programmable, full duplex UART.
- 5 or 6-source interrupt structure with 2 priority levels.
- On-chip clock oscillator.
- 4 or 8 Kbytes of on-chip program memory (8751 & 8752: EPROM).
- 64 Kbyte program memory address space.
- 64 Kbyte data memory address space.
- 111 instructions (64 single-cycle).
- Decimal and hexadecimal operations.
- 8 Kbyte BASIC interpreter (8052AH-BASIC).
- Built-in EPROM programmer under BASIC control (8052AH-BASIC).
- Special BASIC commands for I/O, counters, and serial interface (8052AH-BASIC).

The MCS-51 family

Intel's MCS-51 family of single-chip microcontrollers consists of the devices listed in Table 1. It should be noted that the type indication 8051 often refers to the the MCS-51 family as a whole. The pinning and functional representation of some of the chips in the MCS-51 family appear in Fig. 1 and Fig. 2 respectively. The 8051 is a controller with 4 Kbytes of on-chip, mask programmable, ROM. The Type 8052AH, a HMOS II chip, is an an enhanced, downward compatible version of the 8051. It is important to note that the 8051, 8051AH and 8052AH are mask-programmable devices. This means they are only available in large quantities since the on-chip program memory can only be loaded by the manufacturer. The 8031, however, differs from the 8051 in not having the on-chip ROM. Instead, it fetches all instructions from external memory, and is, therefore, ideal for writing and testing software for the 8051. Similarly, the 8031AH and 8032AH are the ROM-less versions of the 8051AH and 8052AH, respectively, while the corresponding EPROM versions are identified as Types 8751 and 8752. Software security can be provided by making the EPROM contents inaccessible for external read devices. A separate product, the 8052AH-BASIC, is essentially a 8052AH with a powerful and fast BASIC interpreter programmed in the on-chip ROM. This microcontroller chip is particularly interesting for one-off applications, and will be reverted to in greater detail.

Memory organization

Essentials of the memory structure of chips in the MCS-51 series appear in Fig. 3. In brief, the memory is divided in 2 blocks of 64 Kbytes. One block is the program memory, the other the data memory. The lower 4 or 8 Kbytes of the

1

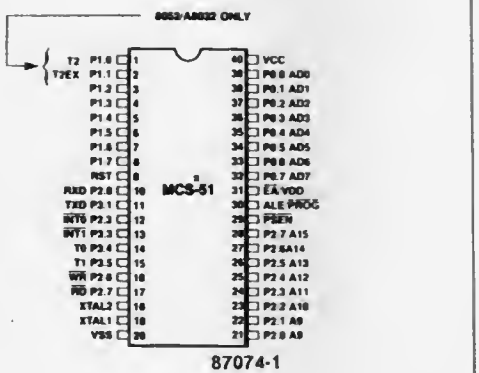


Fig. 1 Pin assignment for the chips in the MCS-51 series.

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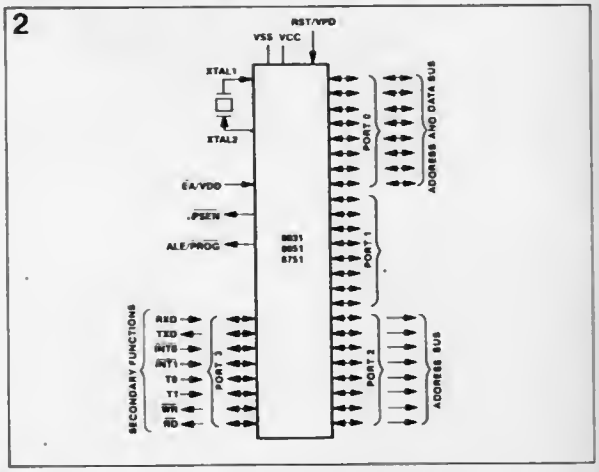

Fig. 2 Showing the port line functions when the controller operates with external memory.

Table 1

Device	Internal Memory: Program	Internal Memory: Data	Timers/ Event Counters	Interrupts
8052AH	8K × 8 ROM	256 × 8 RAM	3 × 16-Bit	8
8051AH	4K × 8 ROM	128 × 8 RAM	2 × 16-Bit	5
8051	4K × 8 ROM	128 × 8 RAM	2 × 16-Bit	5
8032AH	none	256 × 8 RAM	3 × 16-Bit	8
8031AH	none	128 × 8 RAM	2 × 16-Bit	5
8031	none	128 × 8 RAM	2 × 16-Bit	5
8751H	4K × 8 EPROM	128 × 8 RAM	2 × 16-Bit	5
8751H-12	4K × 8 EPROM	128 × 8 RAM	2 × 16-Bit	5

Table 1 The MCS-51 family of microcontrollers.

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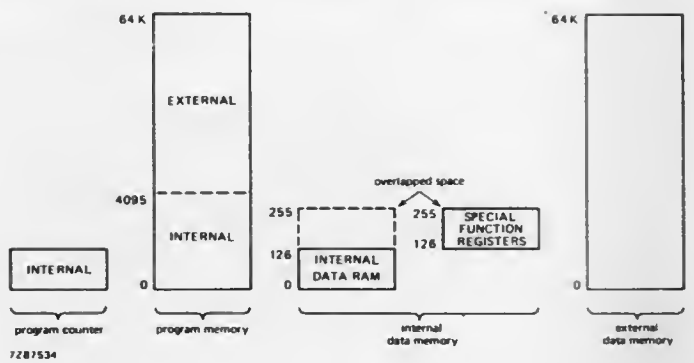

Fig. 3 The MCS-51 memory structure.

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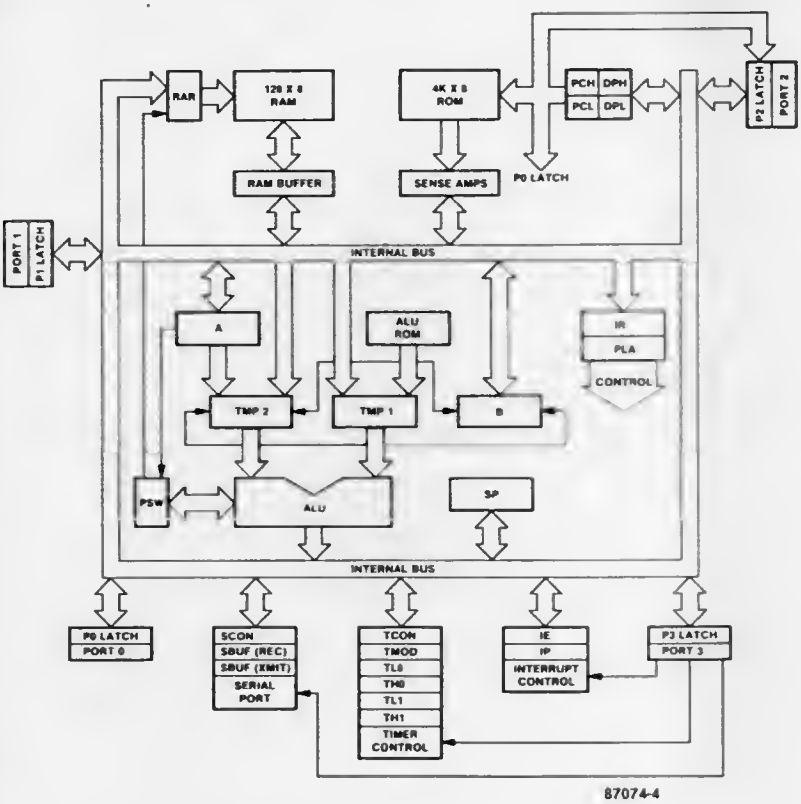

Fig. 4 The MCS-51 architecture.

program memory is on-chip ROM. In the ROM-less controllers, all program memory is external, and may, therefore, be RAM or (EP)ROM. The microcontrollers can only read from the program memory, which holds the sequence of executable processor instructions in the form of machine code. The data memory is used for storing variables, intermediate results of calculations, processed datawords, look-up tables, and the like. Up to 64 Kbytes of external ROM, RAM or EPROM can be addressed in the external data memory space. A number of special register functions are located in a separate 128 or 256 Byte RAM area. The main registers are the accumulator, register B (for multiplication and division), status register, stack pointer, data pointer (2×8 bits or 1×16 bits), port 0...3, the double serial transmit/receive register, the 16-bit timer/counter registers, capture registers for the third counter (8052), and the command registers for special functions (interrupts, RTC, serial I/O).

Most MCS-51 instructions are executed in a single machine cycle, i.e., within 12 clock periods. When the clock frequency is 12 MHz, one machine cycle lasts 1 μs, so that the processing speed of the MCS-51 chip equals that of a 6502 CPU running at 2 MHz, or a Z80 at 8 MHz. A noteworthy aspect of the microcontrollers is their ability to manipulate fewer than 8 bits at a time, relieving the programmer of cumbersome bit-masking routines.

Buses and ports

The basic internal structure of a controller in the MCS-51 family is shown in Fig. 4. It is seen that there are, in theory, 4 bidirectional, 8-bit wide ports. In practice, these are only available when the internal memory (ROM or RAM) is used. In all other cases, ports 0 and 2 function as the data and address bus (refer back to Fig. 2), so that 2 ports remain for I/O applications. Port P2 supplies address signals A15...A8, port P0 address signals A7...A0 and databits D7...D0, multiplexed with the aid of the ALE pulse (adress latch enable). Outputs $\overline{RD}$ and $\overline{WR}$ are simply output lines on port 3, internally pro-

grammed for supplying the pulses for read and write operations in the external data memory. The read strobe for external program memory is the signal $\overline{PSEN}$ (program store enable). It is interesting to note that $\overline{PSEN}$, as well as ALE, is activated twice in every machine cycle during execution of a program in (EP)ROM, because two bytes are fetched successively during each cycle. $\overline{PSEN}$ remains inactive when the machine code is stored in the internal memory, and the external memory (if available) is empty. $\overline{PSEN}$ is not normally used in designs incorporating the 8052AH-BASIC, because the internal ROM holds the BASIC interpreter. Input $\overline{EA}$ (external address) is activated when the processor is to read opcodes from the external memory, rather than from its internal (EP)ROM. The $\overline{EA}$ input is also used for applying the 21 V programming voltage for the internal EPROM (8751, 8752).

Timers and counters

It was already seen in Table 1 that the 8052 has one more 16-bit timer/counter than the 8051. Below is a necessarily concise overview of the functions performed by the timer/counter blocks.

In the timer mode, the register contents are incremented once in every machine cycle. The maximum count rate is therefore $^1/_{12}$th of the processor clock speed. In the counter mode, the register contents are incremented on the trailing edge of the signal applied to input T0, T1, or T2 (the latter is only available on the 8052). The maximum count rate is $^1/_{24}$th of the processor clock speed. Counter/timers 0 and 1 have 4 programmable modes, including 8 or 16 bit operation, and automatic loading of a preset value. Timer/counter 1 can be programmed to function as a baudrate generator for the asynchronous serial interface. Timer/counter 2 (8052 only) has 3 modes: 16-bit automatically reloadable counter, 16-bit capture counter, and baudrate generator.

The serial port

All microcontrollers in the MCS-51 family feature an on-chip, bidirectional serial inter-

Table 2

ARITHMETIC OPERATIONS

Mnemonic		Description	Byte	Cyc
ADD	A,Rn	Add register to Accumulator	1	1
ADD	A,direct	Add direct byte to Accumulator	2	1
ADD	A,@Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A w. Borrow	1	1
SUBB	A,#data	Subtract immed. data from A w. Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal Adjust Accumulator	1	1

LOGICAL OPERATIONS

Mnemonic		Destination	Byte	Cyc
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1

DATA TRANSFER

Mnemonic		Description	Byte	Cyc
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	2

DATA TRANSFER (cont.)

Mnemonic		Description	Byte	Cyc
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order Digit ind. RAM w A	1	1

BOOLEAN VARIABLE MANIPULATION

Mnemonic		Description	Byte	Cyc
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

PROGRAM AND MACHINE CONTROL

Mnemonic		Description	Byte	Cyc
ACALL	addr11	Absolute Subroutine Call	2	2
LCALL	addr16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Absolute Jump	2	2
LJMP	addr16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if No Carry flag	2	2
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit Not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp. immed. to A & Jump if Not Equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. & Jump if Not Equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. & Jump if Not Equal	3	2
DJNZ	Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ	direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn	Working register R0-R7
direct	128 internal RAM locations, any I/O port, control or status register
@Ri	Indirect internal RAM location addressed by register R0 or R1
#data	8-bit constant included in instruction
#data16	16-bit constant included as bytes 2 & 3 of instruction
bit	128 software flags, any I/O pin, control or status bit

Notes on program addressing modes:

addr16	Destination address for LCALL & LJMP may be anywhere within the 64-Kilobyte program memory address space.
addr11	Destination address for ACALL & AJMP will be within the same 2-Kilobyte page of program memory as the first byte of the following instruction
rel	SJMP and all conditional jumps include an 8-bit offset byte. Range is +127 - 128 bytes relative to first byte of the following instruction.

Table 2 The complete instruction set of the 8051/8052 series of microcontrollers from Intel.

face (UART) capable of transmitting and receiving data simultaneously. A special data buffer is provided for the asynchronous receiver to speed up communication with serial peripherals.
The serial port can be programmed to operate in 1 of 4 modes, with software-controlled baudrate and data format. All the usual baudrates up to 19,200 can be selected, as well as clock rates up to 1 MHz for use in networks and multiprocessor communication systems. The clock speed selection is effected with the aid of the timer/counters.

Interrupts and the instruction set

The 8051 and 8052 recognize 5 and 6 interrupt sources, respectively: $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ (programmable for pulse level or pulse edge detection), timer/counters 0 and 1 (and 2 on the 8052), and the serial port. Interrupt programming with 2 priority levels is completely independent of the hardware configuration. Each of the 5 or 6 interrupt sources can be assigned an individual vector (address pointer). Thus, when an interrupt request is received, the processor jumps to the relevant service routine after having saved the contents of the program counter onto the stack. The full instruction set of the controllers in the MCS-51 family is shown in Table 2.

The 8052AH-BASIC

The Type 8052AH-BASIC microcontroller is undoubtedly the most interesting of the MCS-51 family, since it offers an elegant and efficient way of writing control programs for computer-based projects. Intel have loaded the 8 Kbyte ROM in this chip with a powerful BASIC interpreter, while an additional counter/timer, T3, enables split baudrate operation of the serial interface. The BASIC instruction set (version 1.1) is listed in Table 3. On close examination, it is seen that special commands are included for functions otherwise requiring assembly language. After numerous tests and evaluations, it was concluded that the 8052AH-BASIC is eminently suitable for various applications connected with remote data logging, instrumentation and measurement, and industrial process control. The BASIC interpreter is, of course, slow as compared with machine language routines, but has the advantage of being programmable in "normal" language. Also, debugging and editing programs are significantly less difficult, and inexperienced programmers can learn about the processor's capabilities fairly quickly with a minimum of hardware. It is reassuring to know that Intel can supply a 200-page reference manual for 8052AH-BASIC programmers.
Some special features of the 8052AH-BASIC deserve particular attention. The controller can program virtually any type of EPROM if the correct programming voltage is applied to pin $\overline{\text{EA}}$. Both the "old" (50 ms per address) programming standard and several versions of the interactive algorithm are supported—see the last 14 items under **Commands** in Table 3. RAM, ROM and XFER are commands for manipulating and transferring blocks of memory.
The versatily and programming power of the BASIC processor is evident from a number of special **Statements.** BAUD sets the data transfer rate on the previously mentioned additional serial channel. CALL enables calling machine language subroutines from BASIC. CLOCK1 and CLOCK0 control a real-time clock, and CLEARS initializes the data stack, which is primarily used for exchanging machine language parameters, or for storing local variables. Further interesting possibilities are offered by ONTIME, a statement that allows generating an interrupt at a preprogrammed time, ONEXI, for jumping to a subroutine following an $\overline{\text{INT1}}$ interrupt request (interesting because external and timer interrupts can be dealt via BASIC), PH0 and PH1 for printing in hexadecimal format, PUSH and POP for stack manipulation in BASIC, and, finally, PWM for generating a pulse-width modulated signal. The statements also include a number of useful instructions for calling up interpreter routines direct from BASIC: UI1, UI0, UO1 and UO0.
The third column in Table 3, **Operators**, not only lists the well-known arithmetic and logic operations, but also a number of *special function operators*, starting with CBY( ). These operators offer direct control over I/O lines and memory locations. CBY( ) and DBY( ), for instance, give read/write access to the internal program and data memory, respectively. GET allows a character to be read from the serial interface. The remaining special operators, up to and including TIMER2, are intended for reading from and writing to the register indicated by the relevant abbreviation.
Operator XTAL provides the processor with information about the clock frequency used. This is needed to ensure correct operation of the real-time clock.
The status of the memory can be read at all times thanks to operators MTOP, which returns the highest available memory location, LEN, for information on the length of the program, and FREE for the number of available memory locations. Quite remarkably, the 8052AH-BASIC allows BASIC functions to be called up from assembly language. These functions include floating point calculations, complex arithmetic operations, and input-output routines.
The microcontrollers in the MCS-51 series will be at the heart of a number of projects currently under development in the Elektor Electronics design department. Details on availability and programming will be announced in due course.

Th;DM

Table 3

COMMANDS	STATEMENTS	OPERATORS
RUN	BAUD	ADD (+)
CONT	CALL	DIVIDE (/)
LIST	CLEAR	EXPONENTIATION (**)
LIST#	CLEAR(S&I)	MULTIPLY (*)
LIST@	CLOCK(1&0)	SUBTRACT (-)
NEW	DATA	LOGICAL AND (.AND.)
NULL	READ	LOGICAL OR (.OR.)
RAM	RESTORE	LOGICAL X-OR (.XOR.)
ROM	DIM	LOGICAL NOT
XFER	DO-WHILE	ABS( )
PROG	DO-UNTIL	INT( )
PROG1	END	SGN( )
PROG2	FOR-TO-STEP	SQR( )
PROG3	NEXT	RND
PROG4	GOSUB	LOG( )
PROG5	RETURN	EXP( )
PROG6	GOTO	SIN( )
FPROG	ON-GOTO	COS( )
FPROG1	ON-GOSUB	TAN( )
FPROG2	IF-THEN-ELSE	ATN( )
FPROG3	INPUT	=, >, >=, <, <=, <>
FPROG4	LET	ASC( )
FPROG5	ONERR	CHR( )
FPROG6	ONEX1	CBY( )
	ONTIME	DBY( )
	PRINT	XBY( )
	PRINT#	GET
	PRINT@	IE
	PH0	IP
	PH0 #	PORT1
	PH0 @	PCON
	PH1.	RCAP2
	PH1 #	T2CON
	PH1 @	TCON
	PGM	TMOD
	PUSH	TIME
	POP	TIMER0
	PWM	TIMER1
	REM	TIMER2
	RETI	XTAL
	STOP	MTOP
	STRING	LEN
	UI(1&0)	FREE
	U0(1&0)	PI
	LD@	
	ST@	
	IDLE	87074-5
	RROM	

Table 3 The BASIC instruction set of the Type 8052AH-BASIC includes a number of powerful and efficient commands, statements, and operators.

Source: *Embedded Controller Handbook*. Intel Corporation.
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For distributors in the UK see Infocard 512 in this issue.

TESTING THE INSTRUMENTS OF TOMORROW

by Adrian Morant

The increasing use of digital technology, rather than the previous generation of analogue systems, in both satellite and terrestrial communications, has resulted in a demand for widely differing testing techniques. Even though the integrated services digital network (ISDN) may largely still be in the future, planning for the necessary testing must be carried out in parallel with the planning of the networks themselves.

These needs have been exacerbated by the introduction of fibre optics which allows a single fibre, with its diameter measured in micrometres rather than millimetres, to carry far more traffic than a bunch of coaxial cables, each 10 mm in diameter.

In addition, there have been major technical advances in mobile communications. Here, one of the outcomes is cellular radio, which relies for its operation on sophisticated techniques originally developed for radio equipment for military and defence purposes.

Reliability essential

Whereas previously there were separate networks for voice, telex, data and so on, the trend is towards the one ISDN. The fully digital transmission and switching, plus the integration of a wide range of services on to the one digital network, increase the need for great reliability in the networks.

The requirements become even more stringent since, with the increasing use of computer-to-computer communications, users are demanding a larger degree of network availability.

Nowhere is this more apparent than in the City of London, where the financial community has moved with the deregulation known as the "Big Bang", to electronic trading. With individual deals worth £1 million or more—and the value of an entire day's trading running into thousands of millions—loss of telecommunications is not so much a problem as a disaster.

In these circumstances, testing must be carried out wherever possible, both as a form of preventive maintenance, and in the event of failure. In the latter case, it is frequently cost effective to use what may, at first sight, be excessively sophisticated equipment, because it will provide quicker and better results.

Wide range of users

Marconi Instruments Ltd, one of the traditional names in test equipment, recently announced its data communications analyser model 2871 for detailed error performance testing. It consists of a pattern generator and error detector, plus a powerful processing facility, providing an extensive range of measurement options. The menu driven instrument, which uses a cathode ray tube (CRT) display, provides for both out-of-service and non-intrusive in-service monitoring and testing at up to 150 kbit/s data rates.

It is aimed at three main user groups: digital network support staff involved in maintenance, installation or commissioning activities; telecommunications design and development engineers; and production testing and quality assurance (QA) departments. These users operate in public and private communications carriers, energy utilities, military and government networks. They include also telecommunications equipment suppliers.

Continuous monitoring

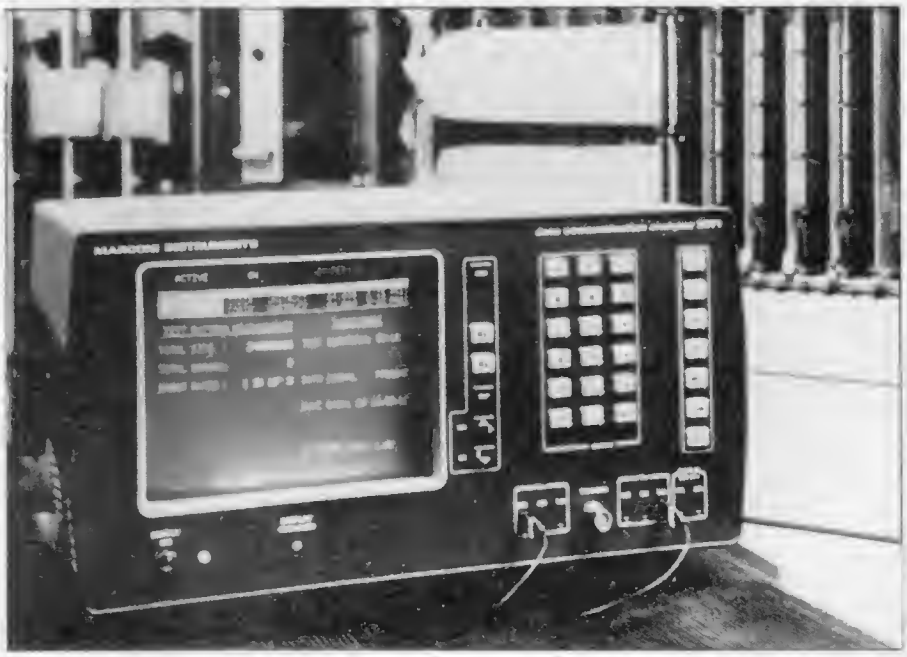
Among the special features of the 2871 is the ability to present test results, not only as bit error ratios, but also as detailed information about the type and time of the error occurrence. This is essential when diagnosing fault conditions in telecommunications networks.

In addition, it is designed to carry out 24 hour unattended error performance monitoring. This is of increasing importance for today's users, whose networks operate around the clock but who find difficulty in recruiting the technical staff to maintain them.

Where the distances spanned by telecommunication cables, either going point-to-point or linking switching centres, are more than just a few kilometres, it is necessary to insert electronic equipment to compensate for losses in the cable. With coaxial cables this is typically every five or 10 km. Today's single mode fibre optic cables allow paths of up to 40 km or even more without regenerators, so that when faults in the cable do occur, it is necessary to locate them with some accuracy.

A precise method

The technique used, based on



The Marconi 2871 data communications analyser.

radar, is known as time domain reflectometry (TDR). It relies on the fact that a portion of a signal pulse sent down the cable—electrical in the case of coaxial cables and consisting of light with fibre optics—is reflected back towards the source when it encounters a discontinuity.
This could be an actual cable fault, such as a break in the cable, or a point where there is a slight kink. While it might not be a problem at the time, it could indicate potential trouble for the future.
Knowing the velocity of propagation, that is, the speed of the signal down the cable, the instrument can be calibrated directly in distance of the fault from the sending end where the instrument is sited. The CRT display, together with calibrated digital controls, allows the operator to learn both the location and type of the discontinuity.
Cossor Electronics Ltd had been manufacturing cable TDRs for a number of years before it introduced units for fibre optical applications. In addition to models for the 850 nm wavelength at which the earlier optical systems operated, the company's range now includes the model OTDR 213S, which has been specifically designed to handle single mode fibres at 1300 nm up to distances of 40 km.

Higher frequencies

In addition, the company is launching a new instrument, the OFL 215, designed to operate at the 1550 nm wavelength, which is increasingly being adopted for telecommunications networks because of the lower attenuation window it offers.
The trend in mobile radio systems is to move to ever higher radio frequencies. Farnell Instruments Ltd has produced a communications test set, model CTS520, designed for service and production testing of simplex or duplex radio transceivers, paging equipment and base or relay stations in frequency bands up to 520 MHz.
It provides the measurement capability of nine separate instruments, plus weighting filters and radio frequency (RF) power load, housed in a readily transportable case. They can be used either independently or together to carry out a comprehensive variety of tests.
The instruments include synthesized RF signal generator, RF counter, modulation meter, RF and audio frequency (AF) power meters, AF voltmeter, distortion analyser, signal interference noise and distortion (SINAD) meter, and a selective calling (CTCSS) tone generator.

Many tests

Only four connections are necessary to the device under test, and measurement are displayed on either light emitting diode or analogue meters. An internal loudspeaker is fitted.
With the test set, it is possible to carry out a wide range of tests that normally require a host of separate instruments. Because of the complexity involved, these frequently need to be carried out by more highly skilled technicians.
Farnell also manufactures test gear covering the frequency bands extending to 1 GHz employed by modern cellular radio networks, such as those operating in Britain.
Racal-Dana Instruments Ltd is another important company on the scene. It is part of the Racal Electronics Group, well known throughout the world for tactical radio equipment, some of which employs frequency hopping. Here, the radios change from one channel to another many times a second in a previously agreed pseudo-random sequence to avoid being jammed and, at the same time, to give a degree of communications security.

Quick response

In the same way, when a cellular phone is moved from one cell to an adjoining one, it has to switch on to a channel associated with its new cell. This has to be carried out in a specified and very short period of time. Consequently, test gear used in conjunction with cellular systems must respond quickly enough to meet these requirements.
The Racal-Dana 9087 signal generator, for example, is capable of implementing over 1,000 complete changes of frequency per second in its fast learn mode. It is a complete instrument, offering excellent purity, a wide range of internal and external modulation facilities, and many output amplitudes.
It is an extremely versatile instrument for use in most areas involving frequency agility. Modern advanced instrumentation often involves automatic testing, so the general purpose interface bus (GPIB) compatibility allows the 9087 to be connected into a complete automatic test equipment (ATE) system.
Similarly, the now well established model 1998 frequency counter is a microprocessor based instrument which measures frequency, time intervals and so on over the frequency range to 1.3 GHz and is consequently an ideal instrument for testing modern communications systems, including cellular radio and satellite systems. Again, being GPIB compatible, it is suitable for ATE applications.

EW PRODUCTS • NEW PRODUCTS • NEW

High-stability subminiature crystals

Manufactured by Japanese crystal specialist Citizen Watch Crystal Company using the AT-cut cleavage technique, the operating frequency of Quantelec's new CSA quartz oscillator crystals drift less than ±30 ppm over 70 ° temperature range.
The new crystals, designated the CSA 309 and CSA 310, are available in frequencies from 3.5 to 3.9 MHz and 4 to 20 MHz respectively. All are designed for operation between −10 and +60 °C with negligible frequency drift between +15 and +40 °C.
CSA crystals are housed in a subminiature hermetic package, 9 mm long and 3 mm in diameter, which imparts excellent shock and humidity resistance. They will survive a 75 cm drop on to a hard surface without degrading the electrical performance or affecting the sealing.
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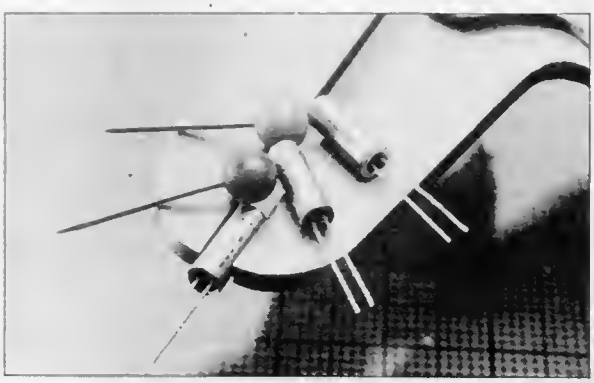


STREAM ENCRYPTION

by B.P. McArdle

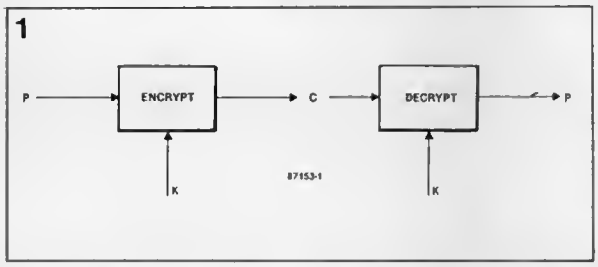
One of the evils peculiar to the computerized world is hacking—the unlawful accessing of computers. One way of effectively combatting this nefarious activity is encrypting the data.

Encryption is the process that turns data into secret form. The original data is known as the plaintext or cleartext and the encrypted data as the ciphertext. If the plaintext is P and the ciphertext is C, the encryption operation is described by

$$\hat{E}_K[P] = C \qquad [1]$$

where K is a parameter called the **key** which is used to vary E. The effect of a change of key is to generate a different C for the same P. The user chooses a particular key from a set of possible keys (K) and encrypts the plaintext. The ciphertext is stored or transmitted over a channel as illustrated in Fig. 1 to a receiver. The receiving operator must know the particular key in use to enable him to recover the plaintext with the inverse or decryption operation

$$\hat{E}_K^{-1}(C) = \hat{D}_K(C) = P \qquad [2]$$



From the point of view of maintaining secrecy, it must be assumed that a cryptanalyst (hacker) would have unlimited ciphertext and would probably know the method of encryption (which means $\hat{E}$), but would not know the particular K. To ensure real secrecy, two main tests to assess cryptosystems have evolved over the years:

(a) the set of possible keys must be large enough to make a search with each key in turn impractical. This is called an **Exhaustive Search** and is based on the fact that only the true key will produce meaningful text;

(b) deduction of the true key from known plaintext-ciphertext pairs should be impossible except by an exhaustive search—this is called a **Known Plaintext Analysis**.

Linear functions

A function f is said to be linear if it satisfies the following two conditions

(1) $f(x+y)=f(x)+f(y)$

(2) $f(ax)=af(x)$

where a is a constant. If these conditions are not met, the function is non-linear. It has been stated that linearity is the friend of the cryptanalyst and the enemy of cryptographers. This statement will become clear later in the article.

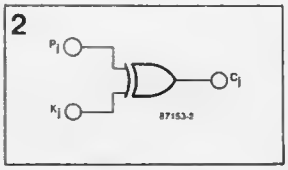
Euler's Totient Function

Euler's Totient Function states that $\Phi(n)$ is the number of integers less than n that are relatively prime to n, that is, have no common factors. For example, $\Phi(31)=30$.

Stream encryption

In electronic terms, the plaintext is a binary sequence that consists of 1s and 0s. The encryption operation is a **Boolean Exclusive—Or Logic Operation**, illustrated in Fig. 2 where a bit of the plaintext P_j and a key bit K_j are combined in an exclusive-or gate to generate C_j. The operation is described mathematically by

$$C_j=(P_j+K_j) \bmod 2 \qquad [3]$$



The reasons for using this operation as opposed to OR or AND are that C is 0 or 1 with equal frequency and that the decryption operation only requires the same operation:

$$P_j=(C_j+K_j) \bmod 2 \qquad [4]$$

The following example for encrypting/decrypting five bits explains the overall procedure

Encryption operation

P_j	: 1 0 1 0 1
K_j	: 0 1 1 0 0
P_j+K_j	: 1 1 2 0 1
$(P_j+K_j) \bmod 2$	: 1 1 0 0 1

Decryption operation

C_j	: 1 1 0 0 1
K_j	: 0 1 1 0 0
C_j+K_j	: 1 2 1 0 1
$(C_j+K_j) \bmod 2$	: 1 0 1 0 1

To summarize, a stream cryptosystem is essentially a deterministic process for generating a key sequence (K_j) which should have approximately equal numbers of 1s and 0s, and have a very long period so as to appear random to an observer.

Linear-feedback shift registers

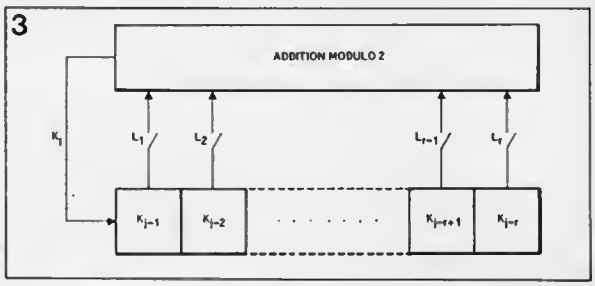
A linear-feedback shift register is illustrated in Fig. 3. Each stage is a JK bistable (flip-flop). The output is taken from the last stage. The feedback function generates successive states from an initial state or **seed** as follows:

$$K_j=f(K_{j-1},K_{j-2},\ldots,K_{j-r}) \quad \text{for } j>r \qquad [5]$$

which for a linear-feedback arrangement may be rewritten as

$$K_j=\sum_{i=1}^{r}(L_iK_{j-i}) \bmod 2 \text{ for } j>r \qquad [6]$$

$L_i=1$ for latch i closed [7]



$L_i = 0$ for latch i open [8]

To ensure that (K_j) has an approximately equal number of 1s and 0s, latch r is usually left closed. If, for example, $r = 5$ with L_3 open and the other latches closed, the linearity of f can be shown by the following results:

$f(1,0,1,0,1) = 0$ [9]

$f(1,1,1,1,0) = 1$ [10]

$f(0,1,0,1,1) = 1$ [11]

The 3rd state on the left can be generated from a modulo 2 addition or an exclusive-OR between the other 2 states. The same result can be obtained on the right-hand side. Thus, the arrangement satisfies the first condition for a linear function. There is no need to consider the second condition, since a is 0 or 1 in modulo 2 arithmetic. Note, however, that the state "all 0s" always generates itself.

In the operation of the shift register, each state has a unique predecessor and successor. The total number of possible states for r stages is 2^r, but the state "all 0s" is never used, which means that the maximum possible period is $2^r - 1$. In the previous example, the key sequence from a seed (1,0,1,0,1) is (1,0,1,0,1,0,0,1,0,0,0,1,0,1,1,1,1,1,0,1, 1,0,0,1,1,1,0,0,0,0,1) and has a period 31, which means that the choice of latches results in maximum period. Obviously, not every arrangement of the latches produces maximum period. There are $\Phi(2^r - 1)/r$ different arrangements, where Φ is Euler's Totient Function. For $r = 5$, this gives $\Phi(2^5 - 1)/5 = 6$.

In encryption applications, the question of secrecy must be examined. If a cryptanalyst knows the value of r and the last 10 bits of the key, he can construct the following sequence of states:

0 — (1,1,1,0,0)

0 — (0,1,1,1,0)

0 — (0,0,1,1,1)

0 — (0,0,0,1,1)

1 — (0,0,0,0,1)

and these 5 equations:

$0 = (L_1 + L_2 + L_3) \bmod 2$ [12]

$0 = (L_2 + L_3 + L_4) \bmod 2$ [13]

$0 = (L_3 + L_4 + L_5) \bmod 2$ [14]

$0 = (L_4 + L_5) \bmod 2$ [15]

$1 = L_5 \bmod 2$ [16]

From Eq. [16], $L_5 = 1$. Therefore, Eq. [15] can be rewritten as

$0 = (L_4 + 1) \bmod 2$ [17]

which gives $L_4 = 1$. Continuing in this manner gives $L_3 = 0$ and $L_1 = L_2 = 1$.

The mathematical problem can also be formulated in matrix form such that the solution requires the calculation of the inverse matrix. This method is more suitable for large values of r, because a cryptanalyst could make use of computer packages. But once the latch arrangement and a state for the shift register are known, the full sequence can be generated. Consequently, the linear function, irrespective of the value of r, is too predictable for secrecy and does not satisfy test 2.

Shift register with non-linear logic

In the shift register with non-linear feedback logic—see Fig. 4—the incoming bit is generated according to

$K_j = f(K_{j-1}, K_{j-2}, \ldots, K_{j-r}) \bmod 2$ [18]

where f is a non-linear function. Normally, f is chosen such that

$K_j = [f'(K_{j-1}, K_{j-2}, \ldots, K_{j-r+1}) + K_{j-r}] \bmod 2$ [19]

which ensures that (K_j) has approximately equal numbers of 1s and 0s.

The new function, f' is also non-linear, which is made clear by the following example. If,

$K_j = (K_{j-1}\overline{K}_{j-4} + \overline{K}_{j-2}\overline{K}_{j-3} + K_{j-5}) \bmod 2$ [20]

then,

$f'(1,0,1,0,1) = 1$ [21]

$f'(0,1,0,1,0) = 0$ [22]

$f'(1,1,1,1,1) = 0$ [23]

An exclusive-OR between the 1st and 2nd states on the left gives the 3rd, but the same operation on the right gives 1 instead of 0, which shows that the feedback function is non-linear. It appears to be more complex than the linear arrangement and the reader would be justified in assuming at first glance that it is also more secure. For a seed (1,0,1,0,1), the key sequence for the first 31 terms is (1,0,1,0,1,1,1,1, 1,0,1,0,1,1,1,1,1,0,1,0,1,0,1,1,1,1,1,0,1,0,1, 1,1). However, the period is short and the sequence repeats more than once. A more detailed examination shows that the **sequence of states** has 6 cycles:

00000-10000-11000-01100-00110-00011-00001

00010-10001-01000-00100

10101-11010-11101-11110-11111-01111-10111-01011

01101-10110-11011

00101-10010-01001-10100-01010

11100-01110-00111-10011-11001

An interesting point is that the state (0,0,0,0,0) does not generate itself. From the point of secrecy, the key sequence actually has period 8 and repeats 3 times within the 31 terms. Thus, non-linear functions are **not necessarily** more secure than the linear variety. But no such cryptosystem, irrespective of the period, offers any real secrecy. If a cryptanalyst knows the feedback function, he can generate the balance of the sequence following r known bits. Consequently, this arrangement also fails test 2.

The arrangement of Fig. 5 attempts to eliminate the two main weaknesses. The linear feedback function generates the incoming bits to the shift register and consequently determines the period of the entire system. The non-linear feed-forward function generates the key bits and protects the shift register from an analysis with known key bits. The two previous examples combined result in

$K_j = (K_{j+4}K_{j+1} + \overline{K}_{j+3}\overline{K}_{j+2} + K_j) \bmod 2$ [24]

$K_{j+5} = (K_{j+4} + K_{j+3} + K_{j+1} + K_j) \bmod 2$ [25]

For the seed (1,0,1,0,1), the key sequence is (1,0,1,0,1,0,1,0,0,0,1,1, 1,0,1,0,0,1,0,1,1,0,0,1,0,0,1,0,0,1,1) and has period 31. The secrecy depends on the cryptanalyst not being able to deduce K_j to

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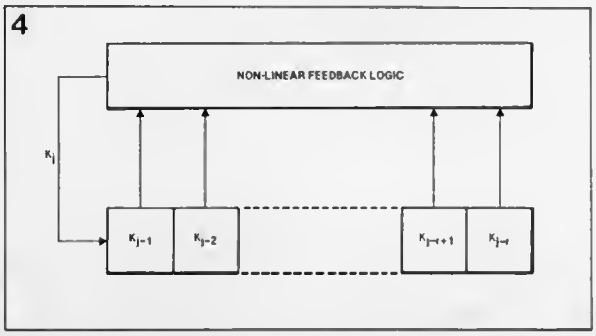

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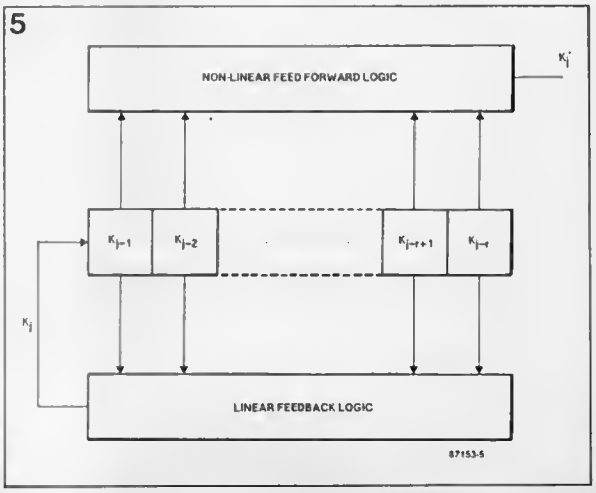

K_{j+4} from K'_j to K'_{j+4} (assuming a worst case analysis where both functions are known). In this simple example, such a deduction is turgid rather than impossible. But an actual commercial system would have $r=128$ or $r=256$. In designing such a system, the feedback logic would be one of $\Phi(2^r-1)/r$ latch arrangements that produce a maximum period of 2^r-1.

The non-linear logic could be chosen with a variety of methods, but the following is simple and straightforward. In Fig. 6, the output or inverted output of each stage (bistable) is connected to an AND gate with the constraints:

(a) each gate has only 2 inputs;

(b) the span of the inputs does not exceed the number of stages.

For example, the pairs 1-4, 2-6, 3-8, and 5-7 satisfy these conditions. The resulting function is not necessarily non-linear in the strict mathematical sense, but for a large value of r, it would be quite complex. A cryptanalyst would have to discover a method of solving equations which have non-linear operations or use an exhaustive search. For $r=256$, this would be impractical. Therefore, this arrangement is reasonably secure. A useful hint for designers is to include a facility to vary the logic arrangements such that the same functions are not used too often.

Congruence generators

The congruence generator method is essentially a computer algorithm for generating a sequence of numbers from a seed X_0 as follows:

number sequence

$$X_j=(AX+B) \bmod M \qquad [26]$$

binary sequence

$$K_j=X_j \bmod M \qquad [27]$$

Thus, K is 0 or 1, depending on whether X is even or odd. The modulus, M, is the largest prime that can be fitted to the processor's word size, while A and B are integral powers of some prime factor. The generated sequences are periodic, because once the seed is reproduced, the complete succession of results after the seed also repeats. For example, $X_0=8191$ $A=13{,}077$; $B=-6925$; $M=32{,}767$ has period 1050. But the simplicity of the operation is also its weakness. Generally, A, B, and M are machine constraints, which means that X_0 is the only parameter that is varied. In addition, some seeds have short periods which in turn limits the choice of seed. In applying test 2, it must be assumed that a cryptanalyst would have all the details except the seed. Thus, the secrecy depends on the difficulty of deducing X_j from K_j. For instance, if $K_j=1$, for a 16-bit word, X_j is an uneven number between 1 and $2^{16}-1$. An examination which would try each possible number in turn in Eq. [26] would **not** be impractical. Consequently, this system implemented on the standard desk-top would not satisfy test 2.

X^2 mod PQ generator

In this method, a sequence of numbers (X_j) is generated from a seed X_0 as follows:

number sequence

$$X_j=X_{j-1} \bmod N$$

binary sequence

$$K_j=K_{j-1} \bmod 2$$

The modulus, N, is the product of two large primes P and Q that are congruent to 3 mod 4 and $gcd(X_0,N)=1$. Therefore, K_j is 0 or 1 depending on whether X_j is even or odd. The set of possible seeds has $\Phi(N)=(P-1)(Q-1)$ elements, where Φ is Euler's Totient Function. The main difficulty here is implementation on desk-top microcomputers which normally handle 12-digit numbers. For secrecy, P and Q must be very large primes in the order of 100 digits. Consequently, the method is considered to be suitable only for Public Key Encryption, which is **not** covered in this article.

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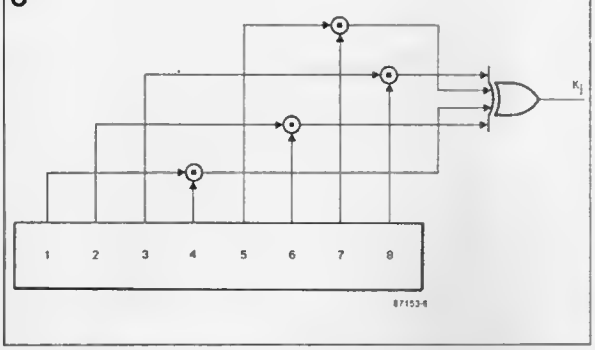

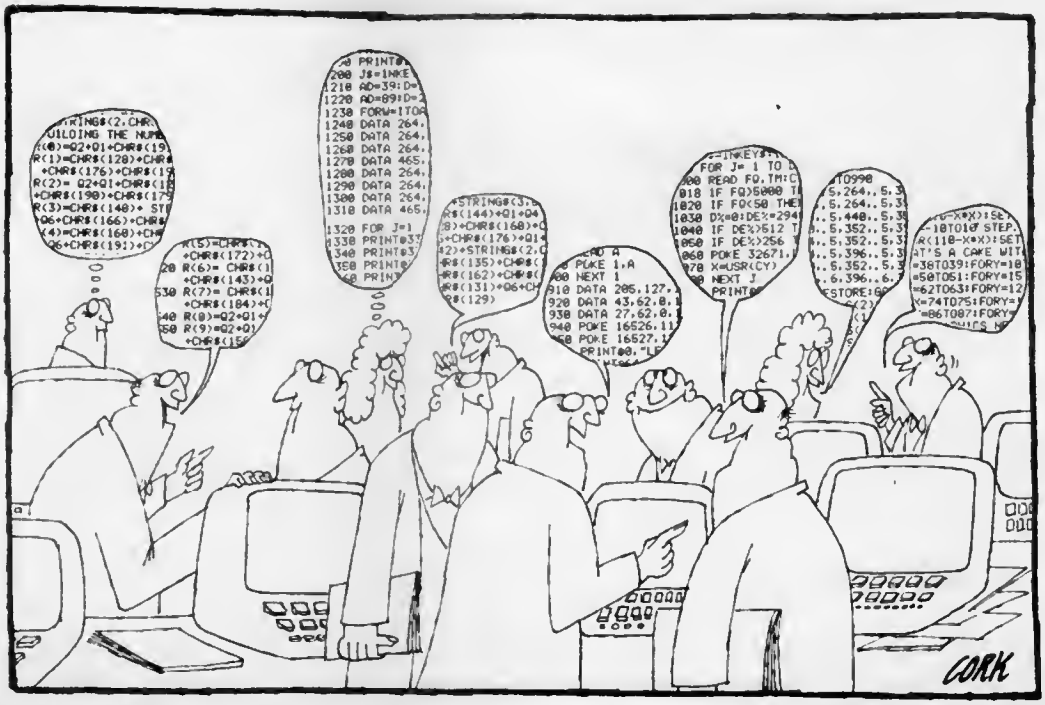

Measurements of ventricular distances by using ultrasonic techniques

by Baki Koyuncu (Physics Department, Kuwait University, Kuwait)

A well known technique was used to determine the external dimensions of the heart on any one of its cross-sectional planes under clinical conditions. The circuit described here used sound radiation in liquid and biological media. Sound was transmitted and received by two PZT-4 transducers placed on opposite sides of the sample heart. The time taken by sound to travel through the medium at a known speed V, was measured electronically. The distance between two transducers was calculated from d = Vxt.

Under clinical conditions, measurements of distances between surface points of a heart are required. This information is coupled with pressure, blood flow, muscle contraction, etc and contributes towards the diagnostic picture of the heart.

Numerous techniques [1,3] with implanted radio-opaque markers have been used to assess global cardiac function both before and after operative procedures. Moreover, attempts have also been made to quantify the dimension changes by means of indirect methods derived from ventricular pressure contours [5-7]. The system developed here employs small oscillating piezoelectric crystals which may be implanted or sutured epicardially. Thus stable, independent alignment of transducers becomes possible and allows precise acquisition of dynamic dimension variations. PZT-4 transducers were placed successfully around the heart to evaluate the ventricular regional function in patients during the experiments.

In this study detailed dimensional changes were quantified. It was confirmed that the system responded predictably to external stimulation as well as alterations in ventricular preload and afterload. Electronic design procedures are presented here together with details of transducer construction. Experiments were carried out on animal hearts for a variety of clinical situations.

Method

The PZT-4 transducers employed during this study were made of barium titanite (Ba Ti O3). They were in rectangular shape with radiating surface dimensions of 10 mm by 10 mm. Two identical transducers were used. One was for transmission (Tx) and the other for reception (Rx) of sound waves. Each was placed in a plastic casing in such a way that half of its height was outside the case. An air cavity was produced between the casing and the transducer by sealing all the edges of the transducer with a silicon based epoxy glue. The whole unit simulated an air backed transducer. Sound radiated from the back radiating surface was reflected back from the air-transducer interface and transmitted from the front radiating surface hence doubling the transmission energy. Copper wire electrodes were attached on both surfaces and transmission voltages were applied across them. A fundamental resonant frequency of 300 kHz was chosen for these transducers. The transducers were implanted externally on opposite sides of the heart. Their weights were small enough to justify assuming that they did not damp the motion of the heart.

A glass tank with dimensions of 1 m x 0.5 m was used for the experiments. The sample was suspended by mechanical clamps in mid air and submerged into the tank. The tank was filled with air and it pro-

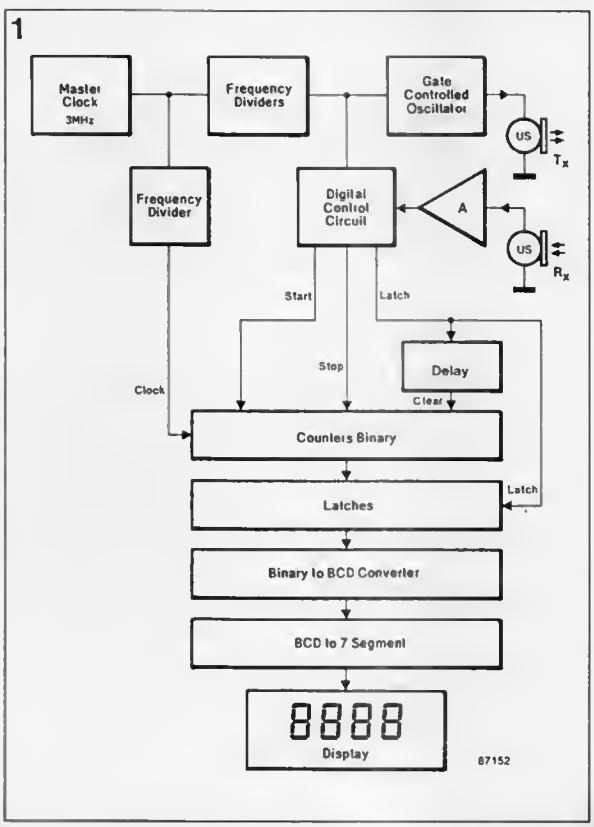

Fig. 1. Block diagram of the complete system.

vided a stable environment free of temperature, air, etc. fluctuations.

A train of pulse bursts was generated from a gate controlled oscillator. Peak voltages corresponding to these pulses were applied across the Tx transducer at its resonant frequency. The tranducer impedance across its terminals was measured at resonance as 30 Ω in air. The transmitted pulses had a duration of 5 μs and a repetition frequency of 1.5 Hz. The amplitude of the applied voltage was 9 V; hence the transmitted signal power level was $(9/\sqrt{2})^2/30 = 0.7$ W. Detection of the transmitted sound radiation was carried out by an identical transducer (Rx). The received pulses were amplified and used to generate START, STOP and LATCH control pulses.

The block diagram of the complete system is presented in Fig. 1. Start pulses indicated the start of the transmission and activated the counters to count the clock pulses corresponding to the unknown distance. Stop pulses were generated when the transmission was received by Rx. They deactivated the above counters counting the clock pulses. Hence the counters contained a particular number of counts representing the distance between Tx and Rx.

A 5 μs duration pulse was produced at every half cycle of 1.5 Hz. These pulses were termed 'latch pulses' and used to reset the counters for the next count sequence. The final count at the counter outputs were also transferred to the latch and display sections of the was also transferred to the latch and display sections of the circuit by means of latch pulses. Timing diagrams of the different pulses are illustrated in Fig. 2.

Circuit description:

Complete circuitry of the system is shown in Fig. 3. A FET collector feedback oscillator with its amplifier was used as master clock. A 3 MHz crystal was used along its feedback path to generate 3 MHz sinewave oscillations. The output was EX-OR gated to convert the oscillations into digital form. These pulses provided the synchronization throughout the system and the control pulses were derived from them. The oscillator frequency was divided by 2×10^6 by decade counters and a JK flip-flop. The frequency divider chain provided a square wave train output with a frequency of 1.5 Hz (corresponding to a period of T=666 μs). An RC combination with a 1.5 V dc offset differentiated the square wave and shifted the resultant above zero volt. A Schmidt trigger gate, N1, produced the latch pulse with 5 μs duration at every half cycle of 1.5 Hz.

The 1.5 Hz square wave was inverted by N2. A Schmidt trigger gate, N3, gave an output pulse with 5 μs duration at the beginning of every 1.5 Hz cycle. Its input was the RC differentiated N2 output. These pulses, termed 'start pulses', were applied to the gate terminal of the Tx oscillator (N4 gate) as trigger pulses. The frequency of the Tx oscillator was set to the resonant frequency of the transducer. The transducer was activated for duration of the start pulse. Hence, a pulse burst of 1.5 cycles at 300 kHz was transmitted with the application of the start pulse. The received pulses at the receiver were time delayed due to the finite distance travelled by the sound. The transmitted pulses also appeared at the receiver due to the electronic interference. The inverted start pulses were applied to multivibrators 1 and 2. The first multivibrator's negative edge trigged the inverted start pulse. Its RC time delay was adjusted to 7 μs. Then the output pulse was used to envelope the unwanted transmitted pulse section of the received pulse train. A 7 μs pulse width set up the limit for minimum distance measurement. It corresponded to approximately $7\times10^{-6}\times1500 = 10.5$ mm distance.

The negative edge of multivibrator 2 triggered the output of multivibrator 1 and produced a digital high. Later, the output was AND-gated by N6 and N7 with the received pulse train. Consequently, the output of N7 contained only the received pulses corresponding to the distance travelled without any interference present. The output of N7 was positive edge triggered by multivibrator 3 and 4 to produce a stop pulse of 5 μs duration. Start, stop and latch pulses were used to control the counters. Initially, a 1.5 MHz signal was applied as the clock signal to the counters. This was derived by dividing the 3 MHz master clock signal by 2. The velocity of sound in the medium was taken as 1500 m/s from the literature. Thus, a conversion factor $\alpha = 1$ mm/cycle was introduced for the counters. This meant that 1 mm distance corresponded to 1 count cycle of the counters. Therefore, the counters would count whole cycles and the numerical display would give straightforward distance measurements in millimeters.

The start pulse was applied to D flip flop (1) as a clock. When D=1, the Q output was set HIGH and the output of N8 copied 1.5 MHz from its input. The output of D flip flop (2) was also set HIGH when a stop pulse was applied as a clock. Therefore, N8 output was transferred to N9 output and applied to counters as clock signal. D flip flops had the inverted latch pulses as their CLR (clear) and PS (preset) inputs. These inputs normally stayed HIGH to let the 1.5 MHz counter clock pulses go through the D flip flops.

When the latch pulses arrived, D flip flop (1) output was reset to LOW. D flip-flop (2) output was preset to receive the next count sequence. The clock pulse train between the start and stop pulses corresponding to a particular distance count were applied to the counter stage. Counters were 4-bit binary counters connected in series to give a maximum count of 2^{11} at its 12 outputs. Delayed latch pulses were applied to the CLR inputs of the counters. A delay of approximately 60 ns was introduced to avoid the counters being cleared at the same instant as the D flip-flops. Otherwise, the count would be lost before it was latched by the latch circuits.

Transparent latches were enabled by the latch pulses. Twelve-bit latch outputs in binary form represented the final number of counts corresponding to the millimetre distance between two transducers. These 12-bit binary numbers were converted to BCD numbers by binary-to-BCD converters and later displayed by 7-segment display units. A variable capacitor C was introduced in series with the master oscillator crystal. It was used to compensate for the frequency changes due to sound velocity irregularities in the medium.

Exact velocity of sound was calculated as 1550 m/s in the experiments. Hence the master clock frequency was adjusted to 3.1 MHz by changing the C value. The new clock frequency for the counters was thus 3.1 MHz÷2 = 1.55 MHz. As a result, the counter conversion factor (α) remained 1550 m/s÷1.55 M cycle/sec = 1 mm/cycle and 1 mm distance would again correspond to 1 count cycle of the counter.

Calibration of the whole system was carried out along the same lines. In the test medium, a precise distance between the Tx and Rx was set by mechanical means. The test medium was

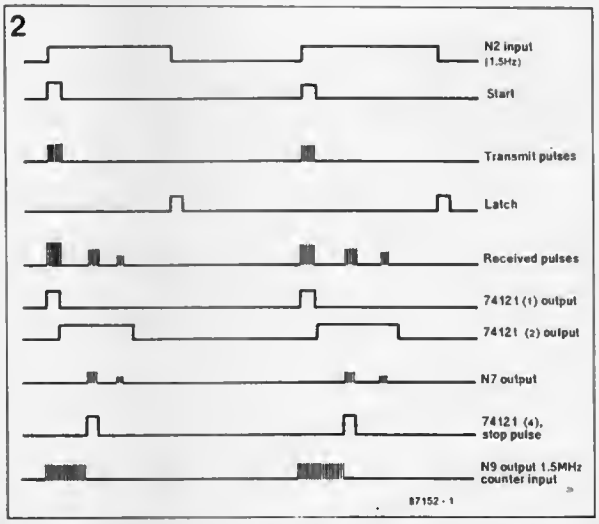

Fig. 2. Timing diagram of different pulses and frequencies present at various points in the circuit.

blood and the distance was set to 30 mm. The display unit readout was adjusted by changing the value of the capacitor in the master oscillator until the display read 30. Similar calibration measurements were made with the stationary heart filled with blood. It was found that the displayed numerical values were consistently the same as the mechanical measurements. Hence, the whole system was ready to measure the dynamic distances in the experiments.

Experimental Considerations

Motion of the heart is a three-dimensional complex motion. The circuit described here would only give the shortest distance along a particular direction between the transducers. The Rx transducer always detected the maximum radiated sound intensity along this direction.

The minimum distance measured was governed by the outputs of multivibrators 1 and 2 and was set to 10.9 mm. Counting was incremented in steps of 1 and the distance was incremented in steps of 1 mm. If the count was more than 0.5 but less than 1, it was approximated to 1 count. If it was less than or equal to 0.5, it was disregarded. Consequently, the maximum uncertainty introduced was 0.5 count corresponding to 500 μm. This error could be reduced by counting more cycles for 1 mm distance. For example, if the 3 MHz master clock frequency was counted, the conversion factor would be 0.5 mm/cycle (2 count cycles per mm) and the above error would be 250 μm. Further increases in frequency would improve the accuracy of the measurement, i.e. 6 MHz would allow a distance step size of 0.125 mm to be measured. This would give an uncertainty of 0.06 mm (if one could position the transducer this accurately!). For clinical purposes distance measurements with $\pm$500 μm uncertainty were sufficient. Hence, no improvement in accuracy was attempted.

The maximum measurable distance corresponded to the time interval between start and latch pulses; and it was equal to $\frac{1}{2} \times 1/1.5 = 0.333$ second. If each count represented the time increment tc = 1/1.5 MHz = 0.66 μs, the maximum number of counts between these pulses would be 0.333 sec/0.66 μs = 5.05×10^5. Hence, a theoretical distance of 505 m

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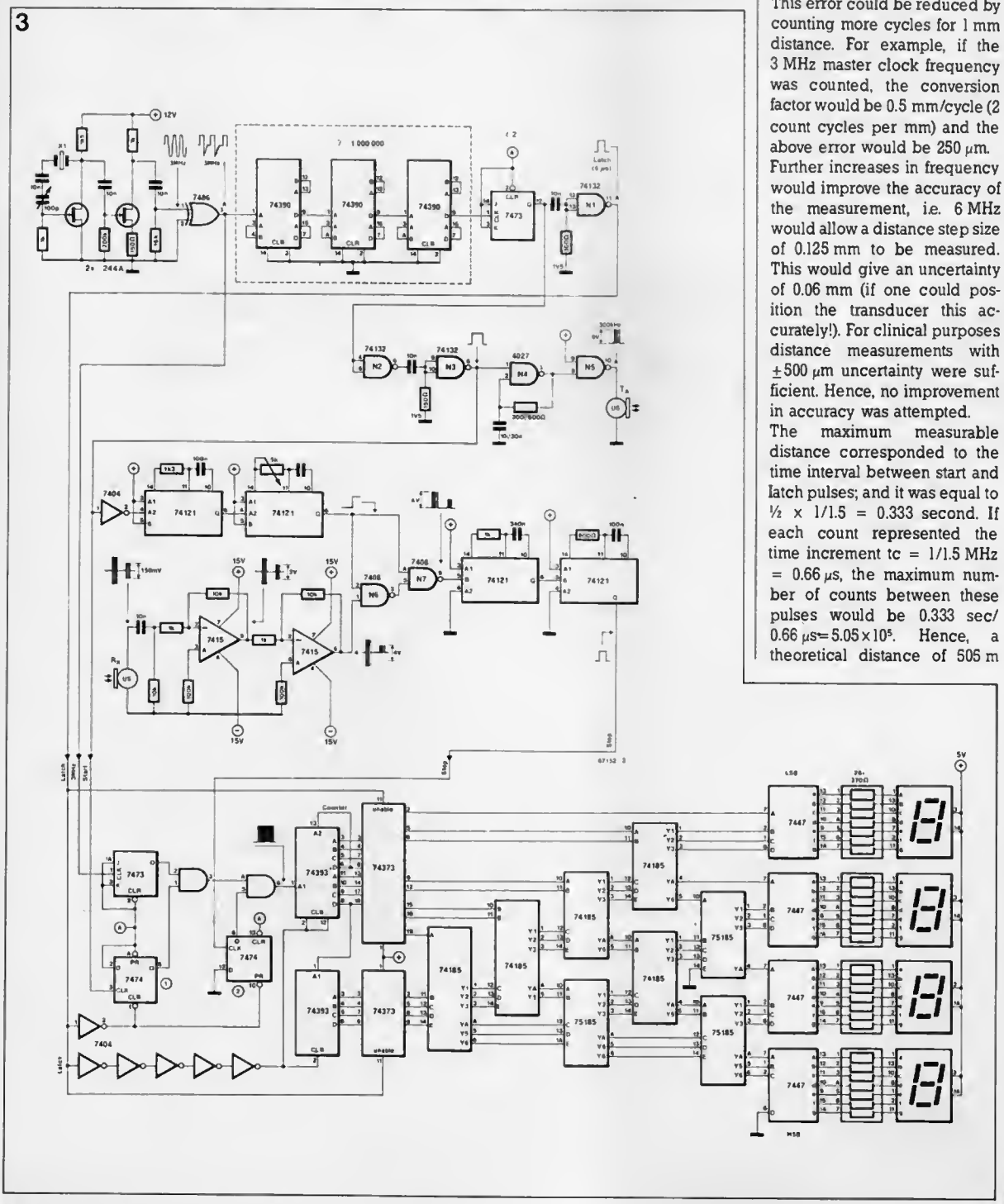

Fig. 3. Circuit diagram of the complete system.

would be displayed by the display units.
The transmitted power levels would set a more stringent limit on large distance measurements. The power received by Rx would decrease rapidly with the increasing distance. Since heart dimensions of 50-150 mm were measured, power considerations were not a limitation on the experiments. The system was in no way comparable to X-Ray tomography, emission tomography or some other advanced ultrasonic devices. These are used for non-invasive clinical applications to man and they are far superior in distance measurements to the system here. The system constructed was solely used in the laboratory to give some notional data of the heart simply and efficiently. It could quite easily be used for any biological sample, once the sound velocity in it was known.
A large signal amplitude was always present at the receiver terminals corresponding to the minimum path through the heart. Other reflections from the side walls were small compared to the main received signal. The circuit did not include automatic gain control in the receiver stage or automatic error compensation (comparing a number of consecutive readings for the same distance) to keep it as simple as possible. Counters were reset by the positive going edge of the delayed latch pulses allowing a new measurement to be taken at every 0.66 seconds.
The previous read-out remained on the display until the information from a new distance measurement arrived. Finally, the accuracy of the measurements was dependent on the factors which influence the speed of sound. The range of the instrument could be extended by increasing the gain of the receiver and the transmitter voltage. This was unnecessary for the measurements described here.

Acknowledgement

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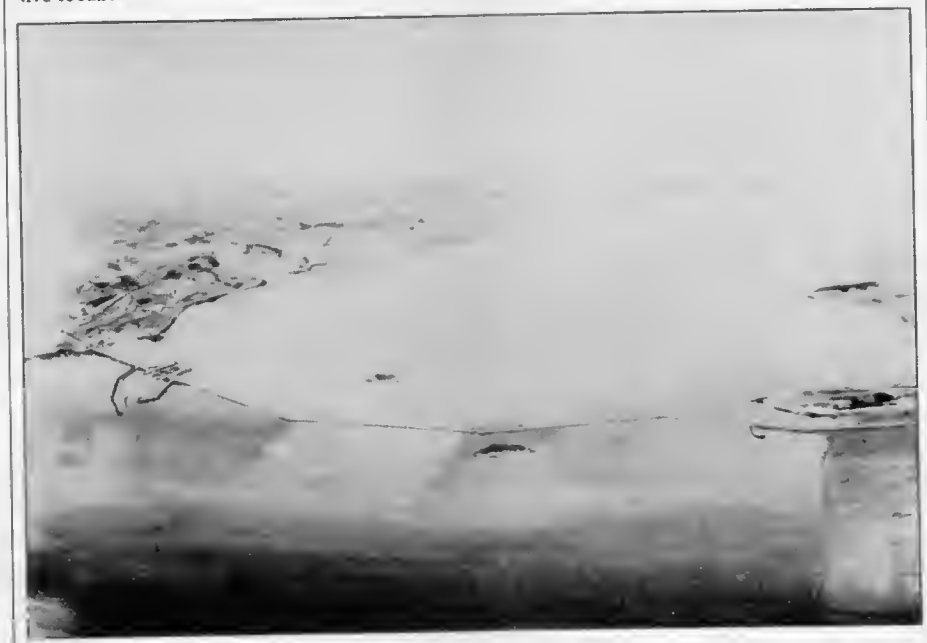
A TIDAL GENERATOR FOR ENERGY AND JOBS

by Vic French

An ambitious plan to produce electricity from a tidal barrage acros the River Severn estuary has been investigated by a special body reporting to the Secretary of State for Energy. The barrage might run from the holiday resort of Weston-super-Mare to Cardiff, though the study also considers an alternative location.

Coincidental with the report—submitted by the Severn Tidal Power Group (STPG)—was a government pledge backing further studies in tidal resources to the value of £5.5 million. This includes a contribution towards research into a River Mersey barrage with generic studies to take in construction techniques and an investigation into the potential of smaller sites around Britain.
The Severn scheme investigation and report were financed jointly by the Department of Energy with the STPG, and a group of companies comprising Sir Robert McAlpine and Sons, Balfour Beatty, GEC Energy Systems, Northern Engineering Industries (NEI), Taylor Woodrow Construction and Wimpey Major Projects (representing Wimpey Atkins Joint Venture).
Among attractions of the scheme are the facts that it would contribute up to 6% of the demand for electricity in England and Wales, would have a life of at least 100 years, and could provide a trunk road across the Severn estuary to link the present and proposed major road networks in south-west England and south Wales, relieving the Severn Bridge.
Its generation costs would be comparable to those of the Sizewell B nuclear power station.



An artist's impression of the Cardiff-Weston barrage looking upriver.

Second option

The study has considered a second option for a barrage adjacent to English Stones, a site some eight kilometres from the Severn Bridge and 36 km upriver from the Weston-Cardiff site. A potential problem there is that fine sediments might affect the barrage, and a major investigative study would be required.
The capital cost of the Cardiff-Weston scheme is estimated at £5,543 million (January 1984 prices). It could provide 45,000 jobs during the construction

period of seven years, with at least another 22,000 jobs outside the energy sector. About 1,700 people would be directly employed to operate the scheme, and there would be considerable benefits in the form of industry, housing and tourism.

The proposed Cardiff-Weston barrage would have a length of 16.3 km, with an installed capacity of 7200 MW from 192 bulb turbine generators in runners of 8.2 m diameter. There would be 48 turbine generator caissons, each 65 m by 72 m in plan, with four turbine generators per caisson and an effective sluice area of 21,600 m². The annual energy output would total 14,4 terawatt hours (TWh), one terawatt hour being a million million kilowatt hours.

Siltation studies by STPG have shown that it will be necessary to use empty caissons to close the barrage on either side of the turbine caissons instead of the more normal embankments. They would be watertight structures open at the bottom and containing air under pressure. There would also be 62 sluice caissons and 50 plain caissons.

PRINCIPAL DETAILS OF THE SCHEMES

	Cardiff-Weston	English Stones
Total length of barrage	16.3 km	7.1 km
Installed capacity	7,200 MW	972 MW
Type of turbine generator	Bulb	Bulb
Number of turbine generators	192	36
Runner diameter	8.2 m	7.5 m
Effective sluice area	21,600 m²	5,976 m²
Number of turbine generator caissons	48	12
Turbine generators per caisson	4	3
Plain caissons in lieu of embankment	50	2
Annual energy sent out (average year)	14.4 TWh	2.8 TWh
Capital cost (January 1984)	£5,543 million	£1,150 million

The advantages

A total volume of structural concrete of 3.1 million m³ would be required. Steel structures have been considered but do not show any cost benefit over concrete. An internal structure of steel might be an advantage but this would need investigation.

Plain caissons used instead of embankments are recommended where the seabed level is even lower than 15 metres below the Ordnance Datum level, as this reduces the total volume of materials required for construction, speeds up the time taken for the work, and improves the closure sequence.

The type of turbine generator has been chosen in view of the long operational experience with this particular design. It could be manufactured with the certain knowledge of its performance and installed as a complete package. The 1600 tonne package would be constructed as a single unit, floated to site on a sea-going barge, and installed in the caisson which could already be in position in the estuary. This would be a considerable advantage, as the plant would be factory tested and partially commissioned, reducing the time and manhours required for installation in the barrage.

The number of turbine generators used in the barrage, of course, controls the "energy capture" of the scheme, but would be restricted by the available depth of channel in which they could be located without the need for expensive dredging.

Variable speed DC generation has been considered in the quest for an improvement in economy, but the gain in energy produced was smaller than expected, and the cost of a high voltage DC system would not be recovered by increased revenue or significant operational benefits. Fixed speed generation and AC transmission have therefore been chosen.

Not a problem

Re-inforcement of the Central Electricity Generating Board (CEGB) transmission system would be required to accommodate the output from the barrage. This would be undertaken by the CEGB and financed from barrage revenue. Intermittent output from the barrage would not pose a major problem as power stations have to contend with much larger power variations in consumer demand.

In order to increase the net value of annual energy put out by an ebb generation barrage, the STPG considers that there would be a net benefit in pumping into the basin at neap and mean tides.

There is a proposal for a smaller schema with a barrage to be built some eight kilometres downstream of the Severn Bridge. This too could carry a trunk road across the Severn estuary to link Wales with southwest England. The cost of this English Stones scheme would be £1,150 million (January 1984 prices).

Bulb turbine generators would also be used for this scheme, with 36 installed in 12 caissons, each 63 m by 50 m in plan. The diameter of the turbines would be 7.5 m each with a rating of 27 MW and a total installed capacity of 972 MW. There would be 42 sluices in all, of which 30 would be 12 m × 11 m and 12 would be 12 m × 14 m. Ebb generation with flood pumping would be used again here, giving a firm power contribution of 250 MW and an average annual energy output of 2.8 TWh.

Needs of shipping

Barrage construction would be very similar to that at Cardiff-Weston although embankments would complete the barrage on each side of the turbines and sluices.

In both cases consideration would have to be given to the requirements of shipping. It is suggested that two alternative lock sizes should be constructed, one for vessels up to 6,000 dead-weight tonnes and one for larger ones of up to 25,000 dwt. The locks would be situated between sluice caissons on the Welsh side. This takes into consideration the prevailing wind and current conditions expected when the scheme is complete.

The STPG considers that the larger scheme between Weston and Cardiff would be a great asset to the United Kingdom, with its potential for creating employment and the fact that it would produce virtually free energy as an insurance against unpredictable increases in primary energy costs. Tidal power is also non-polluting to the environment.

FILTERS: THEORY & PRACTICE — 2

by A.B. Bradshaw

Fundamental sections from which more complex ones are built are called **prototype filters**. The majority of filters used are **high-pass**, **low-pass**, **band-pass**, or **band-stop**. All of these are usually made up of low-loss reactances connected in **T**, π, or **L** form as shown in Fig. 1. Practical filters are normally designed as a combination of these configurations. In the following, the **reactance**, i.e., the imaginary part of a complex impedance, is designated by X, which is equal to $1/\omega C$ or ωL or a combination of these.

Low-pass filters

In a correctly terminated low-pass T filter, see Fig. 15:

$$Z_{0T} = \sqrt{Z_1 Z_2 + Z_1^2/4} = \sqrt{jX_1\, jX_2 - X_1^2/4}$$

which can also be expressed as

$$Z_{0T} = j\sqrt{X_1 (X_1/4 + X_2)} \qquad [20]$$

If X_1 and $(X_1/4+X_2)$ are of **opposite** sign, Z_{0T} is resistive and the filter draws power: it is operating in its **pass-band**—see Fig. 17.

If X_1 and $(X_1/4+X_2)$ are of the **same** sign, Z_{0T} is reactive and the filter reflects power: it is operating in its **stop-band**—see Fig. 17.

In a low-pass π filter—see Fig. 16, Z_{0T} and $Z_{0\pi}$ are related by

$$Z_{0\pi} = \frac{Z_1 Z_2}{Z_{0T}} = \frac{jX_1X_2}{j\sqrt{X_1(X_1/4+X_2)}}$$

$$= \frac{j^2 X_1 X_2}{Z_{0T}} = \frac{-X_1X_2}{Z_{0T}} \qquad [21]$$

Since X_1 and X_2 are of opposite sign, their product is a constant, so that

$$Z_{0\pi} = \frac{\text{CONSTANT}}{Z_{0T}} \qquad [22]$$

in which Z_{0T} varies as in the previous example—see Fig. 17. The value of f_c may be determined from an inspection of the characteristics in Fig. 17, but can also be evaluated from Eq. [19]:

$$\cosh\gamma = 1 + \frac{Z_1}{2Z_2}$$

For the T section,

$$\cosh\gamma = 1 - \frac{\omega^2 LC}{2}$$

but since $\gamma = \alpha + j\beta$,

$$\cosh(\alpha + j\beta) = \cosh\alpha\cosh j\beta + \sinh\alpha\sinh j\beta \qquad [23]$$

Since, $\cosh j\beta = \cos\beta$
and $\sinh j\beta = j\sin\beta$
Eq. [23] becomes

$$\cosh\alpha\cos\beta + j\sinh\alpha\sin\beta = 1 - \frac{\omega^2 LC}{2} \qquad [24]$$

Since the right-hand term in [24] does not contain an imaginary part, the expression can be split into

$$\cosh\alpha\cos\beta = 1 - \frac{\omega^2 LC}{2} \text{ (real part)}$$

and

$$\sinh\alpha\sin\beta = 0 \text{ (imaginary part)}$$

Considering the real part, in the pass-band the attenuation is zero, so that $\alpha = 0$, and

$$\cos\beta = 1 - \frac{\omega^2 LC}{2} \qquad [25]$$

Inserting the two maximum values of a cosine curve, i.e., ± 1, in this expression yields

$$+1 = 1 - \frac{\omega^2 LC}{2}$$

and

$$-1 = 1 - \frac{\omega^2 LC}{2}$$

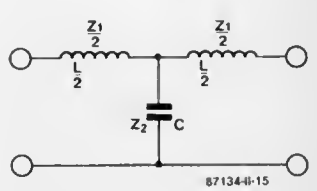
From these, the two cut-off frequencies can be determined:

$$f_1 = 0 \text{ Hz} \qquad [26a]$$

and

$$f_c = \frac{1}{\pi\sqrt{LC}} \qquad [26b]$$

15



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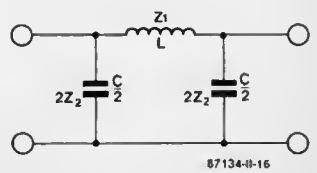

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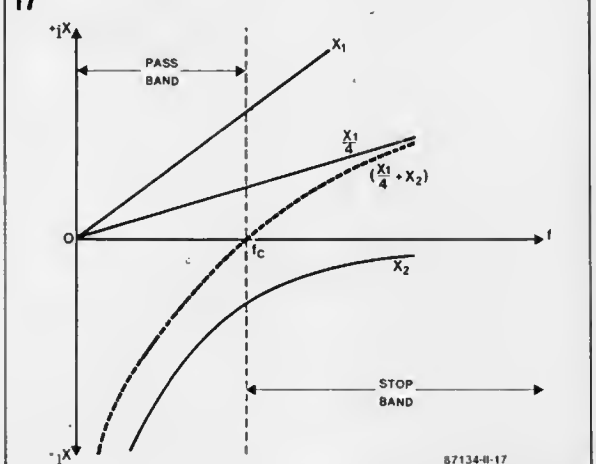


The phase angle, β, can be found by inserting the value of f_c [26b] into [25] to give

$$\cos\beta = 1 - 2(f/f_c)^2$$

so that

$$\beta = \cos^{-1}[1 - 2(f/f_c)^2] \text{ radians} \quad [27]$$

Expression [27] is shown diagrammatically in Fig. 18.
In the stop band $\beta = \pi$, so that $\cos\beta = -1$. Inserting this in [24a] gives

$$\cosh\alpha = \frac{\omega^2 LC}{2} - 1$$

so that

$$\alpha = \cosh^{-1}[2(f/f_c)^2 - 1] \text{ nepers} \quad [28]$$

where α is the attenuation in the stop band. This expression is shown graphically in Fig. 19.
In a low-pass T filter, $Z_1 = j\omega L$ and $Z_2 = 1/j\omega C$, so that $Z_1 Z_2 = L/C$. Inserting this in Eq. [5] gives

$$Z_{0T} = \sqrt{\frac{L}{C} - \frac{\omega^2 L^2}{4}} \quad [29]$$

When $f = 0$,

$$Z_{0T} = \sqrt{L/C}$$

When $f = f_c$,

$$Z_{0T} = \sqrt{\frac{L}{C} - \frac{L}{C}} = 0$$

Therefore, over the pass-band from $f = 0$ to $f = f_c$, Z_{0T} moves from $\sqrt{L/C}$ to zero ohms.
Since the π network is related to the T type, it may be concluded that

$$Z_{0\pi} = \frac{Z_1 Z_2}{Z_{0T}} = \frac{L/C}{\sqrt{L/C - \omega^2 L^2/4}} \quad [30]$$

When $f = 0$,

$$Z_{0\pi} = \sqrt{L/C}$$

When $f = f_c$,

$$Z_{0\pi} = \frac{L/C}{\sqrt{L/C - L/C}} = \infty$$

The variations of Z_{0T} and $Z_{0\pi}$ are shown in Fig. 20.

The basic design equations can be obtained from the foregoing discussions, but are summarized here for convenience's sake: they apply to T and π sections alike.

$$Z_0 = R_0 = \sqrt{L/C}$$

$$f_c = 1/\sqrt{LC}$$

$$L = C R_0^2$$

$$C = 1/\pi R_0 f_c$$

High-pass filters

In similar vein as the considerations on the low-pass filters, the reactances and impedances in a high-pass T filter as shown in Fig. 21 are

$$X_1 = 1/\omega C \text{ or } Z_1 = 1/j\omega C$$

and

$$X_2 = \omega L \text{ or } Z_2 = j\omega L$$

so that

$$X_1/4 + X_2 = \omega L - 1/4\omega C$$

A graphical representation of these reactances is shown in Fig. 22.
Substituting the impedance values given above into Eq. [19] yields

$$\cosh\gamma = 1 - \frac{1}{2\omega^2 LC}$$

By a similar consideration as before,

$$\cosh\alpha\cos\beta = 1 - \frac{1}{2\omega^2 LC}$$

In the pass-band, $\alpha = 0$, so that $\cosh\alpha = 1$, and

$$\cos\beta = 1 - \frac{1}{2\omega^2 LC} \quad [31]$$

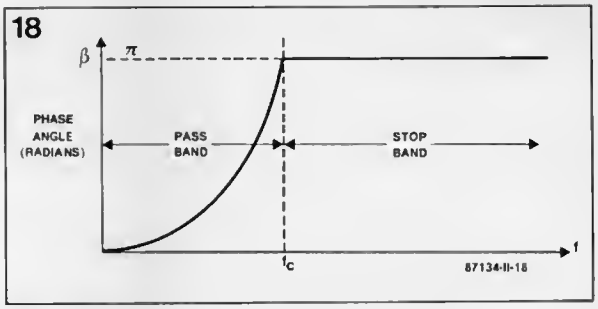
Substituting the limits of ± 1 for $\cos\beta$ in [31] gives

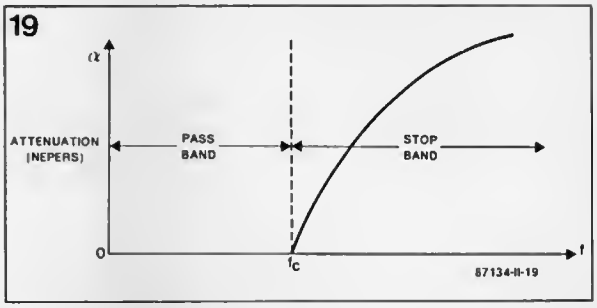
$$+1 = 1 - \frac{1}{2\omega^2 LC}$$

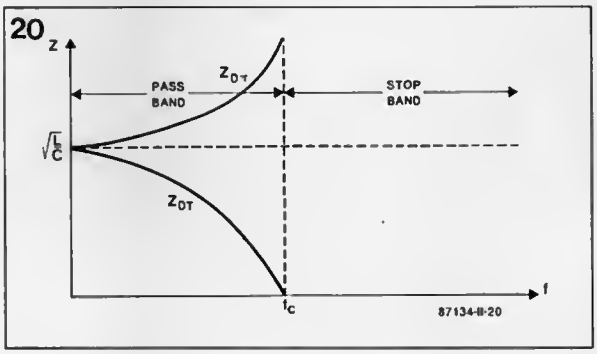
and

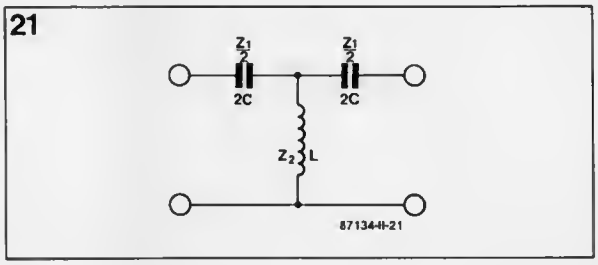
$$-1 = 1 - \frac{1}{2\omega^2 LC}$$

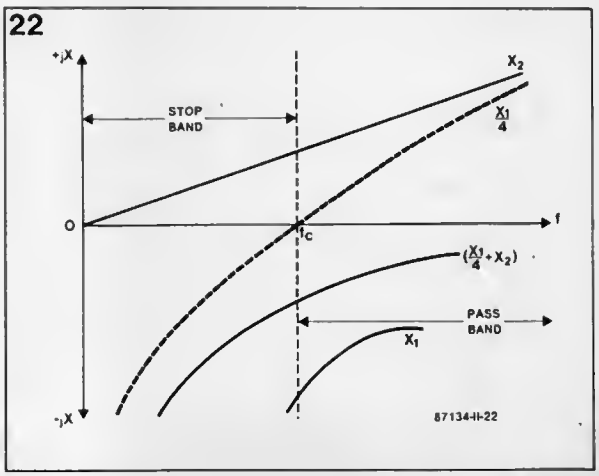
From these values the cut-off frequencies can be deter-

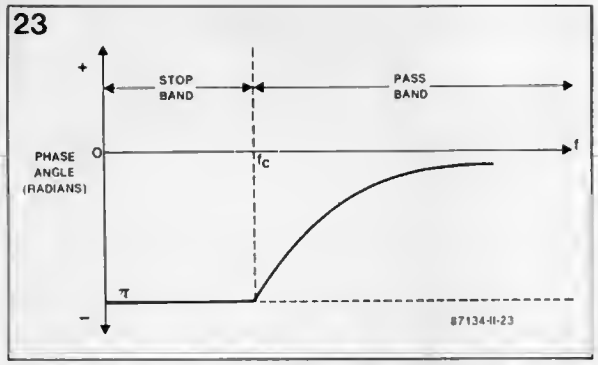


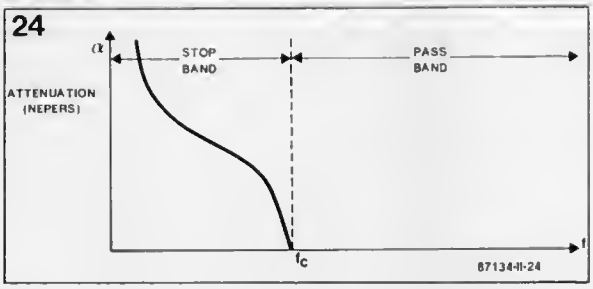


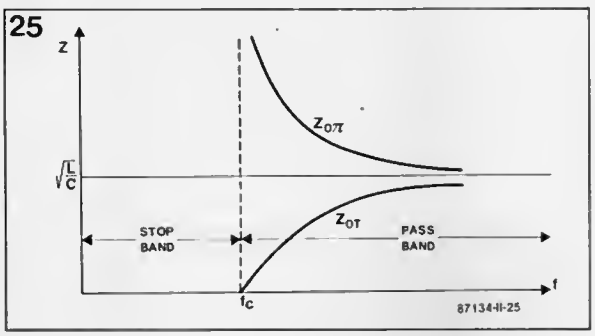


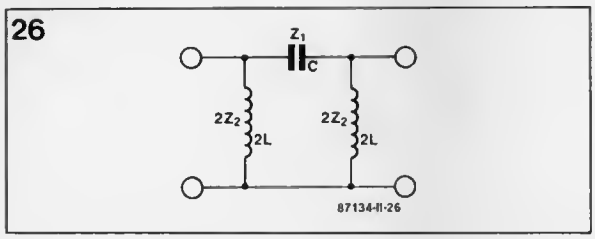


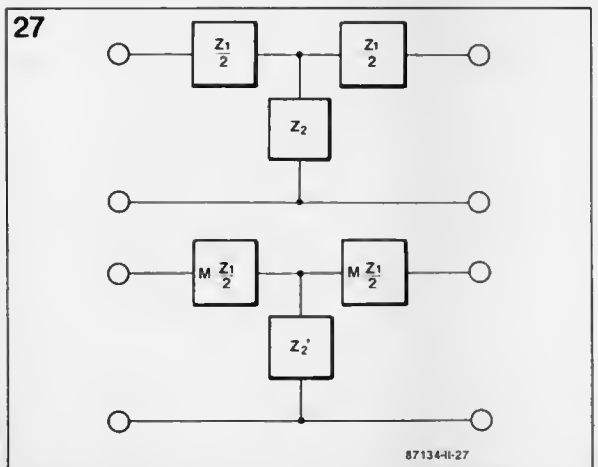


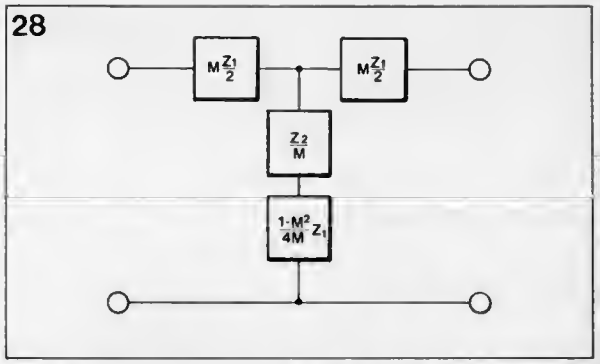












mined:

$$f_c = \frac{1}{4\pi\sqrt{LC}} \quad [32a]$$

and

$$f_1 = \infty \quad [32b]$$

The phase angle, β, is given by

$$\beta = \cos^{-1}[1 - 2(f/f_c^2] \text{ radians} \quad [33]$$

The phase angle characteristic is shown in Fig.23, from which it is seen that $\beta = -\pi$ over the stop band and reduces to zero in the pass band.
Similarly,

$$\alpha = \cosh^{-1}[2(f_c/f)^2 - 1] \text{ nepers} \quad [34]$$

The attenuation characteristic is given in Fig. 24.
The impedance variation in a high-pass T filter is calculated with Eq. [5]:
when $f = \infty$,

$$Z_{0T} = \sqrt{L/C} \quad [35a]$$

and when $f = f_c$,

$$Z_{0T} = 0 \quad [35b]$$

The impedance characteristic is shown in Fig. 25.
The component values can be calculated with the aid of Eq. 32 and Eq. 35.
Eq. [19] applies to the high-pass π filter shown in Fig. 26: the phase angle and attenuation characteristics of this type of filter are the same as those of a T type and are determined by applying the procedures outlined before.
The filters discussed so far are often referred to as "constant-k" types because $Z_1Z_2 = L/C$, which is independent of ω. Although constant-k sections are useful for simple filtering requirements, they have two serious shortcomings:

(a) Z_0 varies over the pass band which can cause mismatch; and

(b) α rises only slowly outside the pass band.

Typical figures in a low-pass constant-k section are a 10 dB increase in attenuation at 1.2 f_c and $Z_0 = 2.3R_0$ at $f = 0.9f_c$. Clearly, what is needed is a constant Z_0 in the pass band and a far more rapid rise in attenuation outside the pass band. These requirements are approached in M-derived filters.

M-derived filters

Figure 27 shows two low-pass T sections, of which that in 27a has series impedances as discussed before, while that in 27b has series impedances that have been modified by a factor M. This factor is an undefined constant (whose numerical value lies between zero and unity), which has given rise to the name "M-derived".
For the constant-k section

$$Z_{0T} = \sqrt{Z_1Z_2 + Z_1^2/4} \quad [5]$$

while for the M-derived section

$$Z_{0TM} = \sqrt{MZ_1Z_2 + M^2Z_1^2/4} \quad [36]$$

These impedances will be equal if

$$Z_2' = \frac{Z_2}{M} + Z_1\frac{1-M^2}{4M}$$

With this result, Fig. 27b is redrawn as shown in Fig. 28. It is seen that the centre limb is made up of the opposite kinds of impedance in series, i.e., a

tuned circuit, where all values depend on M.

By the same type of equivalence, the M-derived π section shown in Fig. 29 is obtained. Here again, the centre limb consists of opposite impedances, which form a parallel-tuned circuit.

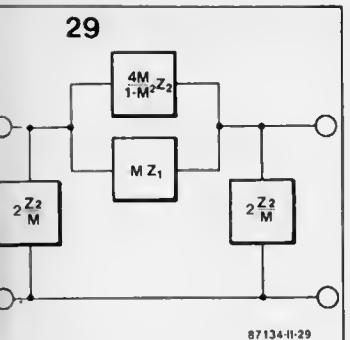
The constant-k low-pass and high-pass sections of Fig. 15, 16, 21 and 26 are modified to M-derived sections in Fig. 30.

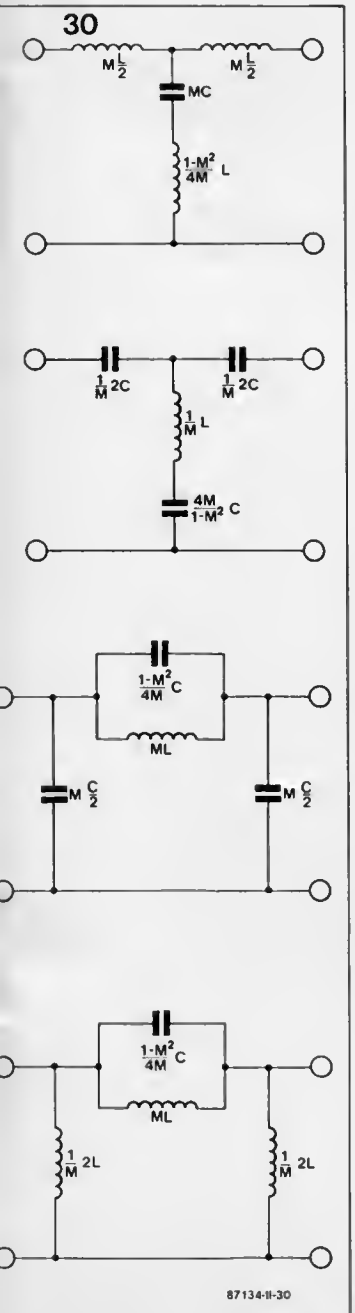
It should be appreciated that series or parallel resonance can occur in these M-derived sections. This aspect makes it possible to improve the rather sloppy performance of constant-k prototypes. None the less, the good attenuation performance far outside the pass band exhibited in constant-k sections will still be of value in combination filters.

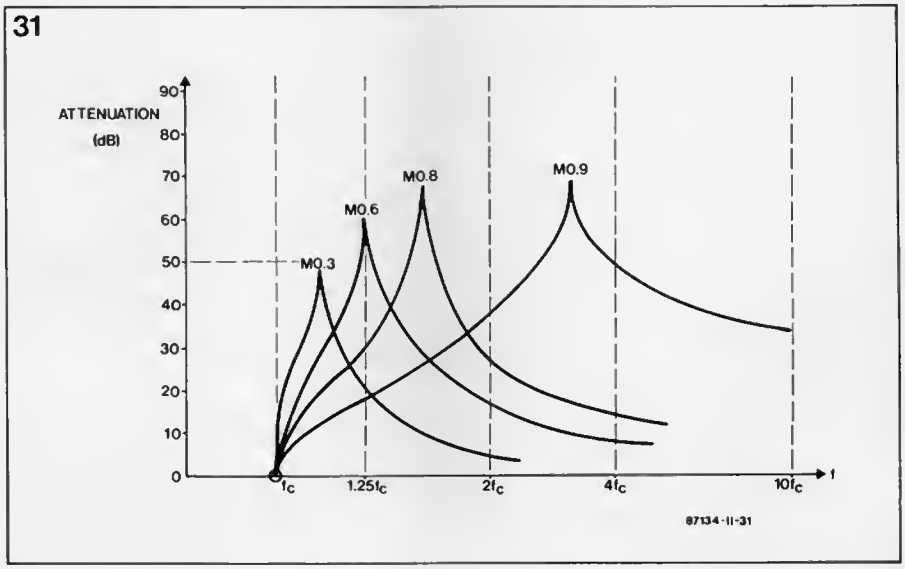
The attenuation vs frequency characteristics with values of 0.3, 0.6, 0.8, and 0.9 for M are shown in Fig. 31.

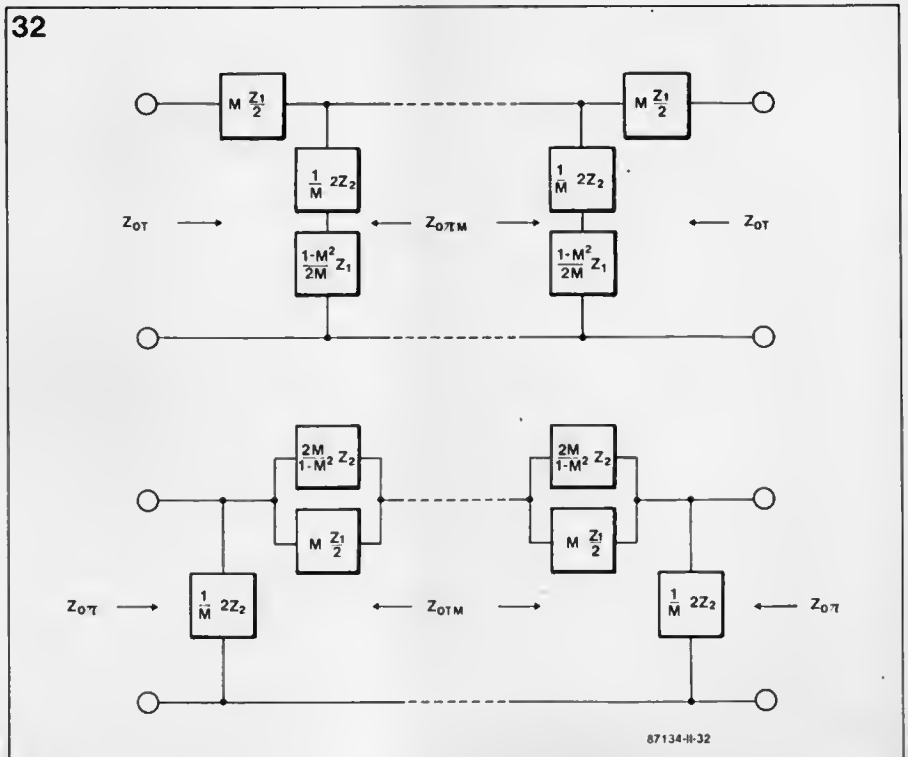
M-derived terminating half sections

The asymmetrical T/2 and $\pi/2$ sections of Fig. 11 are modified to M-derived half sections in Fig. 32. The usefulness of these terminating sections is that if M is given a value of 0.6, Z_0 lies between $0.9Z_0$ and $1.1Z_0$ for most of the pass band. Consequently, this value of M has become the standard for terminating sections. The variation of Z_0 as a function of frequency is









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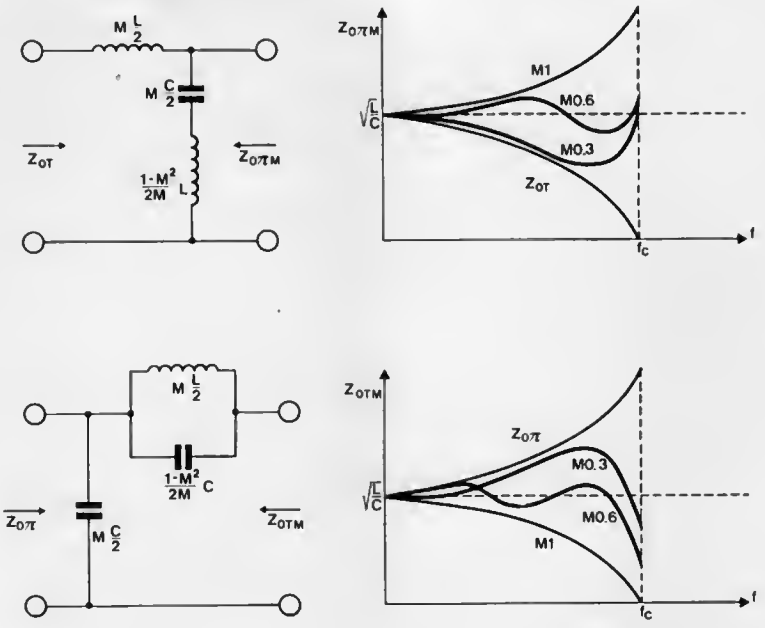

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TERMINATING HALF SECTION M0.6	SHARP CUT M0.3 - M0.4 SECTION	ONE OR MORE CONSTANT K OR LARGE VALUE 'M' SECTION	SHARP CUT M0.3 - M0.4 SECTION	TERMINATING HALF SECTION M0.6

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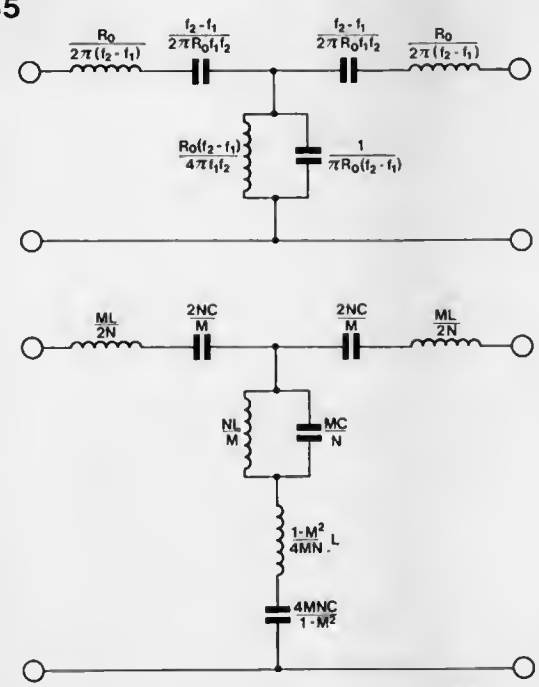

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shown in Fig. 33 for both a T and a π half section.

Low-pass and high-pass filters are designed to a given specification by combining *M*-derived terminating sections with small-value *M* sections, and either constant-*k* or large-value *M* sections in the middle so that the attenuation far from the cut-off frequency can be made large. A typical cascade is shown in Fig. 34.

The foregoing covers the basic principles of the **image parameter network theory**. Band-pass filters, both constant-*k* and *M*-derived, can be designed with the aid of this theory, but the computations tend to become cumbersome. Band-pass filters may be constructed by cascading low-pass and high-pass sections, particularly when large bandwidths are required, but this method presents difficulties with true band-pass designs. None the less, design equations for a constant-*k* and an *M*-derived band-pass filter as shown in Fig. 35 are given here without proof:

$f_1 \cdot f_2 = f_0^2$

$f_2 - f_1 = 2Nf_0/\sqrt{(1-M^2)} = \frac{\text{bandwidth}}{\sqrt{(1-M^2)}}$

In modern network theory (synthesis techniques), tables are available that enable the design of low-pass, high-pass, and band-pass filters from AF up to about 500 MHz to be undertaken with the aid of a hand-held calculator only.

The concluding part of this article will be published in next month's issue.

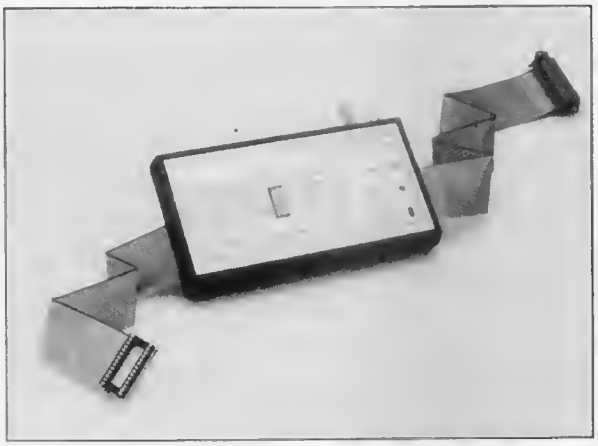
UNIVERSAL EPROM EMULATOR

Any EPROM can be emulated by a RAM with double access: one for reading, and one for writing. The circuit presented here is situated between a host computer and the target system whose resident EPROM software requires fast and efficient editing, that is, without the use of an UV lamp and an EPROM programmer for testing the effect of any small alteration.

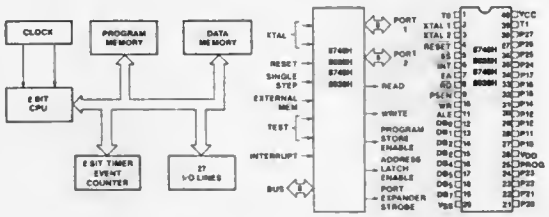
An EPROM emulator can offer a significant time saving to programmers engaged in writing, debugging, or upgrading resident EPROM software. Virtually every computer operator knows that even a single wrong bit in an EPROM may require the device to be taken from its socket, erased with ultra-violet light, verified for complete erase, and entirely re-programmed. Obviously, this is a time consuming procedure that readily ends up in one or more of the EPROM terminals breaking off. The EPROM emulator presented here enables modifying the EPROM contents *while* this is used in the target system. A separate (host) computer is used for editing and filing the contents, and for downloading it into the target system until this runs to satisfaction.

RAM for EPROM

An EPROM emulator is essentially an autonomous block of RAM which can be accessed from two sides simultaneously. For the host system, i.e., the external computer used for editing and downloading the program, this block of memory offers read *and* write access, for the target system read access only. The EPROM emulator therefore comprises a buffered block of RAM whose write enable line can be blocked to simulate the function of a ROM, inserted in the place of the EPROM whose contents require correction or alteration. The EPROM so emulated contains one or more programs or data blocks (look-up tables and the like) that are essential to the operation of the target system. The writing and/or correcting of the EPROM contents is carried out on the host system, which controls and loads the EPROM emulator via a standard serial (RS232) or parallel (Centronics) interface. The target system may be any 8-bit, microprocessor-controlled system, or, indeed, another microcomputer. It is even possible for the host and target system to form part of one and the same computer, which can then modify some of its ROM or EPROM based software via the serial or parallel port. Two EPROM emulators can be operated in parallel to enable working in a 16-bit system. When only one parallel or serial port is available on the computer, the emulators can be connected in turn for alternate editing, filing and downloading of the least significant and most significant databytes.



Device	Internal Memory	
8039H	none	128 x 8 RAM
8035H	none	64 x 8 RAM
8749H	2K x 8 EPROM	128 x 8 RAM
8748H	1K x 8 EPROM	64 x 8 RAM



Intel's 8748H/8035H/8749H/8039H microcontrollers

Universal EPROM Emulator

Technical characteristics:

- Emulates EPROM types 2708, 2716, 2732, 2764, 27128 and 27256.
- Direct communication with the target system via a DIP header inserted in the EPROM socket.
- Serial and parallel (RS232 or Centronics) input for downloading EPROM data from the host computer.
- Serial data format: 1 start bit, 8 data bits, 1 or more stop bits. 4 switch selectable baudrates: 1200, 2400, 4800 and 9600.
- Supports 3 file transfer formats with checksum:
  - Intel
  - Tektronix
  - Motorola

  Binary transfer without checksum.
- Visual indication on DATA and READY (transfer complete) line.
- Audible signal for error reports.
- Fast, cost-effective and easy to use.

Access from two sides

The basic operation of the EPROM emulator is shown schematically in Fig. 1. The EPROM whose contents require editing is removed from its socket in the target system, and its place is taken by a header connected to a length of flat ribbon cable carrying the data, address and control lines available in the target system to the EPROM emulator. In this, the address bus is connected to a buffer controlled exclusively by the emulator, while the data bus is connected to a buffer controlled exclusively by the target system. The other side of the buffers is connected to a 32 Kbyte RAM, in which the emulator CPU—a Type 8748H here—places the datawords received from the host computer. To avoid all misconception, it is necessary to keep the functions of host system, EPROM emulator, and target system quite separate. When a complete block of data has been received by the CPU in the emulator, it arranges for the address buffer between the 32 Kbyte RAM and the target system to be enabled, and its own data and address

bus to be disconnected from the RAM. Control line $\overline{WE}$ (write enable) of the RAM is deactivated, while $\overline{CE}$ (chip enable) is left active. From then on, the relevant area of the 32 Kbyte RAM functions as a read-only memory block in the target system, which gains access to the "EPROM" contents with the aid of lines $\overline{OE}$ (output enable) and $\overline{CE}$ via the 28-way flat ribbon cable.

System control: the 8748H

Briefly recapitulating the foregoing, the EPROM emulator can be considered a quasi-intelligent EPROM which, apart from its data and address bus, has a serial or parallel interface for ready and fast external programming.

The circuit diagram of the programming tool appears in Fig. 2. At the heart of the circuit is the Type 8748H microcontroller, IC_1. When the RESET key, S_{10}, is pressed, the CPU reads the position of S_9 to select between parallel and serial data transfer. The file transfer mode, EPROM type, and serial data speed is read from the configuration of DIL switches S_1-S_8—see Table 1. The parallel, Centronics compatible, input is complete with 8 data inputs plus the associated strobe line, $\overline{STRB}$, and 2 handshaking signals: $\overline{ACK}$ and BUSY for interfaces activated with the aid of a negative or positive level transition respectively. The non-used outputs PE (paper empty), INPUT PRIME RET, and $\overline{FAULT}$ are forced to the inactive logic level, so that virtually any computer should be able to communicate with the EPROM simulator as if it were a standard printer. It should be noted the K_1 is a 36-way header on the PCB for connecting to a Centronics socket on the EPROM emulator. The correct pin connections between these are automatically made with the aid of a length of flat ribbon cable and a 36-way IDC socket. Therefore, the pinning of K_1 is not identical to that of the Centronics socket.

Since the processor is not fast enough for reading the data on the Centronics input, octal latch IC_7 is clocked with the $\overline{STRB}$ pulse for intermediate data storage, while the bistables in IC_8 generate the $\overline{ACK}$ signal when output P1.7 on the CPU goes high, signalling readiness for reception of a new byte. The presence of a new byte in latch IC_7 is signalled to the processor by the negative transition of the inverted BUSY signal, which is applied to input $\overline{INT}$, and used for lighting LED D_2 also, enabling the user to verify reception of data both in the parallel and the serial mode. CPU input T0 is grounded via S_{9b} when the parallel mode is selected. In the serial mode, T_1 and D_1 convert the RS232 levels on the R×D line into 5 V pulses for driving the INT input on the CPU. It should be noted that the absence of handshaking on the serial input necessitates the use of a number of "zero-modem" wire links on the connector at the host computer side, and this will be reverted to under *Construction*. RS232 handshaking lines are omitted to keep the serial interface simple, without compromising the data transfer speed, which is still fairly high at 9,600 baud maximum.

When an error condition arises, the processor arranges for buzzer BZ_1 to be actuated via output P1.1 and MOSFET T_2. The READY LED, D_3, is illuminated by T_3 when the processor activates its P1.2 output. A single RAM chip, IC_2, caters for the entire 32 Kbyte memory to enable programming all the EPROMs in the 27XXX series without running into problems regarding the address configurations.

Three buffers are provided for accepting the bus signals from the target system: IC_5 and IC_4 for the address bus, and IC_6 for the data bus. The outputs of these buffers can be switched to the high impedance state by making input $\overline{E1}$ or $\overline{E2}$ logic high. The function of IC_3 is apparent from the signal applied to pin 11: ALE (address latch enable) is the demultiplexing signal for the databus (D0-D7) and the LS address bus (A0-A7) which share pins 12 to 19 incl. on the 8748H controller.

The target system can only read from the EPROM when IC_4 and IC_5 are activated by the high level on processor output P1.2. In this condition the RAM can place its data onto the databus, since $\overline{OE}$ is low together wit $\overline{E2}$ and $\overline{E1}$ of the buffers, while demultiplexing latch IC_3 is switched to the three-state mode. The target system can activate IC_6, and hence read the RAM, by pulling the $\overline{OE}$ and $\overline{CE}$ lines on the EPROM socket low.

The rather unconventional central clock frequency of 9.216 MHz (X_1) is needed for the timing on the serial input channel, since the 8748H lacks an ACIA based asynchronous communication port. In the present circuit, the processor's interrupt facility is used for reading serial characters. Reception of a serial dataword commences with an interrupt caused by the negative transition of the start bit pulse. When half the start bit period has lapsed, the 8748H starts a counter to introduce a delay corresponding to the period of the start bit. This period depends on the baudrate set with S_6-S_7. When the delay has lapsed, a new interrupt is generated when the counter counts out. This happens when half the period of the second bit has lapsed. The CPU reads the logic level on the R×D line via T_1 and restarts the counter for another bit period, ensuring enough time for processing the received bit, i.e., using it for composing the complete dataword and organizing the hexadecimal file in the memory. This process continues until the last bit of the last dataword has been read into the emulator. The maximum bit rate so achieved is 9,600/s without the use of handshake signals.

Introducing the 8748H microcontroller.

In view of its specialist nature, Intel's microcontroller Type 8748H has not yet been the subject of an article in *Elektor India*, although it has been on the market for some years already. That shortcoming is rectified in the present article.

The 8748H and Intel's more recently introduced MCS51 series (described in *Single-chip microcontrollers*, elsewhere in this issue) are firmly aimed at electronics specialists, and will form the basis of a number of articles to be featured in forthcoming issues of *Elektor Electronics*.

The 8748H affords good introductory experience with these ready-programmed microcontrollers. It is a less complex and less expensive controller than, say, the 8051, but it is none the less perfectly suitable for a number of small-scale applications, such as the EPROM emulator presented here.

The 8748H is the EPROM version of the mask-programmable 8048, which has found numerous applications in computer keyboards and industrial control systems. Neither the 8748H nor the new MCS51 series can be programmed with an ordinary EPROM programmer, but can only be purchased ready programmed from Elektor Electronics or its agents. These devices, therefore, signal the end of the publication of hexdumps, source listings, and other detailed information on the control program.

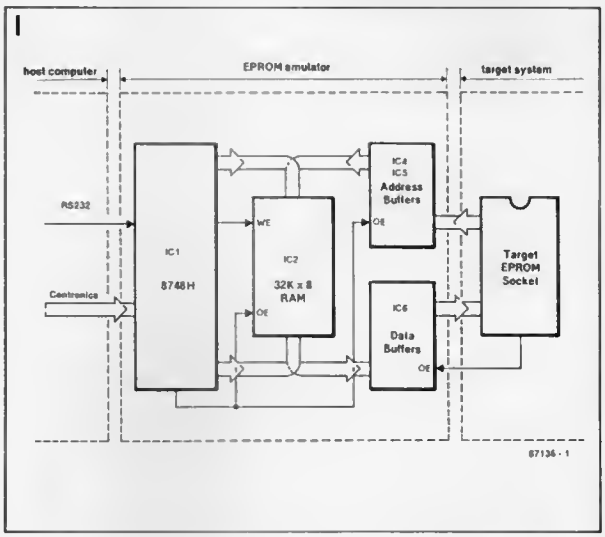


Fig. 1. Illustrating the basic operation of the EPROM emulator.

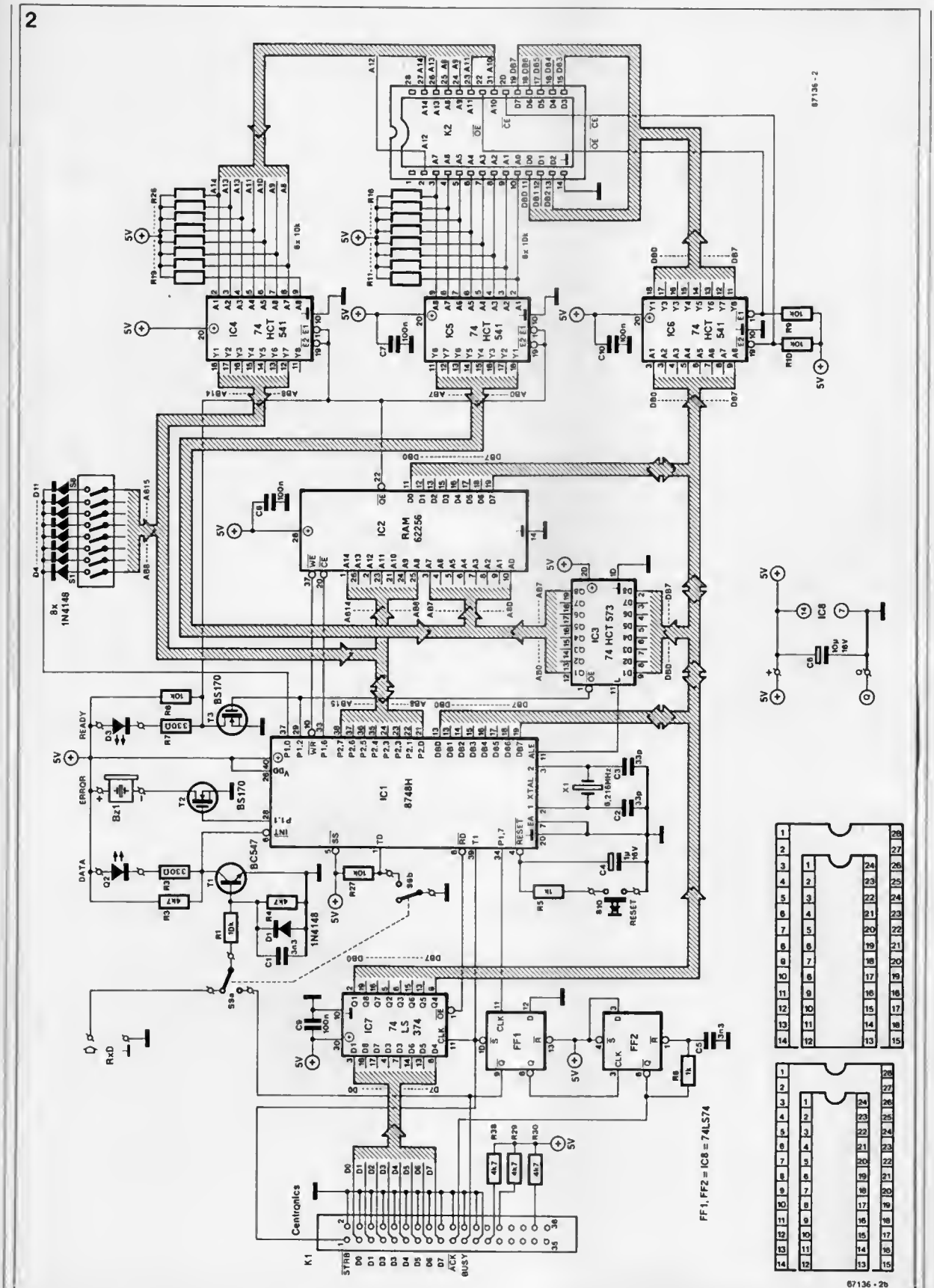


Fig. 2. Circuit diagram of the EPROM emulator.

The CPU clock frequency is determined by the bit period and the internal clock division factors, 15 and 32, of the 8748H. The EPROM emulator draws about 200 mA from an external 5 V supply, which will be part of either the host or the target system in most cases. It is, of course, also possible to build a simple, 7805 based, power supply for the emulator.

Addressing

Figure 3 shows that substitution of the EPROM in the target system by an external block of RAM requires consideration of the implications of this at the address decoding level. This is briefly discussed in the following four points.

1. If the emulated EPROM has a capacity of less than 32 Kbyte, the corresponding RAM area in the emulator is always located **below** the upper bound of the 32 Kbyte area extending between 0000H and 7FFFH. A Type 2764 8 Kbyte EPROM, for example, is emulated with the aid of memory area 6000H (lowest EPROM address) to 7FFFH (highest EPROM address). Therefore, Fig. 3 distinguishes between the read/write address area of the RAM, and the read-only address areas in the RAM considered EPROM by the target system. All operations in the memory are effected by the 8748H alone, and are invisible to the user.

2. The size of the memory area must always correspond to that of the emulated EPROM. In practice, this means that a 27128, for instance, should not be emulated with the settings of a 2732, or vice versa. The contents of the emulated EPROM are only verified when certain conditions relating to the data transfer are satisfied—this will be reverted to in the section on file formats.

3. Non-used address lines should be left unconnected or made logic high in the target system. When, for example, a 2764 is emulated, the address lines used are A0-A12 incl. (see Fig. 3). The socket pins carrying address lines A13 and A14 should then be made logic high, or left unconnected.

4. In addition to +5 V, the now obsolete Type 2708 needs a +12 V and −5 V supply voltage, both of which may **not** be carried by pins 21 and 19 of the EPROM socket that receives the header from the simulator. When the emulation is finished, the relevant connections should be restored before fitting the (re-programmed) 2708.

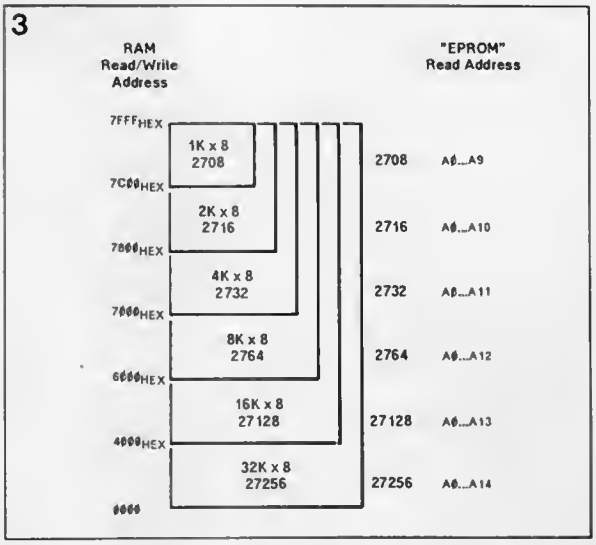


Fig. 3. Memory configurations for the various types of EPROM that can be emulated.

File formats

The contents of the emulated EPROM are transferred via the parallel or serial interface. The bit rate on the serial channel, the EPROM type, and the file transfer format are set with DIP switches S_1-S_8 as shown in Fig. 6.

Four file transfer formats are supported by the present EPROM emulator: binary, Intel, Motorola and Tektronix. The least complex of these is the binary format, in which the bytes for the emulated EPROM are transferred sequentially, starting with the lowest and ending with the highest one. The operating system in the EPROM emulator waits for the last byte in the 1, 2, 4, 8, 16 or 32 Kbyte large block of data before the target system can gain access to the RAM. The READY LED is illuminated when reception is complete. The binary transfer format has no verification procedure(s), but is faster than any of the other 3 for-

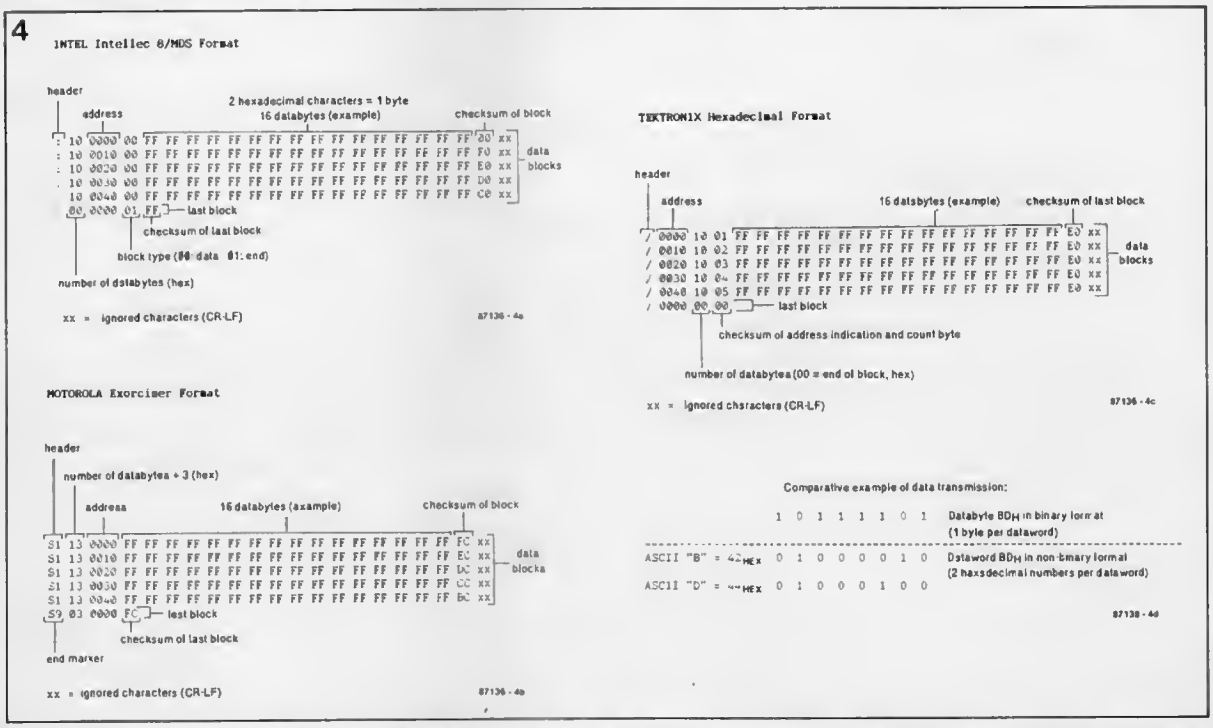


Fig. 4. Examples showing the essential characteristics of the various file formats supported by the EPROM emulator. Note that neither the block size of 16 bytes, nor the sequential addressing method of the blocks is imperative.

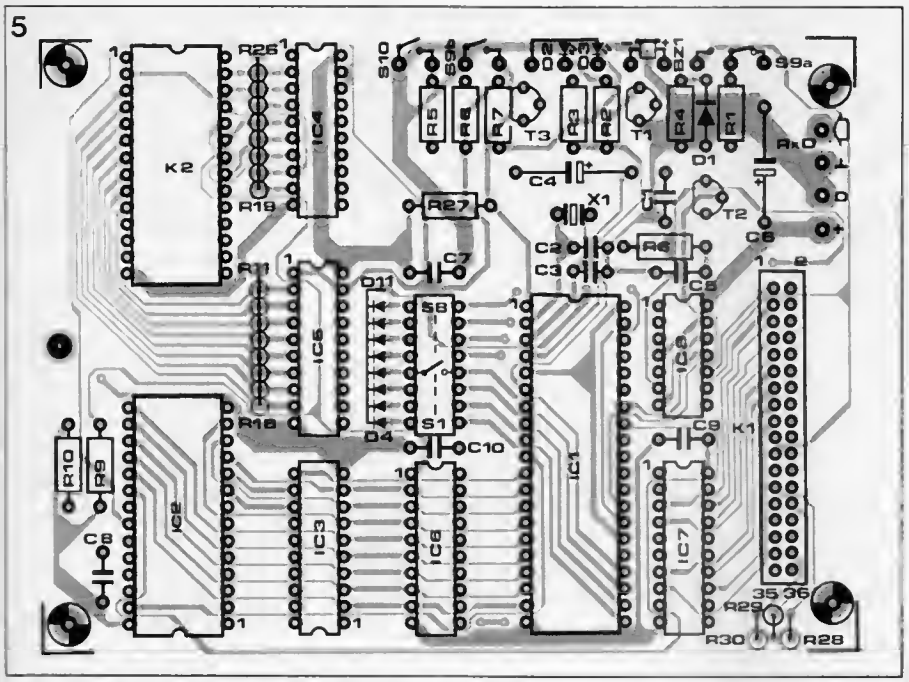


Fig. 5. The printed-circuit board for the emulator.

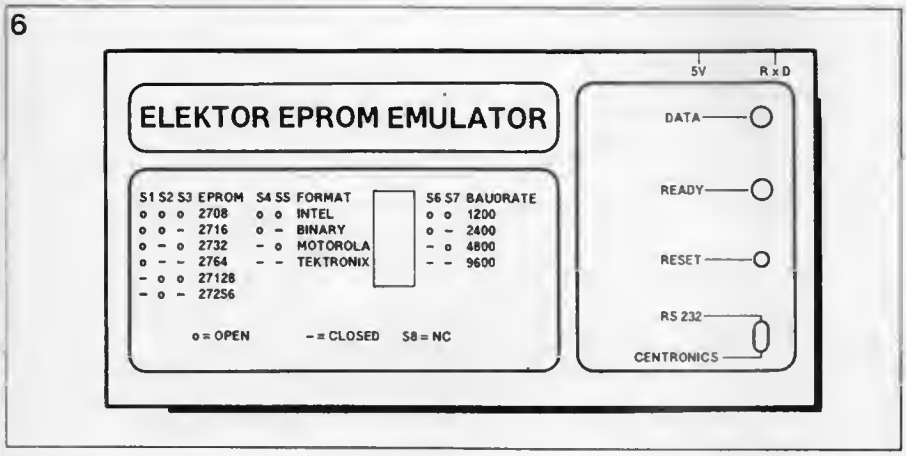


Fig. 6. Suggested front panel for the EPROM emulator (foil is NOT available through Readers Services). True width is 178 mm.

mats for updating or loading all or part of the contents of the emulated EPROM. Active buzzer Bz_1 sounds briefly to indicate that the emulator is fed with more data than can be held in the selected EPROM type—no account is taken of the excess bytes. The EPROM emulator should be reset before downloading a new file. Contrary to the standard adopted for the file transfer formats described below, the binary format does not require data to be converted into hexadecimal characters.

When the EPROM emulator is set to operate with the file transfer formats adopted by Intel, Motorola or Tektronix, the target system can only gain access to the emulated EPROM when the 8748H has received and recognized the marker *end of file record*, which, however, need not necessarily signal the end of the EPROM contents. In fact, these formats permit modification of only a number of bytes at EPROM addresses that can be specified by the protocol. This effectively speeds up the downloading process because only parts of the memory to be modified are involved. A further advantage of the above formats is the use of a *checksum*, which enables verifying the reception of correct data. The ERROR buzzer sounds intermittently when a discrepancy is detected. After reception of the *end of file record* marker, the EPROM emulator verifies the contents of the "EPROM", but the buzzer keeps sounding until the RESET key is pressed. Reports of discrepancies between the EPROM data on the host system and those in the emulator's RAM are due either to errors in the transmission, or—less likely—to a checksum error in the original file. In the former case, correct data transfer is readily achieved by once more sending the relevant block to the emulator, while in the latter case an investigation is needed into the operation of the checksummer on the host sys-

Parts list

Resistors (±5%):
$R_1;R_8;R_9;R_{10};R_{27}$ = 10K
$R_2;R_7$ = 330R
$R_3;R_4;R_{28};R_{29};R_{30}$ = 4K7
$R_5;R_6$ = 1K0
R_{11} . . . R_{18} incl.;R_{19} . . . R_{26} incl. = 10K SIL networks with 8 commoned resistors.

Capacitors:
$C_1;C_5$ = 3n3
$C_2;C_3$ = 33p
C_4 = 1µ; 16 V; axial
C_6 = 10µ; 16 V; axial
C_7 . . . C_{10} incl. = 100n

Semiconductors:
$D_1;D_4$ . . D_{11} = 1N4148
D_2 = red LED
D_3 = green LED
T_1 = BC547B
$T_2;T_3$ = BS170*
IC_1 = 8748H (available through the Readers Services).
IC_2 = 62256 or 43256 (32K × 8 CMOS static RAM)
IC_3 = 74HCT573 or 74LS573
$IC_4;IC_5;IC_6$ = 74HCT541 or 74LS541
IC_7 = 74LS374
IC_8 = 74LS74

Miscellaneous:
X_1 = 9.216 MHz.
S_1 . . . S_8 incl. = DIP switch block.
S_9 = miniature DPDT switch.
S_{10} = miniature push to make button.
Bz_1 = self-oscillating 5 V buzzer.
K_1 = double-row angled 36-way PCB header.
Mating IDC socket for K_1.
36-way IDC Centronics socket.
K_2 = 28-way IC socket with turned pins.
2 off 28-way DIL headers for press-on (IDC) connection on flat ribbon cable.
PCB Type 87136 (available through the Readers Services).
Suitable ABS enclosure.
Battery-mains socket and plug for external 5 V suppy (e.g. Roca 2.5 mm*).

Note: the front panel foil for this project is not available through the Readers Services.

* Available from Cricklewood Electronics Limited (see p.tt)

tem, since the error may well persist no matter how often the block is retransmitted.

Examples of the 3 non-binary file formats are shown in Fig. 4. Each byte is transmitted as 2 hexadecimal numbers, i.e., ASCII characters. Example: dataword BD$_H$ is transmitted as 42$_H$ followed by 44$_H$, which are ASCII codes for **B** and **D** respectively. Data is organized as *records* consisting of 16 bytes, in accordance with a standardized conversion of each dataword in two hexadecimal characters. When a program for supporting these formats is not available for the host computer used, formatting routines need to be written starting from the guide lines given in Fig. 4. The address transmitted at the beginning of each block is that of the first byte. The header (start character) is not the same for the three formats. In the Intel and Tektronix standards, the count byte gives the number of bytes contained in the block, and is, therefore, 00$_H$ in the final block. In the Motorola format, the count byte is the number of bytes in the block plus 3. The checksum in the Intel standard is the 2's complement of the sum of the preceding bytes, including the count byte, address and data. In the Tektronix format, the 2 checksums transmitted for each block are the 8-bit, modulo-256 sum of the preceding 4-bit hexadecimal numbers. Motorola uses yet another verification procedure: here the checksum is the 1's complement of the binary sum of the count byte, address bytes, and databytes. The *end of the block* marker is 01$_H$ (instead of 00$_H$) in the Intel mode, and S9$_H$ (instead of S1$_H$) in the Motorola convention. Characters received after the checksum of the block, and before the header of the next block, are simply ignored, and can not upset the file transfer.

In the following example it is assumed that the Intel format is used. Each line of 16 databytes results in 43 ASCII characters, followed by the expletive CR/LF sequence, i.e., 45 bytes in all for the transfer. The time needed for transferring a memory area of n bytes at a bit rate B is therefore calculated from

$(n/16) \times 45 \times (10/B)$ [s].

Using the Intel format. a file consisting of 4096 bytes can be transmitted in 12 s when the baud rate is 9,600. For the binary format, the time required is simply the EPROM capacity multiplied by $10/n$, i.e., 4 s for 4 Kbytes at 9600 baud.

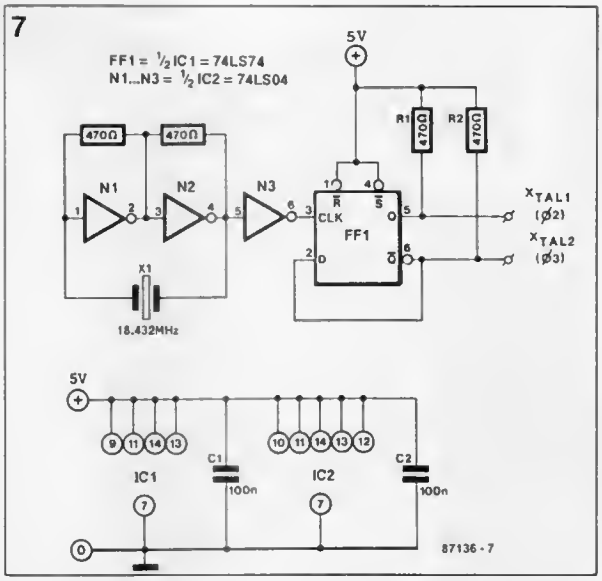


Fig. 7. Build this alternative clock oscillator circuit if a 9.216 MHz crystal is unobtainable.

Table 1.

C	K1	signal	C	K1	signal
1	1	DATA STROBE	19	2	
2	3	DATA 1	20	4	
3	5	DATA 2	21	6	
4	7	DATA 3	22	8	
5	9	DATA 4	23	10	
6	11	DATA 5	24	12	GND
7	13	DATA 6	25	14	
8	15	DATA 7	26	16	
9	17	DATA 8	27	18	
10	19	ACKNLG	28	20	
11	21	BUSY	29	22	
12	23	PE = "0"	30	24	INPUT PRIME RET = "0"
13	25	"1"	31	26	NC
14	27	NC	32	28	FAULT = "0"
15	29	NC	33	30	NC
16	31	NC	34	32	NC
17	33	NC	35	34	"1"
18	35	NC	36	36	NC

Note: C = Centronics connector.
NC = not connected.

Fig. 8. Inside view of EPROM emulator.

Construction and use in practice

The component mounting plan for the double-sided, through-plated circuit board is shown in Fig. 5. As already mentioned, the pinning of connector K$_1$ enables ready connection to a Centronics socket via a 36-way IDC header and a length of flat ribbon cable—refer to Table I. The Centronics or RS232 cable between the simulator and the host computer should not be longer than about 1 metre. The connection between the emulator (K$_2$) and the EPROM socket in the target system is made with the aid of a 20 to 30 cm long flat ribbon cable terminated at both ends in a high quality 28-way DIP header. It is possible to omit K$_2$ and solder the header straight into the relevant holes in the PCB. It is advisable to check the correct connections between the systems, and to mark pin 1 of the target header in write paint to avoid all confusion.

All parts are soldered onto the PCB, except the 2 LEDs, S$_9$, S$_{10}$ and the self oscillating buzzer. Diodes D$_4$...D$_{11}$ incl. are fitted vertically with the cathodes pointing upwards and commoned by a length of horizontally running wire. The same mounting method applies to R$_{28}$, R$_{29}$ and R$_{30}$, and also for R$_{19}$...R$_{28}$ incl. and R$_{11}$...R$_{18}$ incl. if suitable SIL type resistor networks are not available. IC$_7$ and IC$_8$ should be low power Schottky (LS) types in view of the possibility of their inputs remaining unconnected. These 2 ICs can be omitted if it is not in-

tended to use the parallel input of the EPROM simulator. All other integrated circuits can be LS or HCT types. Make sure that IC3 and RAM IC2 are fitted with the correct orientation on the PCB. The power supply connection to the board is made either direct in relatively strong wire, or via a 2-way edge connector with screw terminals. As to the enclosure that houses the EPROM emulator, the photographs in this article should give some idea of the practical realization. Whatever housing is used, make sure that the DATA and ERROR LED are mounted such that their visibility is ensured from relatively far, and also that S10 is within easy reach. It is recommended to have the DIP switches protrude from the top panel to enable rapid changes of the settings. Figure 6 shows a possible layout for the pront panef of the emulator.

ft was already noted that the 9.2f6 MHz crystal may be a difficult-to-find component. Fig. 7 shows a suggestion for an alternative clock oscillator based on a 18.432 MHz crystal. ft should be noted that this circuit can not be located on the PCB for this project, and therefore needs to be built separately on a piece of Veroboard. It is important to have both the emulator and the target system powered when the connection between them is installed or removed.

As already suggested, a zero-modem configuration is used for the handshaking sigals on the RS232 interface if this is used for loading data into the EPROM emufator. Output signal RTS (*request to send*, pin 4) is connected direct to input CTS (*clear to send*, pin 5), and the same goes for DTR (*data terminal ready*, pin 20) and DCD (*data carrier detect*, pin 8). ff necessary, DSR (*data set ready*, pin 6) is connected to DTR-DCD. These connections should enable the RS232 interface to function as if there were real handshaking signals.

Whatever computer or computer-based system is emulated with the present EPROM emulator, both units should be powered before being interconnected. fnitialize the EPROM emulator by pressing the RESET key before transferring a new data block or file. The initialization has no effect on the RAM contents, but informs the 8748H that a new block of data is imminent. Also do not forget to press RESET after making any change in the DIP switch settings.

A 8748 based serial EPROM programmer will be described in a forthcoming issue of *Elektor India*.

Fig. 9. A prototype of the EPROM emulator used in conjunction with an Amstrad PC1512 host computer.

EW PRODUCTS • NEW PRODUCTS • NEW

The Protel PCB Design Package

An enhanced version of the popular low-cost PCB design package—Protef-PCB—is now available from UK distributor Engineering Solutions Limited. Version 3.0, priced at £799.00, features netlist capability from compatible schematic software, Track/Layer swapping, additional text sizes, power and ground planes, NC drill support and EGA support for 640 x 350 pixel display.

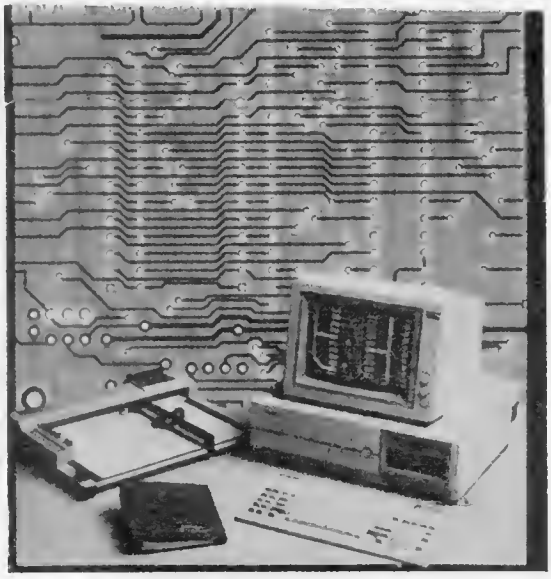
Protef-PCB will design PCBs as farge as 32 x 19 inches on six track layers to a one-thou grid resofution and additionally offers a range of features normally found only on expensive workstation design systems.

Other features include four track widths, six pad sizes, four edge connector pad sizes and two DfP pad sizes to suit a wide variety of applications.

The program generates multi-coloured checkplots, camera-ready artwork, Epson check printout and Gerber-compatible files, in addition to NC drill support.

A fully interactive evaluation disk is available from Engineering Solutions for 25.00.

Engineering Solutions Limited
King's House,
18 King Street,
Maidenhead,
Berkshire SL6 1EF.
Tefephone: (0628) 36052
Telex 849462 TELFAC G
Fax: 0628 74928 (3654:13:F)



ACTIVE PHASE-LINEAR CROSS-OVER NETWORK

The ideal cross-over network is free of phase-shift, resulting in optimum pulse performance and radiation pattern. Although the ideal is not yet within reach, the work of Stanley Lipshitz and John Vanderkooy enables it to be approached very closely.

The most serious problem with ordinary cross-over filters is best illustrated with reference to a two-way system. This consists of a low-pass and a high-pass filter. One of the properties of a low-pass section is that it causes a time-delay of the signal. A high-pass filter on the other hand causes an acceleration of the signal. These actions result in a number of complications at the cross-over point:

(a) the signals from the two sections partially cancel one another;
(b) the strongly varying phase shift between the two signals adversely affects the radiation efficiency of the overall system;
(c) the radiation pattern becomes frequency dependent.

Some years ago, Stanley Lipshitz and John Vanderkooy published a series of papers [1, 2, 3] that have laid the foundation of the so-called phase-linear cross-over network.
Basically, the phase-linear network uses a low-pass section that also provides a high-pass characteristic with the aid of a time-delay and subtraction circuit. True, the time-delay is not constant over the entire frequency range, but it varies only slowly; moreover, there are no phase differences between the two output signals, even near the cross-over frequency.
A block schematic of a two-way, as well as a three-way, system based on the work of Lipshitz and Vanderkooy is shown in Fig. 1. It should be emphasized that the time-delay is an essential facet of the design. There are filters that make use of the subtraction method only, but these do not exhibit phase linearity.

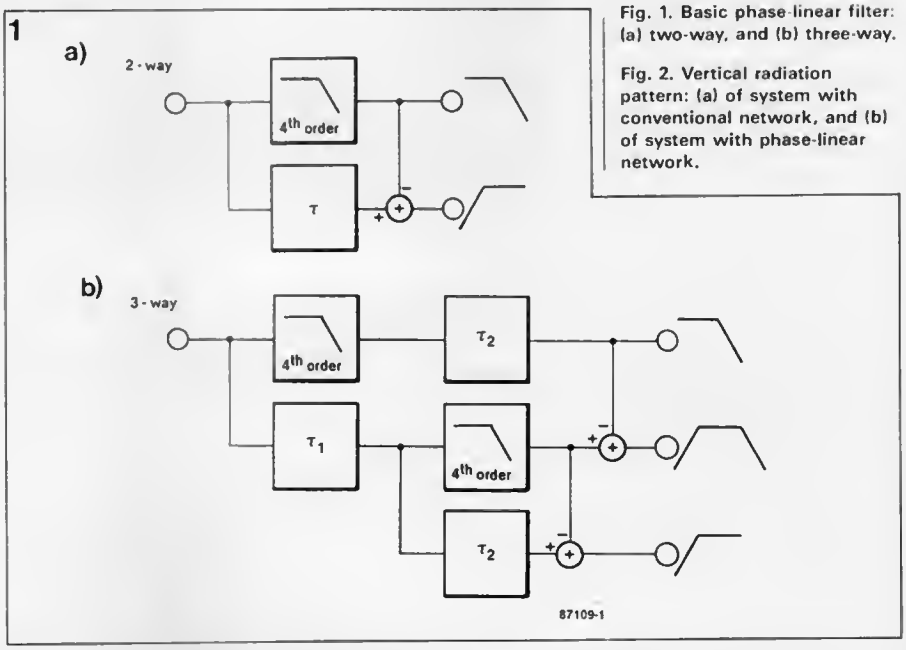


Fig. 1. Basic phase-linear filter: (a) two-way, and (b) three-way.

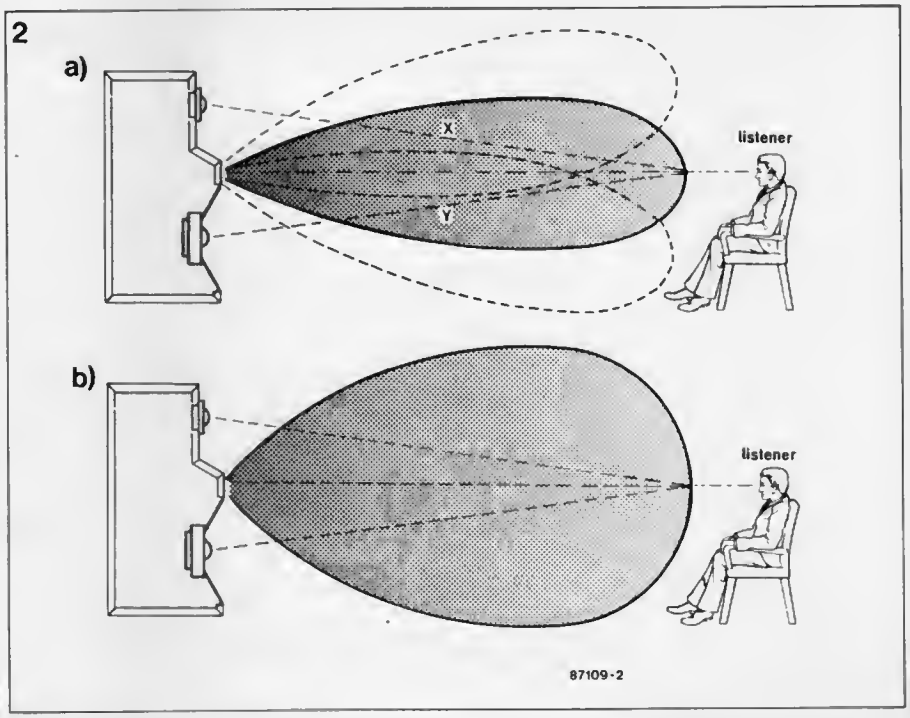


Fig. 2. Vertical radiation pattern: (a) of system with conventional network, and (b) of system with phase-linear network.

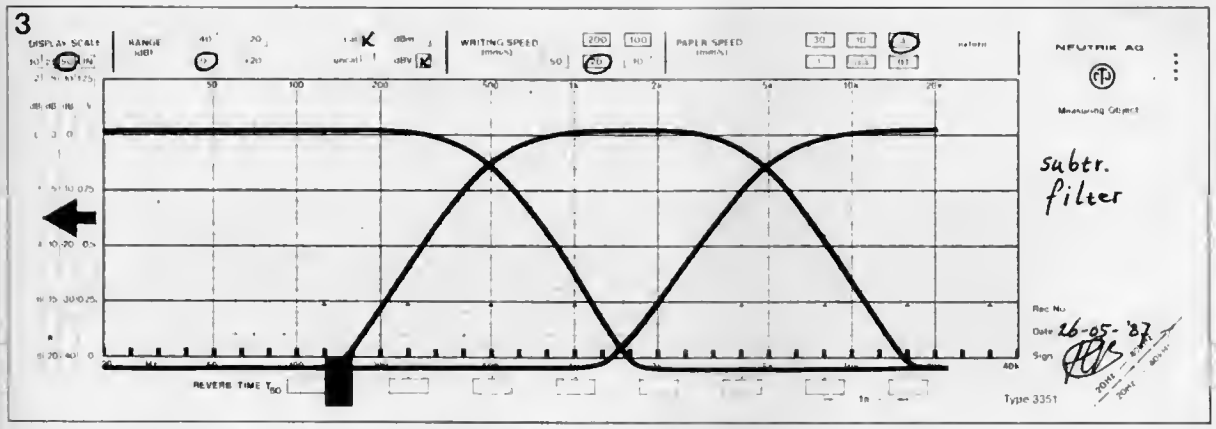


Fig. 3. Amplitude vs frequency characteristic of a three-way phase-linear network.

A customary fourth-order low-pass filter in the upper branch provides the normal low-pass performance. The delay, τ, is designed such that it has exactly the same phase behaviour as the low-pass section, and functions as an all-pass section. When then the output signal of the low-pass section is subtracted from the delayed signal, the result is a high-pass characteristic that has the same phase behaviour as that of the low-pass filter. Summing the two signals results in a perfectly straight line.

The set-up of a three-way system—see Fig. 1b—is a little more complicated, because an additional low-pass section has to be provided in the centre limb to obtain a band-pass characteristic for the middle frequency loudspeaker. This additional section must be compensated by a second delay, τ_2. Thus, in a three-way system, the τ_1 circuit simulates the time delay of the usual bass filter, while the τ_2 delay simulates the delay of the low-pass filter in the middle-frequency section.

The vertical radiation pattern (polar response) of a conventional loudspeaker system is shown in Fig. 2a. The dispersion is fairly small in the region where both speakers provide a signal. The spread also varies with frequency, which causes the lobe to either tilt or sag. The pattern of the phase-linear system in Fig. 2b shows that the lobe is much broader and points forward at all frequencies. In all this it is assumed that the acoustic centres of the loudspeakers lie on a vertical line, otherwise the pattern deteriorates.

A practical network

In a practical network, it is not possible (at least with an ac-

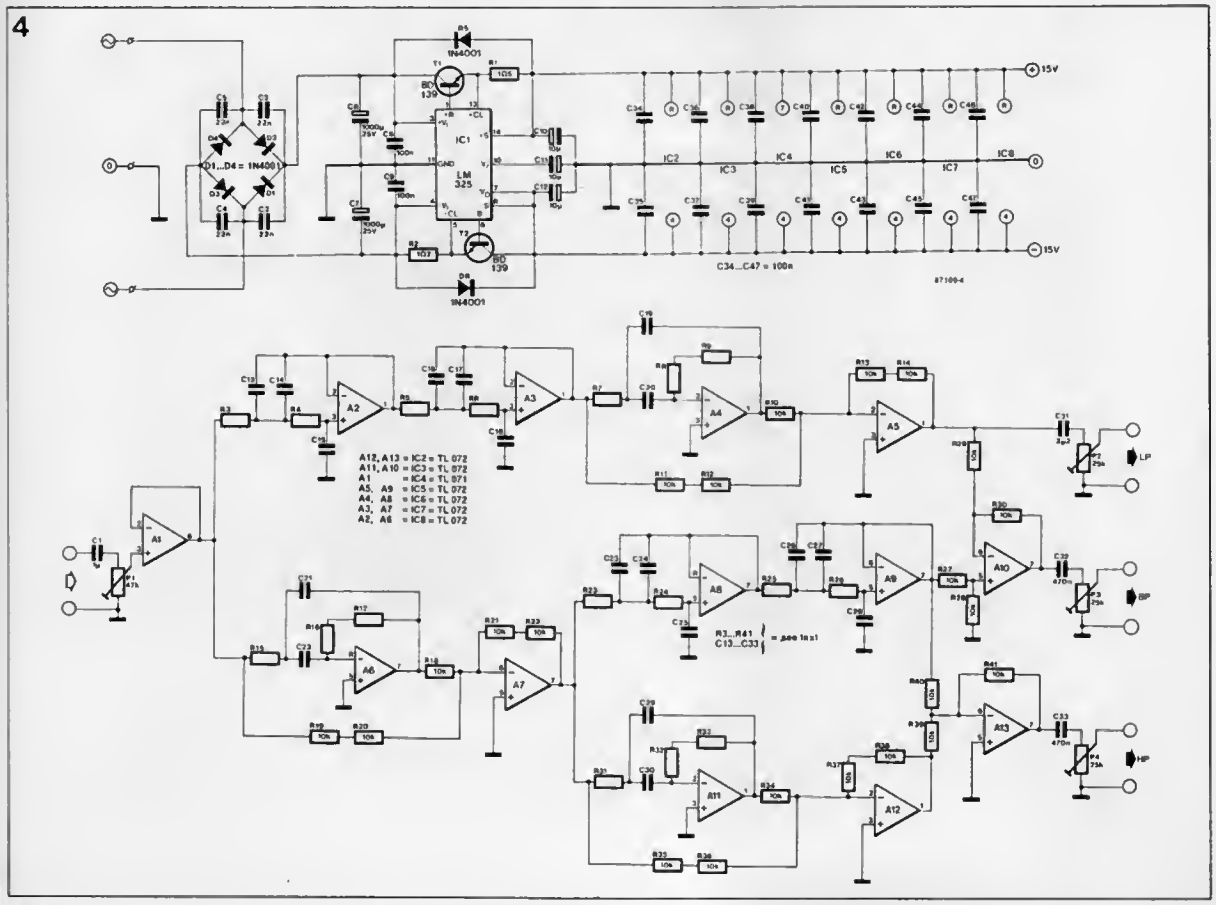


Fig. 4. Circuit diagram of the phase-linear network.

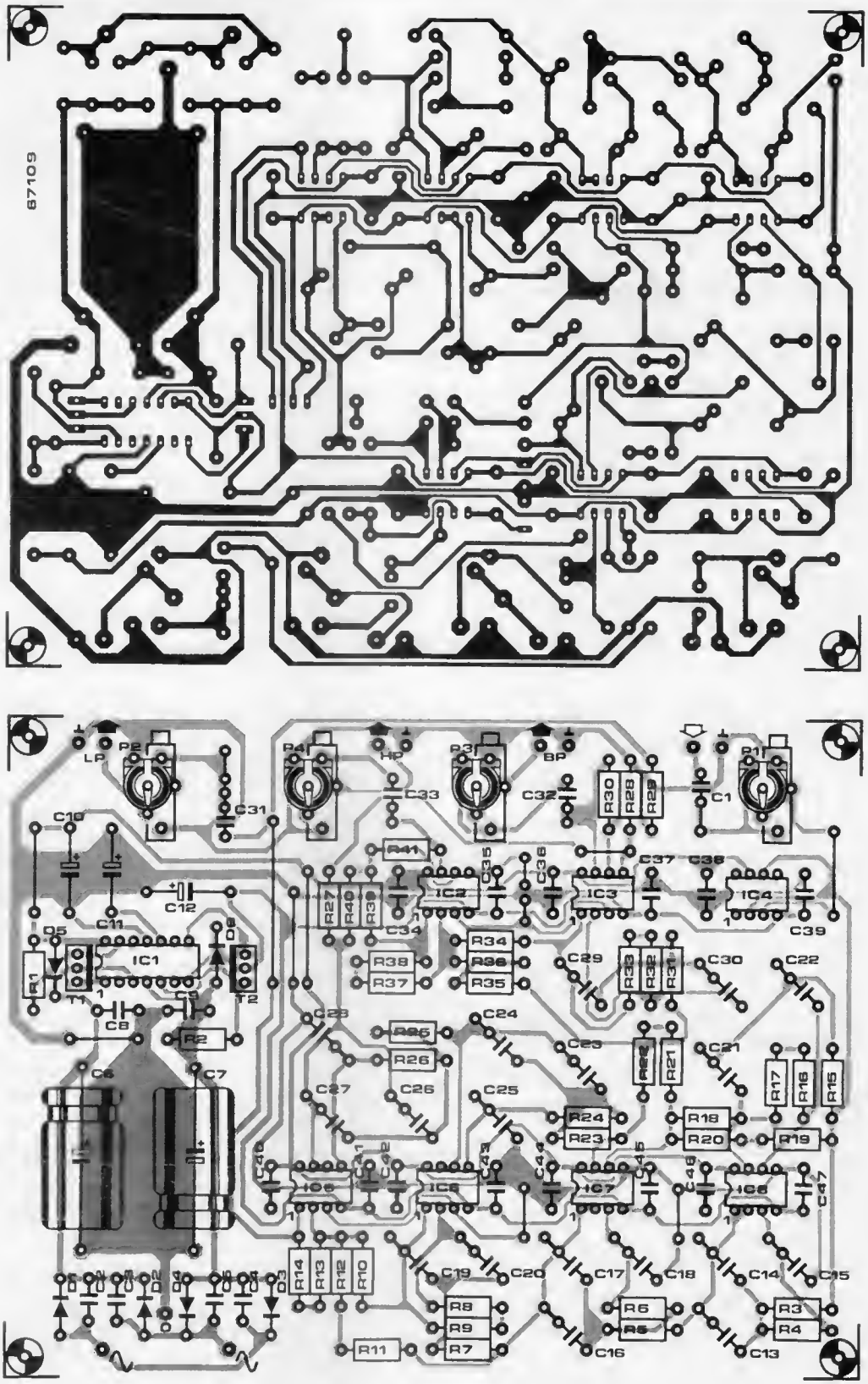
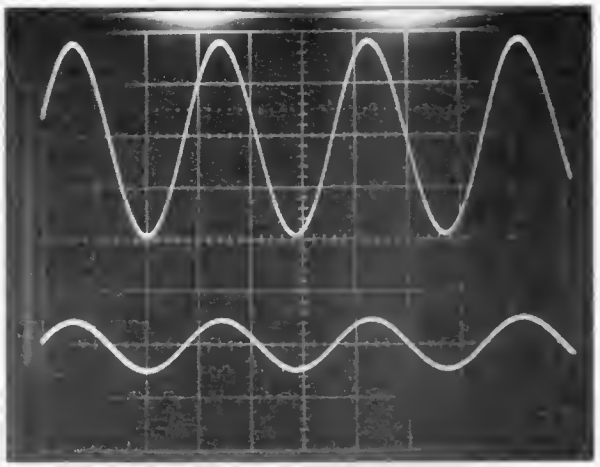


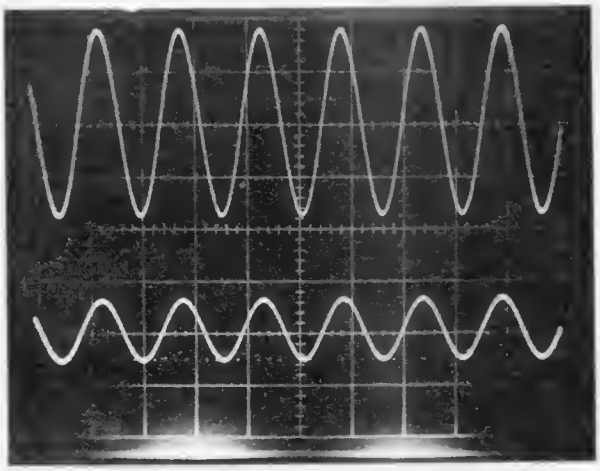
Fig. 5. Printed circuit board of the phase-linear filter.

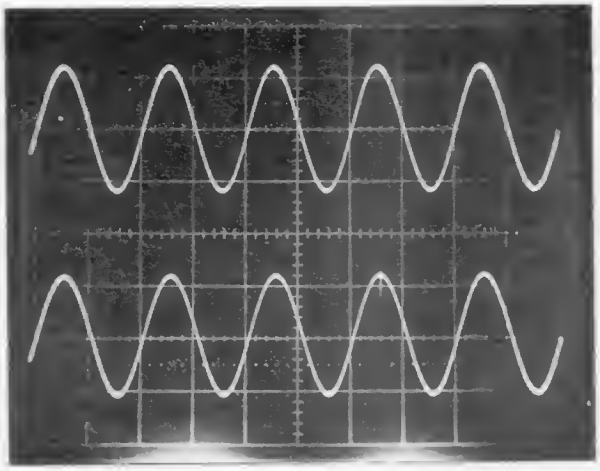
ceptable number of components) to simulate any phase behaviour with the aid of a delay circuit.
All-pass networks have some interesting properties:

(a) they cause a phase shift, but no signal attenuation over a given frequency range;
(b) the phase shift caused by them is twice as large as that caused by a filter of the same order.

From this, it is evident that the low-pass section should be an even-order type, i.e., second-, fourth- or sixth-order. In the present network fourth-order filters are used, since these give a sufficiently steep roll-off and do not unnecessarily complicate the circuit.
Like all fourth-order networks, the present consists of a cascade of two second-order filters. For the present purposes, these should be identical to ensure that the phase behaviour of the all-pass network will be the same as that of the filter.
It was found that the Linkwitz-Riley (Squared Butterworth) filter is eminently suitable for the present network, because it allows a fairly simple all-pass to be designed with only two opamps. The resulting circuit has exactly the same phase behaviour as a fourth-order Linkwitz low-pass filter. Note that the cross-over frequencies are −6 dB points (as in all Linkwitz filters), since there is no phase shift between the two channels. The relative amplitude vs frequency characteristic is given in Fig. 3, while the three photographs illustrate the typical performance of the network. The photographs show the output voltage at the low- and middle-frequency terminals (a) slightly below the cross-over point, (b) at the cross-over point, and (c) slightly above the cross-over point. No phase differences between the two signals are discernible anywhere.







Circuit description

In the circuit diagram of Fig. 4, opamp A_1 is used as a buffer between the input signal and the filter proper. If necessary, the input signal may be attenuated by P_1; the total amplification of the network is unity.
The low-pass filter is constructed around A_2 and A_3, while the associated all-pass filter is based on A_8 and A_7. The attenuation due to band-pass filter A_8 is compensated by A_7. The low-pass section for the middle frequencies consists of A_8 and A_9. Here, two identical all-pass filters are required, and these are formed by A_4-A_5 in the low section and by A_{11}-A_{12} in the high section. That completes the low-pass filter.
For the middle-frequency section, the output signal of A_5 must be subtracted from that of A_9, which is effected by A_{10}.
Finally, the output signal of A_9 is subtracted once more from that of A_{12}, which is done by A_{13}. That completes the high-pass function.

The three outputs of the network are taken to preset potentiometers that enable matching each of them to the efficiency of the associated loudspeaker.
The quality of the power supply matches that of the cross-over network itself. Circuit IC_1 is a voltage regulator, which, in conjunction with two external series transistors, provides symmetrical output voltages. Diodes D_5 and D_6 ensure that the regulator is not damaged at switch-off.

Parts list

Resistors:
R_1;R_2 = 1K5J
R_3 to R_8; R_{15} to R_{17}; R_{23} to R_{26}; R_{31} to R_{33} = 22K5F
R_{10} to R_{14}; R_{18} to R_{22}; R_{27} to R_{30}; R_{34} to R_{41} = 10KF
P_1 = 47KJ cermet preset
P_2 to P_4 = 25KJ cermet preset

Capacitors:
C_1 = 1μ0 plastic film
C_2 to C_5 = 22n ceramic
C_6;C_7 = 1000μ; 25 V electrolytic
C_8;C_9,C_{34} to C_{47} = 100n ceramic
C_{10} to C_{12} = 10μ; 25 V electrolytic
C_{13} to C_{18};C_{21};C_{22} = 10n; 2.5% polypropylene
C_{19};C_{20};C_{23} to C_{30} = 1n0; 2.5% polypropylene
C_{31} = 2μ2 plastic film
C_{32};C_{33} = 470n plastic film

Miscellaneous:
PCB Type 87109 (readers who wish to make their own PCB may order the relevant drawings free of charge on the Order Form on page 69).

NOTE: Many components may be available from
Audiokits Precision Components
6 Mill Close
Borrowash
DERBY DE7 3GU
Telephone: (0332) 674929

Semiconductors:
D_1 to D_6 = 1N4001
T_1 = BD139
T_2 = BD140
IC_1 = LM325
IC_2;IC_3;IC_5 to IC_9 = TL072; NE5532; LF353; LM833, OP215
IC_4 = TL071; NE5534; LF356; OP27; OP15

Construction

The network is most conveniently constructed on the ready-made PCB Type 87109 shown in Fig. 5. The values of the components given in the parts list pertain to cross-over frequencies of 500 Hz and 5,000 Hz. Different frequencies may be calculated with the aid of the Linkwitz formulas in Ref. 4.

In several places, capacitors are shown in parallel and resistors in series: this is done to enable the use of as many components of the same value as possible. As usual, the choice of capacitors is determined mainly by their loss factor and cost, which normally results in plastic film types.

It should be noted that each PCB has its own regulator IC: this is convenient where the network is fitted in the loudspeaker enclosure.

The impedance at the network outputs, depending on the position of the presets, has a maximum value of 12 kilohm. Since this may be on the high side for certain output stages, the value of the presets may be reduced to 5 kilohm, which results in a maximum output impedance of 2.5 kilohm. Where this is done, the value of C_{31} should be increased to 4μ7. A useful rule of thumb is that the input impedance of the output stage must be at least ten times as large as the output impedance of the network.

The PCB may be used to construct a two-way network, in which case the following components are omitted: IC_2; IC_5; IC_6; R_7 to R_{14}; R_{23} to R_{26}; R_{31} to R_{41}; C_{19}; C_{20}; C_{23} to C_{30}; C_{33}; P_4. Furthermore, a wire link should be fitted between pin 1 of A_3 and another between pin 7 of A_7 and C_{32}.

References

1. S. Lipshitz & J. Vanderkooy, *A Family of Linear-Phase Cross-over Networks of High Slope Derived by Time Delay* (Journal of the Audio Engineering Society, Jan. & Feb. 1983).

2. S. Lipshitz and J. Vanderkooy, *Is Phase Linearization of Loudspeaker Cross-over Networks Possible by Time Off-set and Equalization?* (JAES, Dec. 1984)

3. S. Lipshitz and J. Vanderkooy, *Use of Frequency Overlap and Equalization to Produce High-slope Linear-phase Loudspeaker Cross-over Networks*, (JAES, March 1985)

4. *Linkwitz Filters*, Elektor India, May 1987

car headlight alarm

This circuit is designed to give an audible and visible warning to the absent-minded motorist who forgets to switch off the headlamps when leaving his car.

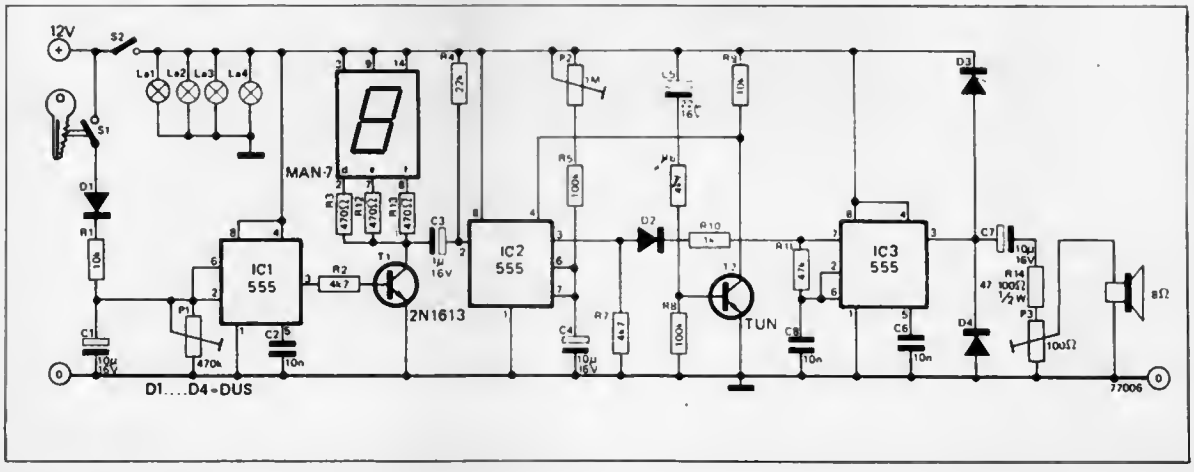
The power supply to the circuit is taken from the headlamp switch, represented by S2. If the headlamps are switched off then the alarm obviously receives no power and does not operate. The actual light switch in the car will be more complex than S2 since it also controls the sidelights. However, examination of the car wiring diagram and a little probing with a multimeter will soon show which terminal of the switch acquires a positive voltage when the headlamps are switched on.

S1 represents the car ignition switch. As long as the ignition is switched on pins 2 and 6 of IC1 are pulled high via D1 and R1. When the ignition is switched off, however, this voltage will fall as C1 discharges through P1. P1 sets the time allowed for switching off the headlamps before the alarm sounds.

When the voltage on C1 falls below the trigger threshold of IC1 then, assuming the headlamps are still switched on, the output (pin 3) of IC1 will go high, turning on T1. This lights the seven segment LED display which gives an 'L' indication. If the expense of a LED display is not thought to be justified then a single LED or lamp could be used. T1 also triggers IC2, which is connected as a monostable multivibrator. The output of IC2 goes high, thus activating astable multivibrator IC3, which begins to oscillate, producing an alarm signal from the loudspeaker.

The length of time for which the alarm sounds is determined by the period of the monostable IC2, which may be adjusted by means of P2. P3 adjusts the volume of the alarm signal.

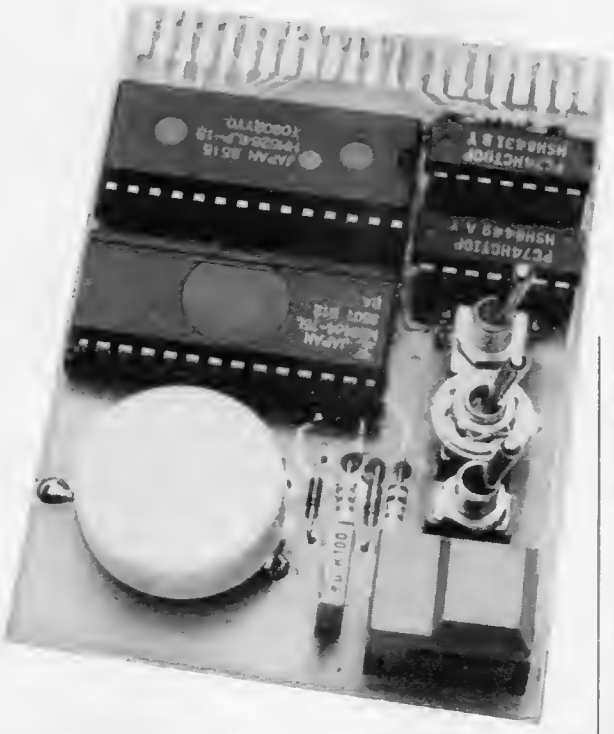
To prevent the possibility of IC2 being spuriously triggered when the headlamps are switched on, T2 is provided. When the headlamp switch is closed C5 begins to charge through R6 and R8, which momentarily turns on T2. T2 thus holds the reset input (pin 4) of IC2 low so that it cannot trigger.



16 KBYTE CMOS RAM FOR C64

by P Verhoosel

A non-volatile block of RAM or pseudo-ROM for plugging into the Commodore 64's expansion slot.



The expansion port at the rear of the Commodore 64 microcomputer is a 44-pin (22+22) female edge connector. The expansion slot—also referred to as bus, cartridge or module port—enables plugging in extension modules that require direct access to the address bus, data bus, and a number of control lines, of the Type 6510 CPU and its support chips inside the computer. Because of this direct connection, due care should be taken not to damage the system by inappropriate connections, overloads, or short-circuits. The signal functions and pin assignment of the expansion port are shown in Table 1 and Fig. 1 respectively. Viewed from the computer's keyboard, and counting from the left to the right, pins 1-22 inclusive form the upper row, and pins A-Z inclusive the lower row. Notice that letters G, I, O and Q are not used. Connections $\overline{GAME}$ and $\overline{EXROM}$ make it possible to gain external control over the C64's memory configuration, and have special significance for the present memory module.

The system configuration

At the heart of the C64's memory decoding circuitry is integrated circuit U_{17}, a Programmable Logic Controller (PLA), manufactured specifically for the C64. A total of 16 lines are fed into this IC, including $\overline{GAME}$ and $\overline{EXROM}$, giving $2^{16}=65,536$ (64 K) possible combinations. The 8 output lines of the PLA connect to internal devices including the BASIC ROM, the SYSTEM ROM, the character generator, CIA1, CIA2, and the RAM. The PLA's input/output ratio, 256:1, already indicates that a number of input combinations are necessarily duplicate and/or illegal to give a useful configuration of the C64' memory map, which is shown schematically in Fig. 2. The decimal and hexadecimal address notations are given to the left and the right of the 4 Kbyte memory blocks, respectively. When the C64 powers up with the original operation system, the following PLA inputs are driven logic high: $\overline{LORAM}$, $\overline{HIRAM}$, $\overline{EXROM}$, $\overline{GAME}$, $\overline{CHAREN}$.

Also shown in Fig. 2 are switches for controlling the logic level on the $\overline{GAME}$ and $\overline{EXROM}$ inputs of the expansion connnector. $\overline{EXROM}$ is active in memeory area \$8000 - \$9FFF (32,768 - 40,959), $\overline{GAME}$ in the next higher 4 Kbyte block, \$A000 - \$BFFF (40,960 - 49,151). The switches for $\overline{EXROM}$ and $\overline{GAME}$ offer four possible logic configurations:

a) $\overline{GAME}$ = 1; $\overline{EXROM}$ = 1.
b) $\overline{GAME}$ = 0; $\overline{EXROM}$ = 1
c) $\overline{GAME}$ = 1; $\overline{EXROM}$ = 0
d) $\overline{GAME}$ = 0; $\overline{EXROM}$ = 0

Although not harmful to the C64 hardware, combination **b** produces a hang-up, which can only be ended by altering the switch configuration and resetting the computer.
Combination **a** is valid when the computer is powered up, while **c** can be selected with the aid of switch S_2 on the present board. An additional switch, S_3, can be closed following S_2, and enables selecting combination **d**. Combination **b** is impossible to select thanks to the practical switch configuration.

Circuit description

The circuit diagram of the RAM extension is shown in Fig. 3. When S_3 is opened, the RAM module is switched to the write protect mode, and resistor R_1 ensures a fixed level at the $\overline{WE}$ (write enable) inputs of RAM chips IC_3 and IC_4, which then behave as ROMs, since they can only be read from, not written to. Gates N_3 and N_5-N_7 combine address lines A13, AI4 and A15 into a $\overline{CS}$ (chip select) line for each of the 8 Kbyte RAMs. Gate N_1 plus switches S_{2a} and S_{3a} ensure the correct set-up times for read operations in the RAMs. Parallel combination R_3-D_1 charges the on-board 3.6 V NiCd battery from the computer's 5 V supply. When the computer is off, the battery supplies the (very low) data retention current for the CMOS RAM chips. Components C_1-R_2-D_2 prevent dips and transients on the RAM supply lines when the computer is switched off, and the battery takes over. It should be noted that a dry battery is preferable over a NiCd cell when the computer is not used for periods longer than

about a month, because a NiCd cell inevitably loses its charge due to its self discharge current. R_3 is omitted when a dry battery is used.

Applications

Switched to configuration **c**, the battery back-up RAM makes it possible to slightly modify the resident BASIC interpreter for individual purposes, copy parts of it into the RAM/ROM module, develop and store new utilities, or have machine language programs permanently available. Memory area 32,768 to 40,959 is covered entirely by IC_3, and is fully accessible to the programmer.
Configuration **d** selects the full 16 KByte RAM block, which then takes the place of the 8 KByte Microsoft BASIC ROM and the internal memory block in this area. When RESET switch S_4 is pressed, the operating system in the C64 searches for the following tokenized code starting at $8004:

$8004	$8005	$8006	$8007	$8008
C3	C2	CD	38	30

Translated into ASCII, this stands for *CBM80* if the MSB, D7, is ignored. If this 5-byte string is found (cold boot), the CPU jumps to the address stored in location $8000 (L) and $8001 (H). The 16-bit vector for a warm start is located in the next two higher locations, $8002 and $8003.

Construction

The compact, ready-made printed circuit board for constructing the RAM extension is a double-sided, but not through-plated, type, which holds all the components—inclusive of the battery and the switches—and plugs straight into the C64's expansion slot. The track layouts and component mounting plan are given in Fig. 4. Commence the construction with fitting the resistors, capacitors, diodes and the wire link. Note that some components, including the IC sockets, are soldered at both sides of the PCB to effect through-plating. At the copper side, all connections are soldered, at the component side only those whose solder islands are not covered by the component overlay. The 2 holes in between S_3 and IC_2 are through-plated with the aid of component wire. The miniature switches can be fitted direct onto the board with the aid of bits of left over component leads. RESET key S_4 is a Type Digitast from ITT/Schadow, and should not present problems as to mounting. The 3.6 V NiCd battery should be fitted securely to make for a compact and sturdy extension module. Finally, plug in the integrated circuits, and the back-up memory is ready for use.

Note: Always switch off the computer before inserting or removing the 16 Kbyte RAM module. *St*

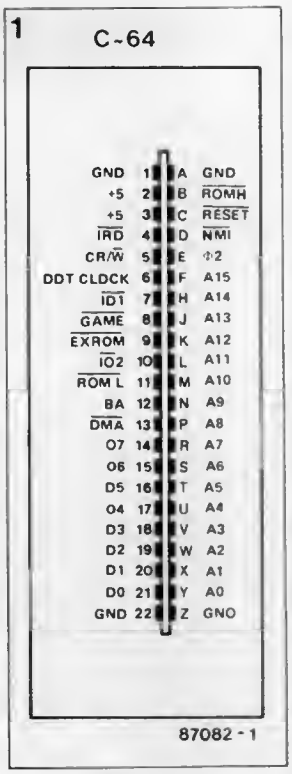


Fig. 1. Pin assignment on the expansion port at the rear of the C64 computer.

Table 1 Signal functions on the C64 expansion port:

Pin	Signal	Function
1 22 Z	GND	System ground
2/3	+5 V (V_{cc})	Power supply for User Port and Cartridge devices (450 mA max.)
4	$\overline{IRQ}$	Maskable CPU interrupt request line (active low).
5	R/$\overline{W}$	CPU output line. Memory read: 1; memory write: 0.
6	DOT CLOCK	8.18 MHz dot clock signal from video controller.
7 11 B 10	$\overline{I/O1}$ $\overline{ROML}$ $\overline{ROMH}$ $\overline{I/O2}$	Active low outputs for memory control.
8 9	$\overline{GAME}$ $\overline{EXROM}$	Active low inputs for memory control.
12	BA	8us available signal from the VIC-11 controller.
13	$\overline{DMA}$	Direct memory access request line.
14 : : 21	D7 : : D0	Unbuffered 6510 databus.
C	$\overline{RESET}$	Direct CPU reset line for initialising the computer.
D	$\overline{NMI}$	Non-maskable CPU interrupt line.
E	Φ2	CPU clock signal.
F : : Y	A15 : : A0	Unbuffered address lines.

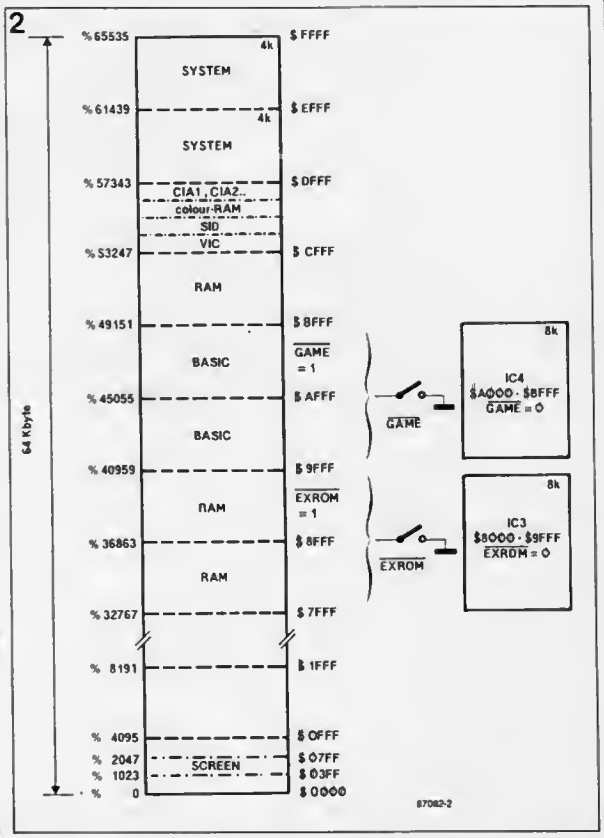


Fig. 2. Essentials of the C64's memory map.

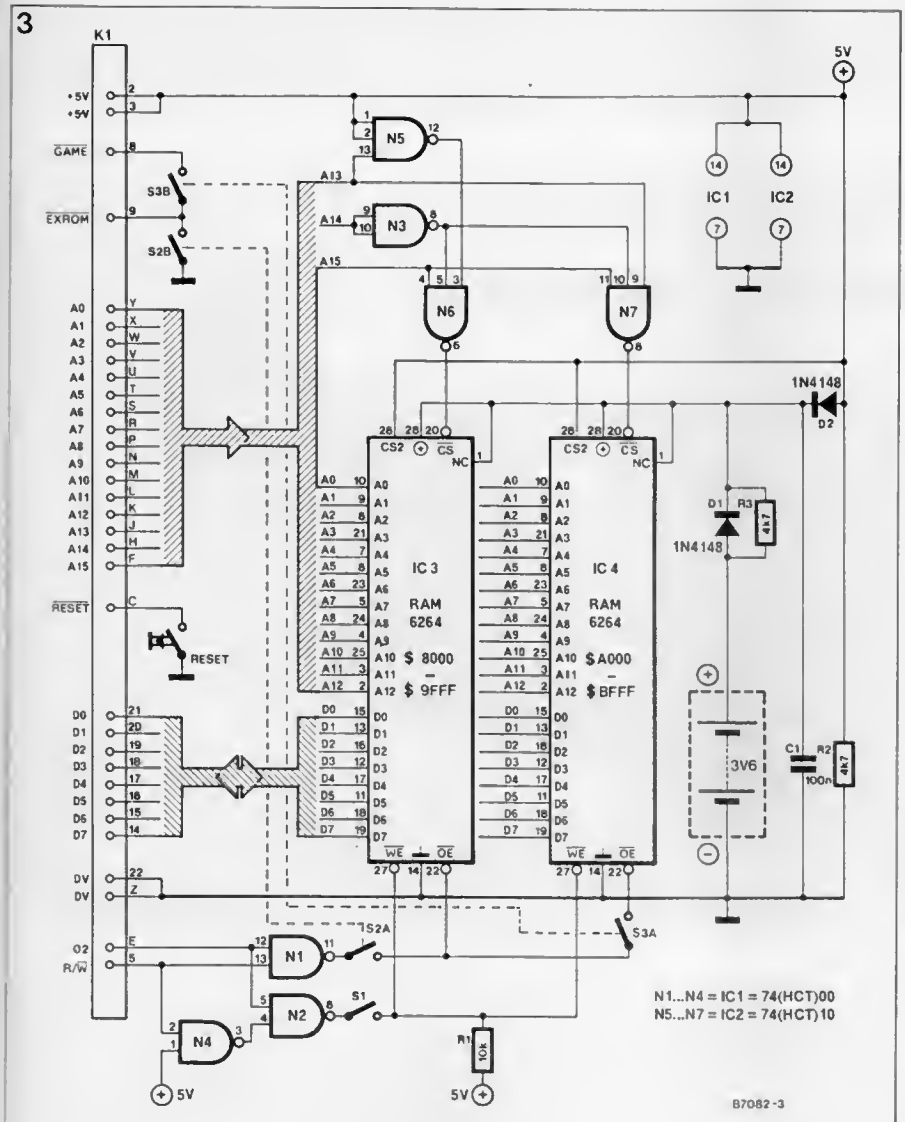


Fig. 3. Circuit diagram of the non-volatile 16 Kbyte RAM module.

Parts list

Resistors (±5%):
R_1 = 10K
R_2;R_3 = 4K7

Capacitor:
C_1 = 100n

Semiconductors:
D_1;D_2 = 1N4148
IC_1 = 74HCT00
IC_2 = 74HCT10
IC_3;IC_4 = 6264 8K x 8 static CMOS RAM

Miscellaneous:
S_1 = miniature SPST switch.
S_2;S_3 = miniature DPDT switch.
S_4 = Digitast momentary action key, Electromail stock no. 337-368.
PCB mount sealed 3.6 V NiCd battery with solder tags, e.g. Maplin order no. RK46A.
PCB Type 87082 (available through the Readers services).

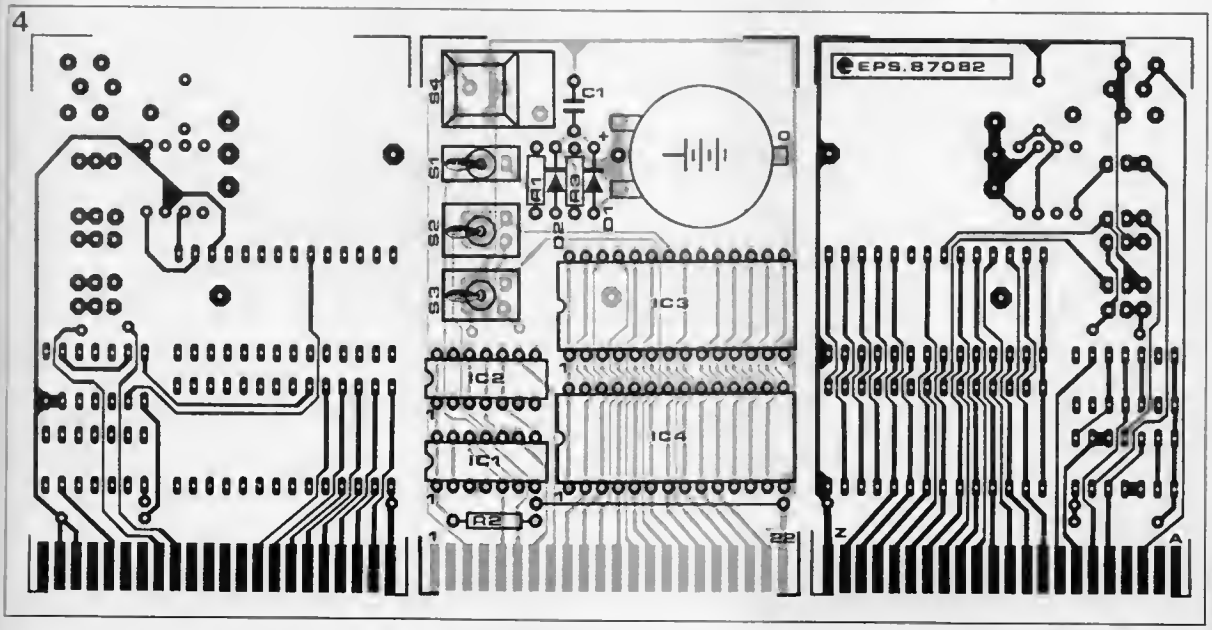


Fig. 4. The printed circuit board for making the RAM module.

Time- Lapse Photography

If you have seen old silent movies having the stars like Buster Keaton and Charly Chaplin, you must have often wondered how they picturised the funny hectic movements of the these stars.

The movie cameras were hand operated in those days and the film making speed could never be maintained steady. When the projector runs at a speed faster than the film making speed, it results into these funny hectic movements. It is exactly the opposite of a film showing a slow motion sequence, where the film making speed has to be much higher than the projection speed.

An amateur movie camera can be easily fitted with a gadget to shoot the fast motion sequences for creating comic effects. If the camera has a socket for accepting remote control release cable, you don't even have to open the camera to make any internal connections.

In case of a super-8 camera, the film-making speed is maintained constant at 18 frames per second. With a simple electronic device described here, it is possible to obtain speeds as low as one frame every four seconds, and a maximum speed of 10 frames per second. When this film is shown with a projector running at normal speed, it results in fast chopped movements of the actors.

Circuit:

The heart of the circuit is the timer IC 555. The timer produces short pulses to activate the relay. These pulses are negative going pulses and allow a current to flow through the relay coil whenever they occur.

As the other end of the relay coil is at 9V, the relay is energised during the period of the pulse, which is approximately 15mS. Such a short duration is selected because we need each pulse just to expose one frame. Potentiometer P1 adjusts the time interval between the pulses, which gives a variable film making speed.

The relay contacts can be connected to the remote control socket of the camera. A reverse biased diode D1 must be connected across the relay coil to protect the IC from the peak voltages of the back EMF produced in the relay coil when the current suddenly falls. D1 becomes forward biased during the occurance of these peak voltages developed across the coil and short circuits them, thus preventing these peaks from damaging the IC.

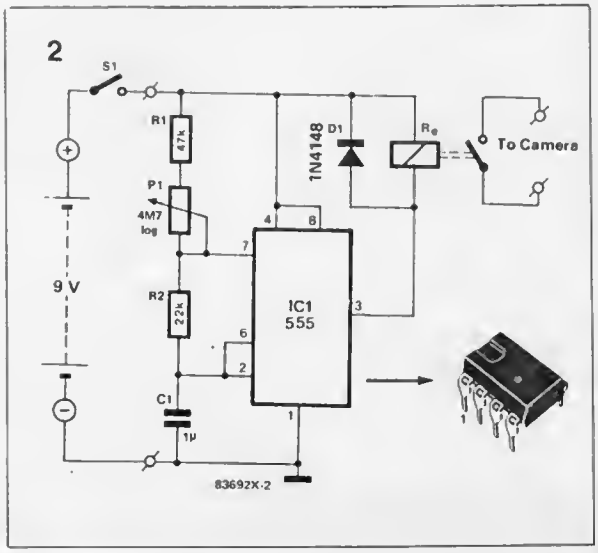
The circuit is supplied by a 9V miniature battery. As we have a 6V relay in the circuit, it is quite likely that the batteries may get exhausted quickly.

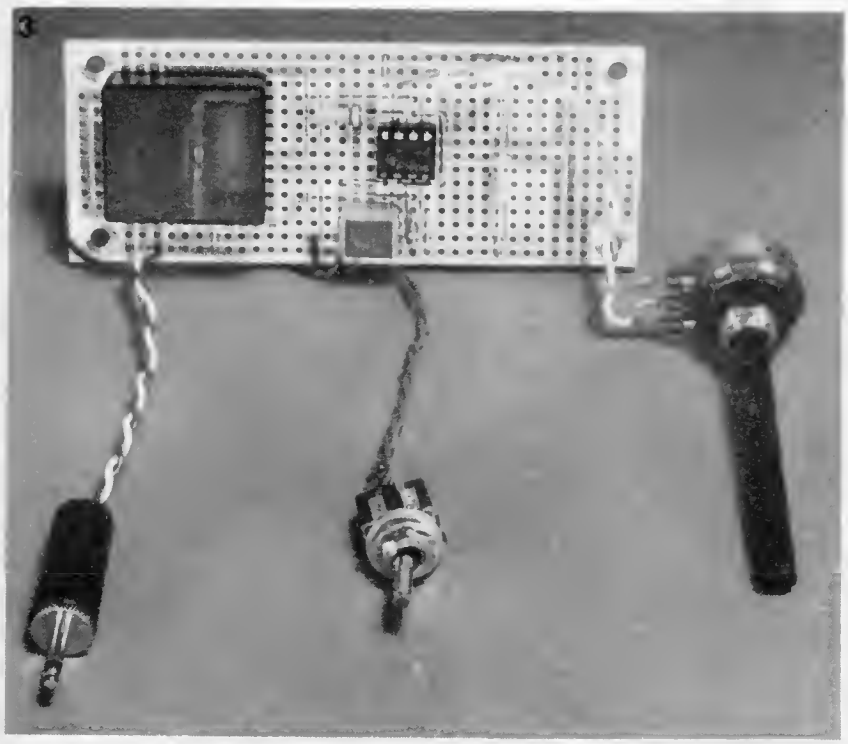
Construction :

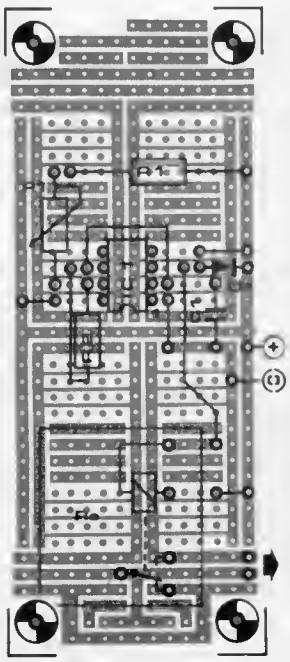
The first step in construction of this project is obtaining a suitable jack

Figure 1 : The time-elapse triggering Circuit enclosed in a standard enclosure.

Figure 2 : The 555 IC timer module is the heart of the circuit.







which correctly fits into the Remote socket of the camera. Mostly the 2.5mm or 3.5mm jack plugs may be suitable. The relay should preferably be a PCB mounting type relay. The coil resistance must be at least 45Ω, because, a lower resistance may overload the IC output.

The IC socket is soldered first, then the jumper wire connections. R1, R2, C1 D1 are soldered next, and finally the relay. The component layout is shown in figure 4. The polarity of diode and orientation of IC pin No. 1 must be carefully maintained. The cathode of the diode points towards may have to be changed depending on the type of relay being used.

Potentiometer P1 and switch S1 and the battery are fitted in the enclosure and connected to the PCB through flexible leads. Only two wires go from the PCB to the potentiometer. Two terminals of the potentiometer are soldered by a jumper wire to each other as shown in figure 5.

If the 4.7 M Ω potentiometer is not available, one can use two 2.2 M Ω potentioneters and connect them in series.

The IC 555 must be inserted into the socket correctly. The pins may have to be bent inwards slightly if the IC is new. The marking notch is towards the relay.

The circuit has been designed around the ordinary 555 IC and CMOS version of the IC should not be used.

After completing the soldering and connections, the operation can be easily checked without connecting the circuit to the camera. Connect the battery and switch on S1. Be careful about the battery polarity, otherwise the IC and diodc is most likely to be damaged.

On switching S1 on, the relay should start making a ticking sound. The rate of ticking must change when P1 is moved. If there is no ticking sound from the relay, check the connections once again.

Now the circuit can be tried out on the camera. Do not load the film into the camera during the first trials. When you are sure that the circuit works properly, you can load the film and start shooting! In case of cameras which require longer start up periods, value of C1 must be increased.

For those readers who do not have access to an amateur movie camera for this project, the circuit will still prove useful as a reference. Additional information on the timer IC 555 is included here for the same purpose.

Timer IC 555

555 is a universal timer IC. Figure 6 shows the internal block diagram enclosed inside the dotted lines. Also

Component List :

R1 = 47KΩ
R2 = 22KΩ
P1 = 4.7 MΩ (Log.)
C1 = 1uF (Foil type)
D1 = 1N4148
ICl = 555
Re = 6V/45Ω Relay with 1 N/O contect.

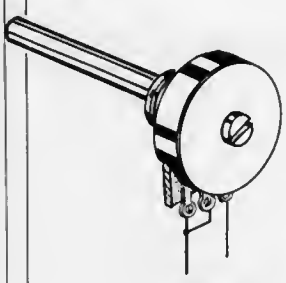
Other perts :

1 9V Battery
1 Battery Clip
1 SELEX PCB (40 x 100 mm)
1 8 Pin DIP Socket
1 Suiteble cesing
1 Knob for potentiometer
1 Suiteble jack for connecting to camera socket.
1 Toggle Switch.

Figure 3 :
Besides battery, Potentiometer end the ON/OFF toggle switch, all other components can be fitted on to one small SELEX PCB of 40 x 100 mm.

Figure 4 :
Component layout of the circuit. Attention must be paid to correct polerities end IC orientetion.

5



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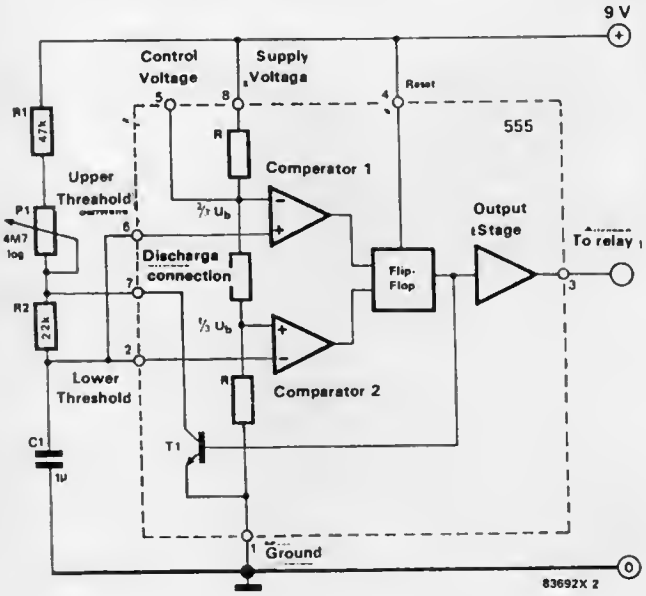


Figure 5 :
Potentiometer with two terminals directly shorted to each other.

Figure 6 :
The internal circuit block diagram of IC 555. The capacitor C1 alternately charges and discharges.

shown for convenience are the main components in the time-lapse circuit.

When the power is applied to the circuit, the capacitor C1 starts changing through R1, R2 and P1. Adjusting P1 modifies the changing current of the capacitor C1 and thus decides the time taken by it to reach full charge. The smaller the value of P1, the faster is the charging. The rise in voltage across C1 is monitored by the two comparators inside the IC. The capacitor voltage is continuously compared with 2/3 and 1/3 of the supply voltage. The reference voltages of 1/3 and 2/3 values are obtained from the supply voltage by the potential divider chain having three equal resistances.

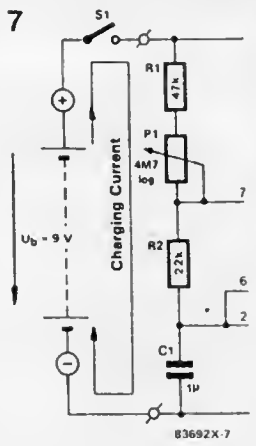
As soon as the capacitor voltage exceeds the value 2/3 Ub, comparator 1 is activated. This sets the flip flop and turns the transistor T1 on. This provides a path for discharging the capacitor C1 through R2 and T1.

When the falling voltage on C1 goes below 1/3 Ub, the comparator 2 is activated and resets the flip flop. As the voltage on base of T1 becomes 0, it is turned off, cutting open the discharging path for C1. It starts charging again through R1, R2 and P1 until, of course, the voltage on C1 reaches 2/3 Ub again. Then the cycle repeats. The flipflop output also drives an inverter at the output of the 555 and gives the output voltage on pin 3. The output at pin 3 thus switches between OV and GV.

The photograph of the CRT screen of an oscilloscope is shown in figure 9 to indicate how the charging and discharging cycles take place. The top curve is the voltage on the capacitor C1 at pin 2 and the lower curve is the voltage on pin 7, that is the collector of T1.

The charging period depends on R1, R2 and P1. Discharging depends only on R2 as R1 & R2 are fixed values, discharging period is fixed — which corresponds to the pulse width. P1 controls the charging period, and in turn, the time interval between two pulses.

7



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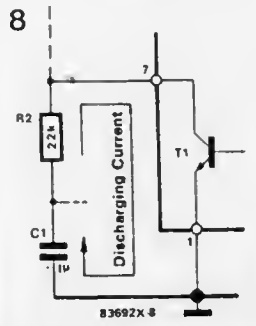

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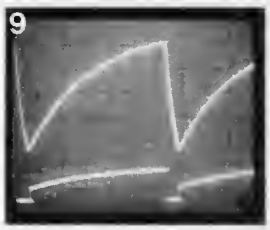

Figure 7 :
The charging cycle

Figure 8 :
The discharging cycle.

Figure 9 :
Waveforms of the capacitor voltage and transistor collector voltege.

Universal Power Supply

A good variable power supply is a basic requirement of every hobby laboratory. It is true that many interesting SELEX circuits can be supplied from dry cells, however, considering the rising cost of these cells, one would rather go in for a good variable power supply. Compare the cost of one Kilowatt Hour power drawn from the mains supply and that of the same power supplied by dry cells and you will immediately realise the importance of having a variable power supply of your own.

The SELEX Universal Power Supply described here, satisfies these requirements. It has two output ranges, one from 2.7 V to 12 V and the other from 10 V to 24 V. The output is short circuit protected. Current limiting is adjustable. These two features are mainly incorporated for preventing accidental damages to the power supply as well as your circuits.

The Circuit

The most important part of the power supply is the integrated voltage regulator L 200, It looks similar to a power transistor-with five terminals! The number of terminals obviously means that there is much more in it. A simplified block diagram of L 200 is shown in figure 1. The regulator is internally protected against electrical and thermal overloads. It is not affected by a short circuit at the output, or by insufficient cooling. The voltage regulation takes place as long as it is ensured that the control input (Pin 4) gets 2.7V. The current limiting sets in when the voltaged between the output (Pin 5) and the current limiting input (Pin 2) exceeds the value of 0.45 Volts. These are inherent electrical properties of the L200 and cannot be altered.

The output voltage has been divided in two ranges, to avoid heay lossess and overheating at low voltages.

If suppose the input voltage is 28V and we need an output voltage of 5V, then somehow the regulator must "destroy" these extra 23 volts. This will result in loss of power as well as overheating. If we have an input of 14V and the output of 5V, then the regulator has to reduce the input only by 9V. By dividing the output into two different ranges the efficiency has been increased and heating is reduced.

The switching over from one range to another is done by switch S2 (figure 4). The effective connection changes inside the circuit are shown in figure 2 and 3.

In the lower range both the transformer windings are connected in parallel and diodes D1 and D3 are in the rectifying circuit. In the higher range the windings are in series and the bridge made of D1, D2, D3, D4 comes into the rectifying circuit, thus doubling the rectified voltage which is fed to the regulator.

The remaining part of the circuit shown in figure 4 serves to adjust the output voltage (P1, R4 .... R9), set the current limiting (P2, T3 etc.) and to give the indication of operation (T1, T2, and the LED D5)

This is how the adjustment of the output voltage takes place: P1 and the resistors R4 ..... R9 form a voltage divider network. The junction of R4 end R6 or R8 and R6 (depending on the range) is connected to the control input of the regulator. The regulator adjusts the output voltage in such a way that voltage at the control input remains constant at 2.7V. The output voltage thus depends upon the setting of potentiometer P1.

The setting of current limiting is somewhat difficult to understand. It becomes effective when voltage difference between pin 2 and 5 of the regulator increases beyond 0.45V.

The voltage present here is equal to the voltege drop over R12 plus the voltage at the sliding contact of potentiometer P2. The constant current source formed using T3 provides for the fact that the value of output voltage does not effect the current limiting function. As the voltege drop ecross R12 depends upon the current drawn by the load and the voltage at pin 2 is derived from a constant current source, the setting of current limiting is independent of the voltage at the output. The green LED D8 has a dual function. It serves for switching control as well as for controlling the constant current source T3.

Transistors T1, T2 and the Red LED D5 are used for fault indication, when output current reaches the limit value that is set for it. In normal condition the voltage on pin 4 is 2.7V, which is greater than the threshold voltage of D6, D7 and base emitter junction of T2. Thus T2 is always conducting. This causes the base of T1 to remain at zero volts and it is always OFF. LED D5 also remains off. But as soon as the voltage on pin 4 reaches about 2V, which is less than the required voltage to keep T2 ON, T2 is turned off and T1 then starts conducting. Red LED D5 glows, indicating a fault condition. Diodes D10 and D11 serve as the protection for the circuit.

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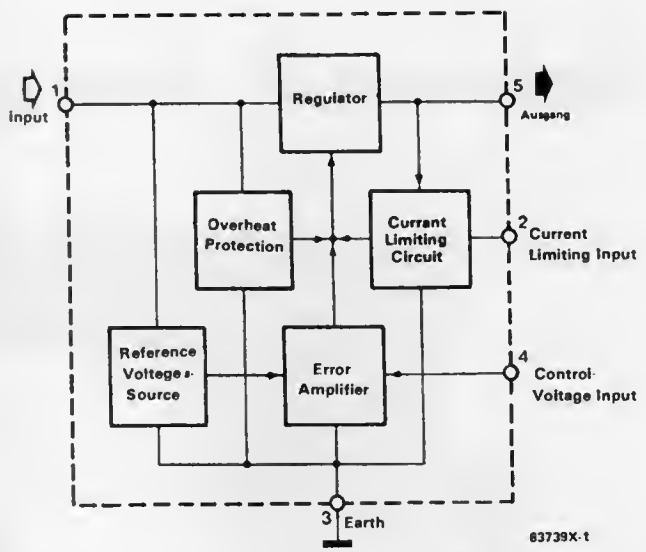
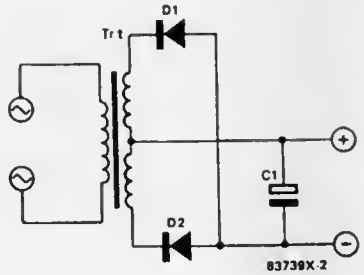


Figure 1:
Voltage regulator IC L200 is the heart of the SELEX-Universal Power Supply. The functions of voltage regulation are also supplamented by protective functions.

Figure 2:
The output voltage is divided in two ranges. In case of low range, the two transformer windings are connected in parallel.

Figure 3:
In the higher voltage range, the transformer windings are connected in series. The rectifier in this case is a bridge rectifier.

2



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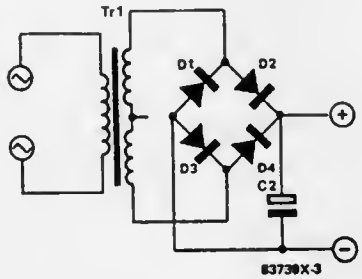
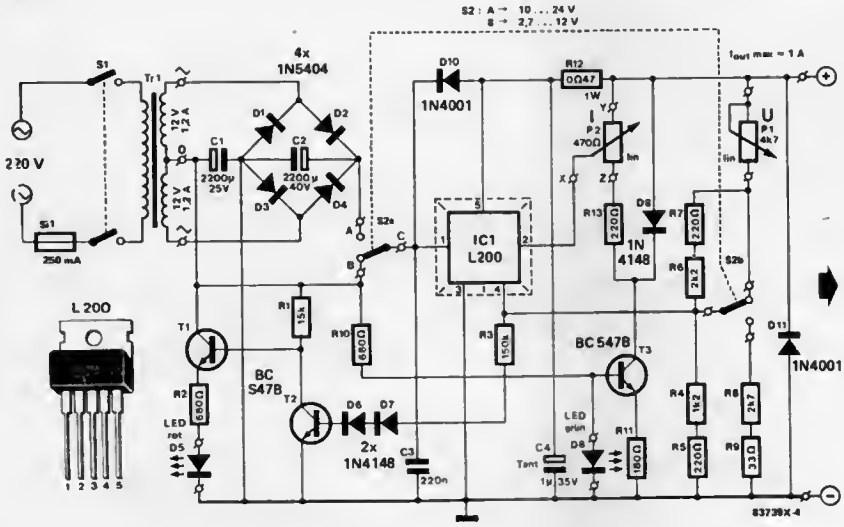




Construction :

SELEX PCB of size 2 (80x100 mm) is required for constructing the component layout of the circuit on the SELEX PCB.

IC1 is the voltage regulator L 200. Conductive paste must be used while mounting the device on the heatsink. It can be mounted on the back panel of the enclosure, and the heatsink can be fitted onto the back panel in such a way that effective cooling takes place. It should be ensured that only thermal conduction takes place, and not electrical, because the cooling fin of the IC is also connected to the earthing pin. No other pin of the IC should ever come in contact with the earthing pin.

Cross section of all conductors which carry the load currents must be at leat 1 mm². The length of these conductors must be kept as small as possible. The same is true for the leads coming from the transformer. The transformer the fuse and the two-pole switch must be placed in such a manner, that the other components of the circuit do not come in

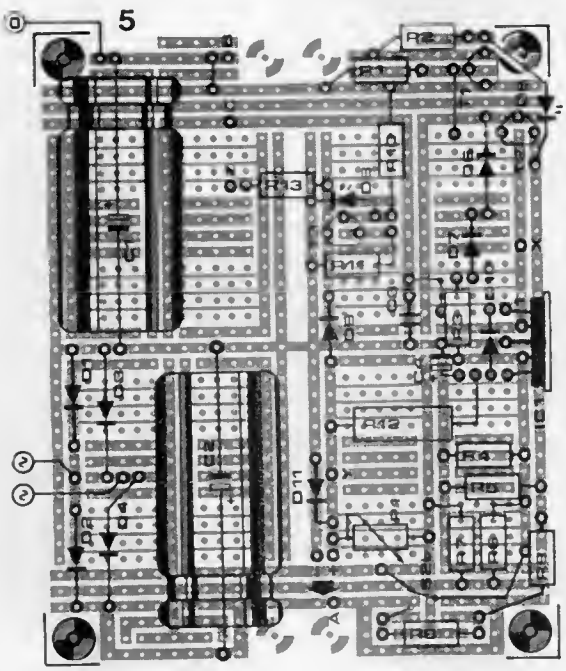


Figura 4:
The circuit of the universal power supply is somewhat complex compared to usual SELEX circuits. The cost also is somewhat higher, but it is worth that much of expenditure, considering the advantage and safety it provides.

Figure 5:
Component layout of the circuit on a SELEX PC8 of size 2 (80 x 100mm). If you follow this layout accurately, nothing can go wrong, in spite of the complex circuit. IC1 must be connected thermally to a heatsink.

Component List:

R1 = 15 KΩ
R2 = 680Ω
R3 = 150Ω
R4 = 1.2KΩ
R5, R7, R13 = 220Ω
R6 = 2.2KΩ
R8 = 2.7 KΩ
R9 = 33Ω
R10 = 680Ω
R11 = 180Ω
R12 = 0.47Ω, 1W
P1 = 4.7KΩ Linear
P2 = 470Ω Linear
C1 = 2200 uF/25V Electrolytic
C2 = 2200 uF/40V Electrolytic
C3 = 220 nF
C4 = 1uF/35V Tantalium

T1, T2, T3 = BC 5478
D1, D2, D3,D4 = 1N 5404
D5 = Red LED
D6, D7, D9 = 1N 4148
D8 = Green LED
D10, D11 = 1N 4001
IC1 = L200

Other parts ;
Transformer = 12-0-12V/1.2A
S1 = DPST Mains Switch
S2 = SPDT Switch, 2A rating.
Heatsink for IC1
Si = 250mA fuse, with holder
1 SELEX PC8, Size 2
(80 x 100mm)

contact with the mains supply. A voltmeter and an ammeter can be used for indicating the output voltage and load current, depending on the budget. Both can be measured with a multimeter and the knobs of patentiometers P1 and P2 can be fitted with calibrated scales on the front panel.

LEDs are fitted with two standard LED holder sockets on the front panel. The enclosure should be of sheet metal, so that cooling can be more efficient. The minus pole of the power supply should not have any connection with the enclosure body.

It is necessary to have the potentiometers and resistors of good quality to achieve the expected performance.

Testing the power supply

If all the components have been soldered correctly as per the component layout the circuit must function correctly after it is switched on. Both the voltage ranges can be confirmed with a multimeter.

Whenever the regulator switches off due to overload, the power supply from mains must be switched off for some time and then restarted.

If the circuit does not function as expected, it can be tested stage by stage with a multimeter. First of all the component layout and interconnections must be checked. The diode and capacitor polarities must be correct. Pin orientation of the IC and transistors must be carefully checked.

It must also be ensured that the cooling fin of the IC is not short circuited with any other pin or with any other component. It must be connected only to the minus pole of the power supply.

Before starting further measurement on the circuit, point C must be disconnected from the pole of switch S2a. By doing this, we have isolated the regulator part of the circuit from the rectifier. Both the LEDs will now glow, when the power is switched on.

The following values should be measured :

- Voltage at each transformer winding : 12 V AC
- Voltage over both windings together : 24 V AC
- Voltage over C1 (Point B to earth) : 18V DC
- Voltage over C2 (Point A to earth) : 36 V DC
- Voltage over both LEDs : 2V

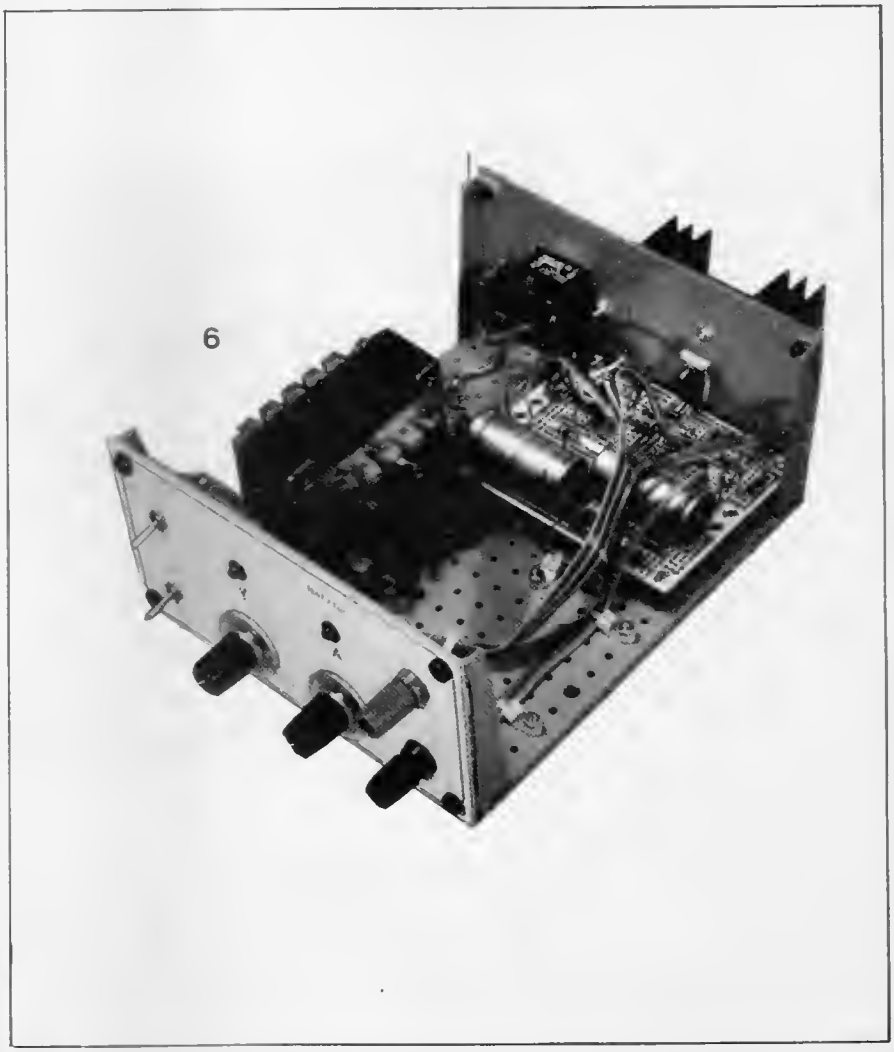
If all these values are correct, it means that the transformer and rectifier part of the circuit is correct.

As the next step, connection between P2 and R13 is desoldered. Now if a multimeter set to 100 mA range is inserted between point B and the collector of T3, it should indicate a current of 13 mA approximately.

The unsoldered connections can now be restored, and following voltages should be measured.

- Voltage between Pin 4 of IC1 and the earth: 2.7V DC, independant of the potentiometer setting. Reduces only when current limiting sets in.
- Voltage between D6 and D7 : 1.2V DC
- Voltage between Base of T3 and earth : 3V DC
- Voltage between emitter of T3 and earth : 2.5V DC Independent of potentiometer setting
- Voltage over D9 : approximately 0.8 V DC.

Any wrong readings during the test procedure indicate that the particular component is either connected wrongly or is defective.



6

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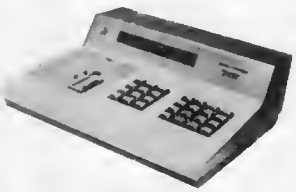

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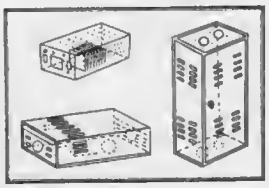

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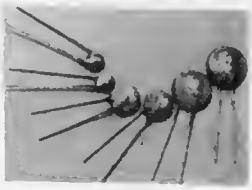

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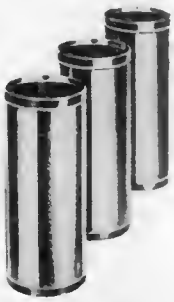

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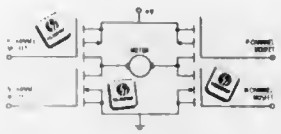

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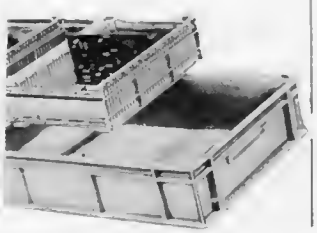
PCB ACCESSORIES

PCB manufacturers in the country can avail of this system for stacking storing and transporting PCBs. Called 'PCB Carrier', the system is manufactured by Nilkamal Crates and Containers. The PCB Carrier consists of grooved plastic panels held firmly by aluminium strips and removable stoppers which plug unused grooves, thus preventing damage. The Carrier can be adjusted, with a simple screwdriver, to fit almost any size of PCB. It is presently available in 4 models in normal & anti-static variety. In the same line the company will shortly introduce a 'PCB Holder' which is a table-top unit for storing PCBs on the assembly line.



For further information please contact:

NILKAMAL CRATES & CONTAINERS
5 Rewa Chambers, First Floor
New Marine Lines
Bombay 400 020.

MARKEM 525 HAND ACTUATED ROTARY OFFSET PRINTER

This is a hand actuated offset printing machine. This is suitable to enhance print quality and productivity on small production runs. This system provides superior print qualities in the rotary offset process for brighter and sharper printing. This machine is suitable for small lots of products—DIP8s, TO·220's, flat packs, chip carriers and general products with at least one flat side. Although cycle speed and through—put are dependent on the operator, production rates of 800—1500 units per hour are attainable.

Specifications:
Print area: 7/8" x 1" (22.2mm x 25.4mm).
Max. part thickness: Variable.
Cycle rate: 800-1500 cycles/hour.
Mount: Bench.
Weight: 30 lb (13.65 kg).

For further information please contact:

M/s. KELLY CORPORATION
1413, Dalamal Tower
Nariman Point
Bombay 400 021.
Telephone No: 244286.
Telex: 11-5858 KELY IN.

TAMAYA DIGITIZING AREA LINE METER

Planix 5000 Area Line Meter Works on a totally new concept developed through unconventional approach leading to unsurpassed performance standards.

The rotary encoder and the state-of-art electronics makes Planix 5000, easiest, fastest area Line Meter. This Meter allows you to measure area and the length of the line. The standard lines are easily measured by simply setting the trace point at each intersection of the figure and the rest is done by the built-in computer with a resolution of 0.05 mm; length of curve line needs to be traced, for measuring.

Planix 5000 is a TOTAL STATION for the draftsman. In addition to its own microprocessor, PLANIX 5000 will interface with the large computer or other RS-232C compatible units. PLANIX 5000 is a compact cordless instrument operating on NiCd Batteries and comes in a carrying case.

For Further details please contact:

TOSHNI-TEK INTERNATIONAL
267 Kilpauk Garden Road
Madras 600 010

SPIKEBUSTER

MAGNUM ELECTRIC COMPANY PVT. LTD. has introduced a voltage spike and noise suppression outlet strip called SPIKEBUSTER. It consists of an EMI/RFI filter and a voltage spike protection circuit built into a power strip with three 5 Amp sockets and a control switch. By plugging SPIKEBUSTER into the electricity mains and your sensitive electronic equipment into SPIKEBUSTER, electrical noise and voltage spikes are totally prevented from reaching the equipment and damaging it or causing it to malfunction. Uses are for colour TV sets, VCRs, computers, computer peripherals, medical equipment, electronic instruments, communication systems and other device containing sensitive integrated circuits. The company specialises in power protection equipment and will soon be coming out with a lowpriced standby battery back-up system aimed at the desktop computer market.

For further information write to:

MAGNUM ELECTRIC COMPANY PVT. LTD'
2 Ramavaram Road
Manapakkam
Madras 600 089

THICKNESS GAUGE

General Tools offer a coating Thickness Gauge. For measurement of a non-magnetic coating on a Magnetic metal.

Application :— Measurement of following nonmagnetic coatings on magnetic metals.

1) Plating—Gold, Copper, Zinc Tin Chromium, Lead etc.
2) Coating—Paint, Resinous coating, Metallic Coating.
3) Lining—Resin, Rubber, Paper or any other films of non-magnetic material can be measured when placed on steel base metal.

For further details contact:

THE GENERAL TOOLS CO.
7, Daulat Mansion
Barrack Road, Behind Metro Cinema, Bombay 400 020

BARREL PUMP (HAND OPERATED) FOR CHEMICALS & OILS

A hand pump, in all plastic construction, namely Polypropylene (PP) and Thermoplastic Polyester (PBT), is introduced for the first time in India. It is ideally suitable for transfer of chemicals and oils from barrels, carbouys, jerry cans, jars etc.

The pump in PP is used for transfer of Acids like Hydrochloric, Sulphuric (Upto 80%) Nitric (Upto 70%), Phosphoric, Acetic, Chromic, Spent Acids etc. It is also used for Inorganic Salt Solutions, Hypochlorite and for Vegetable and Mineral Oils and certain Organic Amines.

The pump in PBT is used for all types of Aldehydes, Ketones, Glycols, Alcohols, Petroleum products and Oils, Acetone and Aniline and their derivatives, Benzene, Toluene, Xylene and their compounds, liquid perfumery products and pesticides, DDB, LAB, Hexane, Liquid Paraffin and other Acetates, Plastcisers, Chlorinated Solvents, Polyols, Isocyanates etc.

In general these pumps are ideally suitable for transfer of liquid chemicals and oils from barrels and carbouys. They offer suction lift of 3 mts, discharge heads of 15mts and capacity of 30 lpm.

They are extensively used at industries like chemicals, textile processing, pharmaceuticals, pesticides formulation, electronics, PCB Mnfg., sugar mills, dye stuff mnfg., etching plants, degreasing plants, research labs., offset presses, installation where oils, kerosene, diesel are used, and all other places where chemicals and oils are handled.

For further information please contact:

CHEMINEERS
6 Jagnath Plot
Rajkot 360 001
Gujarat State, India.

classified ads

CORRECTIONS

Headphone amplifier

Annual '87 September p. 9-45

The Parts list should be amended as follows: $R_6 = 2R7$.

Synthesizer for SW receiver

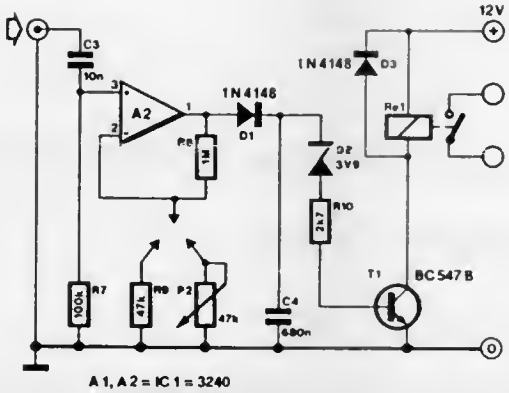
Annual '87 September p. 9-91

The mixer referred to in the 5th line of the text is not described in the Supplement of constructional projects, but forms part of a *Front end for SW receiver*, a project that will be included in *303 Circuits*, a forthcoming book from Elektor Electronics.

Synchronized Slide Changer

Annual '87 September p. 9-109

The circuit diagram given below is left out in the article



A1, A2 = IC 1 = 3240
Re 1 = 12 V, max. 80 mA

87473

Toilet pointer

Annual '87 September p. 9-49

The 6th line of the text should read *proposed toilet pointer may be use–*

Printed Resistors

July 1987 p. 7.31

The unit of resistivity is $\Omega mm^2/m$, not $\Omega/mm^2/m$.

Computerscope

October 1986 p. 10-20

Contrary to the correction given in the June 1987 issue, C_{15} is a 100p capacitor.

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