

elektor

78

October 1981

U.K. 65p

up-to-date electronics for lab and leisure

synthesizer ICs

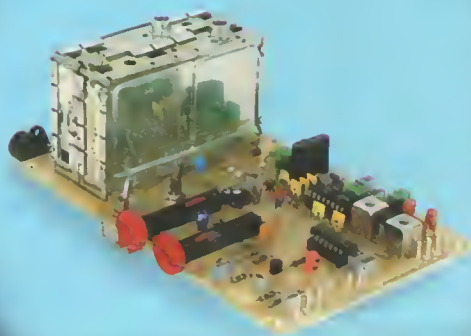
**shutter speed
meter**

**dark room
timer**

**teletext
decoder**

**EPROM
programmer**

Kind's Inf



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EDITOR:
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Summe 81



selektor SELEKTOR

New coinless phones

New public payphones which can be used without cash are coming into operation in London. This further step towards the cashless society is being introduced at major railway and underground stations throughout London. The phones use a special card imprinted with five pence call units. Cardphones will also appear in Birmingham, Glasgow and Manchester in the next few weeks and the cards will be available in those areas as the phones are installed.

To make a call the user inserts the card in the phone and taps out the number being called on a push-button pad. As the call progresses the call units on the card reduce. A digital readout on the phone continually tells the user how many units are left. At the end of the call the card is returned for future use. It will still be possible to make '999' calls free of charge without inserting a card.

As well as being used for inland calls, the Cardphones can be used to ring all countries on international direct dialling, which now numbers more than 100 countries including Australia, New Zealand, Canada and the USA.

Cardphones have a number of attractions. There is no need to worry about having enough change. There is no need to keep feeding the phone with coins when making international or long distance calls. It is hoped that the absence of cash will make the phones less attractive to thieves and less likely to be vandalised. And there is no costly collection of money. About 200 Cardphones are being installed for the trial and if the public takes to them more will be introduced.

A special card — the size and shape of a credit card — is needed to use the phone. These cards can be obtained from post offices and a number of retail outlets, such as railway station bookstalls and Travellers-Fare kiosks. There are two values of card, one of 40 units costing £2 and a 200 unit card at £10. The units are imprinted in strips on the card using holographic technology based on special patterns of light. This offers maximum security against fraud and forgery. Since this process has a whole range of exceptional properties it prevents copying or modifying the card.

The unit value, holographically memorised on the card, is shown on a visual display on the front of the phone cabinet when the card is inserted. Throughout the call, the Cardphone continuously calculates the units used and reduces the value of the card at the rate of the incoming metering pulses — erasing units



by a thermal process. The amount shown on visual display decreases as the call progresses and units are erased. The rate at which units are used up will depend on the distance of the call (ie whether it is local, trunk or international) and the time of day. Twenty seconds before the units on the card run out, the visual display starts flashing and the caller hears a warning tone in the receiver. The call in progress is undisturbed by the warning signal.

If the caller wishes to continue the call, he, or she, can press a button on the cabinet. This automatically removes the remaining units from the card, stores them, returns the exhausted card and allows the caller to insert another card.

The 200 unit card has two imprinted strips and contains 100 units on each side. When the first side is used up and the warning activated, the same method can be used to return the card so that the second side can be used.

When a call is ended and the handset replaced, charging for the call stops immediately and the card is returned after a few seconds with any units remaining. If, after making one call, the phone user wishes to make another call, it is sufficient to tap and release the handset rest. This clears the line for the next call without returning the card.

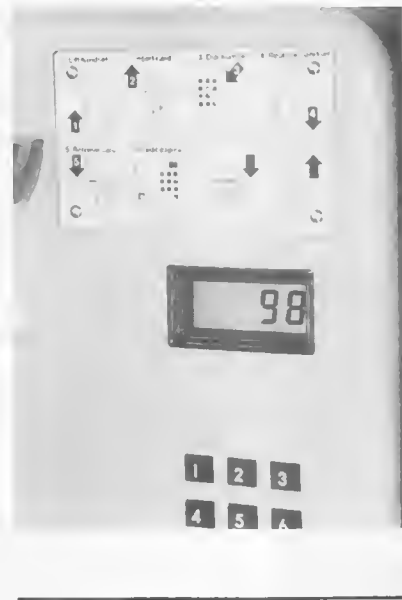
If it is required to know the number of units remaining on a card without making a call, this can be found out by inserting the card without lifting the receiver. The card's unit value will then be shown on the visual display.

The steps in making a call are:

- Lift receiver
- Insert card
- Key telephone number on push-button pad
- Make call
- Replace receiver
- Retrieve card with remaining units

The Cardphone is micro-processor controlled and is programmed so that certain service numbers — such as directory enquiries and '999' emergency calls — can still be obtained free of charge.

British Telecom



(706 S)

selektor SELEKTOR

Although a description of the circuit was published last month, it requires minor modifications for the printed circuit board described in this article. A LED level display using the well known UAA 170 has far more applications than the thermometer and barometer referred to in the previous article. In many instances, an indication of a level is preferable to an exact and precise reading. With a display of 16 LEDs, the circuit now provides an easily read indicator that will prove excellent for a great many purposes. The 3 ICs, the LEDs and a few other components are all mounted on a printed circuit board that measures just 37 x 82 mm, small enough to be used practically anywhere.

When a certain voltage is to be measured with a meter, one of two extreme cases can occur:

1. The voltage may be too high for the range of the meter. A voltage divider consisting of two resistors will remedy the situation.
2. The voltage is too low. In this case, since the range is not fully used, the voltage has to be linearly amplified. Due to the input series-resistor to feedback resistor ratio, the amplification factor of an inverting opamp can be determined with accuracy. The inverting effect of the circuit can be cancelled by adding a second, inverting stage. Another advantage is that the inverting opamp with feedback can also act as an adder, that is another fixed voltage can be added to the input signal being measured. This is necessary if the input voltage level has an offset voltage superimposed on it. Let's take an example. A voltage varying between 8 and 10 V is

universal LED display

including automatic offset and scale adjustment

Another LED display . . . ??!

Before jumping to the conclusion that our designers are being LED astray allow us to explain why a different version of the LED display published last month was considered necessary. Voltage monitoring is not always a simple matter for the meter must be adapted to the voltage levels being measured. The circuit now contains a 'front end' consisting of three opamps in order to eliminate the problems of offset voltage levels and to modify the measuring and display ranges. This will enable the circuit to be used for a variety of applications and not just for the weather station as described in the September issue.

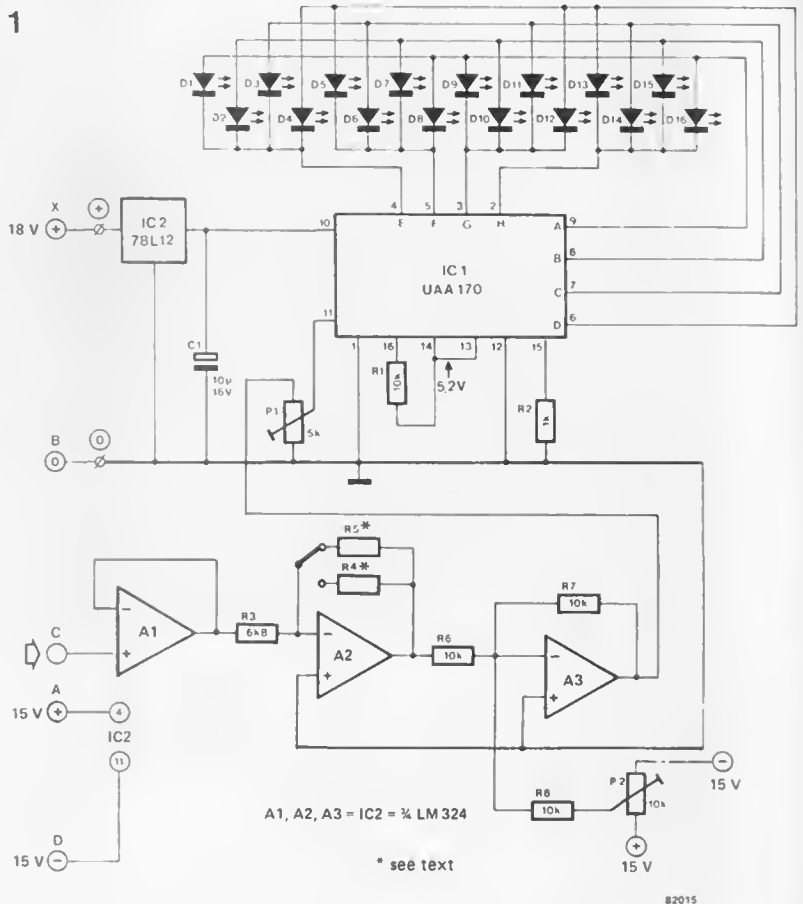


Figure 1. The circuit diagram of the LED display. Thanks to the offset and scale adjustments, the meter has the advantage that improved resolution is possible.

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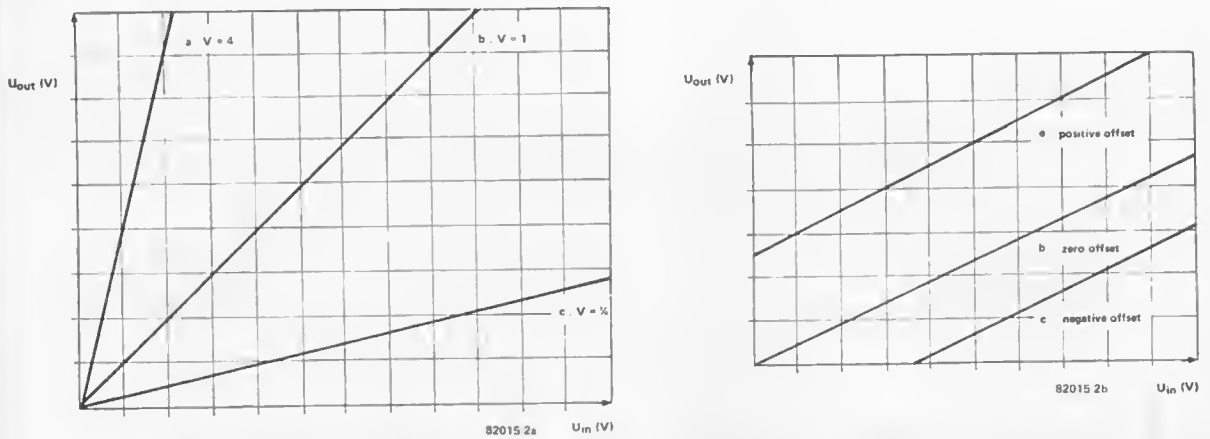


Figure 2. The input to output voltage ratio is fixed. Figure 2a shows the amplification factors with different values for R5. Figure 2b gives various offset levels in relation to the setting of P2.

3

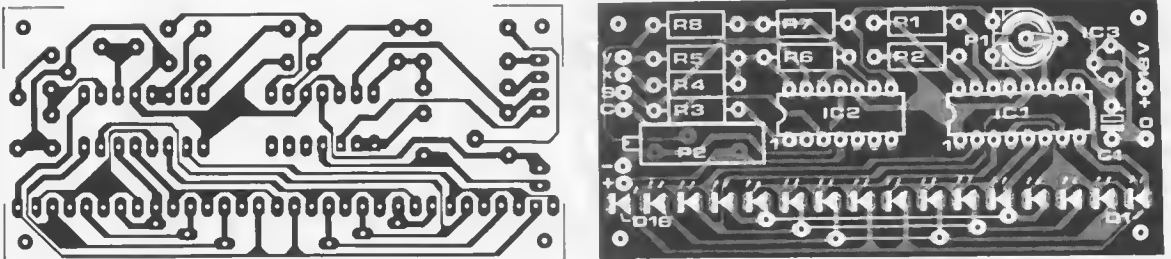


Figure 3. The component overlay and track pattern of the printed circuit board for the universal LED meter.

to be measured. If a meter is used with a range of 0... 10 V, only 20% of the display range will be used. But a 0... 2 V range would lead to an overrange, since the lowest voltage is 8 V. The answer to this is to offset the display range by 8 V by 'adding' a *negative* 8 volts. This method is frequently used in offset and scale adjustments. Figure 2 shows the relationship between various input and output voltages inside the circuit formed by A2 and A3.

The resistor values shown are relevant when the circuit is used for the temperature or humidity display. To display temperature values, connect R5 in the feedback loop of A2 (R5 = 270 k). In the case of humidity indications, only R4 (47 k) needs to be in circuit. A single pole switch as shown can be used here. The total amplification can be calculated as follows:

$$\frac{R5}{R3} \cdot \frac{R7}{R6} = V$$

The amplification factor should be sufficiently high to bring the upper input voltage level to 5,2 V. The required factor is found by dividing the U_{output} by the U_{input} . Since $R6 = R7$, this ratio can be related to R3 and R5:

$$\frac{R5}{R3} = \frac{5 \cdot 2}{U_{in}} = V$$

To avoid problems, choose a slightly greater value than strictly necessary. P1 can readjust it later. P2 helps compensate the offset for temperature problems. The impedance converter A1 ensures that the circuit has a high impedance input.

Testing and calibrating the circuit

Testing the circuit is very straightforward. The input at point C is earthed and P1 is set with its wiper to the input of A3. If P2 is now turned to the negative supply the LEDs should switch on in sequence. When D16 lights P1 can be turned back and the LEDs will 'drop down' the row. Return both P1 and P2 to the original settings and carry out the same check with a positive DC voltage at the input.

If the display is to be used as a voltmeter, readers are recommended to use one LED for each decimal unit (ranges of 0.16 V, 1.6 V or 16 V in other words).

- For a 0... 0.16 V range, R5a = 270 k
- For a 0... 1.6 V range, R5b = 27 k
- For a 0... 16 V range, R5c = 2k7

Parts list

- Resistors:**
 R1, R6, R7, R8 = 10 k
 R2 = 1 k
 R3 = 6k8
 R4 = 47 k
 R5 = 270 k
 P1 = 5 k-Trimmed
 P2 = 10 k-Trimmed

- Capacitors:**
 C1 = 10 µ/16 V

- Semiconductors:**
 D1... D16 = LED
 IC1 = UAA 170
 IC2 = A1... A3 = 1/4 LM 324
 IC3 = 78L12

- Miscellaneous:**
 1 SPDT switch

To calibrate the circuit, connect 0.1 V, 1 V or 10 V to the input and adjust P1 until the tenth LED (D16) just lights. The voltage at the wiper of P2 should be exactly 0 V. If the circuit is to be used for other than the barometer display, the input of IC2 (point X) is linked to point A. The supply voltage in this case will then only be 15 V.

In recent years some amazing electronic steps have been taken in the field of photography. Modern cameras are crammed with all sorts of electronic components and chips, providing automatic exposure control, shutter speed control, etc. In fact our electronic 'brother' keeps such a close check on every photographic enterprise that it has become almost impossible to 'goof up' the shot.

The fitting of electronic devices inside a camera is well beyond the powers of any electronics enthusiast, however keen. Apart from that, any photographer is aware of the great risk involved in 'fiddling around'. The modern camera is very much 'state of the art' both electronically and mechanically

highly suitable for this particular purpose. This is an extremely versatile IC and we have used it before in circuits such as the mini counter and the revolution counter (published last month). As many readers will have guessed by now, it is the well known MK 50398N. This IC contains a six digit BCD counter (counts both up and down), a latch, a BCD-to-seven segment decoder and all the electronics required to control the display.

The MK 50398N is at the heart of the circuit diagram shown in figure 1. Above it are the six LED displays (LD1...LD6) which are common cathode types.

In addition, a timebase is needed to provide the counter in IC1 with a clock

shutter speed meter

For various reasons electronics and photography are hobbies that can often go hand in hand. This is not surprising, considering the number of electronic circuits that can be put to use in photography. In any case, many electronics experts and enthusiasts are also keen photographers. In the past Elektor has published circuits that were primarily designed to facilitate the development process, such as dark room timers (a version of which is included elsewhere in this issue) and exposure meters. On this occasion, however, our designers felt it was high time attention was devoted to photographic measurement techniques. After all, the camera has to be able to take a good picture before it can be developed into a reasonable slide or photograph. Shutter speed is critical but it can differ from the indicated figure by a fairly large margin, especially on the cheaper camera. Bearing this in mind, a shutter speed meter with a digital readout would be a very useful accessory.

and merely loosening a few screws is likely to send thousands of expensive, microscopically tiny parts flying. Even if you were lucky enough to find everything, you'd have to send the whole lot to the dealer's and then pray they manage to put the camera together again.

Fortunately, there are quite a few electronic circuits which are not too difficult to build and which are of great help in photography. Usually, for instance, the camera's operation is not so easy to monitor. All the photographer can do is check whether the shutter is working and whether the diaphragm is still opening and closing, and that's about it. Well, the diaphragm shouldn't give too many problems in practice, but if the camera is several years old the shutter speed may have lost some of its precision. Slowing down the shutter speed will of course cause every photo to be over-exposed. The shutter is a very complicated and delicate mechanism which is easily affected by dropping or knocking the camera. No amount of quartz can remedy such carelessness!

The shutter speed meter described here enables the actual period for which the shutter is open to be measured very accurately. The photographer can then decide whether or not the shutter is still working properly and, if it isn't, take it to the dealer's for repair.

The circuit diagram

In order to measure the shutter speed, the camera itself, ironically enough, can be used; for while the shutter is open light through the lens falls onto the light-sensitive film. By placing a photo diode or photo transistor behind the lens the exposure time can be measured with the aid of an electronic measuring circuit.

An IC is currently available which is

frequency. This is done by a crystal oscillator (N7, R4, C1, C2 and of course a crystal) which produces a very stable 1 MHz frequency. After passing through the Schmitt trigger N8 and the divide-by-ten IC2, a frequency of 100 kHz is left to feed the clock input of IC1. Furthermore, IC1 has a count inhibit input (pin 26). A logic one at this input causes the counter to be disabled. If, on the other hand, it is pulled low, the contents of the counter are incremented by one after every ten microseconds.

The count inhibit input in this case is used to enable the counter for the time period that the photo transistor is illuminated for. The photo transistor T1 is connected between the positive of the supply voltage and the input of Schmitt trigger N9 which is also an inverter. When lights falls onto T1 it will start to conduct. The input of N9 will then become logic one and the output of N9 will be logic zero, so that the counter inside IC1 is enabled. With the aid of resistors R1 and R2, T1 is set so that it will only react to a considerable amount of light.

The counter's contents, as shown on the displays, now indicates the shutter speed in microseconds when the photo transistor is placed behind the shutter and a light bulb is situated in front of the lens. If, for instance, the figure 100 appears on the display, this corresponds to a duration of 1 ms. In photographic terms this means the shutter time is exactly 1/1000 s. Now a method has to be found to reset the counter after every measurement. This is done with the push button S2 which connects the clear input of IC1 to the supply voltage. Seeing as chips form an essential part of the electronic diet these days, the power supply consists of an integrated voltage regulator (7812) and such nutritious ingredients as a transformer, a bridge rectifier and one or two capacitors.

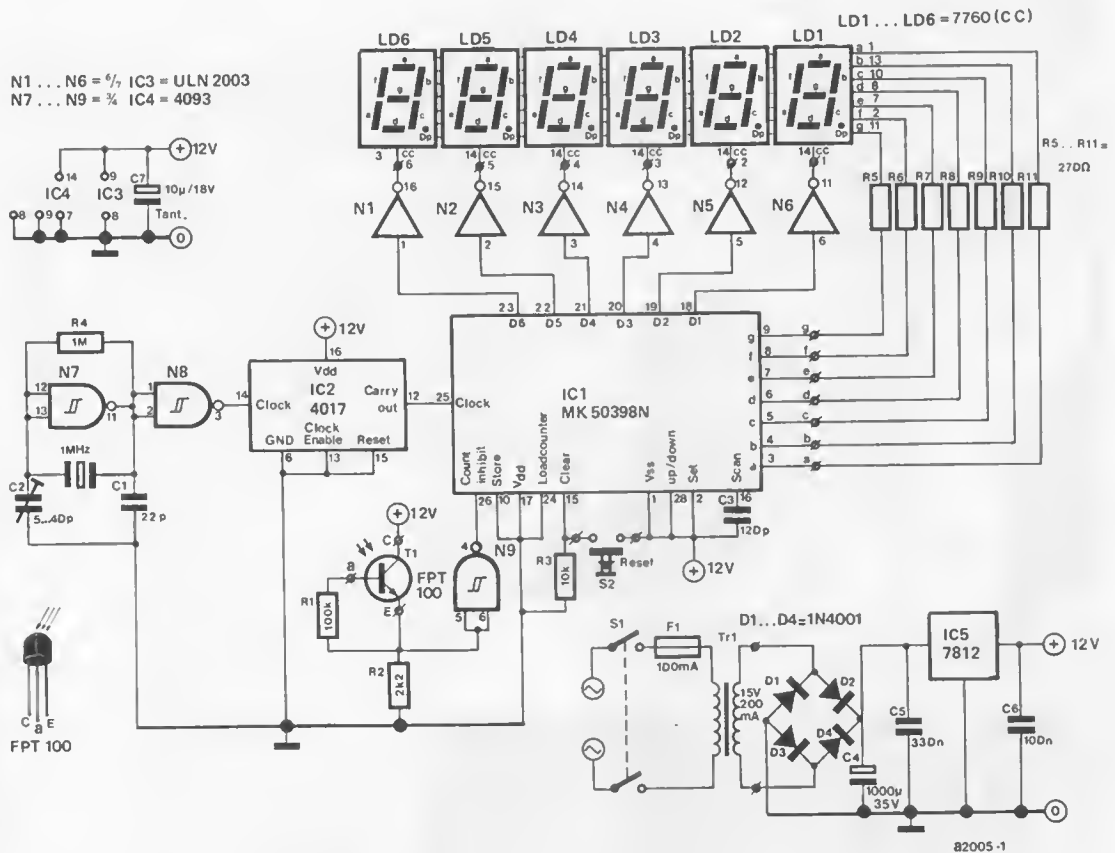


Figure 1. The shutter speed meter circuit diagram. Nearly all the required functions are carried out in IC1, an MK50398N IC. A crystal oscillator acts as a stable reference timebase.

Construction

The printed circuit board on which the whole circuit is mounted is shown in figure 2. It is laid out in two sections, one for the displays and the other for the rest of the circuit. The two sections are carefully separated with the aid of a fine saw, after which the components can be mounted. IC sockets are definitely recommended to avoid any damage being done to the ICs. IC5 can be soldered straight onto the board and does not require a heat sink, provided the secondary transformer voltage does not exceed 15 V. The two boards are then linked together with lengths of wire (connections 1...6 and a...g) so that the boards are at right angles to each other. A piece of red Perspex can be placed in front of the displays to improve legibility.

After this the reset key, the photo

transistor and the transformer can be linked to the board. The wires connected to the photo transistor should not be longer than 20 cm. The oscillator can be calibrated with the aid of the trimmer capacitor C2. This will require an accurate frequency meter which is linked to the output of N8. The frequency is then regulated to exactly 1 MHz. However, readers who do not own such a frequency meter should set C2 at three quarters of its maximum capacity and the frequency will then be sufficiently accurate as well.

Figure 3a gives an idea of what a case for the shutter meter could look like. It will house the two boards, the transformer, the mains fuse and the mains switch. The displays are shown at the top of the drawing with the reset switch above them. The top of the case should be covered with a layer of foam

rubber large enough to cover the back of the camera body. A hole is made in the middle of the foam rubber in which the photo transistor is inserted. The transistor should be level with the foam rubber, so that the camera can be placed on the shutter speed meter without being damaged and, at the same time, the layer of foam rubber prevents stray light from entering.

Using the meter

In addition to the meter and camera we need a desk lamp with a 60...75 W light bulb in it. The meter is placed on a table and the rear side of the camera is opened or, if possible, removed altogether. The camera is then placed on the foam rubber with the photo transistor exactly in line with the centre of the lens. In the case of mirror reflex cameras, make sure that the foam

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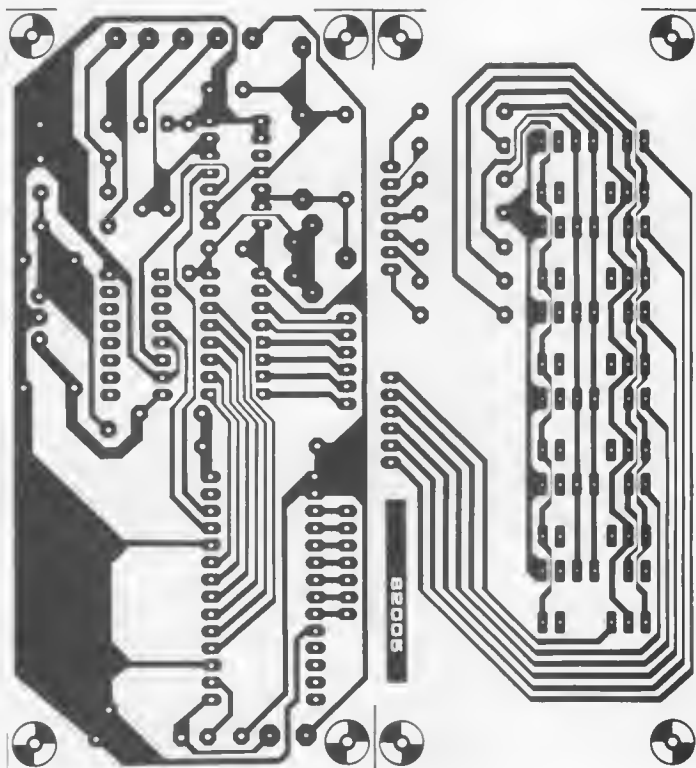
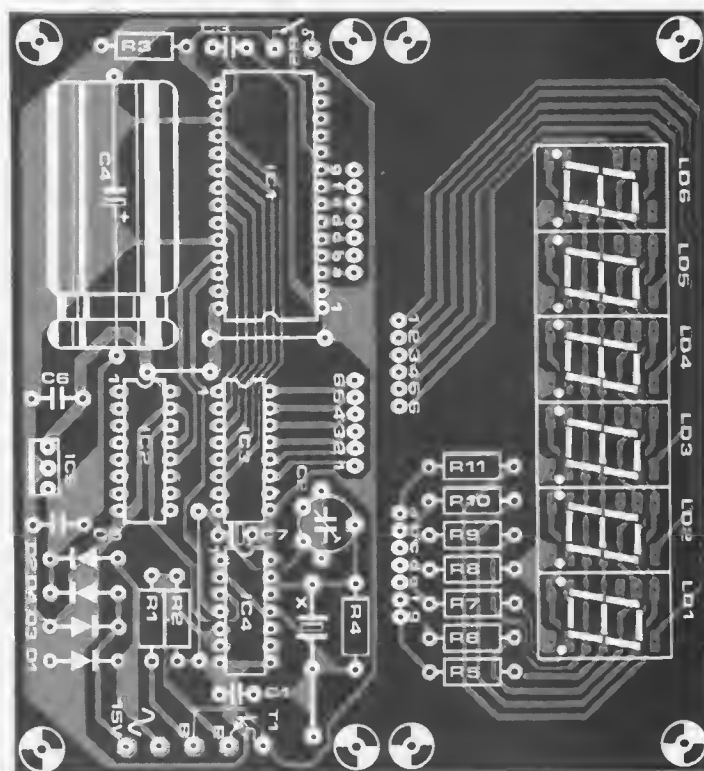


Table 1.

Shutter speed (s)	display reading
1/1000	100
1/500	200
1/250	400
1/125	800
1/100	1000
1/60	1666
1/50	2000
1/30	3333
1/25	4000
1/15	6666
1/10	10.000
1/8	12.500
1/4	25.000
1/2	50.000
1	100.000



Parts List

Resistors:

R1 = 100 k
 R2 = 2k2
 R3 = 10 k
 R4 = 1 M
 R5 ... R11 = 270 Ω

Capacitors:

C1 = 22 p
 C2 = 4 ... 44 p trimmer
 C3 = 120 p
 C4 = 1000 μ/35 V
 C5 = 330 n
 C6 = 100 n
 C7 = 10 μ/16 V tantalum

Semiconductors:

D1 ... D4 = 1N4001
 LD1 ... LD6 = 7760 (common cathode)
 T1 = photo transistor FPT 100 or similar
 IC1 = MK 50398
 IC2 = 4017
 IC3 = ULN 2003
 IC4 = 4093
 IC5 = 7812

Miscellaneous:

Tr1 = 15 V, 200 mA transformer
 X = 1 MHz crystal
 F1 = 100 mA slow blow fuse
 S1 = DP mains switch
 S2 = push button switch

Figure 2. The two printed circuit boards involved in the meter. These have to be separated before any components are mounted.

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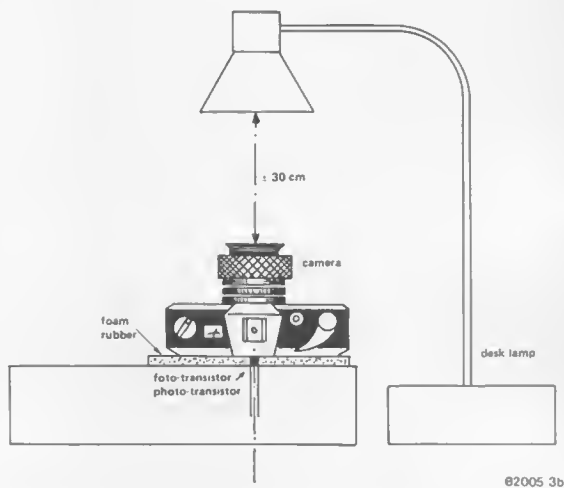
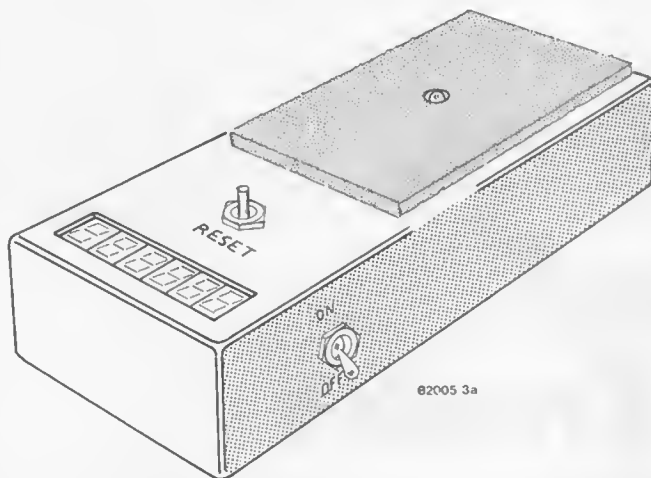


Figure 3. Drawing a illustrates the case of the shutter speed meter. The top is covered in a thin layer of foam rubber to protect the camera and screen the photo transistor against stray light. Drawing b shows the positions of the camera, the case and the lamp when checking the shutter speed.

rubber and/or photo transistor does (do) not come into contact with the mirror, as this is both detrimental to the mirror and to the result of the measurement. In any case; it should be locked up if possible.

The lamp is placed at about 30 cm in front of the lens and is then switched on. Figure 3b illustrates this. The shutter speed button is turned to the required speed, the distance is set on infinite, the diaphragm is fully opened, the shutter is cocked and the meter is reset. The meter's display will then indicate zero. After pressing the shutter button, the shutter speed will appear on the display. If the display continues to

show zero, it will be necessary to move the photo transistor and the lamp around a little. As we mentioned before, the reading will be in tens of microseconds. This means the result will have to be converted into the normal form of shutter speed indication. Table 1 shows the display reading at various common speed levels. If the reading is to be converted in terms of $1/x$, x will represent $10^5/\text{reading}$. The device's measuring range extends from $1/1000$ s to 10 s.

In the case of mechanical shutters it is almost impossible to obtain precisely the same shutter speed at every measurement. The result is bound to fluctuate

slightly. The best solution is simply to calculate the average by measuring the same shutter speed ten times. The reset key is only pressed for the first measurement. After the procedure has been repeated ten times, the final reading is divided by ten and then compared to the table or applied to the formula given above. This gives the average result.

With respect to the values measured, these will never be absolutely accurate, as this just is not possible in practice. So don't worry if the result misses the mark a little. Most photographers are delighted if the shutter speeds are within about 10% of the ideal values. Even a value within 20% is still a satisfactory result and a difference of 30% should not affect the exposure times in practice.

The shutter speed meter is an accurate device and, provided it is used sensibly, will prove to be worth its weight in gold (or at least, film)! M

missing link

Infocard 13 (Elektor 72)

The package for the TL 074 and TL 084 ICs is indicated as IV; this should be V.

Infocard 21 (Elektor 74)

In the tone and frequency table F octave 2 should be 87.3071.

70 cm transverter (1) (Elektor 74)

In figura 6 the pin assignment for the inputs and outputs of IC1 are the wrong way around: 2 should be to the left and 1 to the right. This is correct on the component overlay and the printed circuit board.

LED audio level meter

(Summer Circuits Issue '81, no. 23)

The text mentions an LM3819 IC. This should be LM3915.

scoreboard

(Summer Circuits Issue '81, no. 1)

The mains connection which is directly connected to the triacs also has to be linked to the ground of the rest of the circuit. If triacs are used, IC4 = IC5 = 74248.

TV games extended

(Elektor 77, p. 9-22)

To obtain a good amplitude balance between PVI tone and PSG explosion, it has proved better to modify three resistor values:

R9: was 4k7, becomes 1k5

R11, R18: was 4k7, becomes 2k2

Most fridges are based on the straightforward principle of compressing and evaporating a volatile liquid (Freon). An electric motor drives a compressor which compresses the Freon into a liquid. During the process heat is produced which escapes into the environment through a radiator (usually at the back of the fridge). The liquid Freon is fed to the cooling plates in the fridge where it is evaporated (into a gas) and in doing so causes heat to be extracted from the inside of the fridge (and therefore from the products stored as well).

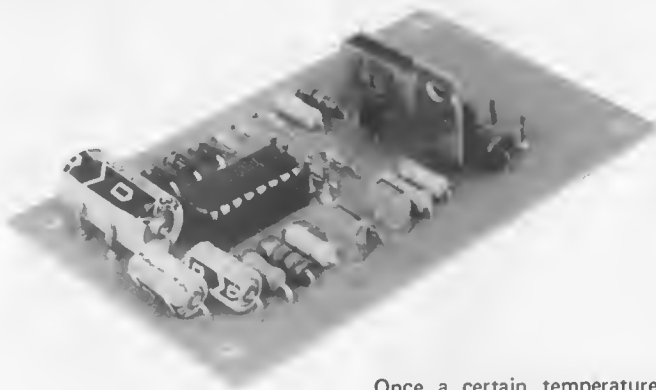
for longer periods and therefore consume more energy. This ends up costing more than the actual products being stored are worth! The remedy is to stop the cooling process whenever the cooler is covered in a thin layer of ice. This can be done by unplugging the fridge. When the ice has melted the water can be removed and the fridge will start operating more efficiently again.

A simpler solution is to provide the fridge with a semi-automatic defrosting unit. The fridge is switched off by pressing the (usually red) button pro-

economical fridge defroster

takes the ice out of the energy price!

Many fridges nowadays are equipped with an automatic defrosting unit to prevent the cooler from icing up. A thick layer of ice will affect operation and raise the electricity bill considerably. This can be remedied by defrosting the unit periodically. The trouble is, automatic defrosting units also consume quite a lot of current and what is more they produce a fair amount of heat which adds to the fridge's energy intake. An electronic fridge defroster, on the hand, manages to do the same work at a lower energy cost.



Once a certain temperature has been reached the motor is switched off by a thermostat. After a time, depending on how well the fridge is insulated and the size of its internal surface area (not its volume!) and on the difference in temperature between the internal fridge temperature and that of the room, the temperature will have risen to such an extent that the thermostat switches the motor on again. More often than not the cooling plates enclose a small ice box in which frozen products may be stored. Whenever the door is opened a certain amount of warm air outside will flow into the fridge and cause condensation in the cooler interior. As a result, a thick layer of ice will eventually form in the ice box and so make it more difficult for heat transfer to take place. Consequently, the motor will operate

vided. When the ice has melted on the cooling plates the fridge is switched on again automatically.

The modern defrosting units with which many fridges are equipped nowadays are fully automatic and so make life very easy. The snag is, such luxury ends up putting up the energy bill as well! A vicious circle . . . What happens is that whenever the thermostat switches off the motor, a heating unit (10 . . . 25 W) is switched on thereby heating the cooler and melting the ice. The water produced is led out to a special container outside the fridge. Thus, after every cooling phase the cooler is defrosted. The heating element not only consumes quite a lot of current, but the heat it produces will have to be removed too, which again requires energy. In the end it may be discovered that it is much cheaper to switch off the automatic unit altogether, as it defeats its purpose! Nevertheless, fridges need to be defrosted from time to time. An economical method is to provide the heating unit with a manual switch. In practice, the cooler can be kept in an optimum condition by defrosting it for about half an hour a day. In some respects, how-

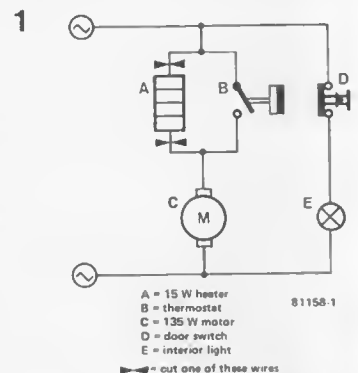


Figure 1. If the circuit of the electrical system in your fridge looks like this, it is all right to use this economical defroster circuit.

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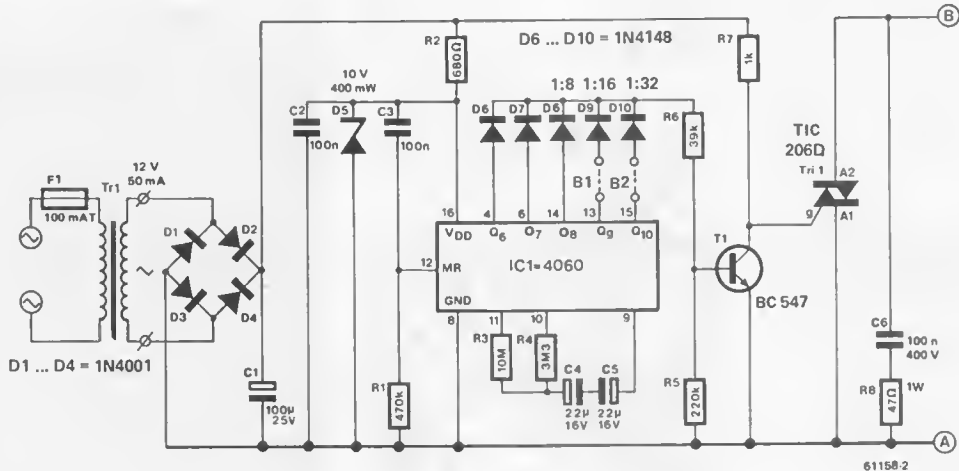


Figure 2. The circuit diagram for the defrosting unit. With the aid of a timer (IC1) the defrosting system is operated for one hour at 7, 15 or 31 hour intervals.

ever, this brings us back to square one, for we now have to remember to do this every day, which can be quite a bind. Fortunately electronics has got the answer: add a circuit which switches on the defrosting unit for one hour every 7, 15 or 31 hours, according to choice.

Before readers jump in at the deep end and grab their soldering irons, it is advisable to check whether their fridge does indeed have a fully automatic defrosting system with a heating unit that is connected in parallel to the thermostat. (This is usually the case in fridges that have a built-in ice box). In other words, the electrical system in your fridge should correspond to the one in figure 1. When the thermostat switches off, the heating unit will be in series with the (low-impedance) motor. The current passing through the heating unit is too low to drive the motor, but produces enough heat to melt the ice on the cooler.

Readers who do not have a drawing of their fridge's electrical system had

better use an ohmmeter (the heating unit and the wire connections are often well hidden). Plug in to mains. Wait until the motor stops and then pull the plug out. If the meter does not measure any resistance between live and neutral, you can be sure that the circuit diagram described here is not suitable for your type of fridge. This also refers to semi-automatic fridges for such types do not have a heating unit.

If, on the other hand, the measurement shows that the fridge can be provided with an electronic defrosting unit (the resistance measured should be several kΩ) check to see whether you can find the wires connecting the heating unit. The wires usually connect the thermostat to the cooler. One of them (it doesn't matter which) will have to be cut to allow the electronic circuit to be connected in series with the heating unit (see figure 1).

Note: The cooler should never be removed as this is linked to the cooling motor.

The circuit diagram

Figure 2 shows the complete circuit diagram for the defrosting unit. In fact the circuit consists of a simple time switch, built up around a 4060 binary counter. This IC contains an internal oscillator which produces a Q10 output cycle time of around 112 seconds with the values chosen for R4, C4 and C5. The voltage at pin 9 will therefore change in level after every 56 seconds. This can be checked with the aid of a voltmeter and a wrist watch. If this parameter is not met, adjust the value of R4. A divide-by-two is situated between every output in IC1 (the first 5 outputs are not used). The output at Q6 has a cycle time duration of about 2 hours (low for 1 hour and high for 1 hour). Output Q7 goes high on the negative-going edge of this signal and so does output Q8. Outputs Q6...Q8 control the triac (Tri1) by way of diodes D6...D8 and transistor T1. As a result, the triac stops conducting for 7 hours and then conducts for 1 hour (see figure 3). This triac is connected in series with the heating unit. As a result, the defrosting system is operated for one hour at seven hour intervals, that is, the heating unit is switched on after the motor stops. If the motor is switched on again by means of the thermostat, the fridge will not be defrosted for an hour after which it takes another seven hours before the thawing process is resumed. If after a few days there is no ice on the cooling plate (depending on how often the door is opened!) diode D9 can be connected to the circuit using the wire link B1, so that the intervals now last 15 hours. If necessary, wire link B2 can also be made to create intervals lasting 31 hours.

In order to obtain a stable clock frequency, IC1 is supplied with a voltage that is stabilised by the zener diode D5. The R1/C3 network makes sure the

3

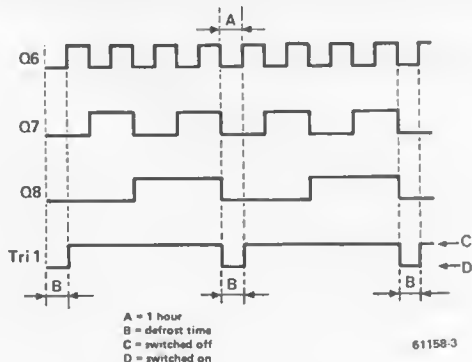


Figure 3. The pulse flow chart of the levels at the Q6...Q8 outputs of IC1. If all three outputs are logic 0, the defrosting system will operate.

Parts list

Resistors:

R1 = 470 k
 R2 = 680 Ω
 R3 = 10 M
 R4 = 3M3
 R5 = 220 k
 R6 = 39 k
 R7 = 1 k
 R8 = 47 Ω /1 W

Capacitors:

C1 = 100 μ /25 V
 C2, C3 = 100 n
 C4, C5 = 22 μ /16 V
 C6 = 100 n/400 V

Semiconductors:

IC1 = 4060
 T1 = BC547
 Tri1 = TIC 206D
 D1... D4 = 1N4001
 D5 = zener 10 V/400 mW
 D6... D10 = 1N4148

Miscellaneous:

Tr1 = 12 V/50 mA
 F1 = 100 mA slow fuse + holder
 3 strain relief glands
 plastic case BOC 435 West Hyde

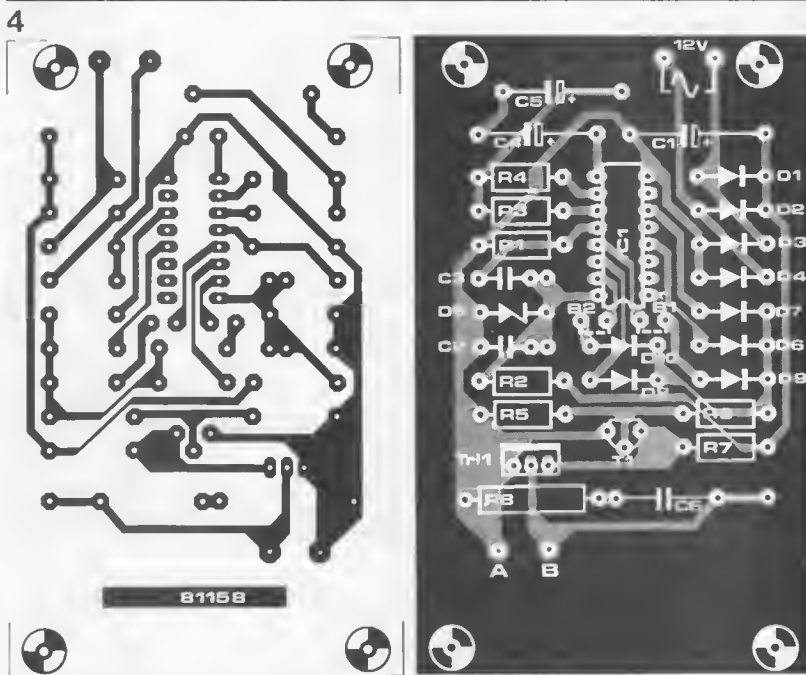


Figure 4. The track layout pattern and component overlay for the fridge defroster printed circuit board. The board should be housed in a plastic case.

counter is automatically reset when the supply voltage is switched on, so that the thawing process always starts first.

Construction

Figure 4 shows the component overlay and the copper tracking pattern of the printed circuit board for the economical defroster. Mounting the components on the board should be straightforward enough. Leave the wire links B1 and B2 until later. The triac does not need to be provided with a heat sink.

As can be seen from the circuit diagram, the power supply is not grounded — this is exactly how it should be! The board must be housed in a plastic case (BOC 435 from West Hyde). For safety reasons it is advisable to use plastic nuts and bolts to fix the board to the bottom of the case and also to mount the transformer onto the lid. In addition, a 3 way connector (choc-block) is attached to the inside of the lid with a plastic nut and bolt. Three holes are drilled in the lid for 3 strain relief glands for the mains leads.

The circuit is connected to the fridge in the following manner. Unplug the fridge and cut the mains lead in the position that the defroster circuit is to be connected (in other words, outside the fridge). The mains lead with the plug, still hanging on it is passed through the strain relief and wired to one side of the connector. The primary of the transformer is now wired between live and neutral. Please, under *no circumstances* connect it to the earth wire! The fuse should also be connected in series with the primary side of the transformer. The mains lead that is still linked to the fridge has to be connected to the other

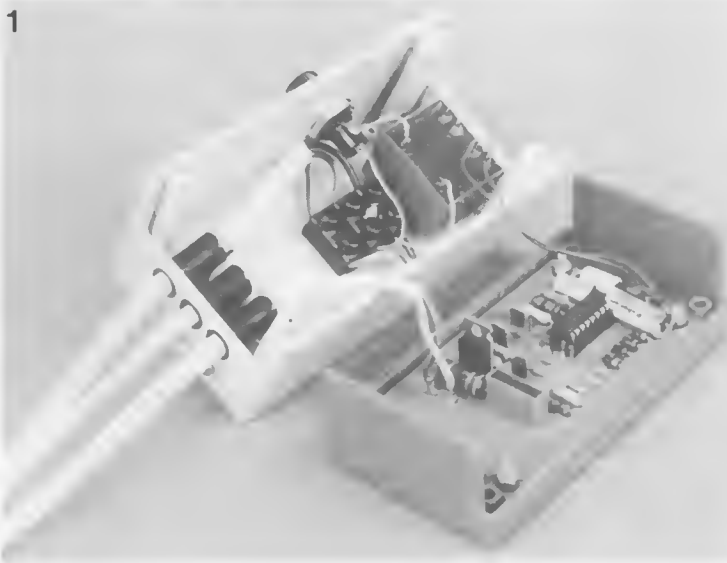


Photo 1. The complete defroster is housed in a West Hyde BOC 435 plastic case. Note the cable strain relief glands and the 'choc-block' connector.

side of the 3 way connector. Finally a 2 wire mains lead is soldered to outputs A and B on the board. The ends of the lead are led into the fridge and connected 'in series' with the cut wire leading to the heating device. It does not matter which way round the wires are connected, but it is important to know if the correct wire is being cut (see figure 1). The case can be mounted on the back of the fridge.

After a thorough check the fridge can be plugged in which will start the motor. If after a few days the cooler is

still not covered in ice, wire link B1 may be added to make the economical defroster even more economical. If necessary, link B2 can also be fitted, but if ice starts to form on the cooler (several mm thick) B2 should be removed. If this doesn't help B1 should be taken out as well. Readers will have to experiment and see what is best, since every fridge is different!

Warning! Remember that in spite of the transformer the circuit may well be connected to a lethal voltage, since it is connected to mains via the heating unit. ⚡

Voltmeters are always useful as far as anybody interested in electronics is concerned. Junior Computer owners can use this straightforward circuit and program to convert their computer into an excellent digital voltmeter.

The basis of the circuit is an A/D converter from Intersil. This IC has binary outputs and will convert the input signal

plete voltmeter circuit for a 3½ digit display including automatic polarity indication. This means the whole circuit can be very straightforward.

Figure 1 shows the circuit diagram. The voltmeter IC contains a 12 bit A/D converter with tri-state outputs. The outputs B1... B8 are displayed in two bytes. Which byte is displayed depends

using the Junior Computer as a voltmeter

With the addition of a small circuit and the aid of the accompanying program the Junior Computer can be used as a digital voltmeter . . . and a good one at that! The voltmeter has 3½ digits and an automatic polarity indicator, even though the program is less than 180 bytes long.

level into the BCD code. Since the IC has tri-state outputs, it is suitable for use with microprocessors.

The circuit

The Intersil ICL7109 contains a com-

on the address decoder IC2. The low order byte contains the eight least significant bits and the high order byte the four most significant bits plus an overflow bit and a polarity bit.

Using the given specifications, the

G. Sullivan

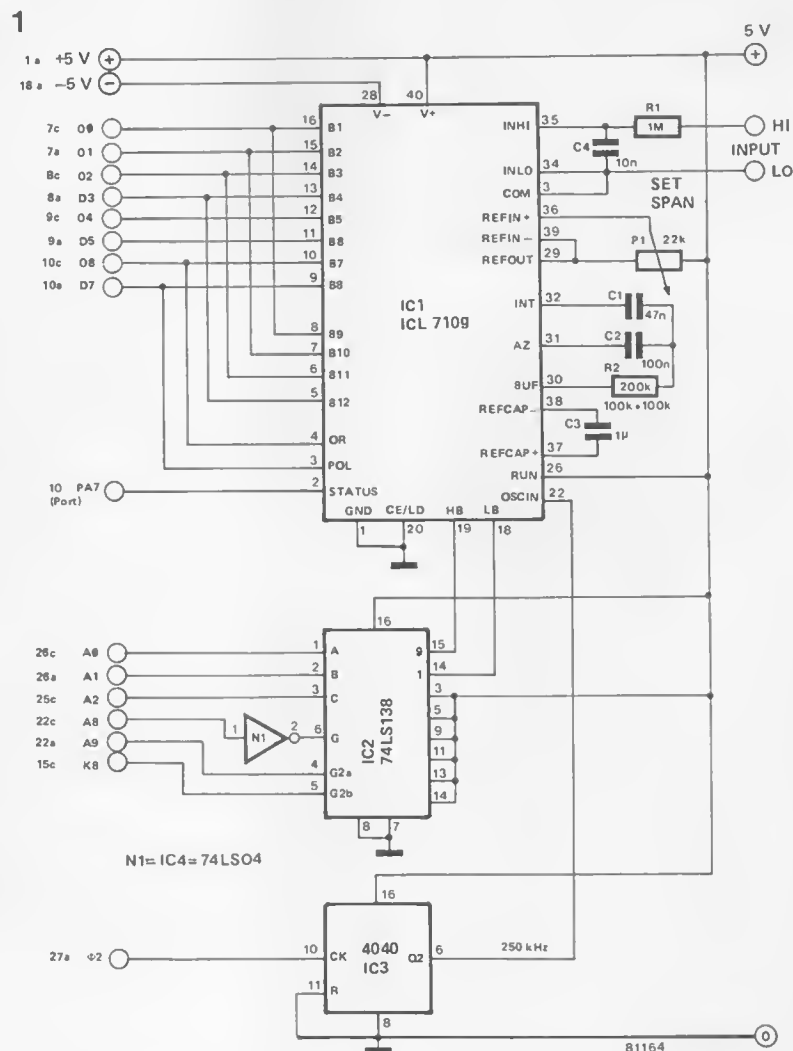


Figure 1. The digital voltmeter circuit diagram which enables the Junior Computer to measure DC voltages. IC1 takes care of the whole process, converting an analogue input signal into a 12 bit code for the computer.

input voltage for 'full scale deflection' will be 4.096 V. The conversion speed is about 30 per second. The input range can be varied by changing the value of R2 and by modifying the reference voltage which is set by P1.

Thus,

$$R2 = \frac{U_{\text{full scale}}}{20 \mu\text{A}} \text{ and}$$

$$U_{\text{full scale}} = 2 \cdot U_{\text{ref.}}$$

The value of C1 and C2 is determined by the oscillator frequency used, where

$$C1 = \frac{2048 \cdot \text{period} \cdot 20 \mu\text{A}}{3.5 \text{ V}}$$

$$\text{and } C2 = 2 \cdot C1.$$

The 250 kHz frequency that is used for the converter is derived from the micro-processor clock. For this IC3 is connected as a divide-by-four. If required, the converter may be run at a different frequency by choosing a different output of IC3. This will also alter the number of conversions per second. Because of the converter's high input impedance, input attenuators can be included fairly easily to provide several voltage ranges.

The program

The program which enables the JC to be used as a digital voltmeter is shown in table 1. This will read in the two bytes produced by the converter, after which a binary-to-decimal conversion takes place and the result is then shown on the display. In the case of a negative input signal the status of the polarity flag is detected and a minus sign is shown on the display. If the maximum input voltage of the converter is exceeded, the display will indicate OL (overload) together with the polarity.

In the circuit diagram in figure 1 the converter is connected in the 'free run mode'. This means it will start with the next conversion as soon as an analog-to-digital conversion has been completed. This is fine under normal circumstances, but it may prove necessary to detect the actual moment a conversion has ended and then read in the data to avoid this happening while the data is changing.

This can be done by connecting the status output of IC1 to PA7 of the port connector and by using the negative-going edge of this output to enable an interrupt (IRQ) at the end of a conversion. The interrupt routine can then read in and store the two bytes before the following conversion comes to an end. An example of this interrupt routine is provided in table 2.

Once the two programs have been loaded beginning with address 0200, the

Table 1.

LINE	LOC	OBJECT	SOURCE
0001	0000		,DIGITAL VOLTMETER PROGRAM
0002	0000		,FOR INTERSIL ICL 7109.
0003	0000		,
0004	0000		,AUTHOR: G. SULLIVAN
0005	0000		,
0006	0000		* = #0000
0007	0000	ACUM	*+*+2
0008	0002	SUM	*+*+1
0009	0003	DELAY	*+*+1
0010	0004	TMFX	*+*+1
0011	0005		,
0012	0005		,DEFINE A/D CONVERTER.
0013	0005		* = #1800
0014	1800	HB	*+*+1 ,HIGH NIBBLE + FLAGS
0015	1801	LB	*+*+1 ,LOW BYTE
0016	1802		,
0017	1802		,DEFINE PIA
0018	1802		* = #1A80
0019	1A80	PRA	*+*+1 ,DATA A REG.
0020	1A81	DDRA	*+*+1 ,A DIRECTION REG.
0021	1A82	PRB	*+*+1 ,DATA B REG.
0022	1A83	DDRB	*+*+1 ,B DIRECTION REG.
0023	1A84		,
0024	1A84	SCAND1	=#1DCC ,DISPLAY 1 BYTE
0025	1A84		,
0026	1A84		* = #0200
0027	0200		,
0028	0200	MAIN	DISPLAY ROUTINE
0029	0200	MAIN	BIT HB ,TEST OVERANGE BIT
0030	0203		BVS OL
0031	0205		JSR DISVLT ,SHOW VOLTS
0032	0208		JMP NOL
0033	0208	OL	LDX #00 ,DISPLAY OL MESSAGE
0034	020D		LDY #03
0035	020F		JSR DISTAT
0036	0212	NOL	LDA HB ,TEST POLARITY BIT
0037	0215		EMI NOT
0038	0217		LDX #08 ,DISPLAY MINUS
0039	0219		LDY #00
0040	021B		JSR DISTAT
0041	021E	NOT	JSR HEXBCD ,CONV. BINARY TO BCD
0042	0221		JMP MAIN
0043	0224		,
0044	0224		,VOLT DISPLAY SUBROUTINE
0045	0224	A9 7F	DISVLT LDA #7F ,SET PIA TO OUTPUT
0046	0226	8D 81 1A	STA DDRA
0047	0229	A2 0C	LDX #0C ,ADDRESS OF FIRST BYTE
0048	022B	A0 FF	LDY #FF
0049	022D	C8	LOOP INY
0050	022E	E9 D0 00	LDA ACUM,Y ,GET BYTE
0051	0231	20 CC 1D	JSR SCAND1 ,LIGHT DISPLAY
0052	0234	E0 14	CPX #14 ,TEST IF TWO BYTES YET
0053	0236	D0 F5	BNE LOOP
0054	0238	AD 00 18	LDA HB ,TEST POLARITY
0055	023B	30 07	EMI NXT ,SHOW - IF NEG.
0056	023D	AC 06	LDX #06
0057	023F	A0 00	LDY #00
0058	0241	20 49 02	JSR DISTAT
0059	0244	E6 D3	WRT INC DELAY ,DELAY ON DISPLAY
0060	0246	D0 DC	BNE DISVLT
0061	0248	60	RTS
0062	0249		,
0063	0249		,DISPLAY -- , OL
0064	0249	A9 7F	DISTAT LDA #7F ,SET PIA TO OUTPUT
0065	024B	8D 81 1A	STA DDRA
0066	024E	E9 D0 02	LDA CHART,Y ,GET MESSAGE BYTE
0067	0251	30 14	EMI ENDD
0068	0253	8D 80 1A	STA PRA ,LIGHT SEGMENTS
0069	0256	5E 82 1A	STX PRB ,SELECT DIGIT
0070	0259	86 14	STX TMFX
0071	025B	A2 FF	LDX #FF
0072	025D	CA	DLV2 DEX ,DELAY
0073	025E	D0 FD	BNE DLV2
0074	0260	A6 D4	LDX TMFX
0075	0262	E8	INX
0076	0263	E6	INX ,NEXT DIGIT
0077	0264	C8	INX
0078	0265	D0 E2	BNE DISTAT
0079	0267	A9 00	ENDD LDA #00 ,DISPLAY OFF
0080	0269	8D 82 1A	STA PRB
0081	026C	60	RTS
0082	026D	7F	CHART .BYTE #7F,#3F,#80
0083	026E	3F	
0084	026F	80	
0085	0270	40	.BYTE #40,#47,#80
0086	0271	47	


```

0083 0272 80
0084 0273
0085 0273
0086 0273 A9 00 ,CONVERT BINARY TO BCD
0087 0275 85 D0 HEXBCD LDA #00
0088 0277 85 D1 STA ACUM ,CLEAR ACCUMULATOR
0089 0279 AE 01 18 STA ACUM+1
0090 027C F0 08 LDX LB
0091 027E A0 01 LOOP1 BEQ HIGH
0092 0280 98 LDY #01 ,CONVERT LOW BYTE
0093 0281 85 D2 TYA
0094 0283 20 9E 02 STA SUM
0095 0286 CA JSR ADD
0096 0287 D0 F5 DEX
0097 0289 AD 00 18 HIGH BNE LOOP1
0098 028C 29 0F LDA HB ,CONVERT HI BYTE
0099 028E F0 0D AND #0F ,REMOVE FLAGS
0100 0290 AA BEQ LAST
0101 0291 A9 08 LDA #08
0102 0293 85 D2 STA SUM
0103 0295 A0 20 LOOP2 LDY #20
0104 0297 20 9E 02 JSR ADD
0105 029A CA DEX
0106 029B D0 F8 BNE LOOP2
0107 029D 60 LAST RTS
0108 029E F8 ADD SED ,ADD 1 OR 256 TO ACUM
0109 029F 18 LOOP3 CLC
0110 02A0 A5 D2 LDA SUM
0111 02A2 65 D1 ADC ACUM+1
0112 02A4 85 D1 STA ACUM+1
0113 02A6 A9 00 LDA #00
0114 02A8 65 D0 ADC ACUM
0115 02AA 85 D0 STA ACUM
0116 02AC 88 DEY
0117 02AD D0 F0 BNE LOOP3
0118 02AF D8 CLD
0119 02B0 60 RTS
0120 02B1 .END
    
```

IRQ vector has to be specified:

```

1A7E 80
1A7F 03
    
```

Finally, the initialisation routine which is needed whether or not the interrupt routine is used:

```

0000 8D 86 1A STA 1A 86
0003 58 CLI
0004 4C 00 02 JMP-MAIN
    
```

Now a reference voltage is connected to the input of the meter circuit (4 V, for instance) and P1 is adjusted so that the display indicates the value of the reference voltage. In the absence of a known voltage, any DC voltage of about 4 V can be used instead and the display can be compared to that of another, accurate meter.

These instructions make sure the PIA produces a negative-going edge at PA7 and that the interrupt-disable bit is restored once the processor is reset. When this has been done and the circuit in figure 1 is connected to the Junior Computer, the program can be started at address 0000.

ERRORS 0000

SYMBOL TABLE

ACUM	0000	ADD	029E	CHART	026D	DDRA	1A81
DDRB	1A83	DELAY	00D3	DISTAT	0249	DISVLT	0224
DLY2	025D	ENDD	0267	HE	1800	HEXBCD	0273
HIGH	0289	LAST	029D	LB	1801	LOOP	022D
LOOP1	027E	LOOP2	0295	LOOP3	029F	MAIN	0200
NOL	0212	NOT	021E	NXT	0244	OL	020E
FRA	1A80	PRB	1A82	SCAND1	1DCC	SUM	00D2
TMPX	00D4						

END OF ASSEMBLY

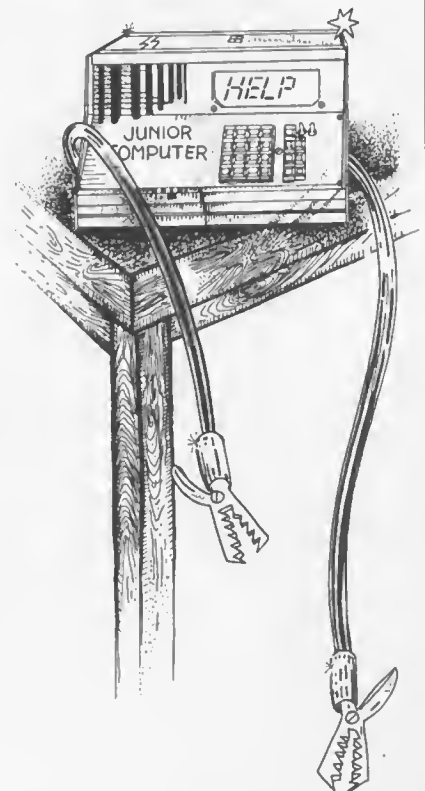
Table 2.

IRQ service routine:

```

0380 48 INTS: PHA ; save A
0381 8A TXA ; save X
0382 48 PHA
0383 98 TYA ; save Y
0384 48 PHA
0385 AD 85 1A LDA 1A 85 ; reset IRQ
0388 AD 00 18 LDA 18 00 ; read high byte
0388 85 D0 STA D0 ; store it
038D AD 01 18 LDA 18 01 ; read low byte
0390 85 D1 STA D1 ; store it
0392 68 PLA ; restore all registers
0393 A8 TAY
0394 68 PLA
0395 AA TAX
0396 68 PLA
0397 40 RTI ; return to main program
    
```

The Junior Computer...



... as a voltmeter ?

The 2716 is rapidly becoming one of the most popular of EPROMs. And with good reason. The price is right, for one thing — although we would be the last to complain if it drops any further! Furthermore, it only needs a single supply voltage, which makes life a lot easier, and it is virtually pin-compatible with the 'old' 2708s. The last remaining obstacle to widespread use is the need for a means to program them.

The rules of the game are fairly simple, as shown in figure 1. You need a 25 V programming voltage, and a program-

ming pulse at ordinary TTL level and lasting for 50 ms. To be more precise, the \overline{CE} pin must be pulled high and then the \overline{OE} input is also set to logic 1. This situation must be maintained for 50 ms, after which \overline{OE} and \overline{CE} go low again. To check whether this programming cycle was successful, the data can now be read out without first having to switch off the 25 V supply.

A normal EPROM programmer is quite a complicated machine, since it must be capable of retrieving the desired data from another EPROM or whatever; putting the various signals onto the new EPROM's pins in the correct sequences; checking for a successful 'store' and repeating the process if necessary. A self-contained unit to do this can't possibly be a 'simple' circuit. However, it helps a lot when you hit on the idea of letting an existing microprocessor system do most of the work. The system described here takes this idea one step further.

In many cases, the EPROM will be intended for use in the microprocessor system. This means that there will be a socket for it on the board. A small auxiliary circuit can be plugged into this socket, after which the EPROM is plugged into the top of this. A piggy-back arrangement, in other words. Four flying leads go to the auxiliary circuit, after which the 2716 can be programmed by means of an ordinary write operation to the corresponding address! This is followed by a normal 'read' to check whether the data was transferred correctly. It is interesting to note that any single location or group of locations

plug-in EPROM programmer

program 2716s the easy way!

The circuit described here can be used to load programs or other data into 2716 EPROMs. For this fairly complicated job it uses only a single 555 timer and one TTL IC, plus a handful of little components. Impossible? Not when you are going to use the EPROM in a microprocessor system! In that case, you can often get the μP itself to do most of the work.

R. Pequet

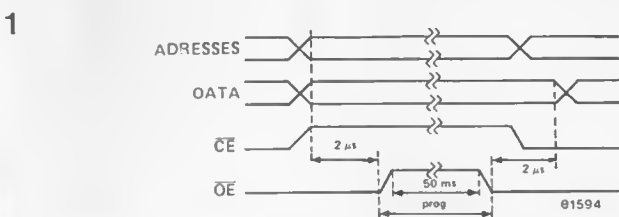


Figure 1. A 2716 is remarkably easy to program. Provided the programming voltage (25 V) is connected, you only have to ensure that both \overline{OE} and \overline{CE} are pulled high at the correct times.

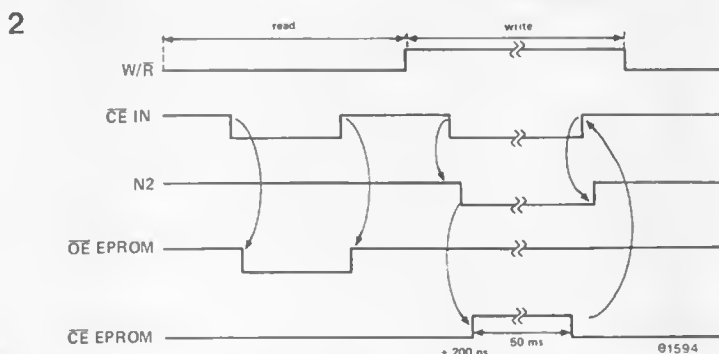


Figure 2. The circuit converts the $\overline{W/R}$ and \overline{CE} signals from the processor into the necessary \overline{OE} and \overline{CE} pulses for the EPROM. Note that \overline{OE} must be low for Read and high for Write.

3

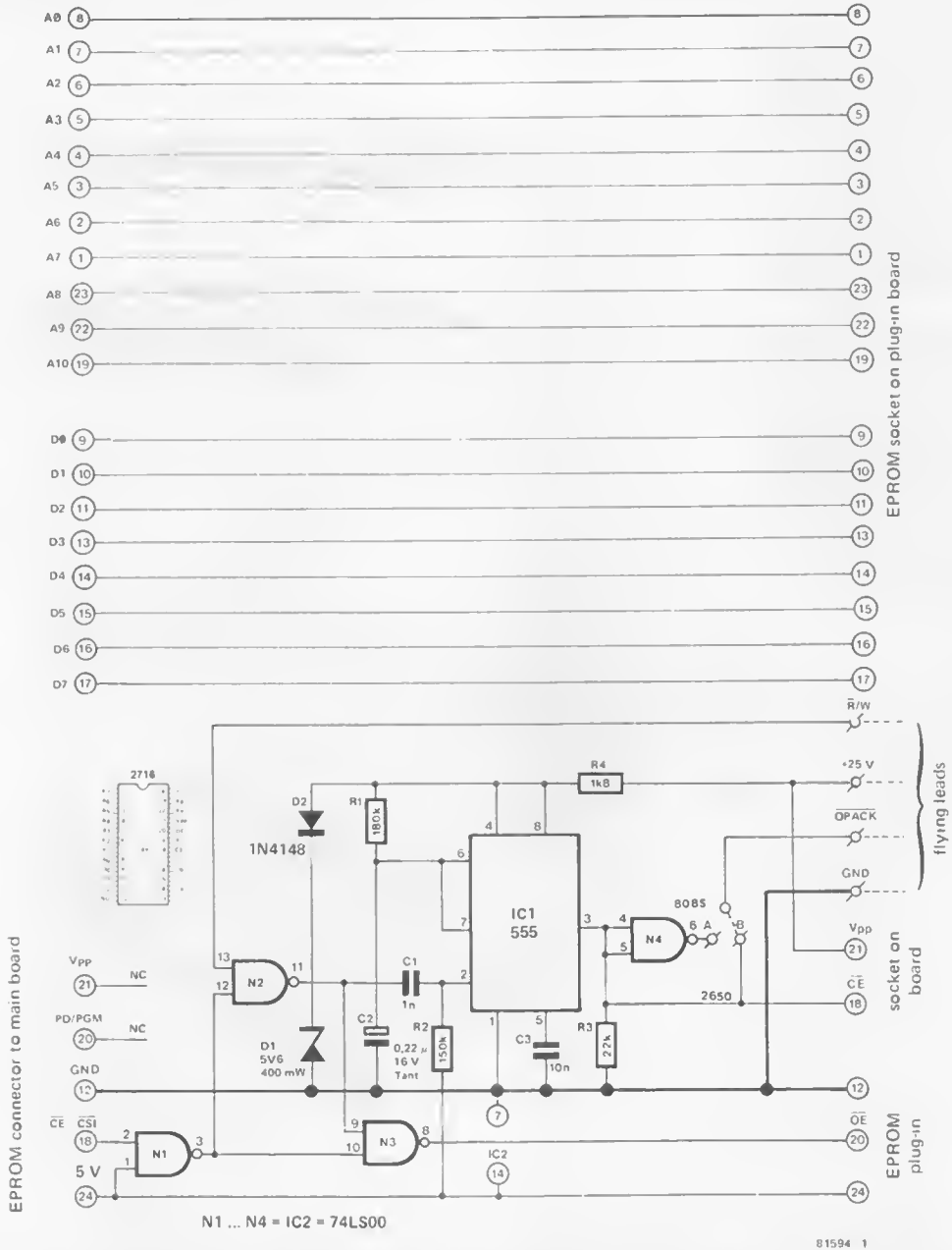


Figure 3. The complete circuit. Most of the signals that are present at the original EPROM socket can be left unmodified for programming. The original CE signal is combined with R/W (the latter is connected via a flying lead) to produce OE and CE for the EPROM to be programmed and OPACK for the μP. The supply to the 555 is derived from the 25 V programming voltage.

can be programmed in this way. In other words, starting from an erased EPROM, bits and pieces can be loaded at different times - you don't have to fill the whole thing in one go. Before every microprocessor enthusiast in the Empire goes rushing out to buy the chips, we must give a word of warning. For the system to work, it must be possible to stop the μP during the write operation - for the required 50ms. In fact, this programmer was originally designed for the Signetics 2650, as used in the TV games computer, which has an OPACK input for that purpose. The first thing, therefore,

is to check whether your processor has an input of this type. If so, the circuit can almost certainly be used - possibly with one or two minor modifications. On the 8085, for instance, the READY input can be used. Unfortunately, the 6502 has not got this feature and so it is unsuitable. However, in the near future we will be publishing a larger 'Eprommer' that can be used in all applications.

The circuit

When using the 2650, for example, the OPACK signal stops the processor 'in its tracks' as it were, and the data and

address lines remain unchanged. This makes it an easy matter to keep all the address and data bits stable during the 50ms programming cycle. The necessary OPACK signal can be generated quite easily by means of a 555 timer. The basic requirements are given in figure 2. The EPROM is enabled by pulling the CE input low. For a read cycle, nothing special happens. As can be seen in figure 3, the R/W input (at logic 0 for Read!) will cause the output of N2 to go to logic 1; this, combined with the logic 1 from N1, will pull the OE pin low via N3. The data is now read out from the EPROM in the normal



Note that, for clarity, D1 and D2 are not shown in the drawing.

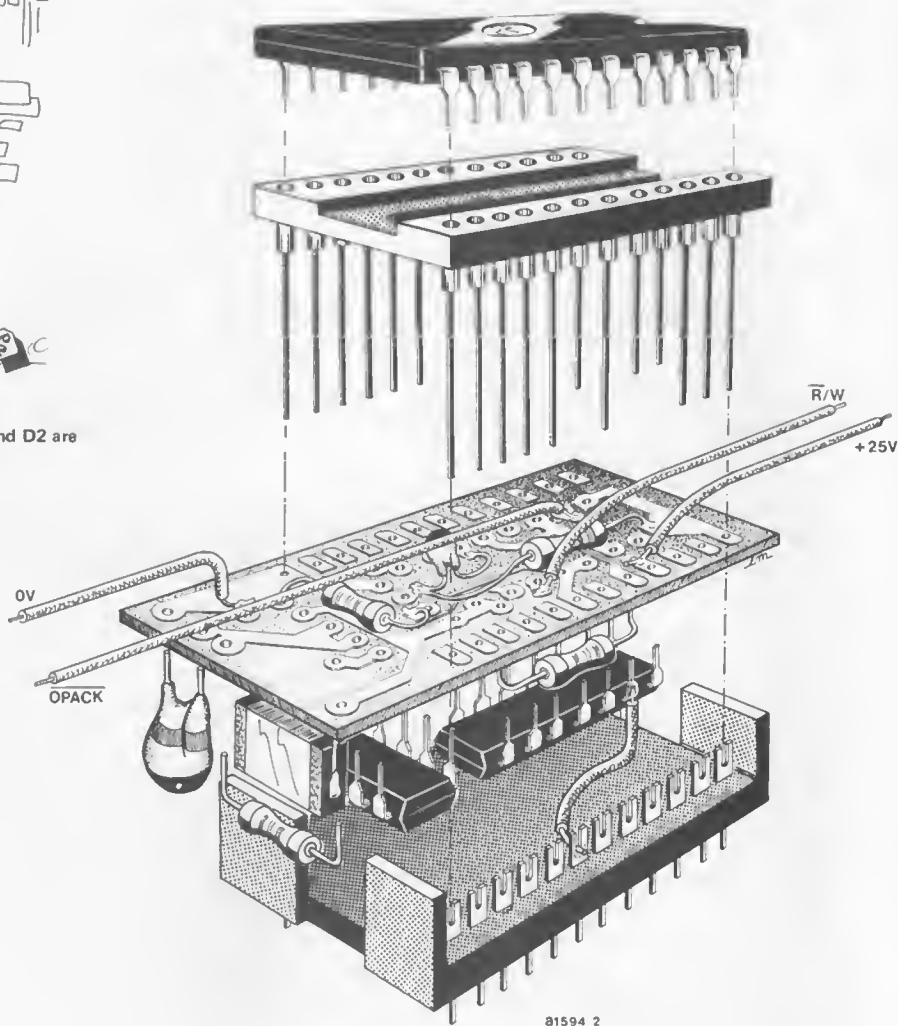


Figure 4. This drawing clearly illustrates the construction. After mounting all components on the p.c. board, short and stiff wires are soldered through the corresponding holes for mounting the DIL connector underneath and the IC socket on top. Alternatively, a wire-wrap socket can be used at the top; its pins are long enough to go right through the board to the connector underneath.

way; its \overline{CE} input remains low throughout.

For a write operation, things must obviously become slightly more complicated. The \overline{CE} and $\overline{R/W}$ inputs to the circuit are both logic 0 in this case, so the output from N3 (\overline{OE} for the EPROM) is maintained at logic 1 throughout. Furthermore, the negative-going edge at the output of N2 triggers the timer (IC1) so that its output goes high. This is the \overline{CE} signal for the EPROM. As can be seen in figure 1, both \overline{OE} and \overline{CE} for the EPROM being at logic 1 corresponds to the programming mode! During the 50 ms output period from the timer, the \overline{OPACK} output is also held at logic 1 to stop

the processor — for an 8085 μP , this signal can be inverted via N4.

Using the unit

In practical terms, the whole procedure for programming a 2716 EPROM is as follows:

- Insert the auxiliary circuit in the EPROM socket and plug the (erased) EPROM into the top; connect the $\overline{R/W}$, \overline{OPACK} and 25 V lines with flying leads.
- For the 2650, the program given in table 2 can now be run: it will load up to 256 bytes from a specified address and transfer them to the specified EPROM address. Obviously, this pro-

gram can be modified or relocated according to the desired application.

- Disconnect the flying leads, remove the auxiliary circuit and insert the EPROM in its intended socket. Job done!

There are a few points to note, when using this circuit in other microprocessor systems. In the first place, the $\overline{R/W}$ must be present prior to or, at the very latest, simultaneously with \overline{CE} . For the 8085, this means that \overline{ST} should be used instead of \overline{WR} .

Furthermore, the \overline{CE} signal for the circuit should not be derived in any way from the $\overline{R/W}$ signal. In practice, this means that the block address decoder that selects the EPROM should only be

Table 1

PINS \ MOOE	\overline{CE}/PGM (18)	\overline{OE} (20)	Vpp (21)	VCC (24)	OUTPUTS (9-11, 13-17)
Read	VIL	VIL	+5	+5	OOUT
Standby	VIH	Don't care	+5	+5	High Z
Program	pulsed VIL to VIH	VIH	+25	+5	OIN
Program Verify	VIL	VIL	+25	+5	OOUT
Program Inhibit	VIL	VIH	+25	+5	High Z

Table 2

0100	xx	xx		start address data	
0102	xx	xx		start address EPROM	
0104	xx	xx		number of bytes	
76	60		PPSU	disable interrupts	} is EPROM empty?
00	01	04	LOOA	number of bytes in R1	
00	C1	02	LOOA	is EPROM byte FF?	
E4	FF		COMI	if \neq FF error	
98	17		BCFR	test next address	
59	77		BRNR		
74	40		CPSU	flag = 0	} program
09	F1		LOOR	number of bytes in R1	
04	FF		LODI	wait for 2.5 ms	
F8	7E		BDRR		
OD	C1	00	LODA	fetch data	} EPROM
CO	E1	02	STRA	data to EPROM	
ED	E1	02	COMA	is EPROM correctly programmed?	
98	02		BCFR	if not, error.	
59	6F		BRNR	next byte to EPROM	
40			HLT		

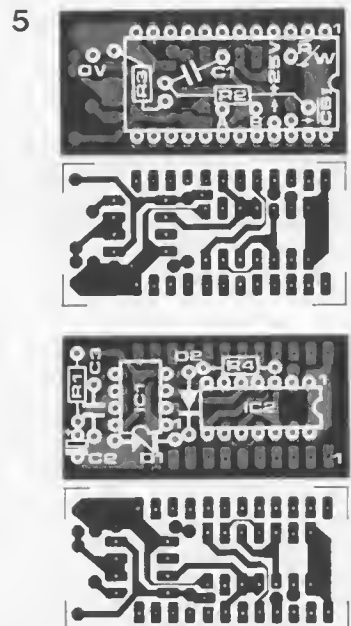


Figure 5. The printed circuit board and component layout. Components are mounted on both sides of the board. Note that pins 20 and 21 of the DIL plug are not connected to the board, and that pin 18 is linked by means of a separate wire to pin 2 of IC2. This is indicated as 'CSI' on the board.

Parts list

- Resistors:
- R1 = 180 k
- R2 = 150 k
- R3 = 22 k
- R4 = 1k8
- all resistors are 1/8 watt types
- Capacitors:
- C1 = 1 n
- C2 = 0.22 μ /16 V tantalum
- C3 = 10 n
- Semiconductors:
- O1 = 5.6 V/400 mW zener diode
- D2 = 1N414B
- IC1 = 555
- IC2 = 74LS00
- Miscellaneous:
- 24 pin IC socket
- 24 pin IC connector

enabled by some type of 'address valid' signal. For a 2650 system, \overline{OPREQ} or M/I/O are both possible candidates. After each programming cycle, the circuit must be given time to 'settle' (2.5 ms at least). In the program example given, a delay is included for this. R1 and C2 give a calculated 555 period of 45 ms, when C2 has its nominal value. This is on the short side, but in practice this type of capacitor has an effectively larger capacitance in this very-low-frequency application. If measuring equipment is available, R1 can be tailored until the period is exactly 50 ms; however, the values given have proved reliable in all our tests.

Perfectionists may have noticed that the programming signals for the EPROM are not quite right: there is no 2 μ s delay between the moment that the address and data is applied and the start of the \overline{OE} pulse. In practice, this has never caused us any trouble. The 555 gives a delay of at least 200 ns between the trigger pulse at pin 2 and the resulting output at pin 3. In practice, this could mean that the \overline{OPACK} signal would appear too late to stop the processor. For a 2650, using a 1 MHz clock, this signal must appear within 600 ns — so that leaves plenty of time. An 8085, working on 3 MHz, should receive the signal within 100 ns. Again, practical tests have shown that problems

are not likely to occur, however; even so, it is worth bearing in mind that reducing the clock frequency temporarily may help to make the programming procedure more reliable. One final point: databooks do not seem to agree entirely on which 2716 pin is the \overline{CE} and which is \overline{OE} ! However, if you use the pin numbers given in the circuit (18 for \overline{CE} and 20 for \overline{OE}) the circuit will work. M

H.P. Baumann

synthesiser

ICs



makes building synthesisers less of a headache

The American Curtis company has recently introduced a set of special music synthesiser ICs onto the market. These 'musical chips' have now found their way across the Atlantic and are well worth looking at (and listening to). The following analysis weighs up the pros and the cons.

The four ICs involved are: a VCO (CEM 3340), a VCF (CEM 3320), a VCA (CEM 3330) and a voltage controlled ADSR generator (CEM 3310). Before readers rush out to the shops, however, it should be mentioned that although their quality is very good, this does not herald the 'perfect IC', able to do anything. This simply does not exist. However, the ICs we're about to introduce are very clever, but nonetheless still require the assistance of a few other components. Readers will find the ICs to be quite useful — provided they are properly used. So if you are thinking about building a synthesiser based on the Curtis ICs, take heed of the following information and advice... and read the next issue of Elektor, there is definitely something up the editorial sleeve!

General remarks

Although the chips are fairly rugged, 24 volts between any two pins will almost certainly lead to sudden death. The supply voltage should not exceed 18 V. The data sheets show that series-resistors must be included to limit the

negative supply voltage: these, together with an internal zener diode, serve to limit this voltage. The resistors may only be omitted if the negative supply does not exceed -6 V at any time.

The maximum current consumption is less than 10 mA for all four types. Readers who own a test power supply with an adjustable maximum output current should limit this to 10-20 mA if they intend to use it to power the circuit. This affords protection in the event of a short circuit — the chips are not designed to survive one!

One further warning: don't add capacitors when the power is still 'on'. This could cause voltage transients which would immediately send the IC to 'the big siliconmaker in the sky'. Thus, the warning in the data sheet 'not short circuit proof' is to be taken quite literally!

The voltage controlled oscillator CEM 3340

The block diagram in figure 1 shows that the IC contains all the bits that are needed to convert a control voltage into an output frequency. Input adders, temperature compensated exponential converters, and VCO; and resonance frequency converters for triangle and square waves, pulse width modulation and sawtooth.

Temperature compensation works here

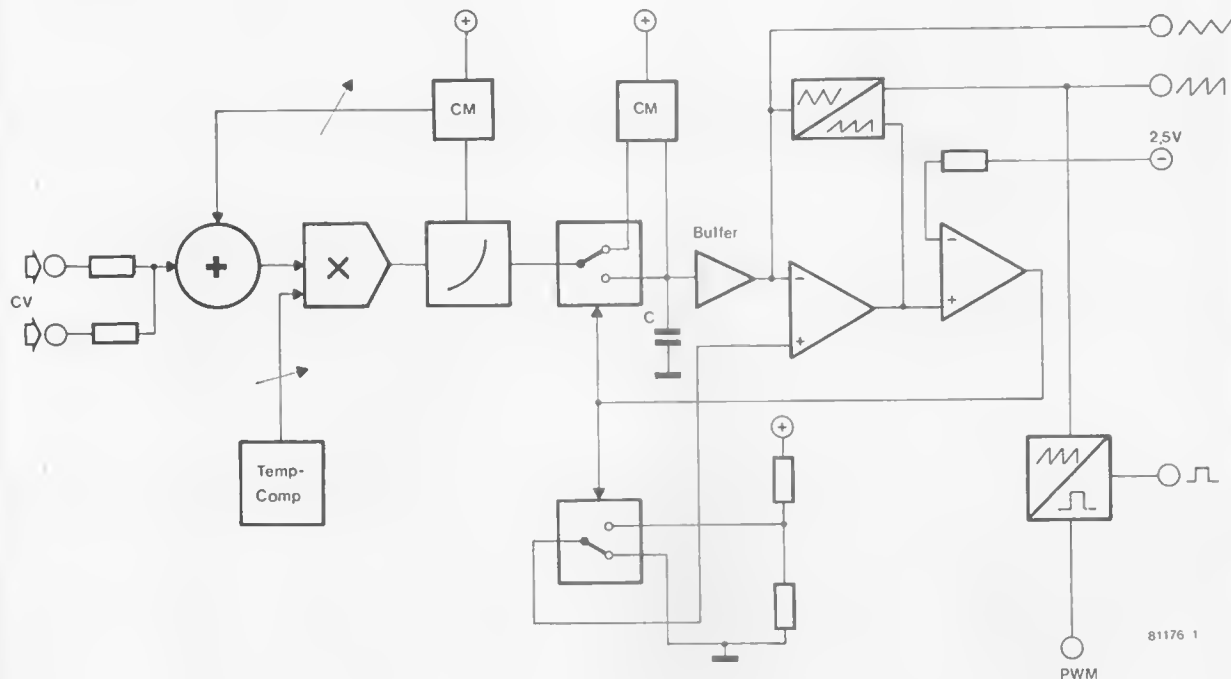


Figure 1. The block diagram of the CEM 3340. It contains all the components required to construct an exponential synthesizer VCO: input adders, a temperature compensated exponentiator, a triangle oscillator, a triangle-to-sawtooth and sawtooth-to-squarewave converter. The latter has a control input for pulse width modulation. The IC is highly suitable for use in precision frequency generators.

on the basis of multiplying the VCO's current with a coefficient which is derived from the absolute temperature. Provided this coefficient is correctly adjusted, variations in the exponential converter's temperature will be completely compensated.

The exponential converter's operating range covers a total ratio of 1:500,000; the highest accuracy is in the operating current range between 50 nA and 100 μ A. In the 5 Hz... 10 kHz frequency range $C_F = 1$ nF is a reasonable value. It is preferable to use good quality capacitors (such as polycarbonate types).

The reference current is set by means of R_R . In the interests of optimum linearity and stability, this current should be between 3 and 15 μ A. The value of the summing resistors at the input adder (pin 15) should be 100 k, to provide the 1 V per octave standard control feature. In principle, it is quite possible to obtain a precise linear volts-per-octave curve by calibrating every single summing resistor. It is simpler, however, to use a preset potentiometer as part of R_Z , since this acts on the total summed control voltage.

Once the temperature effects have been fully compensated and the conversion factor has been set at 1 V per octave, discrepancies in the exponential curve for the frequency range above 3... 5 kHz

have still to be ironed out. Due to various effects (the transistors' base-spreading resistance, which becomes increasingly important at higher control currents, and the internal comparator's delay time) the higher frequencies tend to go 'flat'. One way to compensate for this has been provided: using a current mirror, part of the exponential converter output current is fed to pin 7. This is converted into a voltage, and a fraction of this is fed back to the input adder. In this way, an increasing control voltage is produced at the VCO for higher frequencies. Provided the level is correct, this will straighten out the volts-per-octave curve.

Practical results

Although the circuit provided in the Curtis data sheet does work (figure 1), it is not advisable to use it in this simplified form. The manufacturer states that the VCO IC can be operated on +15 V/-15 V, but omits to mention that the positive voltage should be adequately stabilised.

The reason for this can be seen in figure 1. The reference voltage for the upper threshold of the comparator is derived directly (at pin 9) from the positive supply voltage with the aid of two integrated resistors of 14.4 k and 7.2 k, respectively. However, since the

control voltage for the oscillator is not affected by the supply voltage, every ripple in the positive supply will greatly affect the output frequency. The same is true, to a lesser extent, for the negative voltage: the internal 6.5 V zener diode serves to protect the circuit against excessive voltages — it is not intended as a voltage regulator. If its temperature stability has been better, things might have been different. As it stands, however, the potential at pin 3 alters when the temperature changes, taking the voltage across R_Z and R_T with it. The best results are obtained by stabilising both supply voltages and by leaving the internal zener diode out of action.

A further point concerns the supply voltages. The full ± 15 V has been found to increase the chip's leakage currents considerably. This leads to excessive drift and poor linearity. In general, therefore, the supply voltages should be kept as low as possible.

Also apparent from figures 1 and 2 is the fact that the buffered triangular wave form is connected to pin 10. Without any further buffering this is only suitable for constant loads due to the relatively high output resistance. Even a 100 k load will shift the oscillator frequency by 0.15%. This is not surprising, considering that the same (internal) buffer stage also drives the

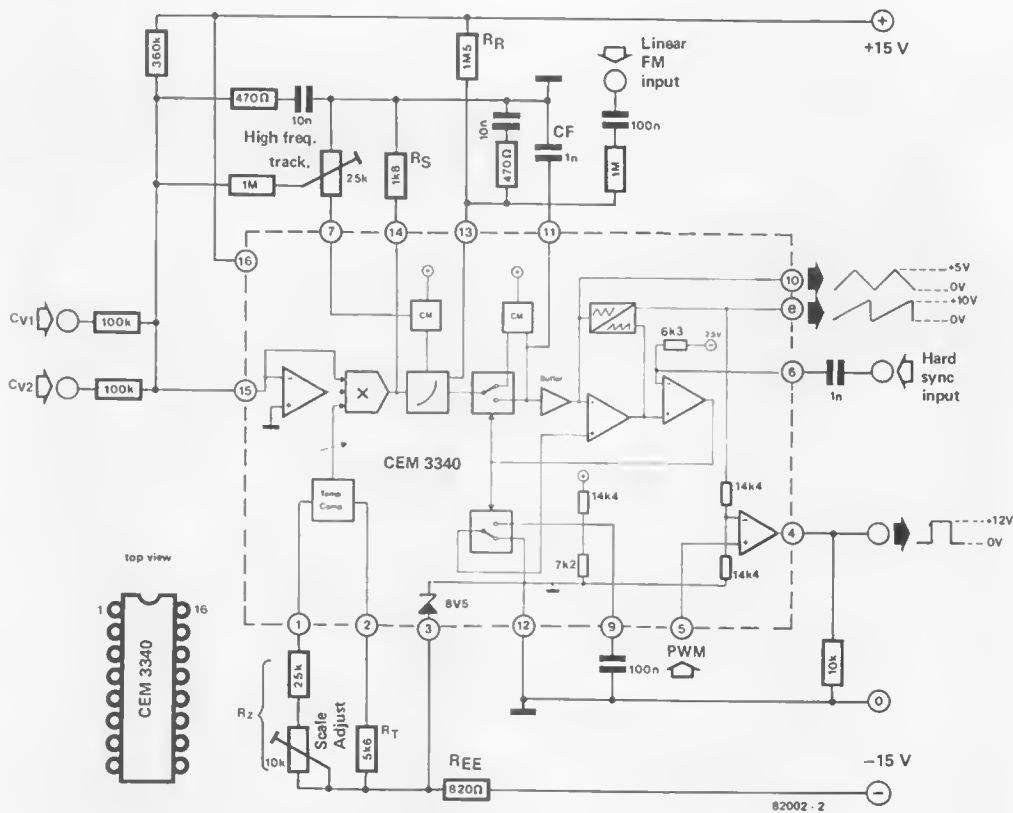


Figure 2. The practical circuit, as suggested by the manufacturer, involves very few components.

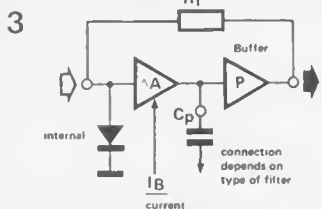


Figure 3. The block diagram of one filter stage in the CEM 3320. This IC contains four of these stages.

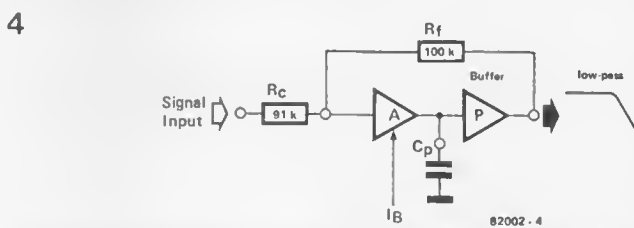


Figure 4. One filter stage connected as a low-pass filter with a slope of 6 dB per octave and unity gain in the passband.

comparator: its output impedance together with the load resistance make a voltage divider which alters the switching threshold. Thus, where variable loads are involved, an external buffer stage at pin 10 is indispensable. Whereas the frequency drift values using the IC in the manner indicated in the data sheet (and figure 1) were around 0.25% per hour at even highly stable operating voltages, the circuit in figure 2 will give a drift of only 0.08% per hour.

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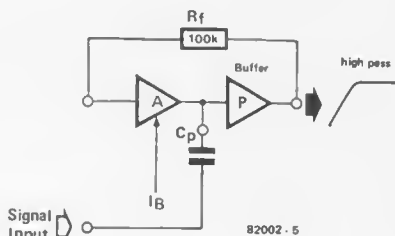


Figure 5. A 6 dB per octave high-pass filter, again with unity gain in the passband.

The filter IC: CEM 3320

The CEM 3320 chip is a 24 dB filter, consisting of four identical filter sec-

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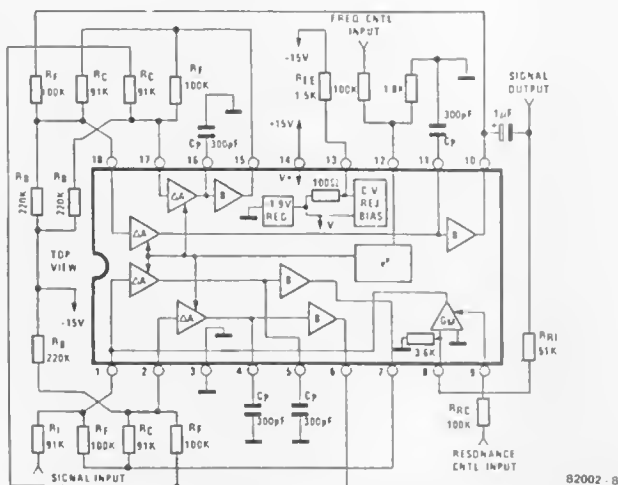


Figure 6. The circuit diagram of a 3320 connected as a 24 dB per octave low-pass filter. A special feature is the filter resonance voltage control system (IQ factor), using a transconductance (GM) amplifier as an electronic potentiometer.

tions of the type shown in figure 3. Operation is simple. Each section produces a filter 'pole' with the aid of a variable-gain amplifier Δ_A , a capacitor C_p and a buffer amplifier. The latter ensures a low output impedance. The variable-gain amplifier is current-driven, both at the signal and control inputs. Moreover, it is fully temperature compensated. The centre frequency is calculated as follows:

$$f_c = \frac{A_{10}}{2\pi R_{EQU}} \cdot e^{-V_c/V_t}$$

where A_{10} represents the current gain of the first stage at zero control current (typical value = 0.9) and R_{EQU} stands for the actual feedback resistance (this is determined mainly by R_f ; the typical value is 91 k). V_c is the control voltage at pin 12 of the IC and V_t the 'temperature voltage' (about 26 mV at room temperature).

Figure 4 shows a stage connected as a low-pass filter. The input signal is fed in through a resistor $R_c = 91$ k; this sets the overall gain to unity. The filter capacitor is grounded. In the same straightforward manner, a 6 dB high-

pass filter may be constructed (see figure 5). The signal is now fed in through C_p . R_c is omitted in this case to obtain unity gain.

The complete internal block diagram of the IC is shown in figure 6. All the variable-gain stages Δ_A are internally linked to the output of an exponential converter.

In order to be able to vary the resonance of the filter (right up to the point where it oscillates!) a common transconductance amplifier G_M has been integrated on the chip. This simply acts as a VCA to vary the 'overall' feedback signal.

The best output range and least 'break-through' of the control voltage is obtained at a quiescent buffer output voltage of $0.46 V_{CC}$, thus at 15 V this will be 6.9 V.

The filter circuit

Figure 7 gives a clearer view of a complete 24 dB low-pass filter. The circuit contains all the components required to buffer and adjust the system. An input adder has been connected to two, for multiple control voltages. This neatly takes care of one further point: the basic circuit given in figure 4 would provide a filter cut-off frequency that drops when the control voltages rises. The inverting adder stage ensures that a rise in control voltage will correspond to a rise in the cut-off frequency.

This circuit allows a range of 10 octaves to be covered with great accuracy. P1 sets the lowest frequency (for zero control voltage). P2 is used to minimise break-through of the 'resonance' control voltage to the output; P3 does the same job for the filter frequency control voltage. P3 is the easiest to adjust, by con-

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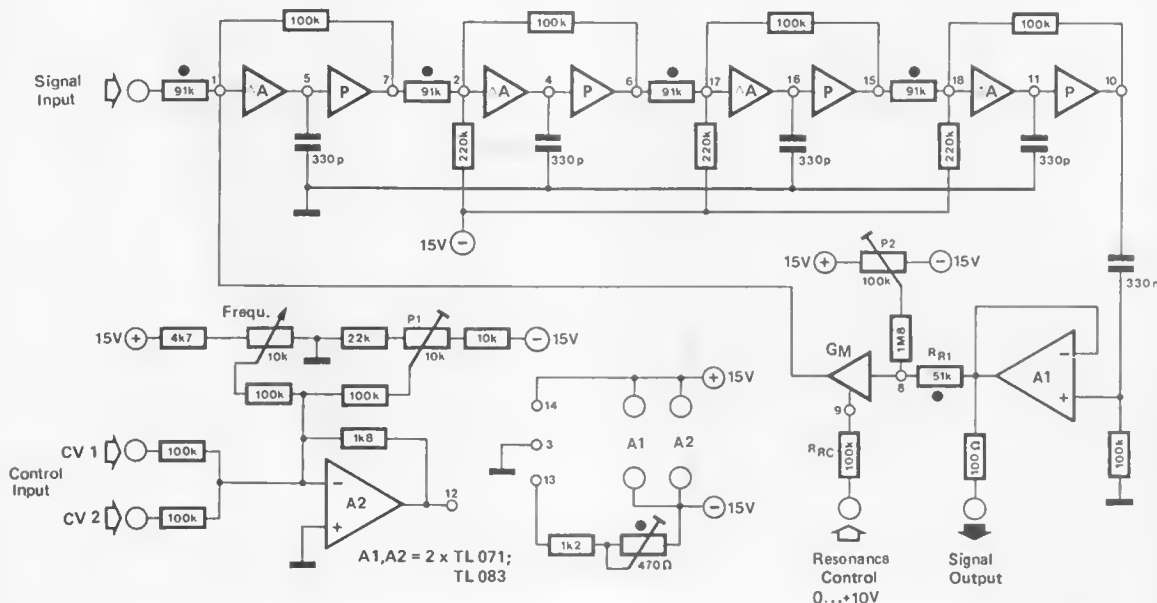
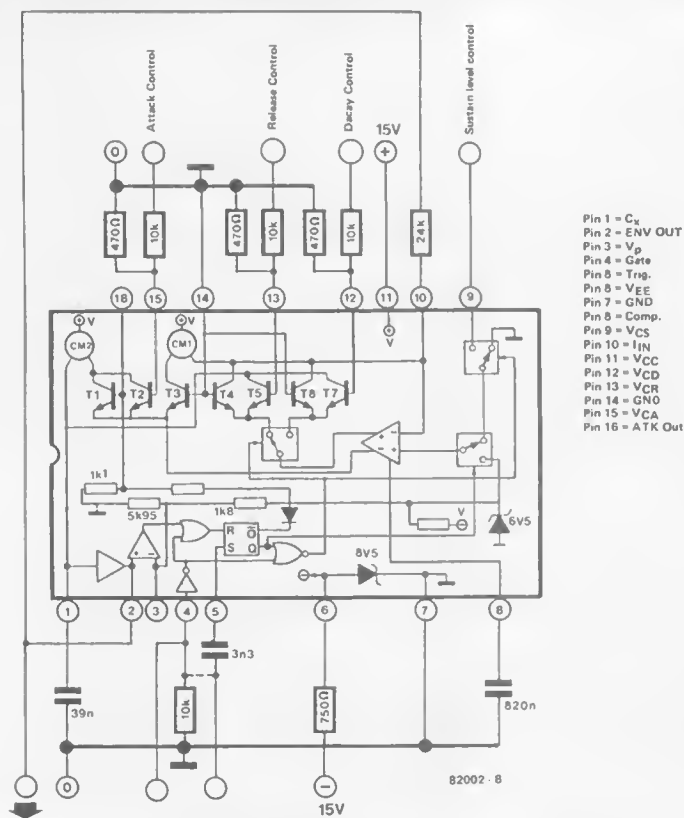


Figure 7. The complete, tested circuit of a 24 dB VCF (low-pass) using the CEM 3320. When high stability requirements need to be met (if the filter is used as a sine wave VCO, for instance) the resistors and potentiometers that are marked with a dot should be metal foil and Cermet types.

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- Pin 1 = C_x
- Pin 2 = ENV OUT
- Pin 3 = V_p
- Pin 4 = Gate
- Pin 5 = Trig.
- Pin 6 = V_{EE}
- Pin 7 = GND
- Pin 8 = Comp.
- Pin 9 = VCS
- Pin 10 = I_{IN}
- Pin 11 = V_{CC}
- Pin 12 = VCD
- Pin 13 = VCR
- Pin 14 = GND
- Pin 15 = VCA
- Pin 16 = ATK Out

Figure 8. The circuit diagram of the CEM 3310 envelope generator. Very few additional components are required. The normal ADSR envelope voltage is produced.

necting a ± 300 Hz square wave signal and a full 0... +10 V swing (control voltage range!) to either CV1 or CV2. With no input signal applied, the level at the filter output is reduced to a minimum with P3.

Practical results

The noise level of the circuit given in figure 7 proved to be around 78 dB, which is well within the manufacturer's specifications. Distortion is low: around 0.12% depending on the frequency and signal amplitude. The break-through of a 10 V control voltage jump was found to be only 25 mV once P3 was calibrated (52 dB below the signal level, in other words). At the output, the resonance control voltage was measured as -40 dB.

The maximum output signal of the filter was around 13 V peak-to-peak. When used as an oscillator a fairly symmetrical sine wave form was obtained.

The transition from filter to oscillator is remarkably smooth. The filters did not 'howl' at critical points like some of their counterparts. This is partly due to the uncritical type of filter used and partly to the modified linear curve featured by the resonance VCA. At higher values the feedback slows down and so allows for fine adjustment.

Since the remaining temperature drift is around 0.3% per degree centigrade, it is hardly worth compensating. As far as filters are concerned, the total drift may

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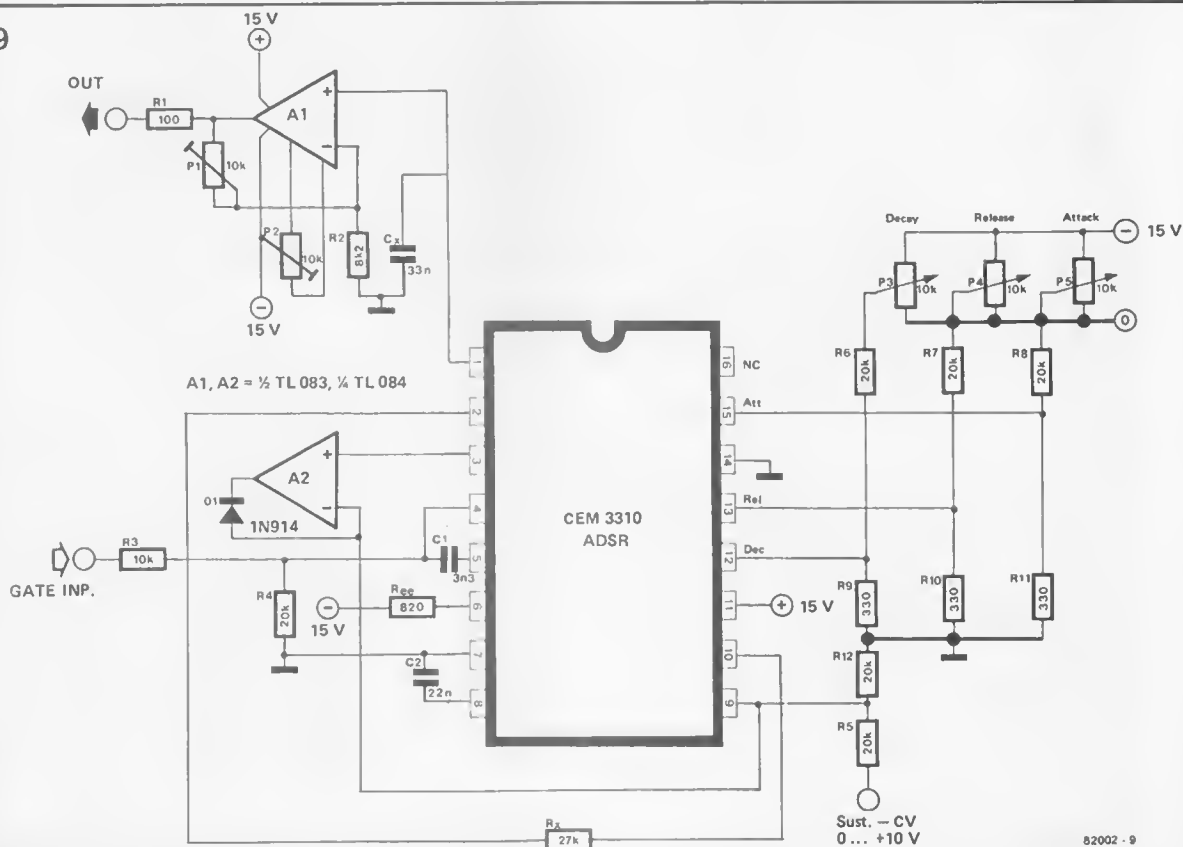


Figure 9. The complete circuit diagram for a standard ADSR generator using the CEM 3310.

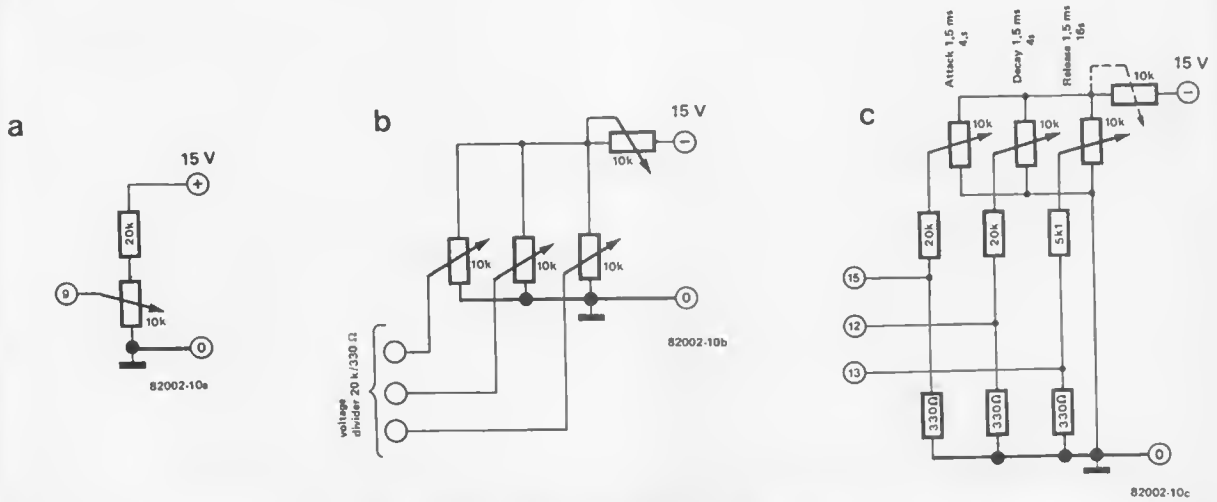


Figure 10. Potentiometers offer various preset facilities in the envelope generator in figure 9. Figure 10a shows a possible sustain preset and figure 10b shows how the Attack, Decay and Release times can be adjusted simultaneously with the aid of an additional potentiometer.

will be 6% (at 20° temperature change, for instance) and still not affect the filters, quite apart from the fact that such drastic changes in temperature hardly ever occur.

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The envelope generator CEM 3310 IC

The IC requires very few external components, as shown in figure 8, and has excellent features. The attack-decay-sustain-release times are voltage controlled over an (exponential) range of about 1 : 50,000. The conversion factor is 60 mV per decade, which corresponds to 18 mV per octave. Over an operating range of 1 : 10,000 the voltage must therefore vary by 240 mV. This can be done with the aid of a voltage divider which derives the voltage from the supply. The sustain level is determined by a linear control voltage.

If several envelope generators are used, all the control voltage inputs can be driven in parallel from a single potentiometer. A good control range is obtained when C_x is 33...68 nF. R_x should not be more than 240 k when the internal buffer is used and not more than 1 M when an external FET opamp acts as a buffer. The time values are smallest at 0 V and increase when the control voltage becomes negative. The circuit in figure 8 gives the longest periods for -5 V at the control inputs (corresponds to -240 mV at the pins). The sustain level voltage must be in the 0...+5 V range.

Figure 9 shows an example of an envelope generator using the CEM 3310. Potentiometers are provided to set the period times and there is a control input for the sustain level.

The envelope signal is produced across C_x . P1 sets the gain of the output amplifier, A1; P2 sets the output slightly negative (about -10 mV) under

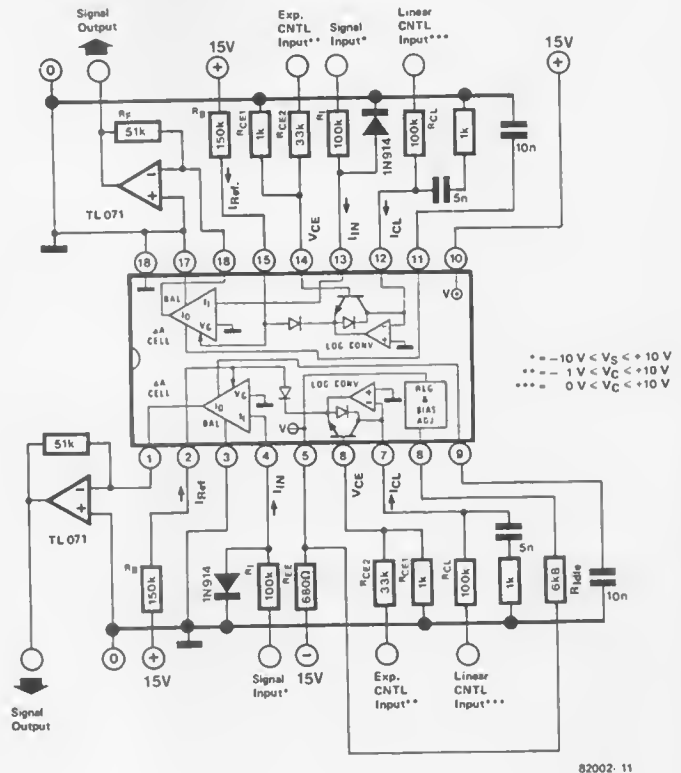
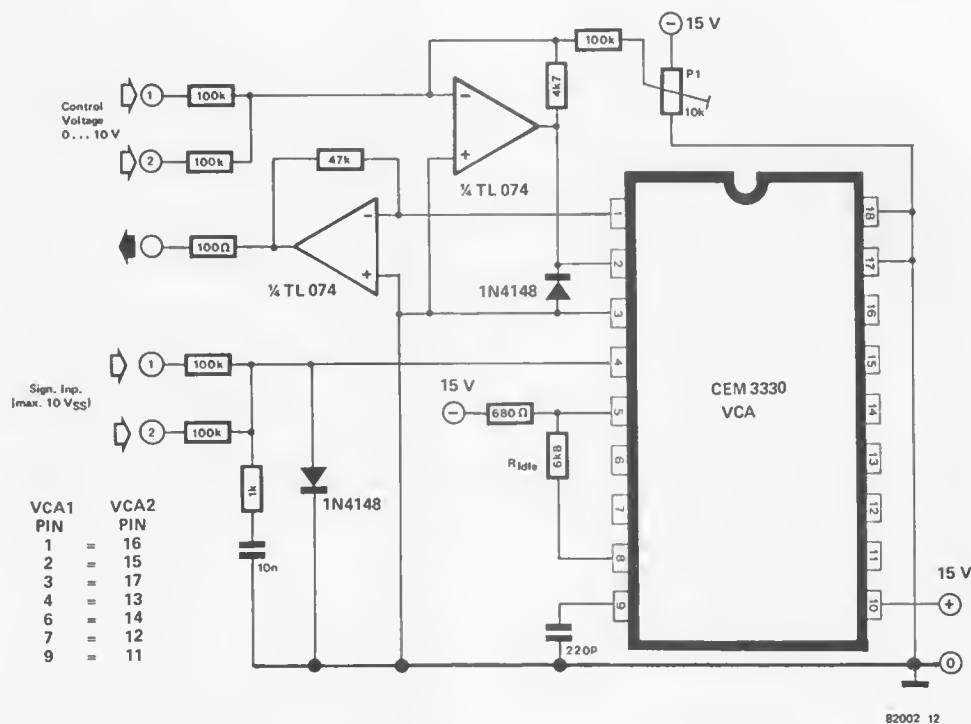


Figure 11. The circuit diagram of the DUAL VCA CEM 3330. This IC contains two voltage controlled amplifiers which can be operated either linearly or exponentially.



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Figure 12. The complete circuit diagram of the CEM 3330 for linear control. The second VCA is identical to the first, except for the pin assignment.

quiescent conditions, to turn following VCAs hard 'off'.

A useful reference voltage appears at pin 3: the comparator threshold for the envelope's peak value. To prevent this level from being exceeded by the sustain voltage, the latter is 'clamped' to it by means of an additional opamp. At pin 4 there should be a gate voltage of 3...15 volts. It is a good idea to add an attenuator at this input, to protect the IC.

A 3n3 capacitor derives the trigger signal required for pin 5 from the positive gate edge. R_{EE} is the series resistor in the negative supply.

The potentiometers and voltage dividers provide the 0...-240 mV control voltages. Several alternative arrangements are possible, and figure 10 gives a few examples. The circuit shown in figure 10a may be used to preset the sustain level using a potentiometer, instead of the voltage divider at pin 9. In figure 10b, an additional control reduces all the time values simultaneously. When P6 is turned fully clockwise, for instance, the slowest attack will only take 25% of the normal time. Since the total voltage across every potentiometer also drops by 25%,

the potentiometers can be regulated with greater accuracy. Figure 10c shows the basic ranges for attack, decay and release.

The dual VCA: CEM 3330

Two identical VCAs are included in an 18-pin DIL package and operate according to the same principle as the CA 3080 OTAs. Each VCA has its own exponential converter so that they can all be controlled either linearly or logarithmically.

Resistor R_{IDLE} at pin 8 of the ICs sets the bias current — the smaller the value, the greater the current, and vice versa. A low value resistor (not less than 2 k) leads to less distortion, a high slew rate and less control voltage suppression. If a greater value (up to 200 k) is chosen for the resistor, the noise will be reduced, but at the same time the distortion will be increased and the band width and slew rate will be reduced. A good compromise between the two extremes is a value of about 6k8.

The VCA in practice

The circuit diagram as published in the Curtis data sheets required some modifi-

cation. Instead of connecting the RC network 1 k/10 nF between pin 7 and ground, it should be between pin 4 and ground. The capacitor at pin 9 can then be reduced to about 220 pF. If the VCA is to be controlled by way of the EXP.CONTR.INP. pin, either pin 7 or pin 12 must be connected to 10...15 V by way of the resistor R_{CL} (100 k).

The amplifier gain is decreased by 6 dB for each 18 mV rise in control voltage. Since most envelope generators already produce logarithmic control voltages, the circuit in figure 12 only uses the linear control voltage input. The circuit for one VCA is shown; the second is identical except for the pin numbers (see figure 11). P1 is the only calibration point and must be adjusted for unity gain at the maximum control voltage level.

The circuit has an excellent linearity of 0.1...0.2%. At 18 kHz bandwidth, the signal-to-noise ratio was 90 dB. The crosstalk between the two VCAs is 60...70 dB. ◀

UHF equipment is rather sensitive to external influences. It is well known that a tuned circuit, for instance, can be 'detuned' simply 'by pointing at it'. Metal components in the vicinity of tuned circuits will also affect their operation at the high frequencies involved here. As a rule (even at lower frequencies) the circuits can 'see' each other, pick up each other's frequencies, if they are in close proximity. To what extent this affects their tuning depends on their radiated power (the transverter will radiate about 10 mW of power without the help of the output stage). Unless effective measures are taken to reduce this phenomenon, therefore, the transverter is likely to cause considerable problems (with the G.P.O. in particular).

It does not matter in which order the screens are fitted, but before soldering is started holes will have to be drilled to allow for connections between the sections, for the BNC connectors and for the supply connections. Figure 10 shows where the connections are to be made. The four solid white blocks are feed-through capacitors of about 1 nF. These are used on the lower side of the board and supply power to the various sections in the transverter. The signal feed connections are mounted on the upper side and since feed-through capacitors are of course prohibited here, low-capacitance teflon leads must be used (see photos 8 and 9). In addition, several other screens will have to be included here and there. The dummy load, in particular, has to be

construction and calibration

70 cm transverter (2)

Now that we know the theoretical principles behind the transverter circuit (see Elektor 74, p. 20), it is time to deal with the construction and calibration. Using the printed circuit boards ensures straightforward construction but the whole of the circuit has to be screened. Calibration is fairly critical.

All in all, the job at hand is not an easy one which is why every step in the procedure must be followed in detail.

P. de Winter PEØPJW

Clearly, success depends largely on the case and on the screening of and between the radiating components. Great care should be taken when putting the following instructions into practice.

Construction

All the components, except for the transmit/receive relay and the non-stabilised power supply can be incorporated on the single large board. This is divided into four separate sections, each containing one of the circuits shown in figure 6...9 (see part 1, June 1981).

The board, shown full-size in figure 10, is designed to allow the transverter to be built in one of two ways. The board can either be left in one piece or it can be cut into four separate sections. Cutting the board is a little difficult, but has the advantage that each section can be screened more easily from the others. If the board is left in one piece, the screens will have to be placed on the dotted lines on both sides of the board. Whichever method is chosen, the screens must be at least 3 cm high on the upper side and 1 cm on the lower side. It is best to use 0.3 mm thick tin or copper/brass plate. Copper or brass is softer and therefore easier to cut (even with ordinary scissors), but they are of course more expensive metals.

The screens should be soldered along their full length on both sides of the board. The necessary 'plumbing work for the upper side' is shown in photos 3...5 (part 1, June '81) and that for the lower side is shown in photos 6 and 7. The four edges of the entire board are also provided with screening plates to create a rectangular box on which a removable base and lid can be placed.

The vertical edges can best be made from four separate strips, in other words, don't bend one long strip into a rectangle, as this only causes tension in the metal when it is soldered at both ends.

well screened to prevent it radiating to other sections in the transverter. The component overlay is marked with a dotted line for this purpose. Photo 4 (see part 1) shows clearly how the dummy load is screened on the upper side and photo 6 shows the lower side.

A screen will have to be mounted on the lower side underneath the transmission converter between L26 and L28 to prevent the 374.4...376.4 MHz signal from radiating through. After all, any radiation that can be suppressed is worth the effort. The screen runs alongside L28 and its position can be seen in photo 7.

Fitting the screens constitutes the first step in construction of the circuit. No components are mounted until this has been completed as they would make it very difficult to solder the edges (especially the resistors in the dummy load). So: solder the screens first and then the components.

Mounting the components

Most of the components are easy enough to mount. It is best to follow the order in which they appear in the parts list. The ones marked with an asterisk (*) however require special attention. These are R4, R8, R29...R31 and R_a and R_b, which are mounted during calibration (if necessary). Capacitors C42, C54, C59, C76 and C82 improve the decoupling of the strip lines to which they are connected. These capacitors therefore have to be mounted directly on the strip lines, in other words on the copper track side of the board (see photo 7). Their wires have to be as short as possible. They are not shown on the component overlay, but as can be seen in figures 7...9 (see part 1), they are in parallel to C41, C55, C60, C77 and C83, respectively.

As far as the earthed components are concerned: always solder them on both sides of the board! The copper strips in

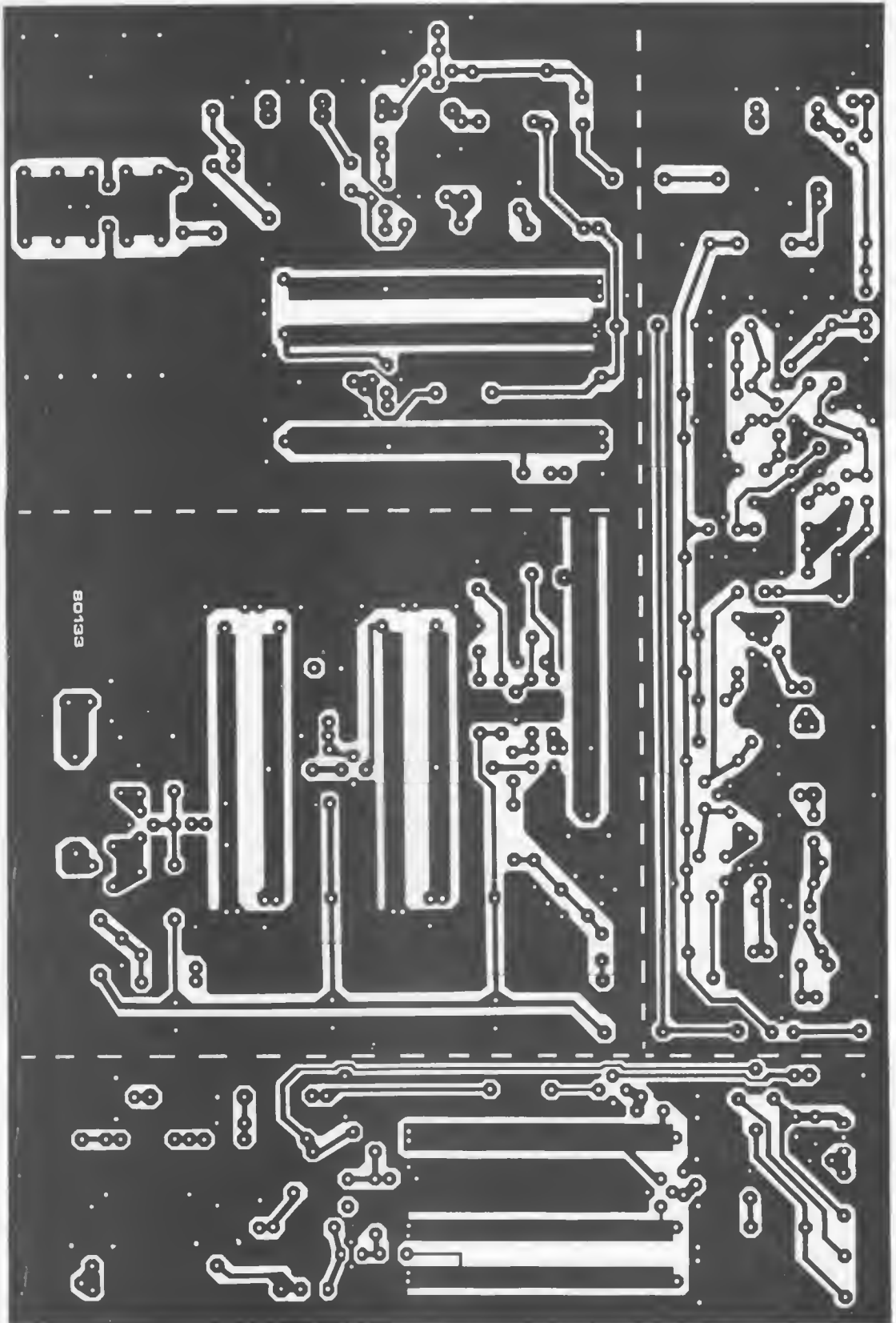
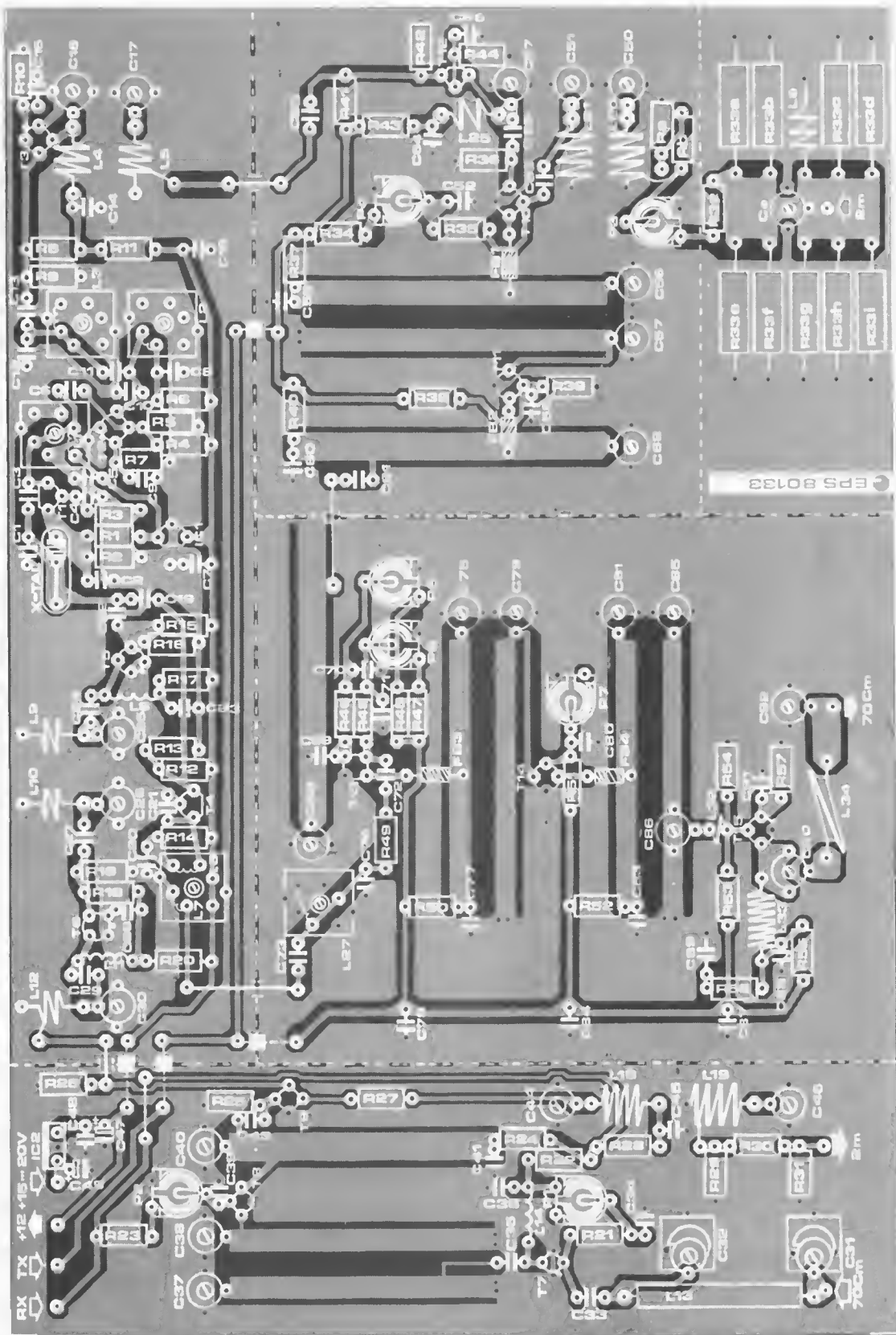


Figure 10. The printed circuit board and the component overlay of the transverter. The four sections have been combined into a single board. A minor modification to the component side is required before assembly begins. The mounting hole under the C of C69 must be opened with a spot cutter to prevent the capacitor from shorting the upper and lower sides of the board.



LEPS 80133

70cm

2m

the track pattern should be treated as components in this respect. The sockets which are grounded must also be 'plated through'. This is especially true for L15, L16, L23, L29 and L31. For this purpose a length of wire can be inserted through the two holes in the base in order to short the upper and lower sides of the board.

In addition to the parts list the photographs give an idea of the way in which to make the coils. The coil in the output stage, L34, needs to be constructed with special care, as this largely determines the output power of the transverter. Using a 6.8 cm length of 1.2 mm diameter silver-plated copper wire (CuAg) it should form a circle with a 13 mm inner diameter. The turn obtained is lengthened until it is 4 mm long. The details are illustrated in figure 12.

Calibration

The entire transverter can be calibrated with a little more than a multimeter. The 'little more' happens to be a diode test head which equips the multimeter with the additional indication facility for (U)HF AC voltages.

Figure 11 contains the circuit diagram for the 'measuring head' and pick-up coil. When connected to a multimeter with an internal resistance of about 30 k/V or more the indication obtained is sufficiently clear to allow the various trimmers to be calibrated. That is all that is needed for correct adjustment. If available, the calibration results may be checked with a grid dipmeter. A TV set may be used as a test receiver during an overall test of the circuit.

To prepare for calibration, P1 is set at maximum resistance and all the other presets are turned down (towards earth). All the trimmers are set roughly in the mid position.

Crystal oscillator

Using the stabiliser on the receiver board or an external 12...13.8 V power supply, the crystal oscillator board is supplied with a voltage and the 78L08 (IC1) may be checked: 8 V across C5.

The crystal oscillator is correctly tuned by connecting the multimeter as an ammeter in series with the power supply line and by slowly adjusting L1. The ammeter will indicate a gradually rising level until a peak value is reached, after which the current will drop very abruptly. At this point the oscillator switches off. The oscillator should always start spontaneously at the peak setting when the power supply is switched on and off repeatedly. This will be the case whenever the ammeter returns to its preset value quickly. In the prototype this was a level of about 50 mA.

The 57.6 MHz amplifier stage

Together with L6/L7 this stage is



Photo 6. The dummy load will have to be screened on both sides of the board. Here the upper side is shown. The screens must be soldered along all their joining edges.

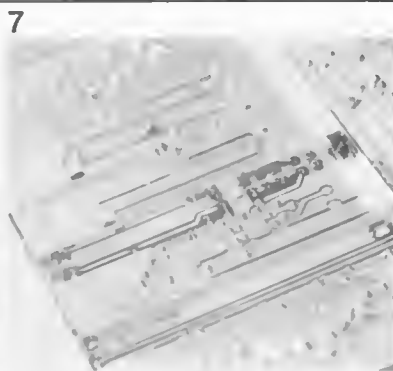


Photo 7. The screen between the 374.4 and the 432 MHz sections of the output transverter. As a result, the 374.4 MHz signal will be better suppressed.

Parts list to figure 10

Resistors:

all 1/8 watt unless stated otherwise

R1, R15 = 68 k
 R2, R5, R13 = 15 k
 R3 = 470 Ω
 R4 = 180 k... 270 k*
 R6, R7, R10, R11, R14, R17, R20, R24, R27,
 R28, R37, R40, R43, R44, R49, R50, R52,
 R29*, R31* = 100 Ω
 R8 = 68 k... 82 k*
 R9, R16, R19 = 4k7
 R12 = 150 k
 R18, R21, R38 = 47 k
 R22 = 2k7
 R23, R25, R34, R35, R36, R38, R45, R46, R47,
 R48, R51 = 100 k
 R26, R3* = 56 Ω
 R32, R54 = 1 k
 R33a... f = 470 1 watt
 R30* = 82 Ω
 R41 = 27 k
 R42 = 2k2
 R53 = 8k2
 R55, R57 = 47 Ω
 R56 = 10 Ω
 Rb* = 1 k
 P1, P4, P5, P6, P7 = 100 k preset
 P2 = 50 k preset
 P3 = 100 Ω preset
 * = see text

Capacitors:

all ceramic unless stated otherwise

C1, C42*, C54*, C59*, C76*, C82* = 47 p
 C2 = 22 p
 C3, C21, C74 = 12 p
 C4, C5, C8, C9, C20, C48 = 10 n
 C6 = 82 p
 C7 = 100 n MKM
 C10, C12 = 4p7
 C11, C13 = 1 p
 C14, C15, C18, C23, C24, C28, C29, C33, C34,
 C35, C36, C39, C41, C43, C45, C52, C53, C55,
 C58, C60, C61, C63, C64, C65, C66, C69, C70,
 C71, C77, C78, C80, C83, C84, C87, C88,
 C91 = 1 n
 C16, C25, C26, C30, C37, C38, C40, C75, C79,
 C81, C85 = 1.5... 6 p trimmer
 C17, C56, C57, C62, C67, C68,
 C86 = 2... 10 p trimmer
 C19 = 10 p
 C22 = 68 p
 C27 = 2p7
 C31, C32 = 2... 10/13 p foil trimmer
 C44, C46, C50, C51, C90,
 C92 = 2... 25 p trimmer

C47, C49 = 10 μ/25 V tantalum

C73 = 2p2

C89 = 47 n MKM

Semiconductors:

T1, T4, T12 = BF 494
 T2, T3, T5, T6 = BF Y 90
 T7 = BFT 66 (NB: BFT 66S from SGS Ates
 has a different lead configuration)
 T8, T9, T10, T11, T13, T14 = 8F 905
 T15 = 2N3866 or 8F Y 90 or BFW 16A
 IC1 = 78L08
 IC2 = 7812

Coils:

Kaschke coil former and 0.3 mm enam.
 copper wire
 L1 = 9 turns
 L2, L3 = 5 turns
 L6/L7 = 9 + 2 turns
 L27 = 6 turns

Striplines air cored inductor

L4 = 3 turns 1 mm CuAg φ 6 mm
 L5 = 3 turns 1 mm CuAg φ 6 mm
 tap of ¼ turns from the 'cold' end
 L8, L11, L14 = 1 μH Toko
 L9/L10 = 2 turns 1 mm CuAg φ 6 mm
 L12 = 2 turns 1 mm CuAg φ 6 mm
 (for tap see text)
 L13 = 3 cm long, 4 mm wide
 copper strip (0.7 mm thick)
 L15, L16, L17, L22, L23, L24, L26,
 L28, L29, L30, L31 = striplines
 L18 = 4 turns 1 mm CuAg
 L19 = 4 turns 1 mm CuAg
 tap at ¼ turn

Note:

L1B and L19 are wound around an 8 mm drill
 and extended to 8 mm
 L20 = 4 turns 1 mm CuAg φ 6 mm
 tap at ½ turn
 L32 = 1 turn 1 mm CuAg φ 5 mm
 L33 = 7 turns 0.4 mm enam. copper wire
 φ 3.5 mm extended to 8 mm
 L34 = Ca. 1 turn (see text)
 1,2 mm CuAg 6,8 cm length

Miscellaneous:

57.6 MHz or 96 MHz crystal without socket;
 solder case to ground
 FB1... 4 = 5 mm ferrite bead

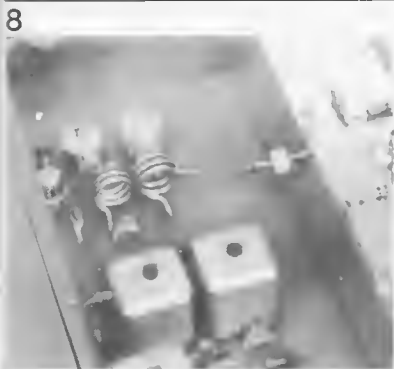


Photo 8. A view of coils L4 and L5. Note they are wound in the same direction and look at the position of the tap! One of the teflon leads can also be seen.



Photo 9. The air coils L9, L10 and L12 belonging to the 288 MHz multiplier. L9 and L10 are bent slightly towards each other to critically couple the band pass filter.

calibrated by adjusting for a maximum meter reading using the diode measuring head (without the pick-up coil) connected to L7. The multimeter is switched to the 50 μ A measuring range. The frequency can be checked by feeding the signal to a TV set with the aid of a pick-up coil. The TV should be tuned to channel 3 (VHF). The frequency will be correct if the normal off-station picture goes dark when the pick-up coil is held close to L6/L7.

Tune the multiplier to 230.4 MHz

Coils L2 and L3 have to be set at 115.2 MHz. In order to determine the point at which the circuits are in resonance, the collector current of T2 must be measured by connecting the multimeter across R6 (1 V/10 mA). The current will be at a minimum level if L2 is in resonance and will rise when L3 is correctly tuned. If this is impossible to adjust because T2 is not conducting, R4 may have to be included. The value of R4 must be large enough for the collector current to be about 0.5 mA when the oscillator is switched off. Depending on the base emitter voltage, its value will be somewhere between 180 and 270 k Ω . The same refers to R8 with respect to T3. The value of R8 will then be between 68 and 82 Ω . In this case the collector current is measured across R11 (about 0.05 V). Coils L4 and L5 can now be brought into resonance at 230.4 MHz with the aid of C16 and C17.

As is clear in photo 8, the two coils must be wound in the same direction. The diode measuring head is linked to the L5 tap at $\frac{1}{4}$ turn (see photo 8). Before they are calibrated, however, coils L4 and L5 will have to be moved towards each other (but not touching each other and thus cause a short circuit!). The multimeter is then switched to the 50 μ A range again. First C16 is used to set a peak level, after which C17 is finally set to a maximum level. This can be repeated several times until the maximum level has definitely been reached. Finally, coils L4 and L5

are moved away from each other until the indicated level starts to drop. The circuits will then be coupled critically. Then the whole multiplier can be readjusted with L2, L3, C16 and C17, and the tuning can be checked again, if necessary, with the TV set, tuned this time to a frequency slightly above channel 12. Most TV sets can just about pick up the 230.4 MHz signal.

Adjusting the multiplier to 288 MHz

This particular adjustment is a lot easier to accomplish than the previous one. The diode measuring head is now connected to the tap of L12. Coils L9 and L10 are bent towards each other. Only the trimmers have to be set at a maximum indication level. First let's deal with the band pass filter and C25 and C26. These trimmers must be adjusted to a maximum in turn until the result cannot be improved on. The output can then be 'peaked' with C30. Photo 9 shows the three coils involved in this calibration stage. As in this case of the multiplier which was adjusted to 230.4 MHz, the band pass filter is critically coupled to L9 and L10. The method used for this is the same as for the other multiplier.

The reception converter

The output of the reception converter is fed directly to the 2 metre receiver via a 50 Ω attenuator, R30. This resistor, however, should be replaced by a wire link for the purposes of calibration. Later depending on the amplification factor of the converter and the sensitivity of the receiver, an attenuator network (-5 or -10 dB) may be mounted in R29... R31's positions. The band pass filter including L18 and L19 may now be adjusted with the aid of C44 and C46 to a maximum noise level. This section is illustrated in photograph 10. Watch the coil coupling! The distance between L18 and L19 is determined by that between the two centre

mounting holes.

The operational range of T7 (BFT 66) is set with the aid of P1. This potentiometer is adjusted so that a voltage level of 6 V appears at the junction of R22, C36 and L14. With C31 and C32 turned to minimum capacitance, a test signal may be fed to the aerial connector socket of the converter.

This may be produced by a powerful local 70 cm station. A suitable frequency is 432.3 MHz, which is the third harmonic of 144.1 MHz. The rear receiver must be tuned somewhere around 144.3 MHz (depending on the accuracy of the 57.6 MHz crystal). With the provisional adjustments so far, the test signal should be fairly audible already. The S meter inside the receiver can now be used as a measuring instrument. C37, C38 and C40 set the circuit at a maximum level indication.

During calibration P2 was grounded, so the amplification factor of T8 will be low. After all the trimmers have been correctly set, P2 may now be turned all the way up. The final calibration concerns the input pi-filter. This requires a weak but stable signal that is received by way of the aerial. The pi-filter which not only works as a low-pass filter but also acts as an impedance-adjustment network, can now be adjusted to a maximum signal/noise ratio. First C32 is set, then C31 and then C32 again until an optimum result is obtained. Note: a maximum noise/signal ratio does not usually correspond to maximum noise or signal reception. The correct level is reached, when even very faint signals are clearly audible. This calibration is therefore carried out entirely 'by ear'.

The transmitter input converter

A 2 metre transmitter having an output between 1 and 10 W is required to produce an unmodulated (FM) control signal to facilitate calibration. In order to keep the dissipation produced by both the dummy load and the transmitter to a minimum, it is advisable to maintain the power output to below 5 W, as low as possible in fact.

Before switching on the transmitter, adjust the 230.4 MHz amplifier. For this the measuring head is linked to the junction of gate 1 of T10 and C65. C67 sets a clearly maximum level (if necessary, modify the physical shape of L25 a little). This adjustment affects the multiplier circuits, so that C16 and C17 will have to be reset. The three trimmers will need to be adjusted several times, as usual. This can be checked by measuring the collector current of T12. This is done by measuring the voltage across R43, which will be at a minimum if the circuit is well tuned.

The 2 metre transmitter may now be switched on, after which the diode measuring head and the pick-up coil (see figure 11) are held near L20. P3 is now turned up until a valid result is obtained on the meter display (mid-scale

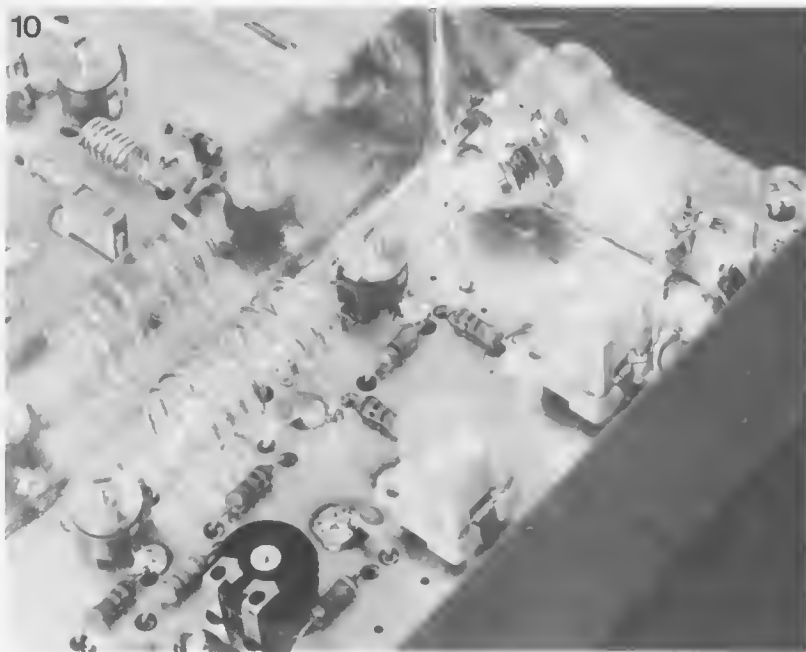


Photo 10. The output of the reception converter consists of the air coils L18 and L19, sometimes followed by an attenuator network. Note how these coils are mounted!

level, for instance). The pick-up coil is then placed between L20 and L21. C50 and C51 are then adjusted for a maximum reading. This may mean having to reduce the control level with P3.

The pick-up coil is now removed and the measuring head is connected to the tap of L22 (this is the drain of T10 behind FB1). During the following calibrations the 2 m transmitter will of course need to be switched on, as this produces the signal that needs to be converted! C56 is adjusted for a maximum reading, after which C50, C51 and C67 (measuring head at same test point) are readjusted. Next the measuring head is moved to C61. Again, a maximum level is sought alternately adjusting C56 and C57 and then C62. Finally, P4 is used to find the maximum level (in the mid position). After this rough calibration of the transmitter input and output converter may be carried out.

The transmitter output converter

During the first part of the calibration procedure, this converter does not need a control signal, because modification of the 57.6 MHz input circuit is involved. The diode measuring head is connected between R49 and C72, after which the core (not shown in figure 9!) of L27 is set to give a maximum reading. The circuits on the oscillator board are affected by this, so L6 and L7 will have to be readjusted. This procedure has to be repeated a couple of times.

The measuring head is now linked to the tap of L28 (this is the drain of T13 behind FB3) and C68 is adjusted for a maximum when the transmitter is switched on. C62 will also have to be

and this corresponds to a voltage of 1 V across R52.

Before calibrating the output stage, a 56Ω resistor must be placed across the output as a load and the diode measuring head is placed across this. The remaining circuit can now be calibrated, starting with C81 and C85. Since a band pass filter is involved, these trimmers are set for a maximum level, beginning with C85. C86 (in the mid position) is left in peace for the moment. Then it is the turn of the output circuit, for which C90 and C92 are adjusted for a maximum indication. This completes the rough calibration of the transverter. Now, with the diode measuring head across the 56Ω load resistor at the output, the calibration of the transmitter section can be slightly improved. This results in a little more output power and a clearer signal. Again, a maximum reading is sought with all the adjustments.

Briefly, the final 'tweaking' is carried out in the following order. First C62 and then C68 is repeated with the final adjustment on C68. The same for C6/C7 and C27, P5 and P6, C75 and C79, C81 and C85. Now C86 can be peaked (set at not more than 50% ca-

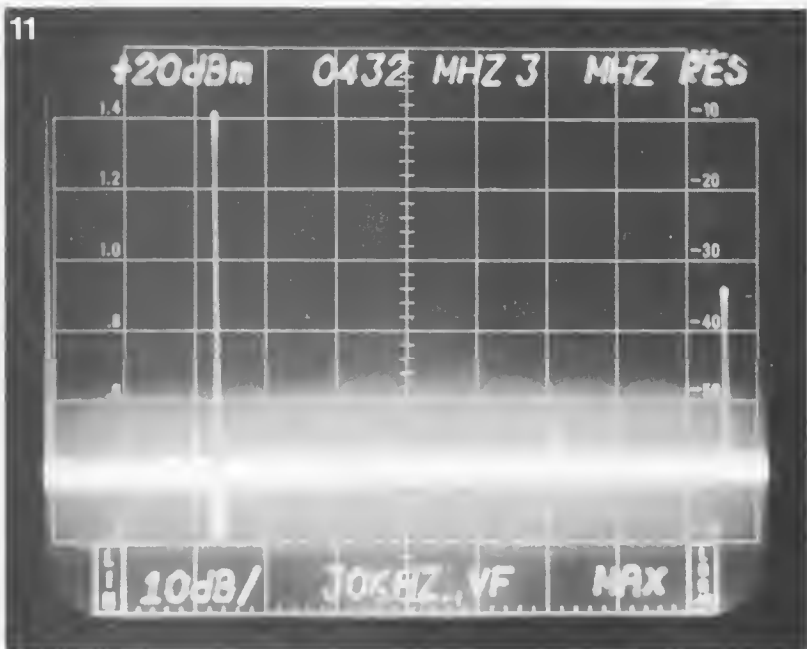


Photo 11. The 0 ... 1.8 GHz spectrum. The output power is 50 mW (+17 dBm) and the output transistor used is a BFY 90 type.

readjusted. Trimming L27, L6 and L7 often leads to a further improvement. With the measuring head still at the same test point, P5 and C75 are also set for a maximum. C81 can increase the reading further, after which the procedure at this test point may be brought to a close by setting P6 to a maximum. The drain current produced by T14, measured across R52, is set with P7. The correct value will be around 10 mA

pacitance). This affects C85, so that this will have to be trimmed. Finally, C90 and C92 are dealt with.

The transverter's linearity is partly determined by the position of P3. If the maximum input power is less than 10W, P3 will have to be turned up until a drop in control power directly results in a reduction of output power. If this is not possible, R_a and R_b will be required. The power produced by T15 is

about 50 mW, which corresponds to a voltage of about 1.3 V across the 56 Ω resistor as measured with the diode measuring head and the multimeter. At the given level the quiescent current passing through T15 is about 10...12 mA, which corresponds to a voltage level of around 0.5 V across R55. A little more or less will of course be harmless, provided the quiescent current does not drop below 1/10 of the collector current during full modulation.

Photo 11 shows the complete 0...1.8 GHz spectrum. In this instance a BFY 90 was used in the output stage. This explains the rather powerful fourth harmonics (1728 MHz); a better performance is obtained with a 2N3866. The spectrum analyser marker indicates the 432 MHz signal. This means that the signal peak shown is lower than the value measured. In reality the peak extends to +17 dBm (= 50 mW).

As photo 2 in part 1 shows, interference suppression is better than 64 dB within the band. Outside the band the figure is nearer 55 dB which is not good enough for direct transmission. The picture in photo 11 can be considerably improved by placing a linear amplifier after the transverter, because the amplifier will only amplify within the band pass range, provided it is well adjusted. Readers who wish to go on the air with just this 50 mW level, however, will have to include another band pass filter behind the transverter to keep their conscience as well as the ether clear.

11

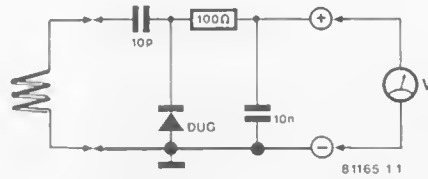


Figure 11. All the calibrations can be carried out with an ordinary multimeter, provided this diode measuring head is added to it. The pick-up coil is only used during 'wireless' measurements.

12

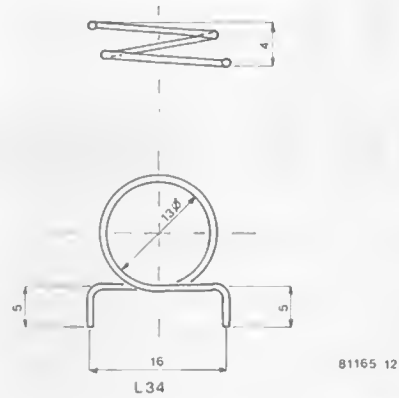
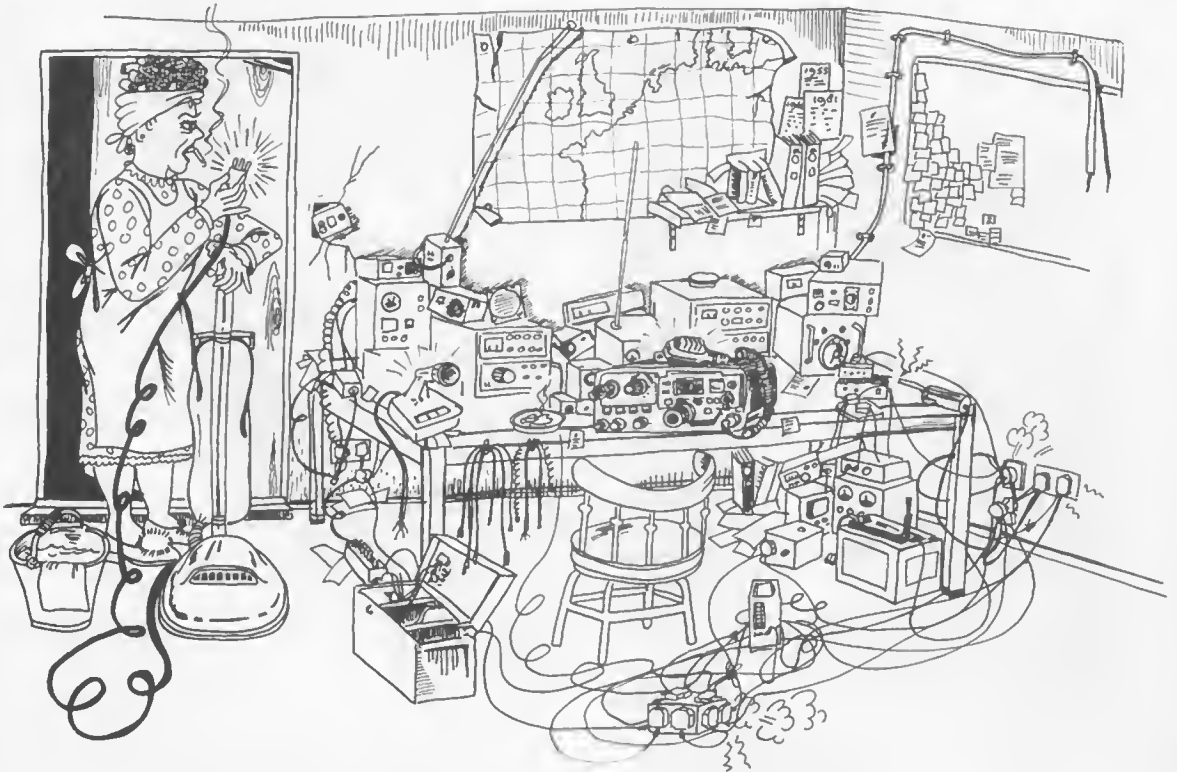


Figure 12. The constructional drawing for L12. The method shown here will provide the best results.



Digital panel meters have one major snag and that is their 'floating' input. This can cause problems resulting in display errors. The reason for this will be explained later. On the other hand, they also have many significant advantages: since they are based on ICs, they require very few external components and therefore take up little space. The IC already incorporates an automatic zero adjustment, an automatic polarity indicator, a clock oscillator and a reference voltage source. The IC used here can also drive a display, has provision for an external reference voltage, indicate an over-range and measure the input voltage off-earth (although the latter will cause problems as mentioned

LCD panel meter

a versatile 3½ digit display

The use of digital voltmeters as panel meters is becoming increasingly popular these days. The version described here was originally designed for the barometer circuit published in the September issue, but it can be used for many other purposes in level measuring devices, multi-meters, power supplies, etc.

above). We will go into the various power supply methods later, but first let us look at the circuit itself.

The circuit

For the advantages offered, the circuit is surprisingly simple, as shown in figure 1. Only very few components are needed in addition to the 7106 IC and an LCD display. The only other active element in the circuit, the VMOS FET BS170 is merely required for the decimal point conversion and could even be omitted. The frequency of the IC internal oscillator is determined by R5 and C2. This will be about 45 kHz here. The dual slope measurement process occurs three times per second. Readers who would like to pursue the details will find them in the article 'Universal digital meter' published in January 1979.

The automatic zero setting is adjusted by the value of the capacitor C4. It will be correct when '000' appears on the display with the input shortcircuited. C3 acts as a charge capacitor for the reference voltage during the automatic zero adjustment.

The IC contains a highly temperature-stable reference voltage source. This is about 2.8 V typ. and appears between pins 1 (+U_B) and 32 (COMMON). The reference for the integrator is derived from this voltage. The full-scale indication on the display will correspond to exactly half the reference voltage. For example: full scale → 200 mV reference

voltage → 100 mV. This voltage is connected to input REF HI by way of P1. The input voltage is divided across R7/R8 into IN LO IN HI. Voltages above 200 mV can be measured when R8 has the following values: 120 k (equivalent to 2 V full scale), 12 k (equivalent to 20 V full scale) and 1k2 (equivalent to 200 V full scale). Since the voltage is not divided in a precise 1 : 10 ratio, the display indication has to be corrected with P1. Another solution would be to use a convertible input voltage divider, in which case R8 could be omitted.

The power supply

The panel meter can be powered either symmetrically or asymmetrically.

1. Symmetrical power supply: the meter input is grounded. If power provided is ± 5V, then R1/D1 and R2/D2 are not required for stabilising the supply. At higher symmetrical supply voltages the values of R1 and R2 are calculated as follows:

$$R1 = \frac{+U_B}{V} - 4.7 \text{ k}\Omega \text{ and}$$

$$R2 = \frac{|-U_B|}{V} - 4.7 \text{ k}\Omega$$

In both cases 'B' and LN LO are connected to each other. The power supply and the panel meter both have the same ground connection.

2. Asymmetrical power supply: the meter input is 'floating' and subject to the problems mentioned earlier: the meter input can only 'process' voltage levels between 0.5 V below +U_B and 1 V above -U_B. If IN LO is connected to the ground of the power supply -U_B, input voltages have to be at least 1 V before they can be indicated... that is, unless the scale is adjusted. Something will have to be done to remedy this. The solution is to connect the asymmetrical supply voltage between +U_B and -U_B, point 'A' to IN LO, thereby causing a floating off-earth input voltage to be produced. The asymmetrical voltage can be provided by a 9 V battery which has a life-span of about 200 operational hours at a maximum current consumption of 1.2 mA.

Construction

The printed circuit board and the component overlay are shown in figure 2 and as can be seen, it is very neat and compact indeed. IC1 should be mounted on a socket. The LCD display is placed in IC connectors on the copper side of the board. Take care — the display is very fragile! By the way, almost any type of display is suitable. A few suggestions have been given in the parts list. Readers who have difficulty spotting pin 1, should hold the display up

against the light to see the position of the decimal point. The decimal point must be at the lower edge when the display is mounted. This is where the connections are marked for the decimal point ('1' ... 'M').

Calibration

This is very straightforward. A known voltage level is connected to the input and P1 is then used to adjust the display to this value. Obviously, care must be taken to ensure that the correct measuring range was selected at the input by means of R8 or a voltage divider. Finally, the value indicated on the panel meter may be compared to that of an accurate DVM at the same input voltage. The comparison should be carried out over a period of time and any deviation should be corrected.

Using the panel meter

Right at the beginning of this article we mentioned how versatile the panel meter is. Nevertheless, if ground referenced voltages are to be measured, the power supply voltage will have to be symmetrical. If, for instance, the meter is to be used as a DVM in power supplies, a separate power supply may well have to be constructed!

If, on the other hand, the meter is to be connected to the barometer published in September, there will be no problem.

The various connections are carried out as follows. The supply voltage is derived from the barometer's power supply. The +U_B voltage of the panel meter is linked directly to the positive terminal of C8 and the -U_B voltage is linked to the negative terminal of C9. IN HI is connected to the temperature and pressure outputs of the barometer via a switch. A second pole of the switch makes sure

Parts list

Resistors:

R1, R2 = 2k2
R3 = 22 k
R4, R7 = 1 M
R5 = 100 k
R6 = 47 k
R8 = 120 k
P1 = 2k5 10 turn trimmer

Capacitors:

C1 = 10 n
C2 = 100 p
C3 = 100 n
C4 = 470 n
C5 = 220 n

Semiconductors:

D1, D2 = 4V7/400 mW zener
T1 = BS 170
IC1 = ICL 7106
LCD = 3½ digit (4305 R 03/data module — 3901, 3902/Hamlin — SE 6902) Standard-version with 13 mm character height

1

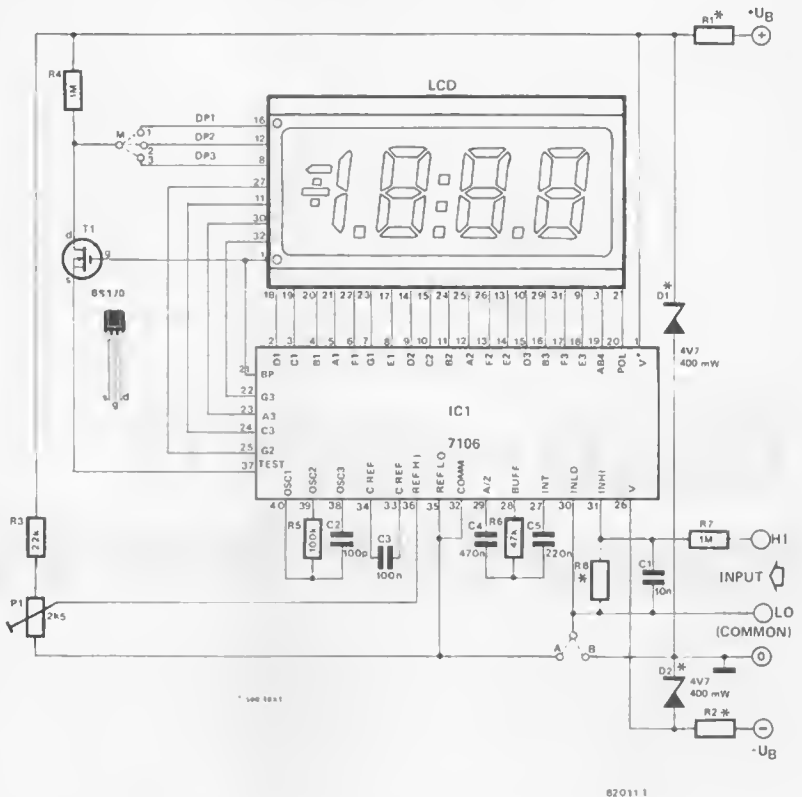


Figure 1. The panel meter circuit. It is based on the well-known 7106 DVM IC which directly drives an LCD display. The supply voltage may be selected to provide either grounded or 'floating earth' measurements.

the decimal point is correctly positioned. A three-way switch with two poles is needed for the humidity sensor for it to be extended into a miniature weather station.

The digital barometer is calibrated in the manner described in the September issue. Afterwards, P1 in the panel meter is adjusted to allow the reference pressure value to appear on the display.

2

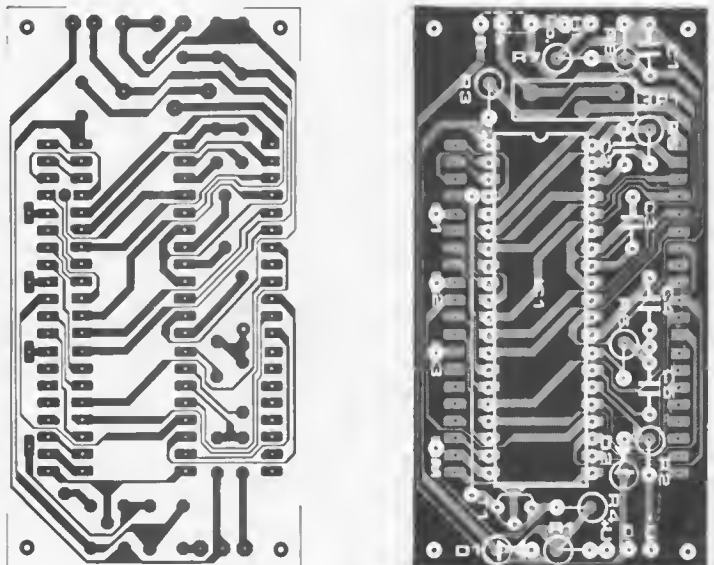


Figure 2. The printed circuit board and component overlay of the panel meter. IC1 should be mounted on a socket. The LCD display is fitted with IC connectors on the copper side of the board.

Just about as much has been written about data storage as about the entire field of microprocessors, which not only goes to show what a crucial topic it is, but also gives an idea of the problems involved. You rarely hear a computer owner complain that his microprocessor is not working; on the other hand, people frequently rant and rage about tapes which their cassette recorder could not read. Unfortunately, such problems are partly unsolvable, because the recorders used are often just not up to the job. Data is often stored on tape in the form of two frequencies: one representing a logic zero and the other a logic one. This is called Frequency Shift Keying (FSK).

found to be rather disappointing, with reliability leaving something to be desired.

On paper, the present circuit does not look very reliable either. This is because cassette recorders which are designed for audio purposes are a lot less error-proof than their professional counterparts. In the first place professional cassette decks operate at a higher tape speed and the tape is always modulated to saturation point. Obviously, this is exactly what audio recorder manufacturers try to avoid, as this is, of course, audio distortion. In addition, this bias current which serves to reduce distortion in domestic recorders is detrimental to the frequency characteristics. All in all, there-

high-speed cassette interface

A high-speed reliable cassette interface is extremely useful to any μ P-owner. This circuit achieves a baud rate of 4800 (!) with only a minimum of components.

A further method is to store the information in a certain number of pulses or with a specific interval between pulses.

These codes have one feature in common in that they allow several wave forms or pulses to be missed out here and there without causing irreparable data losses. In other words, short drop-outs and errors in the tape are catered for. This extra reliability has its price: since all the data must be stored several times on tape, the speed is slower. What is more, the practical results have been

fore, audio cassette recorders are not very suitable for storing digital information. Nevertheless, in practice the cassette interface described here proves to be almost as reliable as more conventional systems. The improvement is due to a much higher transfer speed.

Mr. Tarbell originally suggested the Manchester II-code for use by amateurs. This code had been around for a long time and was also widely used by professionals. Although nearly every firm employed a different version, each one was based on very similar principles.

J. van Laren

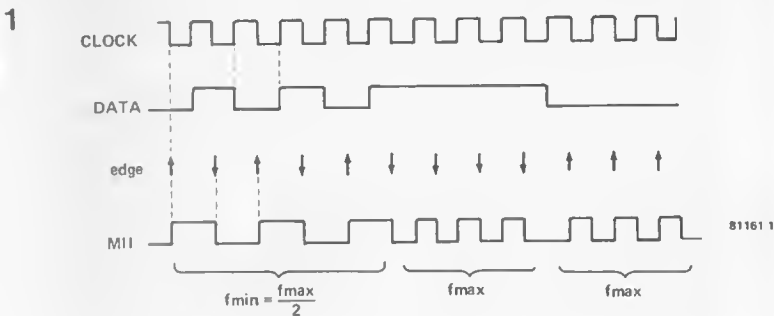


Figure 1. The Manchester code is generated from a data and a clock signal. The data determines whether a negative or a positive-going edge should be produced. If the data does not change in logic level, additional edges will have to be inserted.

2



A	B	C	A = 1	A = 0
0	0	1		
0	1	0		
1	0	0		
1	1	1		
			B/C	B/C
			0/0	0/1
			1/1	1/0

81161-2

Figure 2. The truth table of an ordinary exclusive NOR gate, which is highly suitable for use as an encoder.

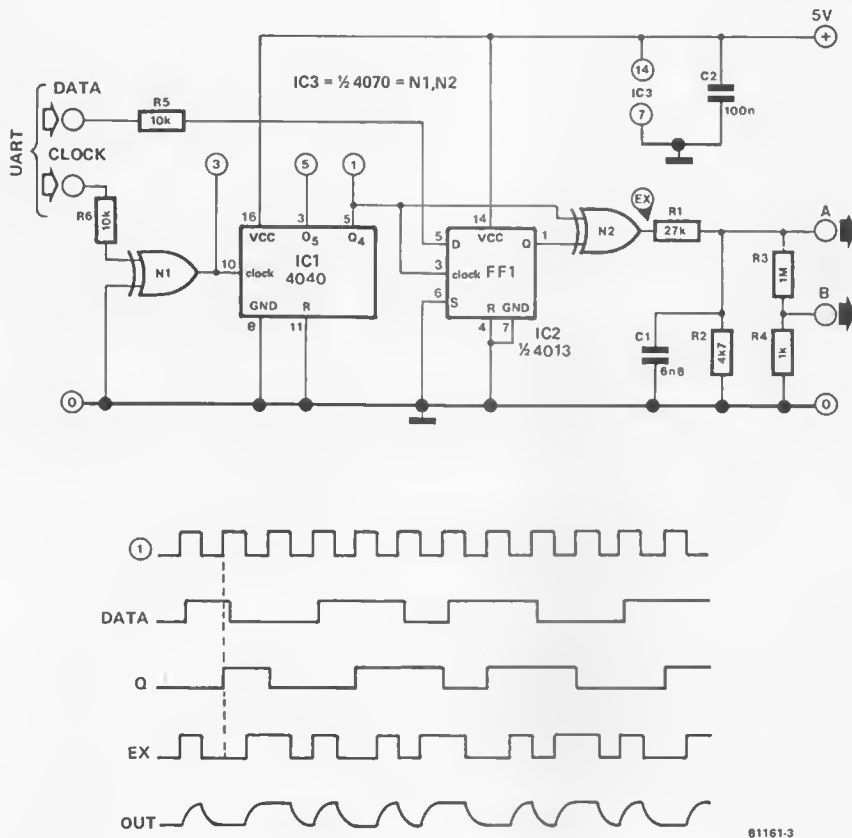


Figure 3. The complete circuit diagram of the Manchester signal encoder. A stage has been included in front of the exclusive OR gate to synchronise the clock and data. The code is inverted at the output with respect to figure 1.

The Manchester code has a number of advantages: it is reasonable efficient, a clock signal can easily be retrieved from it and the circuit used does not have to be complicated. The code features 50% efficiency, this means that the data baud rate may be as high as the highest frequency.

More recent codes manage to operate at twice the baud rate using the same frequency level, but the system involved is much more complex. The nice thing about the Manchester II is that the lowest frequency level is exactly half the maximum frequency. In other words, the recorder does not have to have an absolutely linear frequency curve which is a great advantage to the amateur.

In practice this means that, in order to obtain a data transfer speed of 4800 baud, the cassette recorder must be able to reproduce 4800 Hz well. If the frequency range of the recorder extends up to 10 kHz, a baud rate of 9600 Hz could even be achieved.

Manchester II encoder

What does the Manchester code look like? There are different ways of look-

ing at it and we start here with the most complex point of view.

Supposing we have a clock signal of 4800 Hz. The Manchester signal *must* feature an edge at every negative going edge of the clock. If the data at that particular moment is logic zero, this will have to be a positive-going edge. If, on the other hand, the data concerned is logic one, the edge will have to be negative-going (see figure 1). But what happens if the data is not constantly changing? After all, it is impossible to transmit only negative-going or only positive-going edges. The remedy is have to be included halfway between each data transmission. The information frequency will now be equal to the clock frequency.

Judging from above, most readers should now be able to imagine a complex circuit in which the required pulse edges are generated using logic gates and flipflops as memory devices. As it happens this is not necessary and all it requires is a single exclusive NOR gate!

It can be seen from the truth table in figure 2 that a "1" at input A will allow the output C to follow the B input. With a "0" at input A however, the C

output will now invert the B input. In short, if the clock frequency is connected to input B and the data is supplied at input A, the clock signal will be inverted or not, depending on the logic level of the data. This is like "clock-work" for figure 1, where a data low inverts the clock and a data high does not.

Readers are aware that inversion is often described as a 180° phase-shift. It can be said then that the phase of the clock signal is rotated either 180° (= inverted) or 0° (not inverted). Thus the Manchester II system belongs to a group of codes which use phase modulation since the clock is phase-modulated by the data. This is known as a "bi phase code", in other words, two phases are used, in this case 0° and 180°.

A further aspect makes decoding the recorded information very easy in practice. A long pulse period indicates that the decoder output has to change. It must become logic 1, when the level of the period is logic one, and logic zero, when the level is logic zero.

The decoder

From the latter definition it is a small

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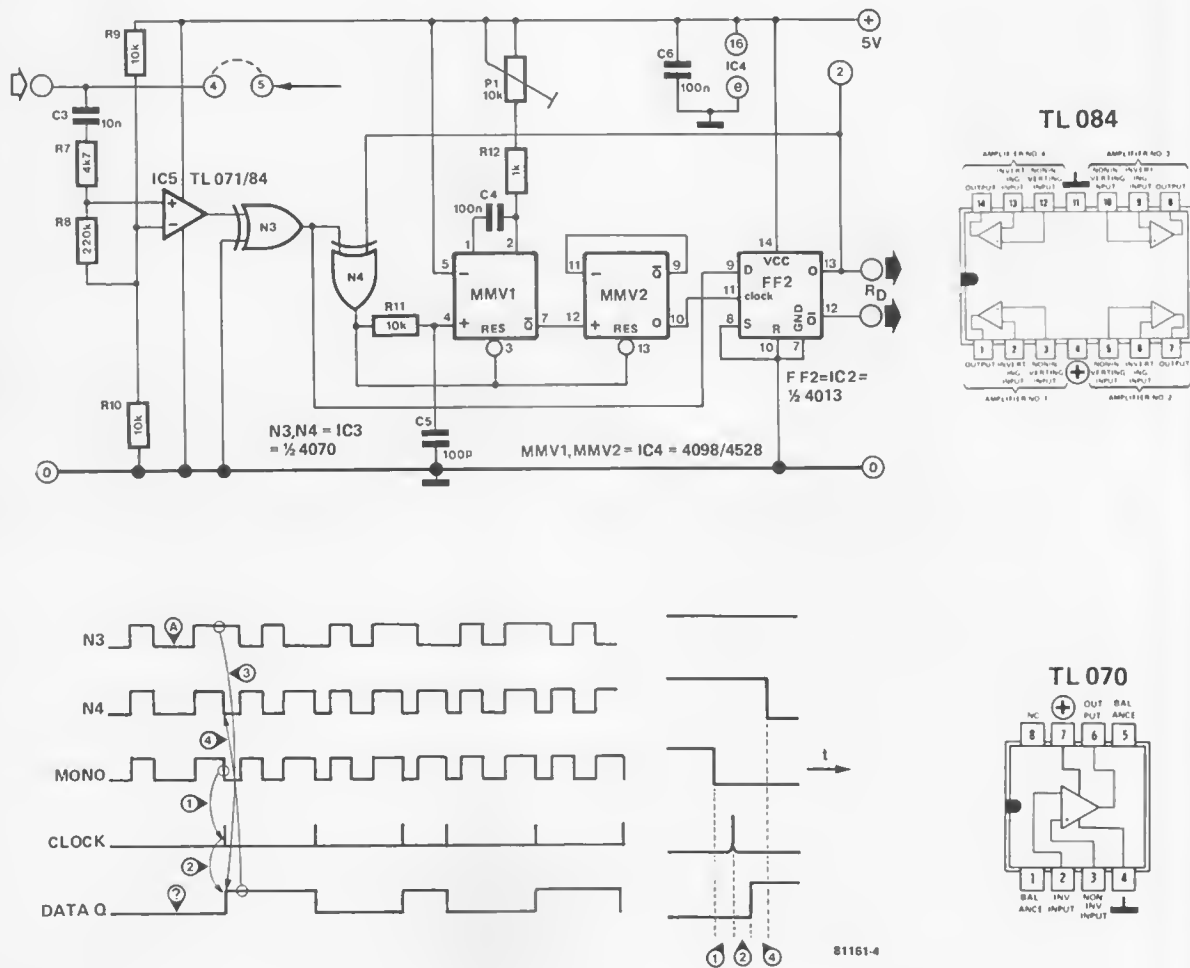


Figure 4. The Manchester code decoder. The cause and effect situation is clarified by the enlarged view of part of the signals; the arrows indicate the chronological order. Note that information may be lost straight after the power supply is switched on (at A), which is why initial data is repeated.

step to the Manchester II decoder. The code consists of a combination of the data and the clock signal and the encoder has already been dealt with — this was the exclusive NOR gate. The decoder is however a little more extensive. During each of the longer pulse period the data must change. A monostable multivibrator can quite easily detect a longer period and, when one arrives, generate a pulse. With this pulse the logic level of the Manchester II code at that time is stored in a memory — another flipflop. The output of this flipflop is then retrieved data. After all, if a longer period was logic one, it stands to reason that the data must also be logic one, and vice versa. It's as simple as that.

The circuit

Now that all the principles behind the

circuit have been explained we can be very brief about the actual encoder and decoder circuits. Figure 3 shows the circuit diagram of the encoder. The data is usually produced by a UART. In any case, the clock frequency will have to be a whole multiplication factor of the baud rate. In other words, in a 16x clock the clock frequency will be $16 \times 4800 = 76.8$ kHz, in a 64x clock this will be 307.2 kHz, etc.

The 4040 is a binary divider which divides by 16 (or by 64 if output 2 is taken instead of output 5). Flipflop FF1 ensures that data changes occur exactly during the positive-going transition of the divider clock frequency. This is necessary to prevent the final data from containing extra pulses which would confuse the issue. The Manchester code is derived from the clock signal and the synchronised data in the usual manner. Since an exclusive

OR is used instead of an exclusive NOR the code will be inverted, but that does not affect the principle.

With the aid of R1 and C1 the square wave signals are tapered off a bit. Two outputs are provided: preferably output A should be used, as output B produces an attenuated signal that is meant for recorders which only have a microphone input.

Figure 4 shows the circuit diagram of the decoder. The recorder signal is fed to a comparator which turns it into a square wave, N3 polishes up the edges. The Manchester code is now fed to the data input of flipflop FF2 and also to monoflop 1 which must detect the longer periods. Gate N4 is included in the signal path to monoflop 1 and, assuming that N4 does not invert, monoflop 1 will be triggered by the first positive-going edge to arrive. If the pulse duration is short, the two monoflops

5

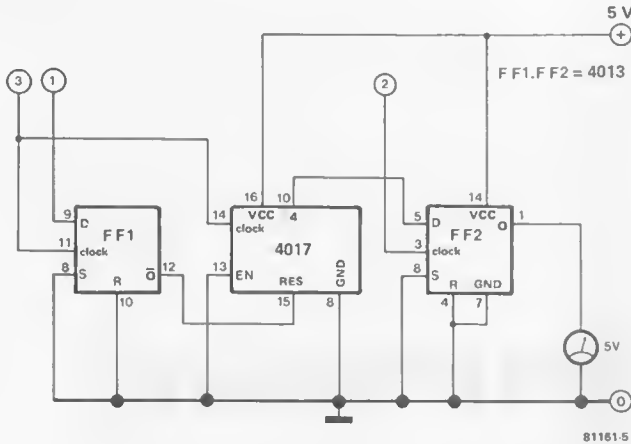


Figure 5. An auxiliary circuit for readers without an oscilloscope. This correctly calibrates the monostable period of monoflop 1. If the baud rate is altered, the calibration procedure will have to be repeated.

6

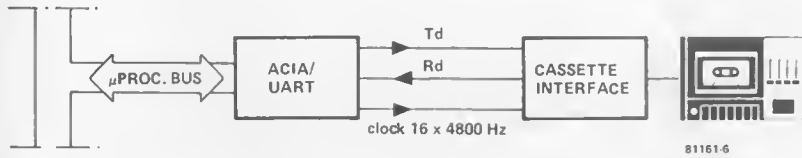


Figure 6. A block diagram which shows how to connect the cassette interface to a micro-processor system.

are reset as soon as the input signal goes low again and nothing else happens. If on the other hand the pulse duration was long, monoflop 2 is activated at the end of the monoflop period. Monoflop 2 again generates the clock pulse for flipflop 2 which then takes over the data when it arrives at its D input. As a result, the outputs of FF2 will (always!) change. The decoded data can be derived from one of these outputs. Both of them are available, so that even the inverted data may be used if necessary. Which output must be selected also depends on the type of cassette recorder in use. If it inverts the data, the other output will have to be used.

So far the operation has been described with reference to positive-going edges. However, there are also long pulse durations which start with a negative-going edge. What's more, any



Photo 1. The lower trace constitutes the signal as produced by the cassette recorder. The output data should change after every long period. The lower left hand corner shows a long positive-going pulse duration followed by a long negative-going counterpart. The data changes accordingly.

long pulse duration that starts with a positive-going edge is bound to be followed by one starting with a negative-going edge. The point is, monoflop 1 does not react to negative-going edges and in this case gate N4 provides the answer. As soon as the data at the output of FF2 changes, N4 inverts the phase. Thus, the negative-going edges are converted into positive-going ones, and vice-versa. That solves the problem, as the monoflop can now react to any type of edge.

Only the very first time are things likely to go wrong, for instance after the power supply is initially switched on. By the end of two long pulse durations however the circuit should work correctly. The hesitant beginning had best taken into account by starting the program with a synchronisation byte!

Calibration

Monoflop 1 is provided with an adjustment to enable the correct time value to be set. The monoflop period must last for not more than three quarters of the long pulse duration. With an oscilloscope this can easily be arranged, otherwise the auxiliary circuit in figure 5 must be used. This produces a logic 1 at the output within the range of P1. It only remains for P1 to be adjusted to the point where the meter indicates a maximum level and the calibration procedure is complete.

During calibration all the points 1 to 1, 2 to 2 and 3 to 3 should be connected to each other. In addition 4 and 5 should be linked. These points apply even if the calibration is carried out using an oscilloscope. The signal will then not have to pass via the recorder but can be derived directly from the encoder section.

Finally

To avoid any misunderstandings, please note the following: The Manchester code is usually implemented for synchronous data transmission. This enables a whole data block of, say, 256 bytes to be transmitted. The circuit described here, however, is designed for asynchronous rather than synchronous data transmission. Slight differences (small percentages= between the recording and the playback speed are permitted, since during asynchronous transmission a break occurs to re-synchronise the UART after every byte. During synchronous transmission, on the other hand, a different decoder (one including PLL, for instance) has to be used to retrieve the clock signal and so prevent the differences in speed from becoming too noticeable.

As an 'extra', the block diagram of the cassette interface connections to the author's microprocessor system is shown. In principle, the circuit is suitable for any speed, both higher and lower than 4800 baud. Only C1 and C4 will have to be adapted accordingly.

At one time or another, Ham radio operators who built their own sets are going to need a generator for receiver alignment. A commercially available test transmitter would, of course, be ideal, but they tend to be rather expensive and rather over-sophisticated. In nine cases out of ten a much simpler device will do the job, provided it produces a reliable, stable test signal within the required frequency range.

There is, however, one snag: an absolutely stable generator with an output frequency that is continuously adjustable is almost impossible to obtain. This

measured frequency. The required frequency (here: 9005.000 kHz) must therefore be tuned precisely with coil L1. With the aid of the varicap diode D1 the oscillator can be frequency modulated. The useable modulation level (presettable with P1) is not particularly high, but high enough to test narrow band FM amateur and other special band receivers.

SSB receivers can be 'whistled through' with the generator. In order to obtain intelligible modulation level for such receivers, the frequency modulation (FM) should merely be converted into a

RF-test generator

a 'mini test generator' for the 2 metre, 70 cm and 23 cm wave bands

This straightforward little circuit will be an extremely useful tool for high frequency enthusiasts. It is a kind of 'harmonic generator' that can be modulated and which will produce test signals in 9 MHz steps up to the giga hertz range. It can be used both for FM and SSB receivers and is a fairly inexpensive circuit to build.

plus the fact that we are looking for an economic alternative meant that another solution had to be found. A crystal generator was therefore designed that was capable of producing a wide frequency range without having to be tuned. The secret is for it not to be a 'clean' oscillator, but one with an output signal that contains many harmonics. Even though it includes an ordinary transistor, the oscillator produces powerful harmonics of gigahertz proportions in addition to its 9 MHz fundamental frequency!

This means that the test generator could also be used for reception and transmission on VHF and UHF. The generator's third harmonics are on the 27 MHz wave band (CB), its 16th harmonics are at 144.08 MHz (2 metre wave band), its 48th harmonics are at 432.24 MHz (70 cm wave band) and its 144th harmonics are at 1296.72 MHz (on the 23 cm wave band).

The circuit is also ideal for testing speech processors.

The circuit

The remarkably simple circuit diagram is shown in figure 1. Around T1 there is a colpitt-like oscillator using a 27 MHz crystal. This does not make use of the third overtone of the crystal but rather the fundamental frequency, this being 9 MHz. This happens to be a very favourable frequency for our present purpose, since its harmonics extend over a range that is very practical for radio amateurs.

When a crystal is used at the fundamental there is always a considerable difference between the theoretical and the

phase modulation (PM). This can be done quite simply by connecting a small capacitor (C1) in series with the modulation input — thus, S1 can now switch between FM and SSB.

In most test generators a separate attenuator is used to measure a receiver's behaviour at very low signal levels. In this particular case this was found to be superfluous since the oscillator continued to be reliable even when barely operating. It is therefore quite a straightforward matter to build an attenuator by making the emitter resistor belonging to T1 adjustable. Pots P2 and P3 have a fairly wide range: at a frequency of 144.08 MHz (2 m wave band) the maximum output signal is around 1 mV and a minimum of around 30 nV (or 0.03 μ V)!

Construction

Obviously, building the board (figure 2) is a simple matter. Even the coil L1 should be no problem; just 22 turns of enamelled 0.2 mm copper wire wound around a Kaschke core, type K3/70/10. If readers happen to dislike this chore, an adjustable 4.7 μ H inductor coil obtainable from Toko will also be suitable.

With the exception of the mains transformer, the simple power supply shown in figure 1 is included on the printed circuit board. Since the circuit consumes very little current (and therefore the transformer can be quite small) the test generator and its power supply can be a highly compact instrument. When putting it into a case, be sure to provide a metal screen between the mains transformer and coil L1, otherwise there will be a lot of hum — a type of modulation that is not always to be desired!

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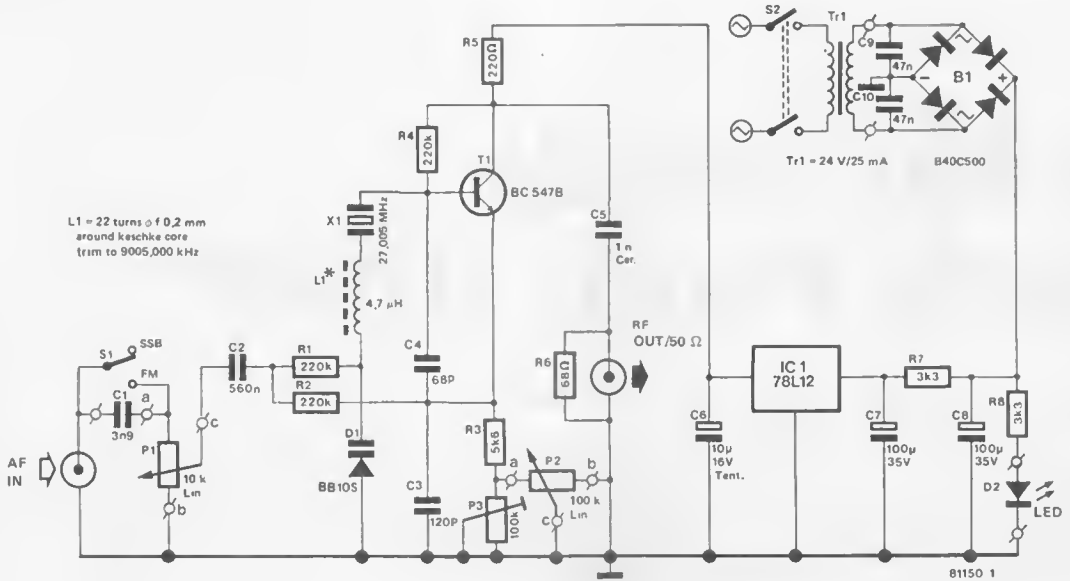
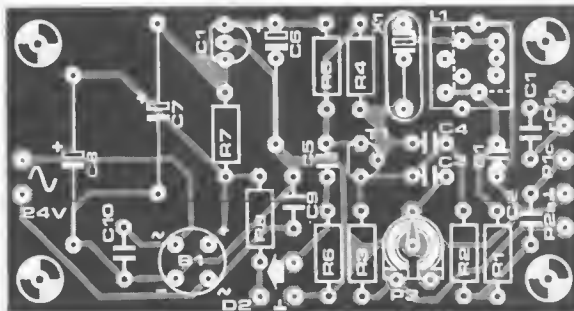
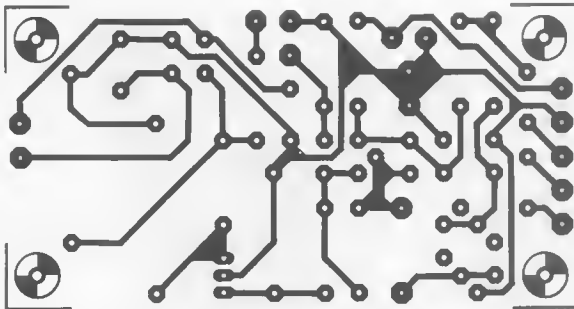


Figure 1. The test generator circuit diagram. It is straightforward and purely functional.

2



Parts list

Resistors:

R1, R2, R4 = 220 k
 R3 = 5k6
 R5 = 220 Ω
 R6 = 68 Ω
 R7, R8 = 3k3
 P1 = 10 k linear
 P2 = 100 k linear
 P3 = 100 k preset

Capacitors:

C1 = 3n9
 C2 = 560 n
 C3 = 120 p
 C4 = 68 p
 C5 = 1 n (cer.)
 C6 = 10 μ /16 V (tantalum)
 C7, C8 = 100 μ /35 V
 C9, C10 = 47 n

Semiconductors:

T1 = BC 547B
 D1 = BB 105
 D2 = LED
 IC1 = 78L12
 B1 = B40L500 round version

Miscellaneous:

X1 = 27,005 MHz crystal
 L1 = 4.7 μ H coil (see text)
 Tr1 = 24 V/25 mA transformer
 S1 = SPDT switch
 S2 = DPDT switch

Figure 2. The printed circuit board for the 'mini test generator' is very compact.

Although dark room timers are widely available from photographic stores, there aren't many economical do-it-yourself alternatives. The nice thing about 'building your own' is that you can modify it to fit in with your own particular requirements. The circuit

wide range dark room timer

electronic developments in the dark room

Photography is probably the fastest growing hobby at the present time and together with all other aspects of life, electronics is involved. For the electronics/photography enthusiast the scope for combination of the two hobbies is very wide indeed. Those of our readers who are fortunate enough to own a dark room do not need reminding that electronics can almost control the whole process. Although many applications spring to mind, this is where the project featured in this article will really be at home. This dark room timer is fully automatic and its range is wide enough to cater for all but the most exceptional requirement of photography. As an added refinement, it even controls the safety light.

featured here tries to do just that by offering a variety of possibilities. The range of 0.1 to 99 seconds with preset 0.1 second steps is switchable to a 1 second to 999 seconds range with preset steps of 1 second. In addition, two LEDs are used to indicate which of the start and stop buttons has been operated. Once an exposure process has been started it can easily be interrupted if necessary. Both the enlarger and the dark room lights are controlled by the circuit. On occasion, the enlarger has to be switched on independently

1

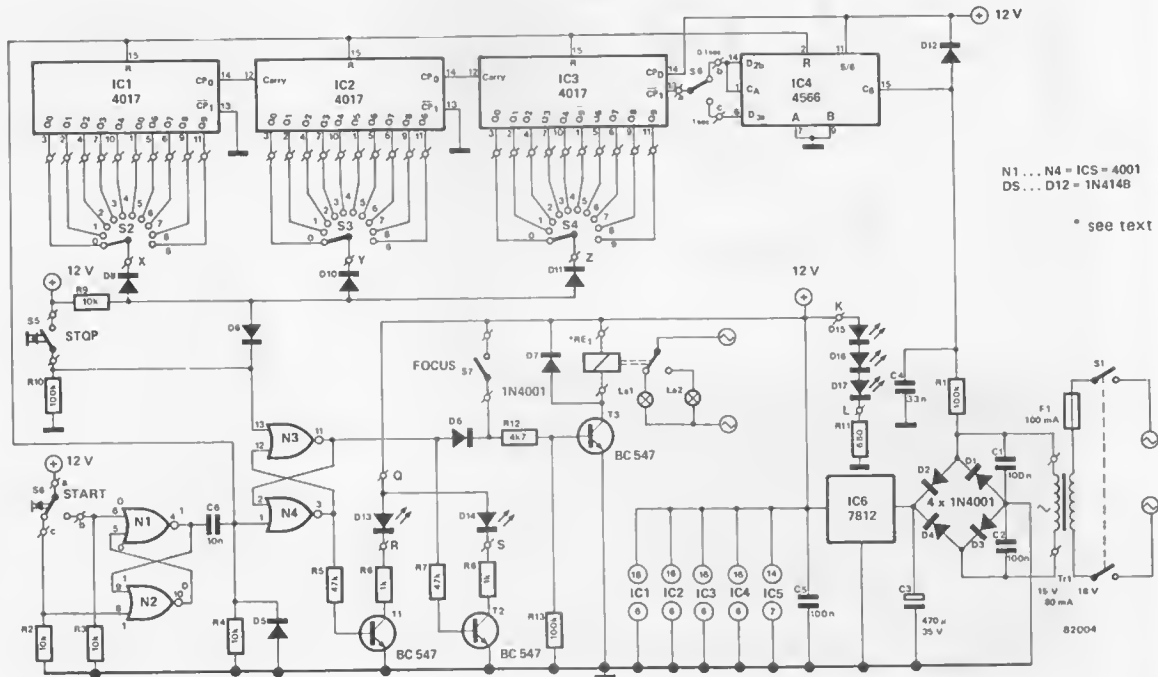


Figure 1. The basis of the dark room timer is a counter chain. This provides a series of outputs from which a range of preset exposure times from 0.1 second to 999 seconds can be selected.

from the timer and this too has been taken into account.

The circuit

IC4 (4566) produces the reference for the timer. The IC incorporates divide-by-five and divide-by-ten counters together with a puls generator, so that a 50 Hz sine wave signal that is derived from the secondary of the transformer can be directly used as a clock signal. The clock signal reaches the clock input of IC4 (pin 15) via the filter R1/C4. The output signal of the divide-by-five is available at pin 14 and the frequency at this point is 10 Hz, which corresponds to a 0.1 s period. This signal is fed to the input of the divide-by-ten, pin 1, to provide an output signal at pin 6 with a frequency of only 1 Hz. The pulse duration will be exactly 1 second.

According to the position of the switch S8 either 10 Hz or 1 Hz clock signals will reach the counter chain IC1... IC3. At each positive edge of the clock pulse the count is incremented by one.

When the start switch S6 is operated, a logic 1 is produced at the output of the flipflop N1/N2 (built with NOR gates). The differentiator network C6/R10 converts the level change into the positive pulse that is used to reset the counter chain. This pulse, at the same time, sets the flipflop N3/N4. The logic 1 appearing at the Q output will now switch on T3 and activate the relay Re1. One of the relay contacts is used

to switch the dark room lights on and off. In short, when the start button is pushed the dark room lights go out and the enlarger lamp goes on. The relay should be a 12 V/35 mA type although the circuit caters for a maximum of 100 mA passing through the relay coil. In the latter case the current rating of the transformer must be updated to cater if a relay requiring more than 35 mA is used.

The counters IC1... IC3 will start to count up from 0 upon the arrival of the start pulse. Once the preset time has been reached, a positive pulse reaches the reset input of the N3/N4 flipflop causing the output of N3 to become logic 0. Transistor T3 will now stop conducting - the enlarger lamp will go out and the dark room lights go on again. The exposure process will start again from scratch when the start button S6 is pressed.

Together with the resistor R9, diodes D8, D10 and D11 form an AND gate, the inputs of which are formed by the cathodes of D8, D10 and D11. The common anode junction acts as the output. If the preset time does not correspond to the output of the counter chain IC1... IC3, the output of the AND gate will be logic 0. A high logic level will not reach the reset input of N3 via R9 and D10 until all the cathodes of D8, D10 and D11 are connected to a positive potential, that is, when the count equals the preset time. When this happens of course, the exposure period

ends. That covers the main principle of the dark room timer but the system also has a few additional features. Switch S5 allows the exposure to be interrupted at any given time. When operated, a positive pulse is fed to the reset input of the N3/N4 flipflop. Transistor T3 then stops conducting and the relay switches the enlarger lamp off and the dark room lights on.

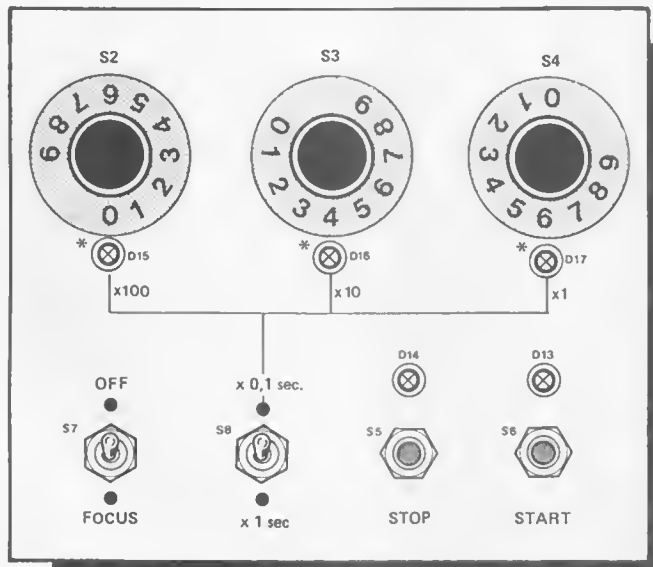
Occasionally the photographer may need to extend the exposure time. Again, this has been taken into account by S7. When this switch is operated transistor T3 will continue to conduct regardless of the logic state at the output of gate N3 and the enlarger lamp can be held on for as long as required.

The rotary switches S2... S4 have knobs with transparent 'skirts' marked from 0 to 9. The LEDs D15... D17 are then mounted beneath the front panel and behind the skirt so that they illuminate the preset time period. This allows the controls to be used with ease in the poor light conditions that exist (hopefully) in your dark room.

The numbers can be put on to plain skirts with letteraset if necessary.

LEDs D13 and D14 indicate which button is ready to operate (START or STOP). As soon as an exposure procedure has started, transistor T2 conducts and the STOP LED D14 lights. This means: the exposure can be interrupted with the STOP key. When this happens, or when an exposure has ended, transistor T2 will stop con-

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82004 2

* see text

Figure 2. The front panel for the timer can follow the suggested layout illustrated here although any layout will be suitable providing the start and stop buttons are placed in prominent positions.

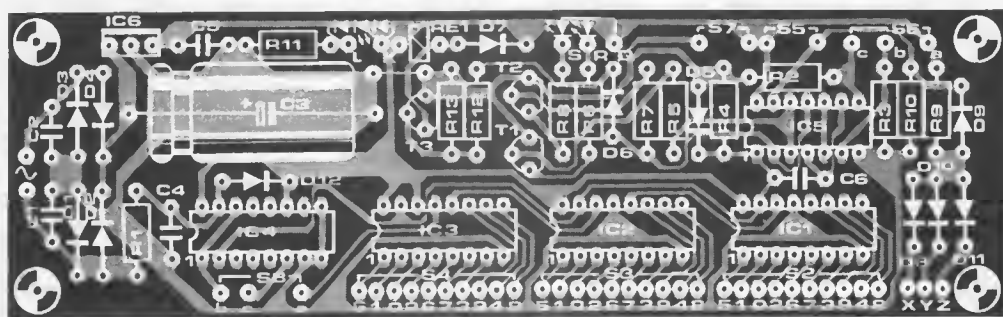
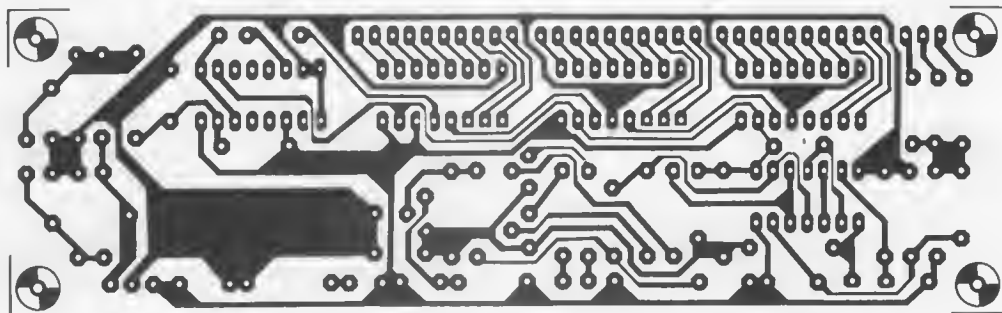


Figure 3. Except for the switches, the mains transformer and a few other components, the timer is contained on the single printed circuit board shown here.

Parts list

Resistors:

R1, R10, R13 = 100 k
 R2, R3, R4, R9 = 10 k
 R5, R7 = 47 k
 R6, R8 = 1 k
 R11 = 680 Ω
 R12 = 4k7

Capacitors:

C1, C2, C5 = 100 n
 C3 = 470 μ /35 V

C4 = 33 n
 C6 = 10 n

Semiconductors:

D1 ... D4, D7 = 1N4001
 D5, D6, D8 ... D12 = 1N4148
 D13 ... D17 = LED
 T1 ... T3 = BC547
 IC1 ... IC3 = 4017
 IC4 = 4566

IC5 = 4001
 IC6 = 7812

Miscellaneous:

S1 = DP mains switch
 S1 ... S4 = 10 way wafer switch
 S5, S6 = Digitast switch
 S7 = SPST switch
 S8 = SPDT switch
 F1 = 100 mA slow blow fuse
 Tr1 = 15 ... 18 V/80 mA transformer
 Re1 = 12 V/35 mA Siemens pcb relay

ducting and LED D14 will go out. Now T1 will conduct and the START LED D13 will light. This shows that the timer is ready for another exposure. Digitast switches with built-in LEDs can be used for S5 and S6.

Operation


For the first timing range (up to 99 seconds) switch S8 remains in the 0.1 s position; for the 1 ... 999 seconds range

this switch is set at 1 second. For example, a time interval of 9 seconds requires the following switch positions: S8 = 0,1; S2 = 0; S3 = 9 and S4 = 0. For an interval of 153 seconds the switches are positioned as follows: S8 = 1; S2 = 1; S3 = 5 and S4 = 3.

Construction

The illustration in figure 2 is a suggested front panel layout. It must be remem-

bered that the timer will almost always be in use during poor light conditions (a dark room should be dark after all) and it is therefore advisable to place the start and stop buttons in prominent positions.

If a metal case is used it must of course be properly earthed. A plastic case, such as the Vero type 202-21033A, will be far safer in view of the fact that liquids tend to be in abundance in dark rooms — liquid + 220 V + darkness do not add up to an ideal mixture. 

Teletext is information that is provided in the form of picture pages on a TV screen which the viewer is free to select. The pages consist of text blocks containing 24 lines of 40 characters, which may be partly replaced by illustrative graphic information (such as weather charts, etc.). In principle, the entire information package could be transmitted 24 hours a day by broadcasting stations along with the daily programs. This is possible, because use is made of two lines during field-blanking interval, so that the usual program material is unaffected. Up to 800 pages can be broadcast during an ordinary program and these are distributed as 8 'news-

can be broadcast continuously together with the TV programs. At the moment, up to 100 pages are being broadcast.

How it all came about

The expression 'great minds think alike' is very appropriate here, as the development of a teletext system was started in various countries at the same time. The leading system was developed in Great Britain in the research laboratories of the BBC and the IBA. The first practical results were realised in 1970. The two companies used a field-blanking system (see figure 1) to transmit internal program information. The field-blanking (shown as a black rectangle at both the top and the bottom of the picture) contains 25 lines which exist outside the normal picture. A number of lines lead to excellent data transmissions (see figure 1). The program identification/information systems used in 1970 enabled up to 15 characters to be broadcast per line, which is very little. New possibilities were created towards the beginning of 1972 when Teledata (BBC) was developed. This allowed for up to 32 characters to be transmitted per line.

In September 1972 the IBA introduced the Oracle system. Around the same period the BBC changed the Teledata name to Ceefax (= See facts). The two systems are based on the same principles, but use different modulation methods and data transmission speeds. This means the two systems cannot be decoded with one and the same decoder. Obviously, a standard solution has to be found.

BBC, IBA and BREMA (British Radio Equipment Manufacturers Association) and later the GPO sent representatives to set up a team which in September 1974 published a report with the dubious title of 'Specification of Standards for Information Transmission by Digitally-coded Signals in the Field-blanking interval of 625-line Television Systems'. This describes a teletext system that combines the best characteristics of both Oracle and Ceefax. In addition, the new system enables graphics and colour to be used.

In the same year, albeit on a small scale to start with, test broadcasts were carried out. These tests resulted in many new ideas and in September 1976 the definitive teletext specifications were established. The 'Broadcast Teletext Specification' gives a description, among other things, of more extensive graphic facilities and the decoder described in this article meets the requirements stipulated in that specification sheet.

Decoding teletext is by no means easy. If the decoder were built up with ordinary TTL ICs, a whole bag of chips would be needed. Thus, Large Scale Integration (LSI) is the only method to produce a compact decoder that can be included inside a television set. Various manufacturers are currently offering package deals which allow a complete

teletext decoder

... that does not require modifications to the TV set

Teletext is no longer a new word especially to our readers. It is also well known that a TV set requires a decoder in order to make use of the service. However, all the decoders available for home construction suffer from one major disadvantage in that they require modifications to the TV set itself. It is understandable that this fact is never greeted with very much enthusiasm. The good news is that the Elektor Teletext decoder system does not require any modifications to the TV at all ... unless you really want to fit it internally. As well as the decoder itself, an additional "black box" enables the Elektor Teletext decoder to be placed between the aerial and the TV set. A lot simpler than persuading the lady of the house that you really must "have the tele in pieces all over the carpet!"

papers' of 100 pages each. Each page requires 0.24 seconds broadcasting time (12 rasters). Since all the pages are transmitted one after the other, the average delay will be about 12 seconds for every 100 pages, which therefore limits the number of pages. If on the other hand an entire TV channel was devoted exclusively to teletext broadcasts, about 30,000 pages could be transmitted simultaneously without any long delays.

The computer plays a key role in this communication process. An editorial team collates the information and it is stored in the computer memory. Whenever a page needs to be updated, new data is entered and the computer ensures that it appears on the correct page. In addition, it is the computer's job to convert the entered data into an acceptable form for broadcasting purposes. The stored pages are combined into an infinite sequence of pages, so that they

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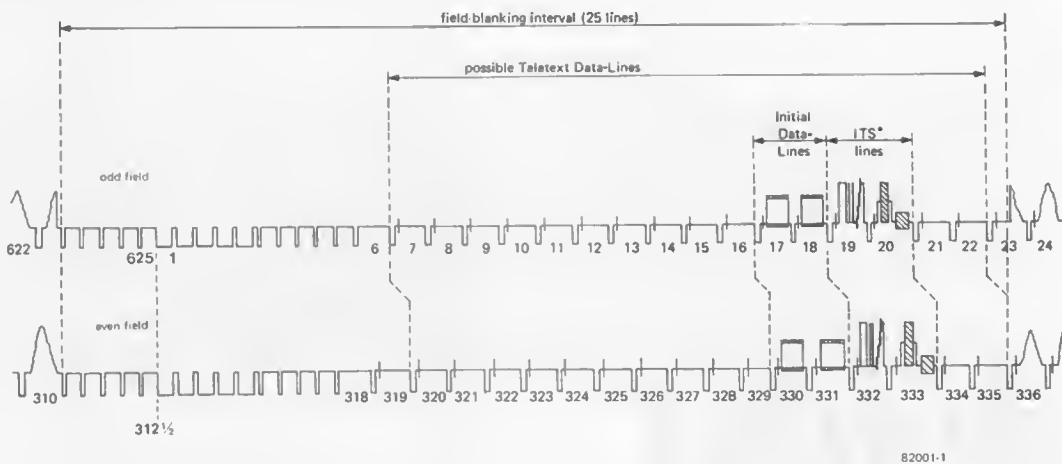


Figure 1. The coded teletext data is transmitted during two row times belonging to the field-blanking interval. The diagram shows what happens on British television.

2

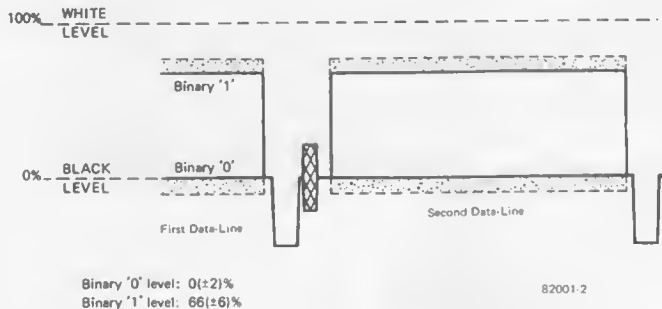


Figure 2. A simplified version of a row filled with teletext data. The modulation levels in the figure correspond to a logic zero and logic one, respectively.

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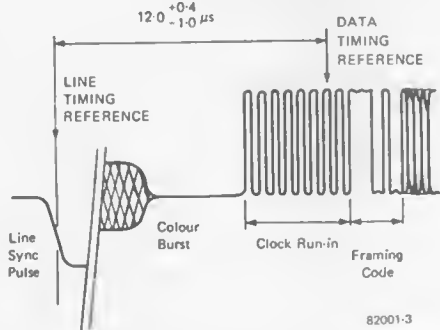


Figure 3. The decoder is synchronised to the teletext data signal during the clock run-in period. With the aid of the framing code the decoder detects the beginning of a data row.

decoder to be constructed from a few RAMs and perhaps a single TTL chip. After careful consideration Elektor chose the four chip option provided by Mullard. Before going into detail about these four ICs, it might be as well to look at a few technical aspects involved in teletext.

Signal formation

As mentioned earlier, data is transmitted during the field-blanking interval. All the television standards in Europe are based on a rate of 50 frames per second. Each frame consists of 312½ lines (see figure 1). Two frames

together constitute one complete 625-line picture. To suppress any frame flyback takes 25 line periods. The flyback stroke in modern television is so short however that usually 6 or 7 lines are enough. The remaining lines in the field-blanking interval are therefore available for other purposes. As early as 1970 the BBC and the IBA were already making use of this facility to transmit program information and for test transmissions. About 15 lines can be used in this manner. At the moment however only two lines are being used for teletext transmission.

The lines are not yet subjected to rules and regulations and, as far as we know, a different set of lines is being used in every country. The Netherlands uses lines 15, 16, 328 and 329, the U.K. lines 17, 18, 330 and 331, Belgium lines 19, 20, 332 and 333 and W. Germany lines 20, 21, 333 and 334.

Which lines are used makes no difference to the decoder, as, provided the information is situated inside the 'data entry window' (see figure 5), the data will be recognised and stored in memory. Sometimes the teletext signal may appear at the top of the picture as an irritating flashing bar. This phenomenon is most likely to occur on German sets, since the teletext lines are very close to the picture height being somewhat too restricted. This is easily remedied. In other cases it is due to the way in which the CRT is built into the set.

The two teletext lines contain digital information known as data. Here the logic 0 level corresponds to $0 \pm 2\%$ brightness modulation and logic 1 corresponds to $66 \pm 6\%$ (see figure 2). A whole row of teletext data is transmitted per line for 53μ seconds of the line period (64μ seconds). The data on a single line is made up of 45 bytes (1 byte = 8 bits). The first three bytes

4

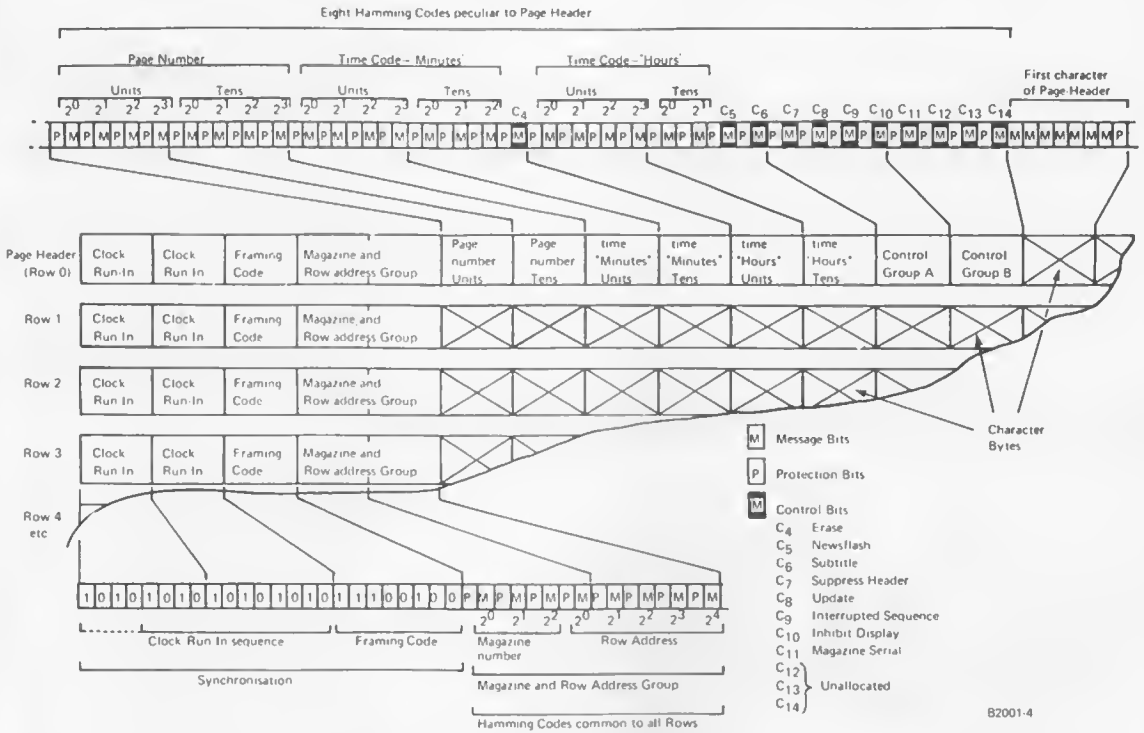


Figure 4. Every teletext row is preceded by a number of clock run-in periods, a framing code and a combination of the magazine and row address. In addition, the page header contains the page address, the time code and a number of control bits for the decoder. For increased reliability the data is transmitted with a Hamming code.

5

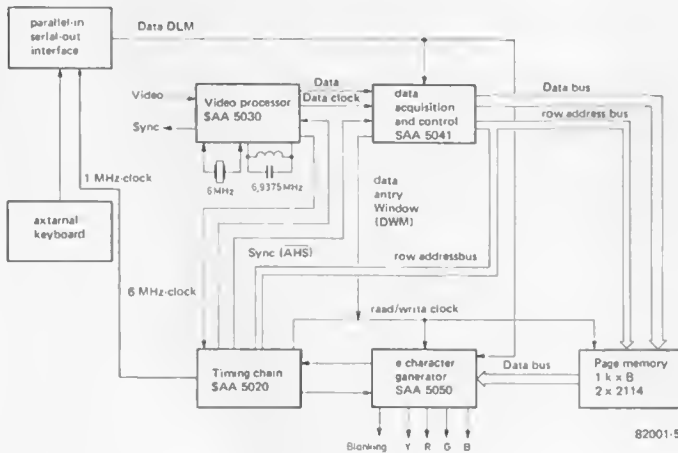
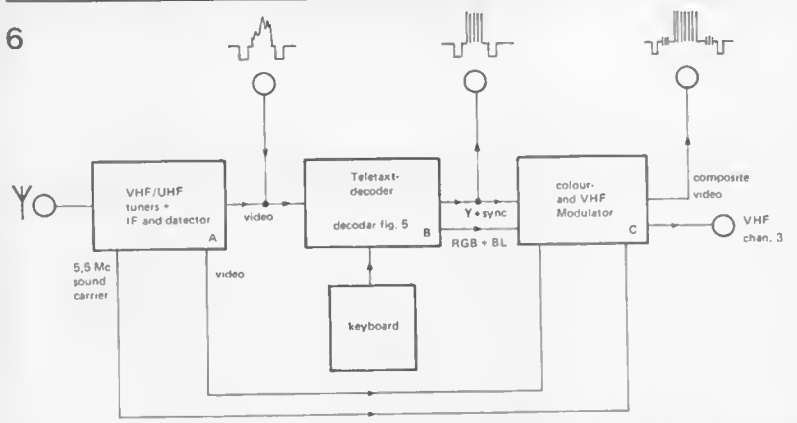


Figure 5. The block diagram of the teletext decoder on its own. The decoder in this form is only suitable for fitting inside a TV set.

are used to synchronise the decoder and to determine the data's starting point. This information is structured around two 'clock run-in' bytes for synchronisation purposes and a 'framing code' byte to indicate the data's starting point.

The remaining 42 bytes contain the magazine number and the row address (2 bytes) and the codes (40 bytes) for the line contents. Both the row address and the magazine number are transmitted on every row (see figure 4). This vital information for the teletext decoder is transferred with the aid of a special code to reduce to a minimum the likelihood of errors during reception. Every bit in this Hamming (error detection) code is accompanied by a protection bit. To describe the Hamming code in detail would take too long, but, in a nutshell, what it does is add extra bits to facilitate a much more extensive parity check. This is so efficient that even mistakes that only appear once can be corrected, the multiple ones leading to a rejection of the character received. The row structure described above is relevant for rows 1...23. These contain the actual page text. Every page is preceded by a page header which has row number 0. This row contains, in addition to the magazine and row number, 8 additional information bytes in Hamming code. These bytes take the place of 8 text bytes, so that the page header may never exceed 32 characters.

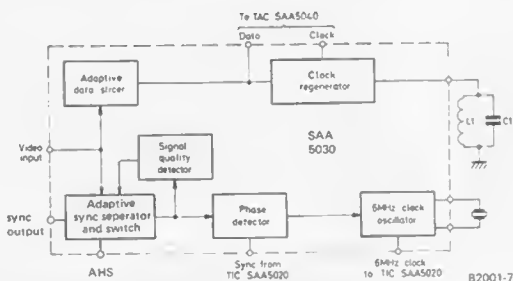
6



82001-6

Figure 6. By extending the block diagram in figure 5 with sections A and C shown here, a teletext converter is obtained which can be installed without difficulty between the aerial end of the TV set.

7



B2001-7

Figure 7. The block diagram of the Video Input Processor.

The information bytes contain a reliable time code and eleven link bits to let the decoder know what kind of teletext page is being received. C6 for instance (see figure 4) serves to switch on the sub-title facility.

The block diagrams

All in all, the teletext signal has a rather complex structure, and is therefore not very easy to decode. Thanks to LSI technology, however, most of the necessary electronics is included in only four chips. Figure 5 shows the functions that each chip fulfils in the form of a block diagram.

The page memory and the keyboard interface are the only other components which the decoder chips need in order to be able to operate properly. With just a few 'extra's, a decoder can be built into any TV with the aid of this block diagram. In most cases however this will result in quite an operation, however, especially if the teletext pages are to be shown in colour. If the user restricts his requirements to a modest system and decides against colour with only essential switching on the keyboard, the circuit can be built fairly easily into the television set. The simplest way to do this is indicated in the instructions provided later on in this article. Figure 6 shows the various connections in the form of a single block diagram. The simplest solution uses only block B and the keyboard.

The video signal is then derived directly after the video detector in the TV set. After being decoded, the teletext signal (Y + sync.) is fed to the TV set at the same point. Obviously, the connection between the video detector and the video amplifier will then have to be broken.

Block C can be connected in roughly the same way and provides a few more facilities. It will still be necessary to modify the TV set, but the teletext pages will be shown in colour of a reasonable quality.

The above alternatives mean having to open up the TV set. Even though this is a relatively easy task as only one signal

wire has to be cut, it is obviously best not to fiddle around with a television unless readers really know what they are doing! The point is, every type of television will require a different operation so that it is impossible to give a standard recipe. Nonetheless, an experienced hobbyist should not have too many problems provided the instructions given below are followed with care.

A teletext converter can also be fitted into the set. This can be done by adding block A to the decoder. The aerial is connected to the teletext converter and the VHF output of the converter is linked to the aerial input of the TV set. The result is a highly acceptable teletext picture and saves having to 'operate' on the TV.

LSI chips

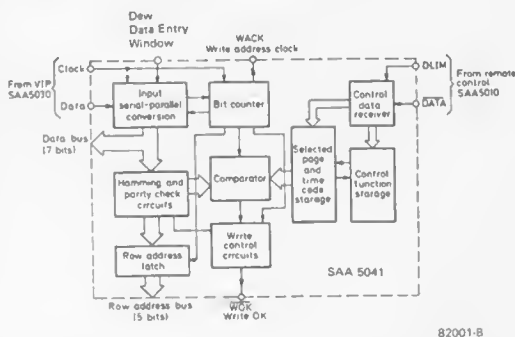
Although the block diagram gives a fairly simplified view of the teletext decoder, the latter will be seen to be far more complex in reality. In fact it is so complicated that a block diagram has to be provided for each chip to be able to clarify the circuit's function.

The teletext decoder is split up into an analogue and a digital section. Before the digital teletext information can be 'gleaned' from the video signal, this signal has to undergo a number of analogue processes. This is taken care of by the video processor.

SAA 5030 VIP (Very Important Processor)

This Video Input Processor fulfils two main tasks: the video signal is split up into a data and a synchronisation section (see figure 7). The synchronisation divider produces a substitute synchronisation signal for the TV set (only used if the decoder is included inside the set). At the same time this signal is used as a reference for a 6 MHz Phase Locked Loop. The VCO in this PLL is a 6 MHz crystal oscillator which can therefore only be mistuned by a small degree. This is necessary, since this oscillator must be able to produce a fairly stable signal even in the absence of the reference signal.

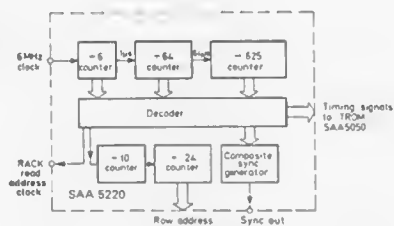
8



82001-8

Figure 8. The block diagram of the Teletext data Acquisition and Control chip.

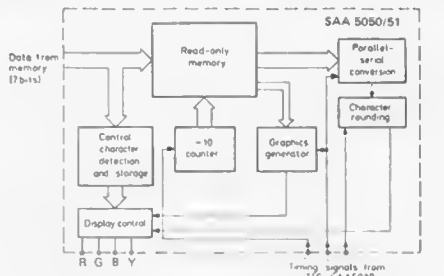
9



82001-9

Figure 9. A block diagram showing the interior of the Timing Chain.

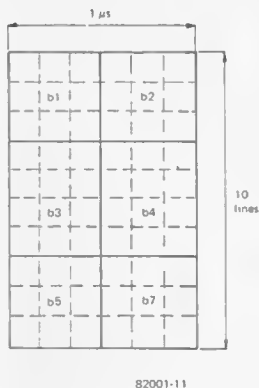
10



82001-10

Figure 10. The Teletext Read Only Memory.

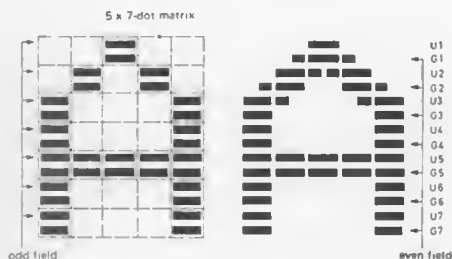
11



82001-11

Figure 11. The graphic characters are directly linked to the bits belonging to the code words. The drawing shows the significance each bit has within a graphic sign.

12



82001-12

Figure 12. Character rounding improves teletext readability and makes it a lot better than other similar text display systems. Interlacing is used to double the 5 x 7 matrix.

A phase detector provides the oscillator with a control voltage and compares a frequency derived from the 6 MHz (15,625 Hz derived from the SAA 5020 see figure 9) to the incoming synchronisation signal. This has the effect that all the clock signals inside the decoder can be latched to the incoming video signal, so that the program and the teletext page may be transmitted simultaneously, one on top of the other.

A signal quality detector determines whether the latch function really took place. If the video signal is poor or totally nonexistent, all the clock signals are derived from the (unlatched) 6 MHz signal. In this particular case the TV will be fed with the AHS signal (After Hours Sync, derived from the SAA 5020) so that a (previously received) teletext page can be displayed.

The data section in the SAA 5030 serves to separate the teletext data from the video signal and also to generate a clock signal to process this data. The 'clock run-in' section of the teletext signal is used to synchronise a loop circuit to the data clock frequency of 6.9375 MHz (= 444 x 15625 Hz). An internal delay line ensures that the positive-going edge of every clock period occurs exactly in the middle of the received data bit.

SAA 5041 TAC

The 'brain' of the teletext decoder consists of the SAA 5041. This chip deals with the control and data processing tasks. TAC stands for 'Teletext data Acquisition and Control' (see figure 8). The teletext data is only received in a certain area of the field-blanking interval. It is only during this period that the SAA 5041 may take action to prevent the wrong data from being processed.

This is done by the DEW signal (Data Entry Window) derived from the SAA 5020. Data received during this DEW is split up into the sections shown in figure 4. Depending on the nature of the data, either Hamming or parity checks will be carried out. Any characters that do not have a suitable parity are written as a space in memory to prevent them from affecting the final teletext page. If the page is received again, the 'gaps' are filled with the correct characters, if at all possible.

The row numbers are passed on to the row address latch as part of the page memory addressing. If the row number is zero (0) the page numbers are compared. If the page number corresponds to the number (DATA + DLIM) selected by way of the keyboard, the new

information is stored in the page memory. For this the serial data is first converted into 7 bit words.

In addition to page numbers the keyboard can give a few other commands which are decoded and carried out by the SAA 5041. Examples are: enlarged displays of half a page, a time indication at the top right-hand corner of the picture (during ordinary programs) and a mixture of program and teletext picture.

SAA 5020 TIC

The Timing Chain SAA 5020 constitutes the clock in the teletext decoder. The divider stages of the SAA 5020 produce all the control signals which are necessary to display a teletext picture. This includes the DEW and AHS signals which were described earlier. In addition, the TIC provides several control signals for the character generator SAA 5051. Page memory addressing is also taken care of by the TIC. For this the IC generates a 5 bit row address and a clock signal (RACK) for the external address counter which must address the 40 columns on a single row (see figure 5). The counter configuration consists of a divide-by-ten followed by a divide-by-24 and partly reveals the

1		Col							Row												
b7 b6 b5 b4 b3 b2 b1		0 ₀	0 ₀ 1	0 ₁ 0	0 ₁ 1	1 ₀ 0	1 ₀ 1	1 ₁ 0	1 ₁ 1	0	1	2	2a	3	3a	4	5	6	6a	7	7a
0	0	0	0	0	0	0	0	0	0	NUL ^①	DLE ^①			0		@	P			p	
0	0	0	1	1						Alpha ⁿ Red	Graphics Red	I		1		A	Q	o		q	
0	0	1	0	2						Alpha ⁿ Green	Graphics Green	"		2		B	R	b		r	
0	0	1	1	3						Alpha ⁿ Yellow	Graphics Yellow	f		3		C	S	c		s	
0	1	0	0	4						Alpha ⁿ Blue	Graphics Blue	\$		4		D	T	d		t	
0	1	0	1	5						Alpha ⁿ Magenta	Graphics Magenta	%		5		E	U	e		u	
0	1	1	0	6						Alpha ⁿ Cyan	Graphics Cyan	&		6		F	V	f		v	
0	1	1	1	7						Alpha ⁿ White	Graphics White	'		7		G	W	g		w	
1	0	0	0	8						Flash	Cancel Display	(8		H	X	h		x	
1	0	0	1	9						Steady ^②	Contiguous ^② Graphics)		9		I	Y	i		y	
1	0	1	0	10						End Box ^②	Separated Graphics	*		:		J	Z	j		z	
1	0	1	1	11						Start Box	ESC ^①	+		;		K	←	k		←	
1	1	0	0	12						Normal Height	Black ^② Background	,		<		L	←	l		←	
1	1	0	1	13						Double Height	New Background	-		=		M	→	m		→	
1	1	1	0	14						SO ^①	Hold Graphics	.		>		N	↑	n		÷	
1	1	1	1	15						SI ^①	Release ^② Graphics	/		?		○	#	o		□	

① These control characters are reserved for compatibility with other data codes

② These control characters are presumed before each row begins

□ Character rectangles

Black represents display colour

Whits represents background

Table 1. The transmission code used largely corresponds to the ASCII code. The only difference is that the 'non-printable', or rather control, characters do not have the same significance here, as they are adapted especially for teletext purposes.

page structure: 24 rows of 10 picture lines each.

SAA 5051 TROM

After the SAA 5041 TAC, this Teletext Read Only Memory chip is by far the most important IC in the entire decoder. The TROM not only acts as a character generator but also fulfils a number of other significant tasks. As can be seen from figure 10, the chip decodes control characters, switches colour outputs, generates both alphanumeric and graphic characters and converts parallel bit patterns received from the character ROM into a serial signal. Finally, it processes each character that is to be transmitted until the

matrix format fades (characters rounding) and each character is clearly legible.

The page memory controls nearly all these functions. All that the signals produced by the SAA 5020 TIC do is make sure everything happens at the correct time. The code in which the teletext information is transferred is practically a perfect copy of the ASCII code. The codes 'unprintable' (or illegal) characters are often used in a computer as control characters. This is the same case in the teletext decoder, only here the code words have a different meaning. Table 1 shows the relationship between the code and the character set + control codes. Wherever neces-

ary, a more detailed explanation will be given in the section describing the use of the teletext decoder to be published in a forthcoming issue.

Whenever a control code is used somewhere in the middle of the page text, the corresponding place on the screen is filled with a space. Although this means that every transition from text to graphics and any change in colour will result in a space, this is not noticeable in practice. This decoder control method has the advantage that no additional memory space is required.

The page memory of a teletext decoder can therefore be restricted to 1 k byte. In any case only seven bits of every byte are used. The 64 graphic characters shown in columns 2a, 3a, 6a and 7a in table 1 are derived directly from the seven bit code word. Figure 11 illustrates how a graphic character is made up of various bits. Bit 6 is not used, because this is always logic 1 (see table 1).

Characters are formed according to the well-known 5 x 7 matrix. Usually text is written on the screen in the non-interlace mode. This means that the two fields which make up the picture are written on top of each other instead of being interlaced (see figure 12). In the case of teletext, however, the interspace mode is used for improved readability. As figure 12 shows, the diagonally opposed matrix dots in a character undergo a sharp transition which is detrimental to the character's legibility. The TROM detects such transitions and adds half a dot wherever necessary in the even raster. This doubles the matrix density, resulting in a 10 x 14 matrix. The final product is an easy-to-read, well-rounded character.

Preview

The complete decoder is drawn in figure 13 and, as readers will see, is a rather complex project and impossible to describe in full detail here. The main circuit diagram is made up of two sections, the actual decoder and the control unit. Further details will be saved for a following issue.

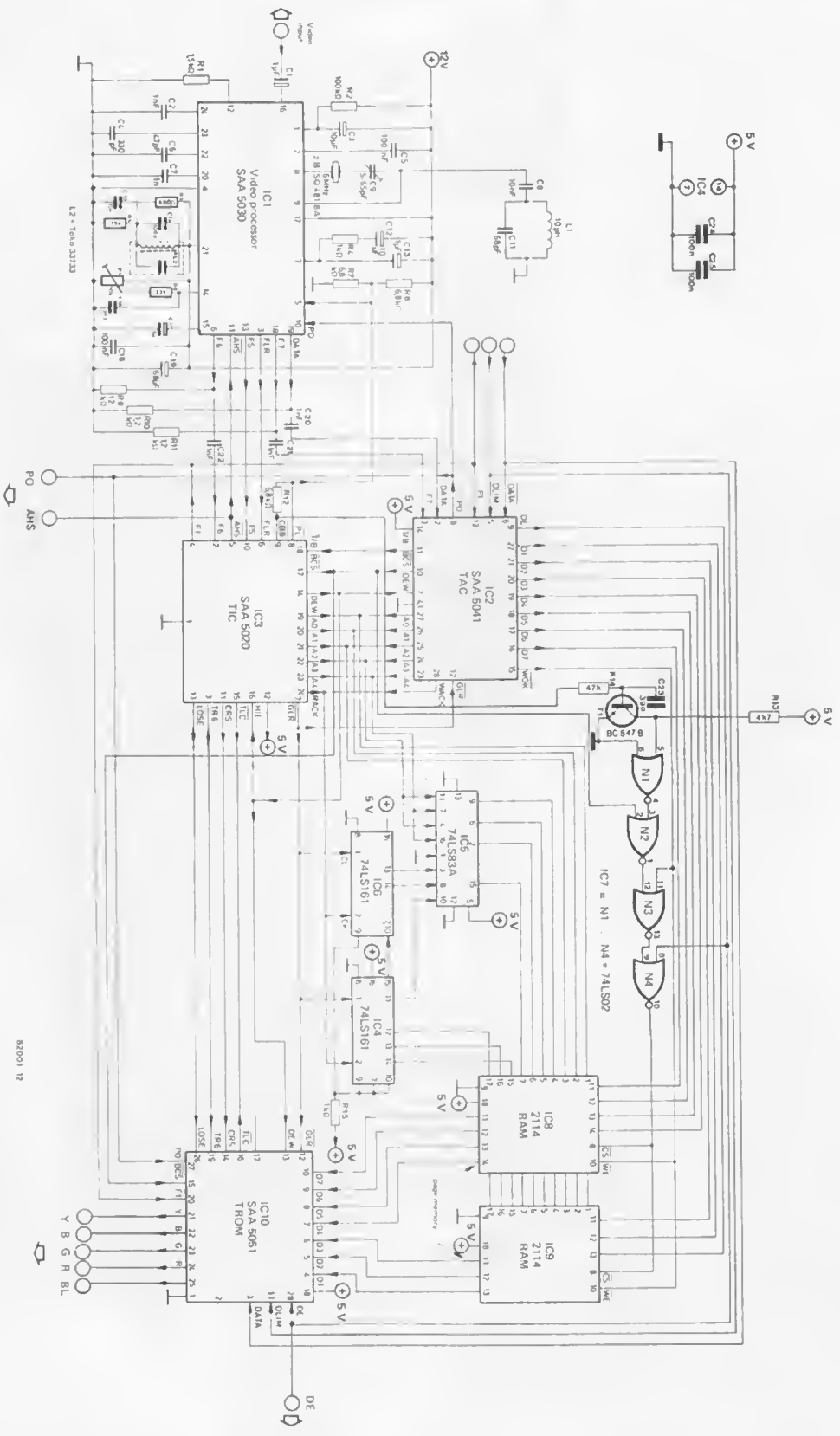
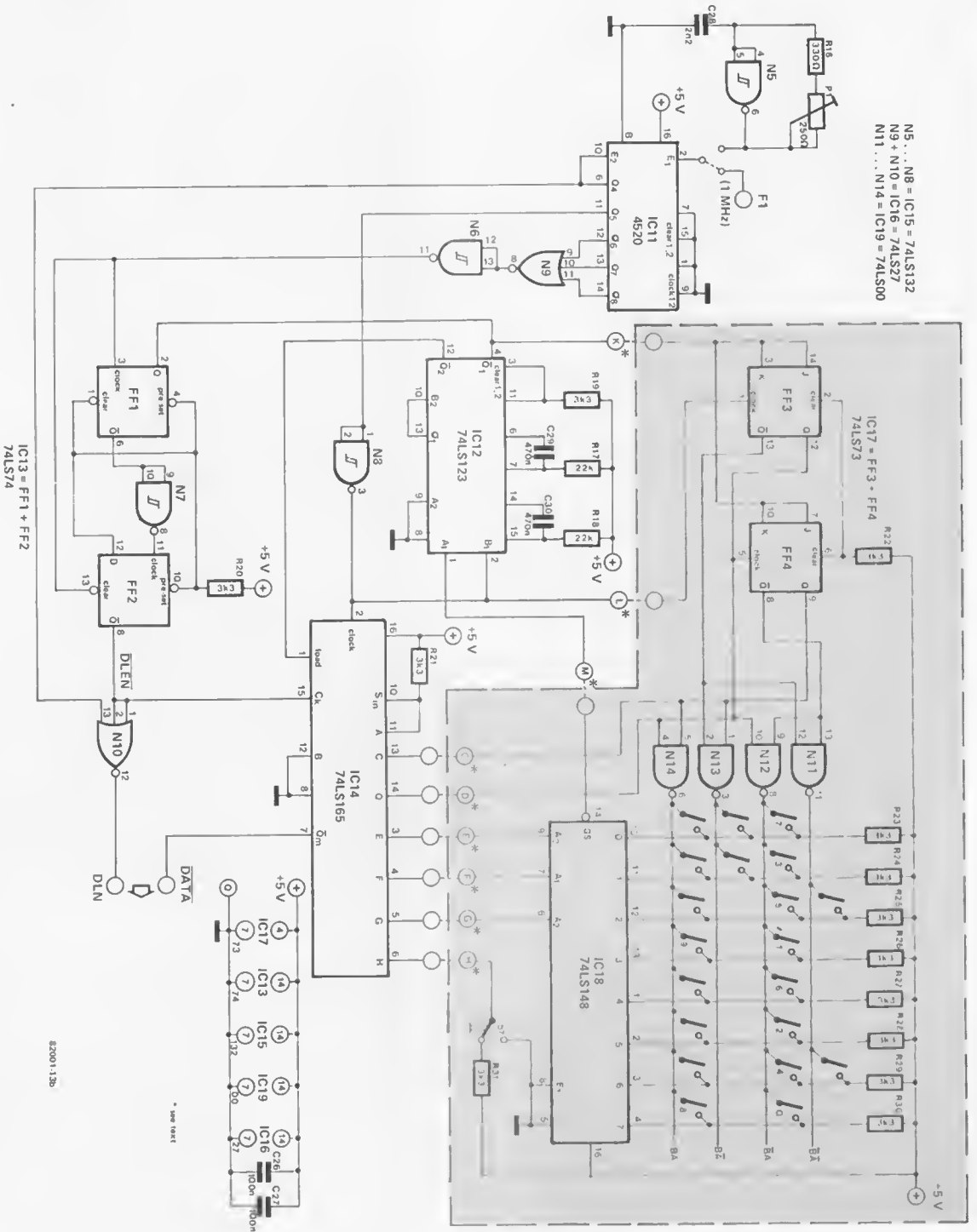
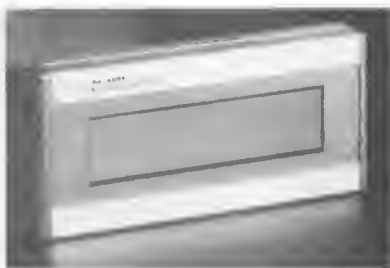


Figure 13. The actual teletext decoder circuit diagram. This section roughly corresponds to the block diagram shown in figure 5.

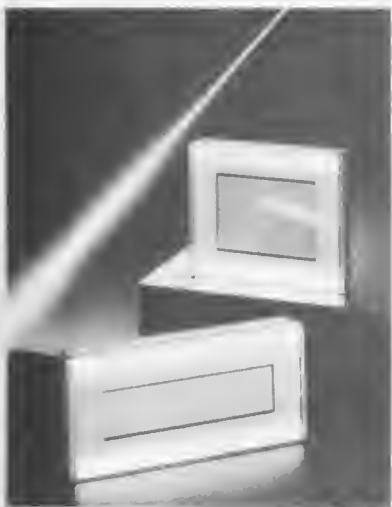


market



Flat-screen display units

Two flat screen electro-luminescent display panels, one intended mainly for messages and the other for general graphics, have been launched in the U.K. by Impectron Limited. The units, both manufactured by Sharp Corporation, are only 39 mm thick and of extremely lightweight construction.



Each unit incorporates all necessary decoding and drive circuitry, and both make use of the well established electro-luminescent principles in which light is emitted when an luminescent layer is excited by an applied electric field.

The Message Display Unit, model S-1050, provides a screen area of 186 x 50 mm, containing 65,536 pixels (picture elements). It is constructed using 512 lines of vertical transparent electrodes on a glass substrate, upon which a layer of luminescent material is sandwiched between two insulating layers. On top of these layers is a stratum of 128 lines of horizontal electrodes. When an appropriate drive voltage is applied to one vertical and one horizontal electrode, one pixel at the 'crossing point' emits a bright orange-yellow spot of light measuring approximately 100 μ m square. The Graphics Display Unit, model S-1021A, operates on exactly the same principles, but has 320 lines of vertical electrodes with 240 lines of horizontal electrodes — providing a total screen of 76,800 pixels.

Both types of display incorporate logic and driver circuits which may be controlled from externally applied signals, and both types may be used to display moving or stationary graphic patterns, symbols or characters as required. Four input signal lines are required, i.e. data signals, data transfer clock, horizontal synchro signal and vertical synchro signal — as well as power supply lines. The desired display position of any image is specified by selecting the appropriate vertical and horizontal electrodes in an X-Y matrix. Because each pixel is generated at a fixed point, the image is sharp, stable and without either distortion or glare. The orange-yellow colouring

and uniform distribution of luminous intensity also combine to minimise eye strain.

Each unit is offered with two control-board options, for simplified interfacing with micro-computer systems. The S-1026S Unit Interface Board is designed for character and coded graphic displays, while the S-1026F board is used for full graphics display applications. A separate power source unit (designated S-1040) is also available.

*Impectron Limited,
Foundry Lane,
Horsham,
West Sussex RH13 5PX.
Telephone: 0403.50111*

(2111 M)

Low-cost speech module

The TINYtalker is claimed as the simplest introduction yet to low-cost speech synthesis. Just announced by Texas Instruments, it is a self-contained unit which speaks any of eight phrases at the touch of a button. Add a 9 V supply and loudspeaker, says TI, and it is fully operational. Priced at £39.50, it can be interfaced with microprocessor control for such applications as warning systems and video games.

TINYtalker uses the TMS 5100 voice synthesis processor, linked with three TTL parts and the TMS 2532 EPROM to make it a stand-alone module. A single EPROM holds eight phrases, each of which — through the high data compression of TI's Linear Predictive Coding technique — can be more than four

seconds long. The module's phrase selection can be simply increased by the addition of TMS 2532s (or TMS 2516s for shorter phrases). If microprocessor control of the module is required, the addition of a TTL part buffers the TINYtalker for interface to any parallel output port.

An evaluation EPROM and full instructions are included with the TINYtalker. Other phrases can be built from TI's extensive speech 'library' or — for production system requirements — can be custom-manufactured. The TINYtalker and speech library are available through all TI's franchised distributors.

*Texas Instruments Limited,
Manton Lane,
Bedford, HK41 7PA.
Telephone: 0234.67466*

(2106 M)

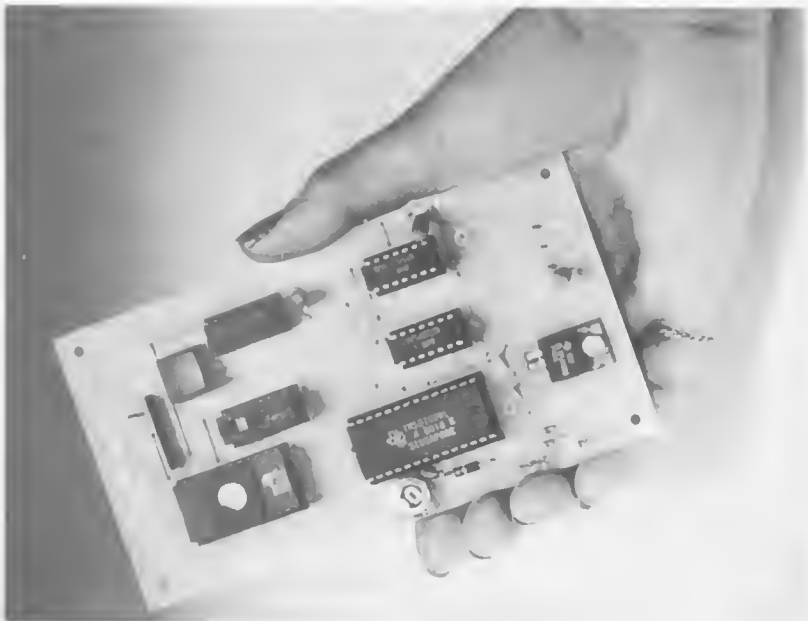
World's first 64K bipolar PROM

Harris Semiconductor has introduced the world's first 64K bipolar PROM (Programmable Read Only Memory). The HM-76641 is a monolithic device, utilising the same basic process technology as the Harris HM-76161 16K PROM. The 64K PROM is in an 8K word by 8 bit/word format, currently available in a 24-pin DIP and guaranteed over the commercial temperature and voltage ranges.

The new device has a TAA (Address Access Time) of 85 NSec maximum. The HM-76641 offers a four-fold increase in memory size over currently available 16K PROM's in the same 24-pin package and with approximately one fourth of the power dissipation per bit. The device is programmed with the Harris generic PROM programming specification. Therefore, presently available commercial PROM programming equipment will program the HM-76641.

*Harris Semiconductor,
Harris Systems Limited,
145 Farnham Road,
Slough,
Berkshire.
Telephone: 0753 34666*

(2104 M)



market

Light weight wire wrapping tool

OK's EW-7D electrically-powered wire wrapping gun has been designed for production use with 22 - 32 AWG (0.8 - 0.2 mm) wire, having a rugged motor designed for extended periods of use with long life and low maintenance.



The tool's body is made of a tough reinforced plastic, for lightness. Versions are available incorporating a backforce device which prevents over-wrapping, which could occur with inexperienced operators, and a reversible model can also be supplied for both wrapping and un-wrapping. A wide range of wire-wrapping bits and sleeves, to handle the various wires, complements the EW-7D.

OK Machine & Tool (UK) Ltd.,
Dutton Lane,
Eastleigh,
Hants SO5 4AA.
Telephone: 0703 610944

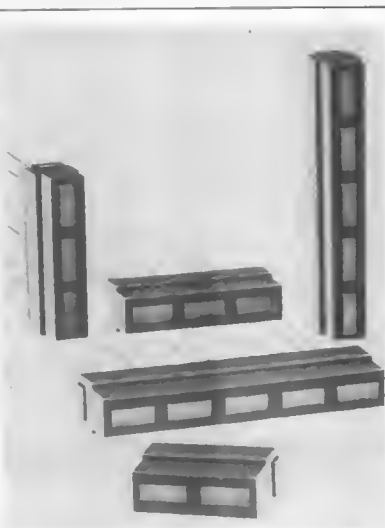
(2069 M)

New multi-LED arrays

Recently introduced by ZAERIX Electronics Ltd. a new range of multi-LED arrays provide a choice of 2, 3, 4 or 5 segment LED lamp units, all housed in black bezels.

Being fully end stackable and thereby enabling multiple arrays of any number of segments to be assembled, the housings are designed to be push-fit into a correctly dimensioned panel cut-out.

Available in any combination, the diffused lens range is red, green and yellow, behind which are housed red (GaP), green (GaP) and yellow (GaAsP/GaP) LED's, giving up to 1.5 MCD @ 20 mA luminous intensity.



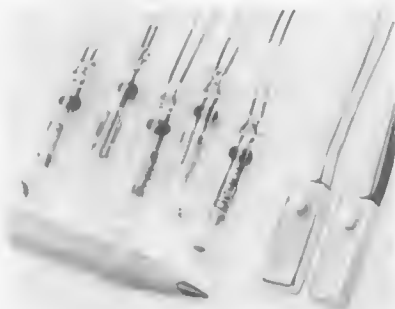
Capable of operating over a temperature range of -40°C to $+80^{\circ}\text{C}$, typical power dissipation figures are 120 mW and wavelengths at peak emission are 695, 565 and 585 nm for red, green and yellow respectively.

Zaerix Electronics Limited,
46 Westbourne Grove,
London W2 5SF,
Telephone: 01.221.3642

(1997 M)

The Heat Beaters!

A recent addition to the thermostat range from Cetronic Dynamics, the dual-purpose Titherm thermo switch will provide protection against over current or dramatic heat rise in ambient temperature. If required, both these functions can be combined, using the same thermo switch, by choosing the correct rating.



Two types are available — 5 amperes in a glass sealed bulb and 9 amperes in a metal case, both measuring no more than 35 mm in length. Typical applications include transformers, chokes, heaters, motors, battery chargers, soldering machines or any type of electrical coil.

Cetronic Limited,
Hoddesdon Road,
Stanstead Abbots,
Ware, Herts SG 12 8EJ,
England.
Telephone: 0920 871077

(2074 M)

Selective level meter

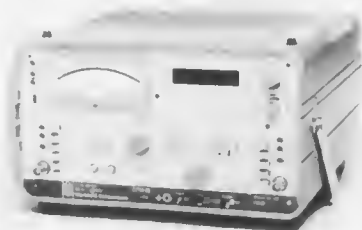
The first instrument to be manufactured in the UK by W & G Instruments Ltd. is a selective level meter, designed and manufactured at the Greenford-based company's Plymouth Factory, recently acquired in their takeover of Hatfield Instruments.

Designated SPM-30, this selective level meter is compact and accurate with a wide frequency range of 200 Hz to 1.6 MHz. The instrument is also capable of wideband level measurement and has been specifically designed for the surveillance and maintenance of modern FDM systems.

Features include semi-automatic calibration and a synthesised local oscillator which greatly increase the accuracy and stability of frequency control enabling 1 Hz resolution in tuning. Frequency setting is shown on a seven segment liquid crystal display. The meter is equally suitable for measurements in the audio frequency range and on balanced or unbalanced FDM systems up to 300 channels.

Another feature of the SPM-30 is the fast signal detector. While tuning through a range of frequencies a signal may appear so momentarily that the meter is unable to respond. However, if the signal is higher in level than a certain defined threshold then the signal detector LED will illuminate for half a second. Location of discrete frequency signals is therefore very much simplified.

The measurement bandwidth is switchable between 24 Hz and 1.7 kHz. Wideband is selected for rough or end-to-end measurements, to speed level measurements, and to enable noise measurements on voice channels, effective noise bandwidth being equal to that of the CCITT psophometrically weighted filter.



The SPM-30 can be used in conjunction with the built-in Tracking Generator PSE-30 which supplies both a balanced output signal in the range 200 Hz to 620 kHz and an unbalanced output signal from 200 Hz to 1.62 MHz. Levels are continuously adjustable from +10 dB down to -60 dB. The combination of SPM-30 and PSE-30 forms a complete level measuring set-up for making end to end measurements on FDM systems.

The instruments are housed in a compact die-cast metal case fitted with a convenient carrying handle, and operates from AC mains or internally fitted re-chargeable batteries.

OO on behalf of:

W & G Instruments Ltd.,
Progress House,
142 Greenford Road,
Greenford, Middlesex.
Telephone: 01-575 3020

(2103 M)

ELEKTOR BOOK SERVICE



JUNIOR COMPUTER BOOK 1 — for anyone wishing to become familiar with (micro)computers, this book gives the opportunity to build and program a personal computer at a very reasonable cost.

Price — UK £4.25 Overseas £4.50

JUNIOR COMPUTER BOOK 2 — follows in a logical continuation of Book 1, and contains a detailed appraisal of the software. Three major programming tools, the monitor, an assembler and an editor, are discussed together with practical proposals for input output and peripherals.

Price — UK £4.75 Overseas £5.00

300 CIRCUITS for the home constructor — 300 projects ranging from the basic to the very sophisticated.

Price — UK £3.75 Overseas £4.00

DIGIBOOK — provides a simple step-by-step introduction to the basic theory and application of digital electronics and gives clear explanations of the fundamentals of digital circuitry, backed up by experiments designed to reinforce this newly acquired knowledge. Supplied with an experimenter's PCB.

Price — UK £5.00 Overseas £5.25

FORMANT — complete constructional details of the Elektor Formant Synthesiser — comes with a FREE cassette of sounds that the Formant is capable of producing together with advice on how to achieve them.

Price — UK £4.75 Overseas £5.00

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