elektor

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up-to-date electronics for lab and leisure

Summer Circuits 79

double issue
with more than 100 circuits

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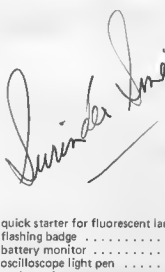
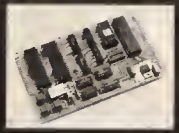
elektor 51/52 contents

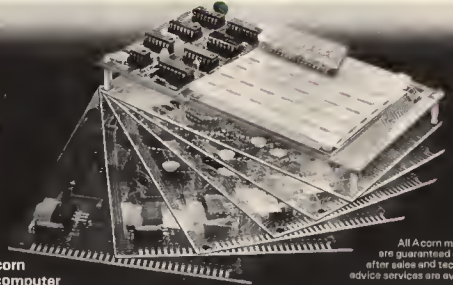


Three Trumps from Acorn



Acorn Controller

Designed as an industrial controller module, it is based on the 6502 CPU with 2K Eprom, 1.25K ram and 32 I/O lines. In eurocard format it is provided with an onboard monitor (2 x 74S571) giving comprehensive development and debugging facilities. Also available in minimum configuration for low cost OEM applications.



The Acorn Microcomputer

The Acorn controller module mounted beneath a matching eurocard with hex keyboard, 8 digit seven segment display and CUTS tape interface requires only a single unstebilised power supply to form the powerful Acorn microcomputer.

Although designed for expandability the Acorn Microcomputer is a complete development system for the Acorn controller and together with the Acorn Users Manual provides the perfect introduction to hex programming; the carefully optimised monitor has the following functions:

System Program
Set of sub-routines for use in programming
Powerful de-bugging facility displays all internal registers
Tape load and store

All Acorn modules are guaranteed and full after sales and technical advice services are available.

Acorn Memory

The first in our series of expansion cards is the Acorn 8K + 8K "state of the art" memory module. On a matching eurocard it provides 8K of ram (2114) and 8K of Eprom (2732) or 4K of Eprom (2716). It requires a single 5V rail, is designed for direct connection via a 32 way edge connector to the Acorn bus and is fully buffered for wiring into any system. Two onboard sockets provide independent positioning of Eprom and ram.

Software available soon includes 4K-Editor-Assembler-Disassembler. 4K Proprietary Fast Basic, Disc operating system with full file handling.
Although a standard strip of veroboard is all that is required for a full backplane, a racking system can be made available by Acorn Computers. The rack shown includes the VDU interface, two memory cards and duel floppy disc interface.

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Send to: Acorn Computers Ltd. 4A Market Hill. Cambridge. Cambs.

- ☐ (qty) Acorn Microcomputer(s) in kit form at £65.00 plus £5.20 VAT
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- ☐ (qty) Acorn Memory(s) assembled and tested at £95.00 plus £7.60 VAT

N.B. Price shown is for full 8K of rem. prices for smaller memory options and Eprom additions available on request.

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ACORN COMPUTER

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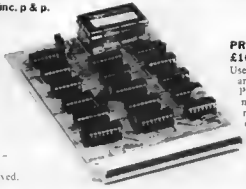
VDU MODULE. £31.62 (£25.14 without character generator) inc. p & p.

Displays up to 1k memory (16 lines x 32 chars. with character generator; or 4096 spot positions in graphics mode) on UHF domestic TV. Eurocard-sized module includes UHF modulator, runs on single 5 V supply. Complete ascii upper-case character set can be mixed with graphics.



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Use to transfer your own program developed and debugged on the MK 14 RAM to PROM - 74S571 to replace SC105 monitor for special applications, e.g. model railway control. Software allows editing and verifying.

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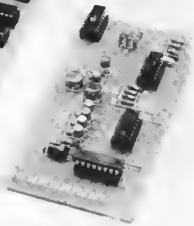

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Widely-reviewed microcomputer kit with hexadecimal keyboard, display, 8 x 512 – byte PROM, and 256 – byte RAM, and optional 16-lines I/O plus further 128 bytes of RAM.

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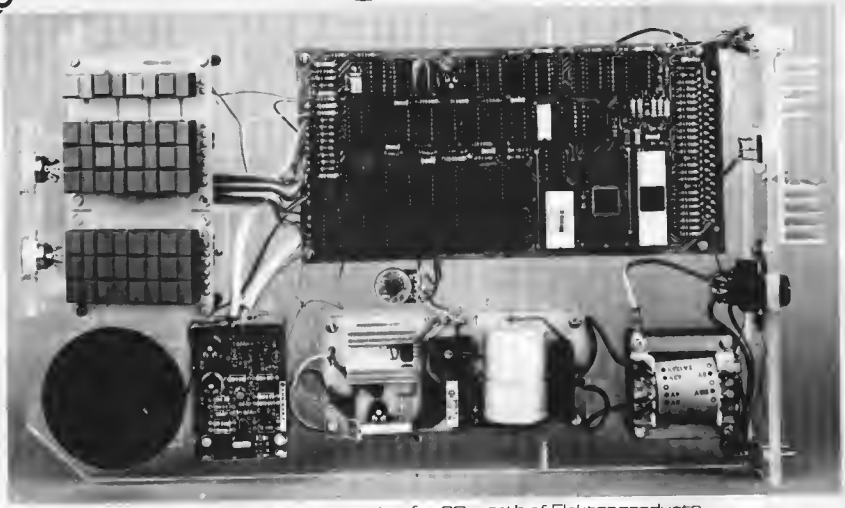


Fifty readers will win a voucher for £8 worth of Elektor products
simply complete and send of the voting card for the

Elektor International Circuit and Design Idea Competition

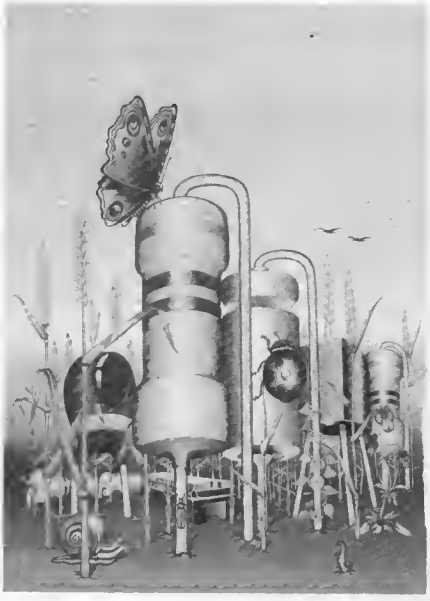
51 Voting cards will be drawn and one could be yours

vote now!

Summer Circuits 79

The Elektor £ 10.000 competition

This edition of Summer Circuits differs from our traditional double issue since almost all of the contents ere entries to our competition.
The response to the competition wes outstanding with over 3000 circuits and design ideas submitted from all corners of the world (and beyond). In practical terms, this is about two miles of paper and presented our steff with an enormous task in sorting and evaluating the various merits of each individual entry.
The standard, as expected, was high, making the selection of a short list very difficult, however the 100-odd circuits included in this issue are those chosen as being the most interesting and original.
All the designs are as submitted by the authors with only minor but necessary modifications in a few cases. It is the intention that the prizewinning entries will, at a later date, get the full Elektor lab. treatment with possible modifications and improvements and a printed circuit-boerd design.



The short short list

The 20 winning entries will be chosen from this issue, by you, our readers. A 'voting card' is included elsewhere in this edition and you ere invited to list, in your order of preference, the circuits and/or design ideas thet appeal most to you. Although the card has positions for ten selections there is no obligation to list them all. Your vote can be any number from ona to ten selections.
It must be noted that those circuits containing printed circuit boards ere not entries in tha competition and should not therefore be included in your selection.

Prizes

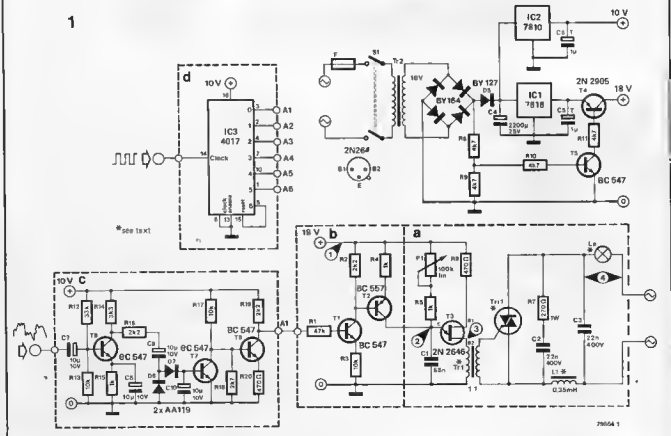
Out of the voting cards returned, 51 will be drawn. One of these cards will win a complete kit for the T.V. games project, while the other 50 will receive gift vouchers for £ 8 worth of Elektor products, books, printed circuit boards or subscriptions. The closing date for returning the card is August 27th (postmark date), so that the final results can be published in our November issue.

More prizes

Over £ 7.500 worth of prizes will be distributed amongst the 20 entries that receive the highest vote. The number of votes for any particular circuit will determine its share in the prize; the more votes, the bigger the prize!
However, in the event of an extreme vote in favour of one or two circuits, a limiting rule will come into effect, the maximum prize for any one entry being £ 2000.
The remaining £ 2500 will be awarded by an Elektor jury consisting of members of the editorial staff for our several language editions. The selection will be made on the same basis as the original selection; the most interesting and original circuits will be awarded.

1 disco lights

1

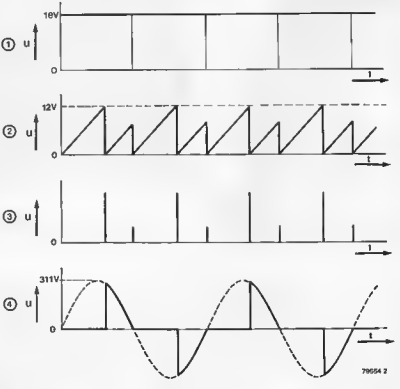


Flashing lights are very much an integral part of the disco scene nowadays. Usually the lights are controlled or modulated in some way by the music, i.e. the lights turn on and off or become dimmer or brighter in accordance with the volume or pitch of the audio signal. The circuit described here can be used either as a dimmer, 'running light' controller, or form the basis of a light organ.

The circuit, as shown in figure 1, is divided into a number of separate blocks, each of which has a distinct function. The supply stage is of course an essential, although if the circuit is used exclusively as a dimmer, IC2 and C6 can be omitted. The remainder of the dimmer circuit is contained in block (e).

Together with T3, components P1, R5, R6 and C1 form a sawtooth generetor which, via the pulse transformer Tr1, is used to trigger the triac. To ensure good synchronisation with the mains waveform the triac is turned off every 10 ms. This is achieved by transistors T4 and T5 momentarily removing the supply to

2



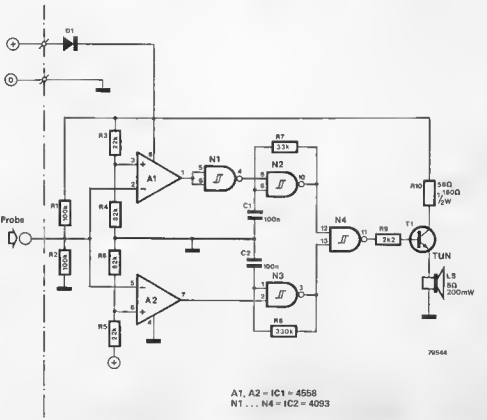
the oscillator (see figure 2). The position of P1 determines the brightness of the lamp, which is continuously variable from zero to full on. With the aid of block (b), the brightness of the lamp can be varied by an external control voltage (4 . . . 8 V) which can be derived from a variety of add-on circuits. An example of one such control circuit is shown in block (d). By connecting each A-output of the 4017 to a circuit consisting of blocks (a) and (b), a running light effect is obtained. The 'speed' of the running light will of course be determined by tha frequency of the clock signal applied to IC3.
If tha brightness of the lamp is to be modulated by the music signal, block (c) is used. The audio signal (from a preamplifier) is first amplified by T6 and then rectified by diodes D6 and D7. A DC voltage proportional to the input signal thus appears across C10. This voltage is then fed via T7 and T8 to the base of T1. Particular attention has been paid to suppression of triac interference, since any mains transients etc. generated by the triac switching on and off will be rendered audible as pops and crackles in the loudspeaker. L1 is a conventional r.f. choke; the gauge of wire used for this coil, and indeed the rating of the triac itself, will depend upon the siza of lamp(s) to be switched. C2 and C3 also form part of the suppression circuit, and should be rated at 400 V.
The satisfactory operation of the circuit is largely dependent upon the quality of Tr1. This should be a transformer with a turns ratio of 1 : 1 and can be home-made by winding 2 x 150 turns of 0.3 mm enamelled copper wire on a partitioned coil former, into which a 6 mm ferrite core is scrawed.
fn view of the high voltages involved, it goes without saying that due care should be taken in the construction of the circuit.

G. Ghijselbrecht (Belgium)

3-state CMOS logic indicator 2

The following circuit will provide an audible indication of CMOS logic states. Logic '0' is represented by a low frequency tone (roughly 200 Hz), logic '1' by a high frequency tone (approximately 2 kHz), whilst an undefined level produces no output signal.
The circuit functions as follows: two comparators are connected such that at voltage levels between roughly 21 and 79% of the supply voltage the two oscillators formed by N2, R7, C1 and N3, R8, C2 are both inhibited. With input voltages greater than 79% of supply, the output of A1 swings low, thereby, (via inverter N1) starting the 'high frequency' oscillator. On the other hand, input voltages below 21% of supply take the output of A2 high, starting the 'low frequency' oscillator. The oscillator output signals are fed to a simple buffer stage and then to a suitable loudspeaker.
The power supply should be drawn from the circuit under test, and must lie between roughly 5 and 15 V.

D. Hackspiel (Switzerland)

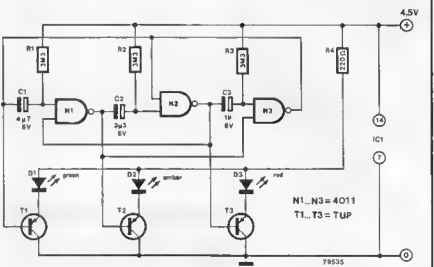


3 miniature traffic lights

Although the following circuit was submitted by the author as a design for an unusual brooch, it is certainly not limited to that application alone. For instance it could prove useful for the model enthusiast, or find favour with our younger readers as a 'novelty' badge.

The operation of the circuit is virtually self-explanatory. Each of the outputs will go low in turn whilst the other two are held high. The time for which each LED remains on is determined by the corresponding RC constant. Three 1.5 V 'pen' cells will prove adequate to power the circuit.

J. Ladage (The Netherlands)



4 model railway block section controller

This simple circuit offers model railway enthusiasts a cheap alternative to the fairly expensive block section controllers which are available commercially. The circuit suffers from one disadvantage, namely that it can be used to control traffic in just one direction. However, cost may dictate that this is acceptable.

The circuit and how it is connected to the rails, is shown in the accompanying diagram, where the direction of the trains is assumed to be from right to left. As can be seen, the 'earth' rail is broken at three places (using insulating track sections which are available in model shops). The lengths of rail sections A and B will influence at what point the train stops, and should be chosen to suit individual circumstances (the length of the train(s) for example). The red and green lamps (L1 and L2) are built into a set of signals.

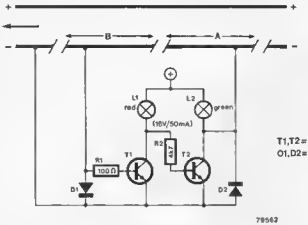
The circuit works as follows: As long as there is no train in the vicinity, the green lamp (L2) will be lit and section A of the track is connected to earth via the circuit. Transistor T1 is turned off, so that transistor T2 is turned on via L1 and R2.

Should a train then approach, nothing will happen as long as it remains on block A of the track.

When the train advances to block B, however, diode D1 is forward biased via the motor of the train, which will slow down slightly since the diode drops 0.7 V of the supply voltage. The voltage dropped across the diode also turns on T1, causing the red lamp (L1) to light up. At the same time T2 turns off, extinguishing the green lamp and breaking the connection between block A of the track and earth. A subsequent train entering block A of the track is therefore forced to a stop.

As soon as the first train leaves block B, the initial situation is restored, i.e. T2 conducts, the green lamp is turned on and the connection between block A of the track and earth is restored. The train waiting in block A can therefore continue on its way.

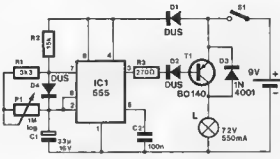
The circuit can also be used to control a crossing. The 'A' sections of track are laid before the crossing, and the B section forms the crossing itself. The signals are of course positioned on the approach to the crossing.



A. van Kollenburg (The Netherlands)

burglar's battery saver 5

Elektor attempt to cater for everyone and included hera is a circuit for gentlemen in the nocturnal profession. Put an end to stumbling in the shrubbery with the torch light controller described here. Incidentelly it is elso en excellent battery sever. Verying the brightness of a torch appears simple enough but using a series resistor or potentiometer is out of the question since power is dissipated in the form of heat. One solution is not to use e d.c. supply voltage but rether e squareweve with a varieble duty cycle. The brightness of the lemp then depends upon the length of the duty cycle.
In the circuit shown, e 555 timer is



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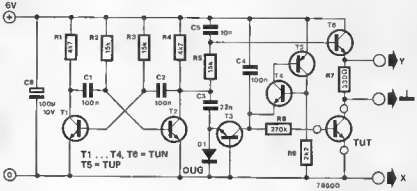
connected es an astable multivibrator and used to supply the squarewave. The duty cycle of the squarewave can be veried by potentiometer P1. Diodes D1 . . . D3 protect the circuit if the polarity of the bettery is reversed in which case the circuit will not operate and the torch will be 'full on'. Gentlemen, do not change your batteries in the dark!

C. Hentschel (Germany)

curve tracer 6

This transistor tester is not intended as a fully-fledged meesuring instrument; it can be used when a general indication is required of the I_C/U_{CE} characteristic of a transistor. Furthermore, it is sufficiently reliable for use when looking for 'matched pairs'. Only NPN transistors can be tested, as well es diodes. Obviously, an oscilloscope with separate X- end Y-inputs is required.
The circuit consists of three sections: a multivibretor, a staircase generetor end a squere-to-sawtooth converter. The multivibrator (T1 end T2) produces a 1 kHz squarewave. Its output is used to drive e so-called 'diode-transistor pump' (C3, C4, D1, T3), to obtein the steircase weveform; T4 end T5 reset the 'staircase' each time the bottom step is reeched.
This second section merits a more detailed explanetion, for those readers who are unfamiliar with the 'diode-transistor-pump'. Let us assume that C4 is initielly discharged — the voltage et the C4-T3-T4 junction is almost equal to the supply voltage.
During the positive half of the squareweve from T2, C3 is charged to the supply voltage. When the collector of T2 swings down to supply common, C3 will pull the emitter of T3 down so that this transistor turns on. The charge on



C3 is transferred to C4, pulling the voltage et the C4-T3-T4 junction down one 'step'. Each following negative-going swing at the collector of T2 pulls the junction voltage down one further step, until T4 turns on. This turns on T5, and an 'evalenche' effect now repidly discharges C4, ready for the next series of steps. The total number of steps in each cycle depends on the retio between C3 and C4; in this circuit, 5 steps are obtained.
The third section, the squere-to-sawtooth converter, is not quite so complicated. It consists of R5, C5 and T6. The 'exponential' sawtooth obtained is good enough for this application.
When in use, the staircase waveform is epplied to the base of the transistor under test (TUT) and the sewtooth to its collector. The voltage across R7 is proportionel to the (varying) collector current end is epplied to the Y-input of the 'scope. The X-input is used to displey the collector-emitter voltage.
Since the base current varies in five steps, five plots are obtained for I_C (verticel axis) es a function of U_{CE} (horizontal axis). If desired, e different number of plots can be obtained by chenging the values of C3 and/or C4.
Diodes can also be tested: the anode is connected to R7 end the cathode to supply common.

B. Darnton (United Kingdom)

7 pachisi

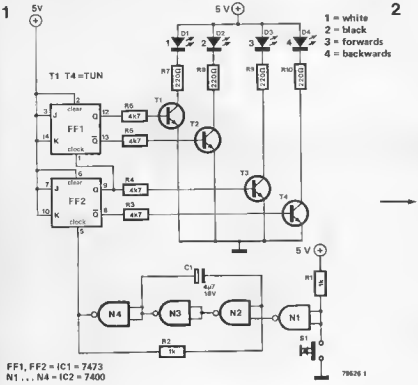
Pachisi is a simpla game for two players, which is designed to test people's 'frustation quotient'. The basic idea is that each player has a countar, which starts on one of the arrowed circles and then attempts to move round the board to the white rectangle in tha centre of the 'M'. The players move alternately and the first person's counter to reach 'home' is the winner. Four different types of move are possible: forwards, backwards, onto tha next white circle, and onto the next black circle. Thus it is effectively possible to move either one or two steps forwards or backwards each turn. If one player lands on the circle currently occupied by his opponent, the former is declared the winner, whilst if a player retreats backwards off the edge of the board, he is deemed to have lost.

The player's moves are determined by two pairs of LEDs. One pair decides whether the move is forwards or backwards, and the other pair whether it is to a white or black circle. Each tima the pushbutton switch S1 (see circuit diagram) is pressed, a new random combination occurs. Thus it could happen that one player is on the point of winning whan he is forced to taka 'two steps backwards'!

The actual circuit is straightforward. Two flip-flops form a two-bit binary counter, which is clocked by an oscillator built round NANDs N1 . . . N4. The oscillator is only enabled when S1 is closed. The output state of tha counter is displayed via transistors on the four LEDs.

H.J. Walter (Germany)

1



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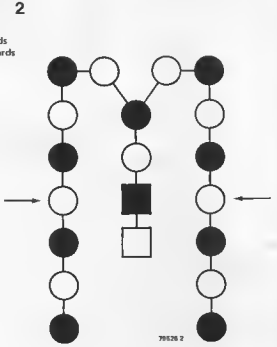
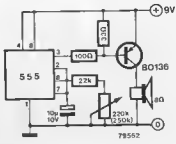


8 metronome

Although not exactly revolutionary, the circuit shown here is both very cheap and reliable. The well-known 555 timer IC is connected as an astable multivibrator, and delivers a regular train of pulses which are rendered audible via the transistor and loudspeaker. The frequency of the metronome can be varied with potentiometer P1. A 9 V supply voltage means that the circuit can easily be powered by batteries.

If a loudspeaker with an impedance of less than 8 Ω is used, it should be preceded by a series resistor (1 W) which will compensate for the difference in impedance (and – due to the lower current consumption – ensure that the batteries last longer).



W. Kluifhout (The Netherlands)

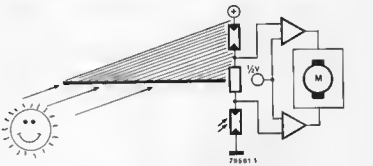
follow the sun . . . . solar tracker 9

Sunlight is now recognised as an important source of 'alternative' energy, and the use of solar panels to convert the sun's rays into electricity is becoming ever more widespread. For solar panels to operate at maximum efficiency, however, it is important that the cells face squarely into the sun. Since the sun's position is constantly changing (epologies to Messrs. Kapler end Galileo), it is thus necessary to employ a 'solar tracker', which will vary the orientation of the solar panel accordingly.

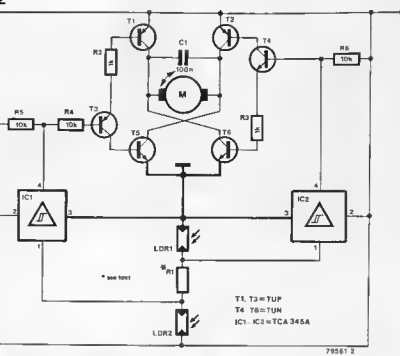
The position of the solar panel is determined by a reversible motor, which in turn is controlled by the circuit described here. The information concerning the alignment of the solar panel and sun is provided by two light dependent resistors (LDRs). These are mounted such that they lie in the same plane and are exposed to the sun, but are separated by a screen (see figure 1) mounted perpendicular to the plane of the LDRs. When the solar panel directly faces the sun, equal amounts of light fall upon each LDR and the motor is inoperative. However when the position of the sun changes, one of the LDRs will fall into the shadow of the screen. This imbalance in the amount of light falling on the two LDRs is detected by two comparators, which provide a control signal, causing the motor to restore the original state of equilibrium.

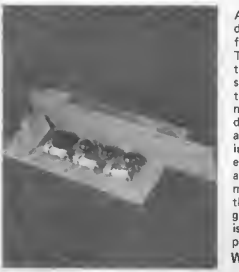
The circuit of the solar tracker (see figure 2) is based upon a transistor bridge configuration (T1 . . . T6) which incorporates the motor, end two comparators (IC1, IC2). The comparators heve a single input, the reference input being provided internally. When the outputs of IC1 and IC2 are both low, T1, T3 and T5 are turned off, whilst T2, T4 and T6 are turned on, with the result that the motor turns clockwise. With both comparator outputs high, T2, T4 and T6 are turned on, whilst T1, T3 and T5 are turned off, and the motor rotates in the opposite, i.e. anticlockwise, direction. If the output of IC1 is high and the output of IC2 is low, the motor is turned off. This situation occurs over a 'dead zone', i.e. a range of differences in tha resistance of the two LDRs over which the system fails to react. This ensures that the solar panel is not continuously turned to and fro as a result of small fluctuations in the resistance of the two LDRs and of the hysteresis of the system.

1



2





A suitable motor (with speed reduction gearing) can be obtained from most modal shops.

To ensure that the opereting range of the LDRs is not exceeded in even the strongest of sunlight, it is advisable to mount them below filters. The most suitable value for R1 will depend upon the speed of the motor, and can best be determined experimentally. The circuit can be powered from the solar panel itself. To avoid exceeding the maximum permissible supply voltage of the ICs, the supply voltage should not be greater than 10 V. The ideal solution is to take a 9 V tap from the solar panel.

W. H. M. Dreumel
(The Netherlands)

10 improved DNL

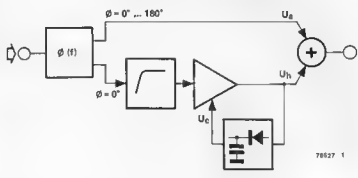
Dynamic Noise Limiting (DNL) is a noise reduction system patented by Philips, which is particularly useful for the reproduction of (cassette) tape recordings. As the name suggests, the system is dynamic, i.e. the noise is only suppressed at the moments when it is most intrusive which, in the case of a music signal, is during the quieter passages. The system also exploits an interesting psychoacoustic effect, namely that during quiet passages the high frequency signal components are less important than is the case during louder sections of the music. A DNL circuit utilises this fact by attenuating the high frequency components, and hence the noise, during low amplitude portions of the input signal.

The circuit described here is an updated and improved version of older DNL circuits. The most significant point in its favour is that the point at which noise reduction starts is continuously variable.

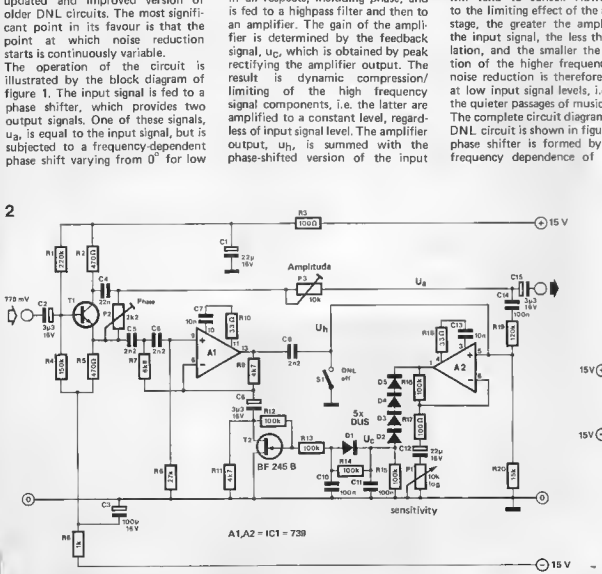
The operation of the circuit is illustrated by the block diagram of figure 1. The input signal is fed to a phase shifter, which provides two output signals. One of these signals, u_a, is equal to the input signal, but is subjected to a frequency-dependent phase shift varying from 0° for low frequency signals to 180° for high frequency signals. The second output signal is identical to the input signal in all respects, including phase, and is fed to a highpass filter and then to an amplifier. The gain of the amplifier is determined by the feedback signal, u_C, which is obtained by peak rectifying the amplifier output. The result is dynamic compression/limiting of the high frequency signal components, i.e. the latter are amplified to a constant level, regardless of input signal level. The amplifier output, u_h, is summed with the phase-shifted version of the input signal. Since the phase shift was frequency-dependent, the high frequencies present in the two signals will tend to cancel. However due to the limiting effect of the amplifier stage, the greater the amplitude of the input signal, the less the cancellation, and the smaller the attenuation of the higher frequencies. The noise reduction is therefore severest at low input signal levels, i.e. during the quieter passages of music.

The complete circuit diagram of the DNL circuit is shown in figure 2. The phase shifter is formed by T1, the frequency dependence of the shift

1



2



being obtained by combining the collector ($\Phi = 180°$) and emitter ($\Phi = 0°$) signals via P2 and C4. The highpass filter is realised by the circuit round op-amp A1. This filter has a third-order Butterworth response with a turnover frequency of 5,5 kHz. The filter output is amplified/limited by A2. The gain of A2, and with it the sensitivity of the circuit, can be varied by means of potentiometer P1.
The peak detector consists of 4 series-connected diodes, which ensures that the control signal, u_c, is only present when the input signal rises above a certain level. A FET, T2, is used to form the voltage controlled attenuator in the feedback loop of A2. The two signals u_a and u_h are summed via preset potentiometer P3 and the series connection of R19 and C14.
The DNL function of the circuit can be rendered inoperative by means of switch S1, which simply shorts the signal u_h to earth.
During construction care should be taken to ensure that the output signal of op-amp A2 is kept at least several centimetres from the signal-carrying leads, so as to prevent the possibility of crosstalk.
The circuit can be set up by driving it with a pure noise signal, such as that from an off station FM tuner, and varying P2 and P3 for maximum attenuation.
The circuit as shown is optimised for standard level audio signal levels, i.e. 0 dB = 770 mV RMS, but can also be used for other signal levels.

R.E.M. van den Brink
(The Netherlands)

resistance bridge 11

Generally speaking, resistors with a 5% tolerance are more than adequate for most of the circuits published in Elektor. However from time to time there may be occasions when 1% resistors are required, or when the value of two resistors must be matched to within 1%. This is the case with for example digital meters, where it is worth the extra expense of using very accurate attenuator resistors in order to fully exploit the accuracy offered by a digital display.
The circuit described here allows two resistors, R_X and R_Y, of the same nominal value to be compared with one another, and the difference to be expressed directly in per cent.
The accuracy and stability of the circuit are better than 0,1%, and resistors from 10 Ω to 10 MΩ can be measured, providing the maximum permissible dissipation is not exceedad, i.e. ¼ W types for example should be greater than 27 Ω.
The operation of the circuit is basad upon the resistance bridge formed by R_X, R_Y and the voltage divider R1, P1 and R2. If R1 and R2 are exactly the same value, the bridge current will be proportional to the extent to which R_X and R_Y deviate from the mean value of these two resistors. For small differences between R_X and R_Y the current is, to all intents and purposes, proportional to the difference between the two resistors. The percentage difference between the two 'unknown' resistances is expressed directly on the scale regardless of which resistor is the greater. However with the aid of the simple comparator formed by T1 and T2, which of the two rasistors is the greater can be displayed on LEDs D1 and D2.
The circuit can be adapted to suit a variety of different meters. If a centre-zero reading meter or a DVM (with a floating input) are available these would be ideal in which case components D1 ... D7, R4 ... R6, T1, T2 and the two LEDs can be omitted. A universal meter with a 0-10 or 0-30 scale would also be suitable.
The table lists other examples of possible meters and indicates the component changes required as well as the range scale obtained.
High stability metal oxide or 1% precision wirewound resistors should be used for R1, R2 and R3.
Calibrating the circuit is quite straightforward. P1, which should preferably be a multi-turn type, is provisionally set to the mid-position and two resistors of the same nominal value are connected in circuit. The meter reading is noted, and then the resistors changed over. If the new reading is the same as the first, no further adjustment is required. If that is not the case, P1 is adjusted until the average of the two readings is obtained. If desired the procedure can be repeated once more for an extra check.

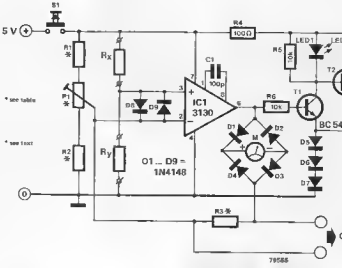


Table:

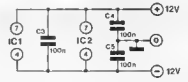
scale	meter M	R1 = R2	P1	R3	DVM
0- 3%	0- 60 µA	1k2	100 Ω	5 k	−0.3 ... +0.3 V
0-10%	0-200 µA	1k2	100 Ω	5 k	−1 ... +1 V
0-10%	0-500 µA	475 Ω	50 Ω	2 k	−1 ... +1 V
0-10%	0-200 µA	1k2	100 Ω	500	−0.1 ... +0.1 V
0- 1%	0- 50 µA	475 Ω	50 Ω	2 k	−0.1 ... +0.1 V

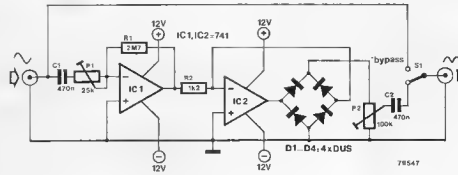
J. Borgman (The Netherlands)

12 octave shifter for electric guitars

Effects units for electric guitars are extremely popular. One of the popular weapons in the arsenal of the well-equipped rock guitarist is an octave shifter, a unit which doubles the frequency of the guitar signal.
One of the ways of achieving frequency doubling — and the approach adopted here — is full-wave rectification, as commonly carried out in power supply circuits. As can be seen from the accompanying circuit diagram, the rectification is performed by a diode bridge. By including the diode bridge in the feedback loop of IC2, the non-linear voltage characteristic of the diodes has no effect upon the signal.
Pre-amplification of the guitar pick-up signal is provided by IC1. The gain of this stage is set (by P1) such that the signal is just on the point of clipping. Preset potentiometer P2 can be adjusted so that the output signal level is the same as that of the input signal. A bypass switch, S1, is included allowing the unit to be switched in and out.
As is apparent from the sketches of the input and output signals, the signal is not only doubled in frequency, but is also distorted. The sound becomes considerably harsher, as well as being shifted up en octave. This feature would probably be considered en asset to the contemporary rock musician.

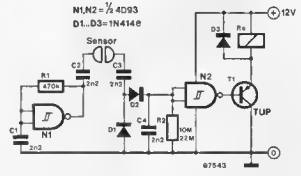
H. Schmidt (Germany)





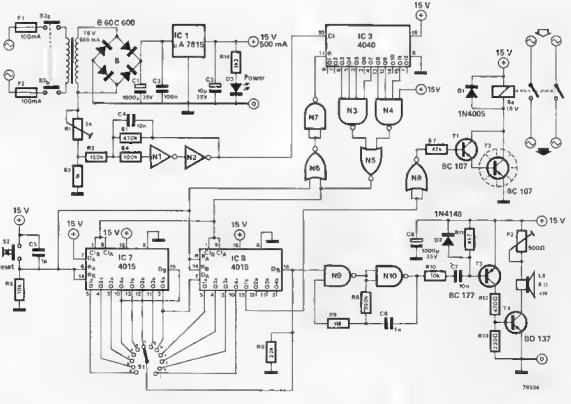
13 liquid level sensor

An annoying drawback of many liquid level sensors is the effect of electrolytic reaction between the liquid and the sensors. Metal electrodes are prone to corrosion and consequent loss of effectiveness (reduced conductivity), with the result that they have to be replaced at frequent intervals.
One solution to this problem is to ensure that there is an AC, rather than DC potential between the sensor electrodes. The constant reversal of electrode polarity drastically inhibits the electrolytic process, so that corrosion is considerably reduced.
The actual circuit of the level sensor is extremely simple. The circuit around N1 forms an oscillator. If the two sensors are immersed in a conducting solution, C4 will be charged up via the AC coupling capacitors (C2 and C3) and the diodes, so that after a short time, the output of N2 is taken low and the relay is pulled in. The relay can be used to start a pump, for example, which in turn controls the level of the liquid. When a conductive path between the two sensors no longer exists, C4 discharges via R2, with the result that the output of N2 goes high and the relay drops out.



E. Scholz (Switzerland)

sun lamp timer 14



Before setting off for (hopefully) sunnier climes, many prospective holidaymakers use a UV lamp to acquire an initial tan. Unfortunately, things can go rather amiss, and instead of a nice golden brown, the careless or forgetful user can end up the colour of one of Har Majesty's pillar boxes! The following circuit was designed to prevent any of our readers from suffering just such a painful experience.

The circuit is basically a timer, which after a preset interval will produce an audio tone to warn the sunbather that his time is up. If the audio tone provokes no response from the user, the lamp is automatically switched off (via a relay) after another 30 seconds. If the sunbather wishes to turn over and brown another part of his or her anatomy, or someone else is to take his place, then by operating a reset button the lamp is prevented from switching off. The operation of the circuit is quite straightforward. A 50 Hz squarewave is derived from the transformer secondary and fed to a 12-bit binary counter (IC3). The outputs of the counter are gated (N3 . . . N5) such that a pulse is supplied to the clock inputs of IC7 and IC8 every 30 seconds. Furthermore IC3 itself is also reset every 30 seconds. IC7 and IC8 are shift registers, the outputs of which are takan high in turn by successive clock pulses. The position of S1 therefore determines how long it takes before the oscillator, which is formed by N9, N10 and associated components, is started. The oscillator, together with an amplifier stage and loudspaeker, provides the audio warning tone. With S1 in position '1', this period equals 12 x 30 s = 6 minutes. Thirty seconds later, the next output of IC8 (Q1b) will go high, causing the relay to drop out and switch off the UV lamp.

At any stage pressing S2 will reset ICs 3, 7, and 8, thereby initiating a new count cycle.

The volume of the warning tone can be varied by means of P2, whilst LED D3 provides a visual indication of whether the circuit is switched on. A relay which is capable of switching reasonably large currants, but which itself has a fairly small pull-in current (max. 100 mA) should be used.

A. W. Zwamborn
(The Netherlands)

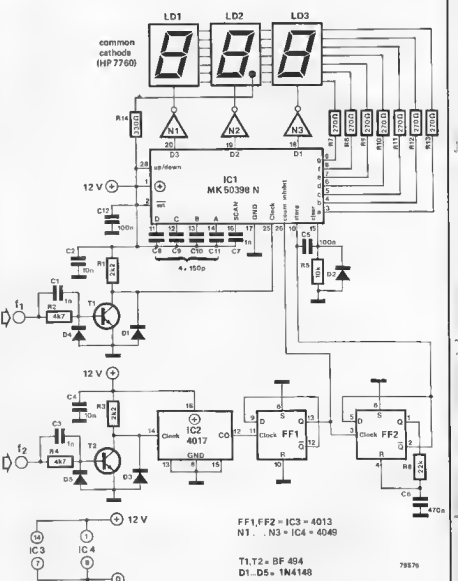
15 frequency ratio meter

There are certain situations, e.g, when checking frequency multiplier or divider circuits, PLL circuits, certain music circuits etc., where it is more important to measure the frequency ratio of two signals, rather than simple measurement of frequency itself. With the aid of the circuit shown here, the ratio between the frequency of two signals, f_1 and f_2, can be measured and displayed directly on three seven-segment displays. The circuit will measure ratios up to 99.9 with an accuracy of 0.1, providing f_1 is larger than f_2.

The heart of the circuit is the counter/display driver IC, MK 50398N, from Mostek, which has already been described in Elektor (see below). The higher frequency, f_1, is fed via the input stage around T1 to the clock input (pin 25) of the counter. Pulses will be counted at this input provided pin 26 (count inhibit) is held low. Decade divider IC2 and flip-flop FF1 ensure that this pin is in fact held low for exactly ten cycles of the lower frequency signal, f_2. Thus a number appears on the displays which is ten times the ratio between f_1 and f_2. By arranging for the decimal point to light between the second and third digits, the resulting figure is thus exactly equal to the ratio f_1/f_2. Flip-flop FF2 is connected as a monostable, and is used to provide the counter IC with the correct 'store' and 'clear' pulses on pins 10 and 15 respectively.

Literature:
¼ GHz Counter, Elektor 3B, June 1978.

W. Dick (Germany)



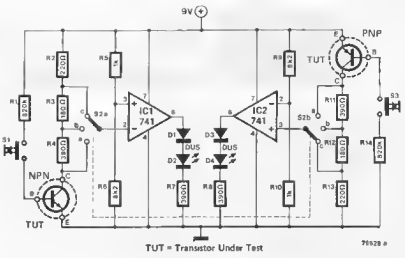
16 transistor tester

Although not a precision instrument, this transistor tester should nonetheless prove a useful aid for checking the quality of 'job lots' of transistors. The circuit will determine whether or not a transitor is defective, and whether the current gain of the transistor puts it in the class of 'A'-type transistors (current gain 140 . . . 270), 'B'-type transistors (270 . . . 500), or 'C'-type transistors (greater than 500).

To test for example an NPN transistor, the device is inserted in the appropriate socket (TUT = transistor under test) and S2 switched to position C. If LED D2 lights up, the transistor is type C, if the LED remains out then S2 should be set to position B, or, if this fails to have any effect, to position A. In each case the position of S2 in which the LED lights up indicates the class of transistor. If the LED fails to light even in position A, then it is defective, or has a current gain of less than 140, which for small signal transistors means that they are basically unusable. The base current to the transistor under test can be interrupted by means of

pushbutton switch S1. If the LED does not go out, it means a short exists between collector and emitter of the transistor.

The operation of the circuit is quite simple: The transistor under test receives a base current of 10 μA via R1. Assuming the transistor is not defective, this results in a voltage drop across R2 . . . R4, and depending upon the position of S2, a portion of this voltage is compared with a fixed reference voltage by IC1. The operation of the right hand side of the circuit is virtually identical, except that it is arranged for PNP transistors. The circuit can be powered by battery.



R. Storn (Germany)

'de luxe' transistor tester 17

Like the previous circuit, this transistor tester will indicate whether the current gain of the transistor under test is that of a class 'A'-, class 'B'- or class 'C' type. The circuit will also determine whether or not the transistor is defective. The advantage of this design, however, is that the class of transistor is automatically determined and shown directly on a seven-segment display.

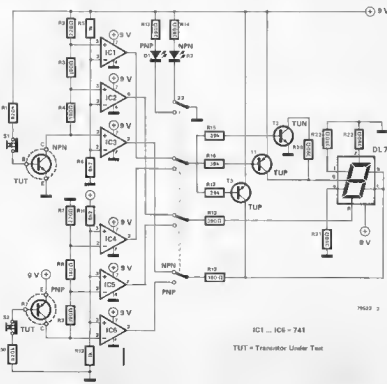
The operation of the circuit is in many respects similar to its predecessor. Depending upon the current gain of the device under test, a certain DC voltage is dropped across resistors R2 . . . R4 in the case of NPN transistors, or across R7 . . . R9 in the case of PNP transistors. As this voltage increases (i.e. the greater the current gain of the transistor under test), the outputs of comparators IC1 . . . IC3 (IC4 . . . IC6 for PNP transistors) will go low in turn. The output state of the three comparators is decoded by R15 . . . R19, T1, T2 and T3, such that 'A', 'B', 'C' or 'F' appears on the seven-segment display.

'F' indicates a defective transistor, and is also obtained if no transistor is connected in circuit, or if the push-button switch in the base lead of the transistor is pressed (opened). If that is not the case, the transistor has an emitter-collector short.

S3 is used to switch between NPN and PNP types.

The display is a common-anode type.

R. Storn (Germany)



18 FM stereo noise reduction

It is a well-known fact that the signal-to-noise ratio of a VHF FM receiver is better on mono than on stereo. This principle is in fact used in some FM stereo noise reduction systems: crosstalk is introduced between the stereo signals to reduce the noise, while retaining some of the stereo effect. Since noise is more annoying at higher frequencies, some circuits only mix the two signals at higher frequencies.

A good noise suppression system would be one where the crosstalk is introduced gradually, as required — not switched on abruptly by an (electronic) switch. It would be better still if the signal level not only determined the amount of crosstalk, but also the turnover frequency above which crosstalk occurs.

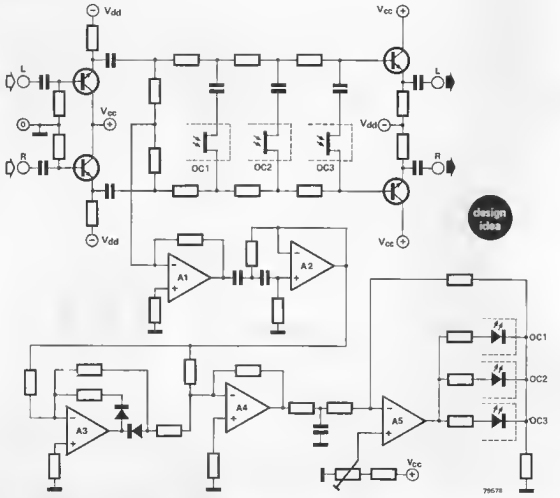
These considerations are the basis for the design idea presented here.

The two channels are mixed via optocouplers (OC1 . . . OC3) that use light-sensitive J-FETs. Admittedly, these are anything but readily available; however, they have better linearity than standard types — and that means less distortion.

The capacitors in series with the optocouplers are chosen so that the turnover frequency decreases as more of the photo-J-FETs are turned on. The control voltage for the optocouplers is derived from the input signals. These are summed in A1 and fed through a high-pass filter (A2). The output from this filter is proportional to the high-frequency content of the stereo signal. After rectification (A3), buffering (A4) and smoothing, this signal is compared to a reference voltage in A5. The output from A5 is used to drive the LEDs in the optocouplers. As the high-frequency content of the input signals rises, the driva to the LEDs is decreased so that the crosstalk between the channels is reduced. Noise reduction therefore only occurs when it is necessary: at low lavels.

Q. A. Rice (United Kingdom)

OC1 . . . OC3 =
opto coupler H11F1
(General Electric)



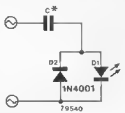
19 LED lamps

When it comes to mains indicator lamps, there are basically three main options: neon lamps, incandescent lamps, and LEDs. Neon lamps have the advantage that they can be connected direct to the mains supply, and also that they consume very little power. Incandescent lamps, on the other hand, must be connected to a much lower voltage (e.g. to the secondary side of the transformer), and therefore provide only indirect indication of whether the mains supply is present, whilst as a rule dissipating a relatively large amount of power.

LEDs would represent an ideal alternative to both the above approaches, since they have a longer operating life than either neon or incandescent lamps, and dissipate no more than 20 to 30 mW. Unfortunately it is necessary to protect the LED from excessive currents by employing a series resistor, which, with a mains voltage of 240 V, will itself dissipate something over 3.5 W. The circuit shown here offers a better solution. The current through the LED is limited to a safe value not by a dropper resistor, but by the reactance of a capacitor. The advantage of this method is that no power is dissipated in the capacitor, since the current though the latter is 90° out of phase with the voltage dropped across it. The formula for calculating power dissipation for DC voltages is only valid for AC voltages provided the current and voltage are in phase i.e.

$$P_c = u_c \cdot i \cdot \cos \phi$$

With a phase shift of 90°, which is the case with capacitors, P_c is therefore 0 W ($\cos 90° = 0$). What little power is consumed by the circuit is entirely converted into light end heat by the LED.



* see text

The value of capacitor C, can be calculated for any given voltage, frequency and current with the aid of the following equation:

$$C \approx \frac{i}{6.28 \cdot u \cdot f}$$ where:

C is the capacitance in Farads
u is the RMS value of the mains voltage
f is the mains frequency in Hz
i is the current through the LED in Amps

With a mains voltage of 240 V, a frequency of 50 Hz and a current of 20 mA, the nearest suitable value of capacitor is therefore 330 nF. The working voltage of the capacitor should be at least twice the mains voltage.

Diode D2 is included to protect the LED from excessive reverse voltages.

U. Hartig (Germany)

20 news detector

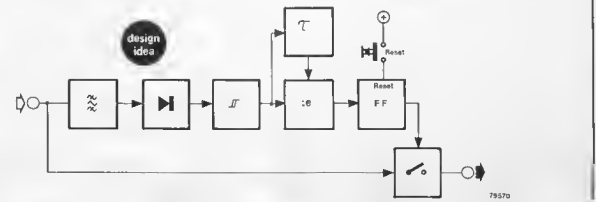
To many people the radio news bulletins are of primary interest. This design idea describes a method of switching on a radio by the 'pips' which of course immediately precede the news.

The principle involved is quite simple, and utilises the fact that the pips have a frequency of almost exactly 1 kHz. The radio is in fact switched permanently on, but because the (electronic) switch is normally open, the audio signal is not allowed to reach the output stage. Rather it is fed to a selective filter with a turnover frequency of 1 kHz. The output of the filter is rectified end used to switch a Schmitt trigger.

The output pulses from the Schmitt trigger are counted, end only when six pulses occur within a predetermined time is the switch closed and the audio signal fed to the output stage.

Once the news is over, pressing a reset button will once more cut out the eudio signal and return tha circuit to its initiel stete.

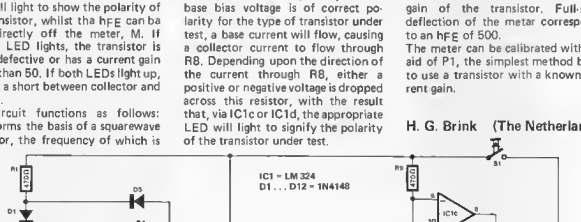
J. Pelsma (The Netherlands)



21 transistor tester

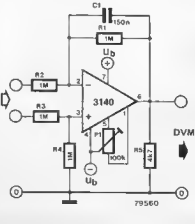
This simple tester circuit will determine whether a transistor is an NPN or PNP type and also measure the current gain of the unknown device.
When tha pushbutton switch, S, is depressed, one of the LEDs D13 or D14 will light to show the polarity of the transistor, whilst tha h_{FE} can ba read directly off the meter, M. If neither LED lights, the transistor is either defective or has a current gain of less than 50. If both LEDs light up, there is a short between collector and emitter.
The circuit functions as follows: IC1a forms the basis of a squarewave oscillator, the frequency of which is roughly 1 kHz. The squarewave oscillates about half supply voltage, and, with the aid of IC1b, is used to generate a base-emitter voltage which is alternately positive and negative. Thus whenever the polarity of tha base bias voltage is of correct polarity for the type of transistor under test, a base current will flow, causing a collector current to flow through R8. Depending upon the direction of the current through R8, either a positive or negative voltage is dropped across this resistor, with the result that, via IC1c or IC1d, the appropriate LED will light to signify the polarity of the transistor under test.
The collector current of the transistor also flows through the diode bridge and the meter, M. Sinca the base current remains more or less constant, the size of the collector current can be taken as a measure of the current gain of the transistor. Full-scale deflection of the metar corresponds to an h_{FE} of 500.
The meter can be calibrated with the aid of P1, the simplest method being to use a transistor with a known current gain.

H. G. Brink (The Netherlands)



22 floating input for DVM

Digital voltmeters are now in widespread use and growing ever more popular. Many of the chaapar types of DVM however suffer from a slight drawback in that they have an earthed input (i.e. one of the input terminals is connected to earth or to a fixed voltage level). In many cases this is not particularly important, however there are situations (if the DVM is used in conjunction with an add-on unit such as an AC millivoltmeter, for example) where it can be something of a nuisance. With the aid of the following circuit, formed around a differential amplifier, any DVM can be provided with a floating input.
It is recommended that 1% (metal film) types are used for the 1 M resistors (R1 . . . R4). The output voltage of the circuit is adjusted to 0 V by means of P1 (with the input shortcircuited). The supply voltages $+U_b$ and $-U_b$ can be anywhere between 3 and 20 V (provided they are symmetrical).



J. Borgman (The Netherlands)

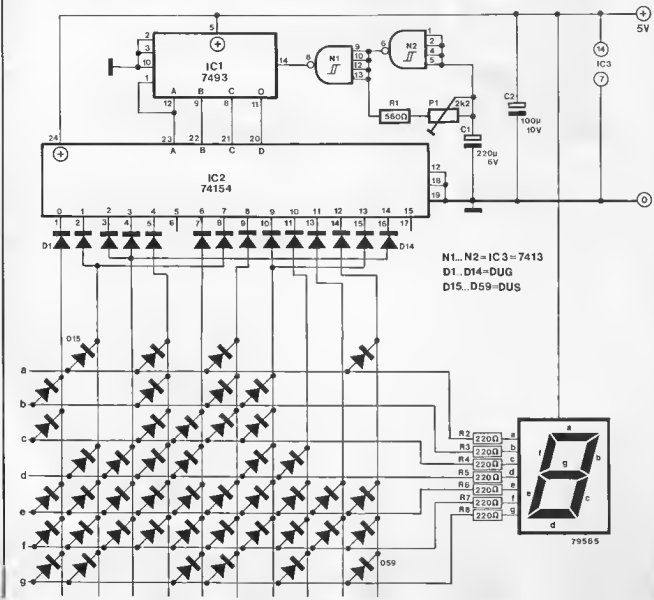
23 digital wooing aid

And now for something completely different . . . . Whether or not one will find the following circuit useful, the originality of the concept cannot be denied. The basic idea is to assist those unfortunate souls who seem to become tongue-tied when confronted with the object of their desires, and are incapable of expressing the intensity of their emotions in words. In such cases the 'wooing aid' can be presented to the prospective partner, who upon pressing the button, will be greeted with the immortal line 'Hello beautiful'! Of course whether this, admittedly ingenious, amorous gambit will succeed in achieving the desired result is another question.

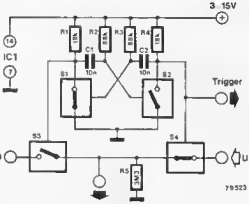
The actual electronics involved are quite straightforward. The circuit contains a clock generator (N1, N2), a 4-bit binary counter (IC1), a 4-to-16 decoder (IC2) and a diode matrix. The pulses from the clock generator are converted into binary code by IC1 and then fed to IC2, so that each of the outputs of IC2 are taken high in succession. The outputs are decoded by the diode matrix which ensures that the correct segments are enabled to produce the desired text. The rate at which one letter follows another is determined by the clock frequency, and may be varied by adjusting P1.

If, as was the case with the prototype version, a Minitron 3015F type display is used, R2 . . . R8 may be omitted. If a different display is employed, care should be taken to ensure that the current consumption is not excessively high. Otherwise it will be necessary to provide buffers (e.g. 7407's or 7417's) between IC2 and the diodes D1 . . . D14.

M. Muhr (Germany)



24 voltage comparison on a scope



There are several different ways to measure DC voltages — multimeters, multichannel oscilloscopes etc. However if one possesses only a single-channel scope, comparing several voltages must involve making more than one measurement. With the aid of the circuit shown here, it is possible to simultaneously measure and compare two different voltages on a single-chennel scope, provided the letter is equipped with an external trigger input.

The circuit is extremely simple, and uses only a single IC, five resistors and a couple of capacitors. The IC is a CMOS quad switch, 4016. S1 and S2 form part of an astable multivibrator, and are opened and closed in turn.

The two voltages to be measured are fed to S3 and S4, which are controlled by S1 and S2. Thus the two voltages ere fed alternately to the Y-input of the scope. The control signal for switch S4 is also used to trigger the scope.

The supply voltage (3 . . . 15 V) can be provided by, for example, a 9 V battery, which, in view of the circuit's low power consumption (under 1 mA), should be assured of a long life.

J. Meier (The Netherlands)

25 linear thermometer

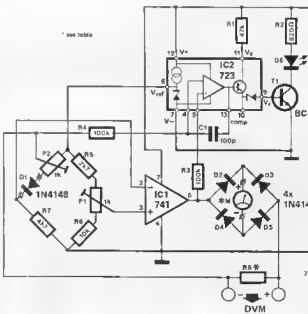
The circuit described here employs e forward-biased diode as temperature sensor. The forward voltage drop of a diode falls by approximately 2 mV for an increase in temperature of 1° C. Since this negative temperature coefficient remains the same regardless of actual ambient temperature, the scale of the thermometer will be linear.

The temperature coefficient of a diode is not particularly large, and is easily exceeded by thet of an NTC (negative temperature coefficient) resistor. However it is not possible to obtein e linear scale over a wide range of temperatures using an NTC resistor. Thus the use of a diode is justified by the wide measurement range obtained and by the ease of calibretion.

The sensor diode — D1 in the circuit diagram — is a common-or-garden 1N4148, which can easily be mounted apart from the rest of the circuit.

The diode forms part of e resistance bridge, comprising P1, P2, R5, R6 and R7. A reference voltage is provided by a 723. Thus the voltage on the non-inverting input of IC2 is held to a (variable) reference value via R5 and P1. Assuming the circuit is initially nulled by adjusting P1 and P2, variations in the forward voltage drop of the diode as a result of temperature fluctuations will cause the output of IC2 to swing either high or low depending upon whether the temperature rises above or falls below zero.

By using a diode bridge, D2 . . . D5, the meter will show a positive deflection regardless of the polarity of the temperature. To provide an



indication of whether the temperature is in fact above or below 0°, the output of IC2 and the reference voltage are effectively connected to the non-inverting and inverting inputs respectively of the 723, which thus functions as a comparator. Assuming the circuit is calibrated for zero deflection at 0° C, as the temperature falls, the voltage drop across the diode increases, therefore the voltage on the inverting input of IC2 falls, the output of IC2 goes high, taking the non-inverting input of IC1 high and with it the output of IC1. Transistor T1 therefore turns on, lighting the LED. When the temperature rises above 0° C, the reverse process occurs, resulting in the LED being extinguished.

Resistor R8 is included to allow the use of a DVM (with floating input) as a means of display. The accompanying table lists a number of alternative values for R8 along with the measurement ranges obtained for various (moving coil) meter scales. Of course, if a DVM is used, then the moving coil meter as well as D2 . . . D5, R1 . . . R4, T1 and the LED can be omitted.

Table 1

scale	meter M	temperature	R8	DVM
0 - 30	0 - 300 µA	−30 . . . +30° C	1 k	−0,3 . . . +0,3 V
0 - 30	0 - 100 µA	−30 . . . +30° C	3 k	−0,3 . . . +0,3 V
0 - 50	0 - 300 µA	−50 . . . +50° C	1.67 k*	−0,5 . . . +0,5 V
0 - 50	0 - 500 µA	−50 . . . +50° C	1 k	−0,5 . . . +0,5 V
0 - 100	0 - 1 mA	−100 . . . +100° C	1 k	− 1 . . . +1 V

* 2 × 3k3 parallel

The circuit can be calibrated by suspending the sensor diode (together with a suitable length of connecting wire!) in crushed ice which is beginning to melt. With P2 provisionally set to the mid-position, P1 is then adjusted so that zero deflection on the meter (or zero voltage across R8) is obtained. The diode is then dipped into boiling water, whereupon P2 is adjusted until a voltage of 1 V over R8 is obtained. The above procedure can then be repeated. It is best to use distilled or demineralised water for both steps of the calibration procedure.

J. Borgman (The Netherlands)

ten channel TAP 26

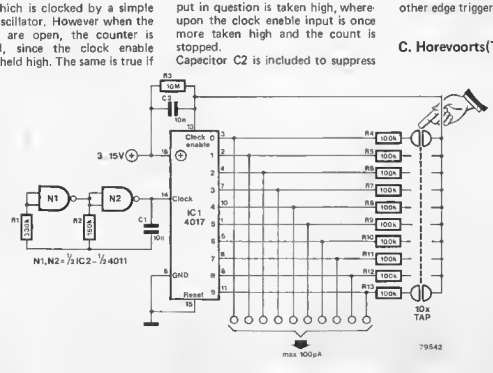
TAP (read: touch) switches come in all shapes and sizes, mainly as momentary action or simple on/off (latched) switches. Using only a handful of components, it is possible to construct a 'ten-channel' TAP, i.e. a ten-pole touch switch. When one of the ten sets of contacts is touched, the corresponding output will be taken high.

The heart of the circuit is formed by a CMOS decade counter/decoder, 4017, which is clocked by a simple CMOS oscillator. However when the contacts are open, the counter is inhibited, since the clock eneble input is held high. The same is true if the contacts are bridged, but the corresponding output is already high, since in that case the additional skin resistance will have no effect. However, if the corresponding output is low when a set of contacts is touched, the skin resistance (which is negligibly small compared to the other resistances) forms part of a voltage divider, thereby pulling the clock enable input low. The counter is started and increments until the output in question is taken high, whereupon the clock eneble input is once more taken high and the count is stopped.

Capacitor C2 is included to suppress mains transients etc., whilst R4 . . R14 prevent the possibility of a shock in the event of a short between the contacts.

It must be emphasised that when the counter is started, each output in turn will go high (for a very short period) until the selected channel is reached. This should not prove to be a problem with most applications, however provision must be made for this when used with flip-flops and other edge triggered devices.

C. Horevoorts (The Netherlands)



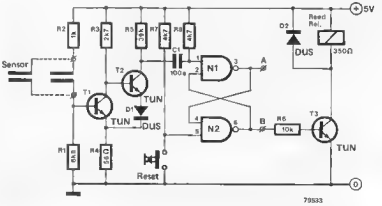
27 moisture sensor

When the circuit shown here detects the presence of moisture, it causes a reed relay to drop out. The relay can be used to disconnect a piece of equipment from its voltage supply, thereby eliminating the possibility of electrical shock.

The original application for the circuit was in an underwater camera which employed an electronic shutter. In the event of ingrass of water into the camera, the shutter circuit was disconnected, thus protecting the photographer from the risk of a high voltage shock. However the circuit can also be used in a variety of other applications, for example a 'leak detector' for boats, or as a 'dry-washing' indicator, etc.

The sensor is formed simply from a pair of copper wires held slightly apart, and the presence of moisture is detected by the resultant drop in the resistance between the wires. When this falls below a certain value, the output of the Schmitt trigger formed by T1 and T2 goes high. The flip-flop formed by N1 and N2 is thus triggered via C1, with the result that T3 is turned off and the relay drops out. The circuit also allows the option of the relay being pulled in when moisture is detected. R6 is simply connected to point A, rether than point B. The circuit is of a sufficiently 'universal' charactar that in place of the moisture sensor, virtually any alternative type of sensor (LDR, NTC etc.) can be used.

J. M. van Galen
(The Netherlands)



N1, N2 = IC1 = 4011,7400

28 digital heart beat monitor

The sight of so many interesting and diverse circuits contained in one issue may well lead to a quickening of the pulse rate for some of our readers. However, we have taken this into account by including the following design for a digitel heart beat monitor. The circuit measures the time interval between successive beats of the heart and then calculates the heart rate in beats per minute before displaying the result on a three digit LED display.

The heart beats are detected by using a miniature lamp and a photo-diode, encased in a clip which is attached to the ear lobe. Each time the heart beats, it pumps blood around the body, and the density of the blood in the ear lobe increases or decreases as the blood pressure varies. These differences in density between the times when the blood pressure is at its highest or lowest are detected by the photo-diode, thereby providing a pulse for each time the hearts beats. The time interval between successive heart beats is measured, and on the basis of this value the beet rate is calculeted. This is done by simply counting the number of pulses of a known frequency during the above time interval. The author chose a frequency of 166.7 Hz for this application, hence for a heart rate of 60 beats per minute, the time between successive heart beats will be 1 second, and e total of 166 pulses will be counted. Onca counted, these pulses are transferred to a 256 bit presettable counter, so that they can be divided into 10,000 by clocking exactly 10,000 pulses into the counter. Consequently, for a heart rate of 60 beats per minute, e total

of $\frac{10{,}000}{166}$ = 60 output pulses will be

available to be counted and displayed on the LEDs.

The circuit functions as follows: The gates N1 end N2 form en oscillator with an output frequency of 1 MHz. This is divided by a factor of 6,000 by counters IC3 and IC4 to produce the required 166.7 Hz reference frequancy. The variations in diode current are amplified by IC1 and IC2 so as to produce a pulsed output which is in sympathy with the heart beat. These pulses are fed to IC6 which gives an output pulse et pin 3 equivalent to the duration between successive beets of the heart. This counter is then inhibited so that no further heart beat pulses will have any effect. Both counters in IC5 are connected in series so that a total division of 256 is availeble. This counter is clocked by the 166.7 Hz reference frequency for the period between successive heart beats. Hence, a heart rate of 60 beats per minute will produce en output pulse from IC6 of 1 second duration which would permit 166 pulses to be counted in IC7.

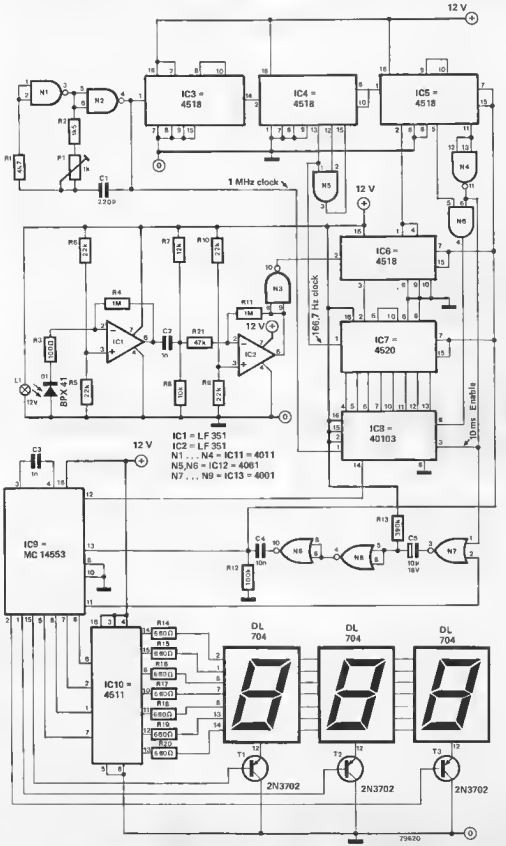
This number is transferred to the presettable counter IC8 which is clocked with exactly 10,000 pulses

so that a total of 60 pulses are available at its output. These heart rate pulses are then fed to the 3 digit counter/display chip IC9, and the result is subsequently displayed on the LEDs.

The circuit is designed so that IC8 will only receive an enable pulse after the initial counting sequence of the 166.7 Hz pulses has been completed. At the falling edge of the 10 ms enable pulse from IC5, the delay monostable is triggered, thereby inhibiting the count for roughly 3 seconds and allowing the display to be read off. Once this delay period has elapsed, all counters are reset in preparation for the subsequent count.

Care should be taken during construction to ensure that the circuit is *well* insulated from any mains voltages. However the use of batteries as power source is strongly recommended.

P. Lesh (United Kingdom)



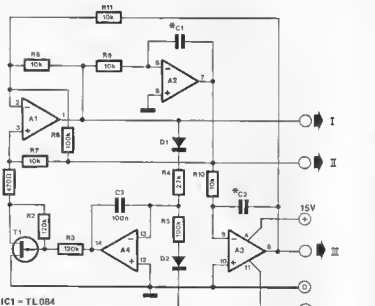
29 sinewave oscillator

Under certain conditions if the output of a selective filter is fed back to the input a sinewave oscillator is produced. In itself, the idea is not new (see for example the various spot sinewave generators published in Elektor), but the way in which it is realised in the circuit shown here is original.

The output of the state variable filter (again, no stranger to Elektor readers) formed by A1 . . . A3, R7 . . . R11, C1 and C2 is fed back (from the output of A2) to the input (left hand side of R7). The amplitude of the output signal is stabilised by the action of FET T1, which in conjunction with R1 forms a voltage-controlled attenuator. The control voltage is derived from the output of A1 via a diode-resistor network and the integrator round A4.

The sinewave signal is available at the outputs of A1, A2 and A3. Since A2 and A3 are connected as integrators, i.e. as lowpass filters, the distortion at output III will be lower than that at output I.

The integrators heve unity gain at the resonant frequency of the circuit.



A1 . . . A4 = IC1 = TL084
D1 . . . D2 = 1N4148
T1 = BF 245

The desired value of C1 and C2 can be calculated by:

$$C1 = C2 = \frac{16}{f}$$

where f is in kilohertz and C is in nanofarad.

G. Schmidt (Germany)

30 automatic heated rear windscreen

Cold weather is one of the banes of a motorist's life. Not only must he worry about the car starting on cold winter mornings, but there is the added nuisance of frozen windscreens to cope with. To help combat this latter problem, many cars are fitted with heated rear windscreens. Useful though these are, it still means one has to wait until the heating element has warmed up sufficiently to melt the frost before being able to move off. The circuit described here is designed to assist the motorist in a 'fast get-away', by ensuring that the heating element is switched on before he reaches the car.

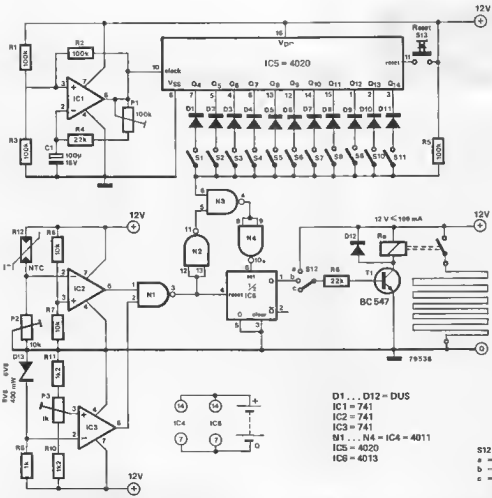
Basically the circuit will switch the heated windscreen on after a variable preset period. The idea is that before leaving the car in the evening, the motorist will calculate what time he expects to be using the car the following morning, and set the circuit accordingly. The circuit also incorporates two important safeguards – for the windscreen to be switched on the temperature must be below zero, and the car battery must be sufficiently well charged to ensure that the current drain of the heating element will not leave it flat.

	hours	mins	secs
S11	12		
S10	6		
S9	3		
S8	1	30	
S7		45	
S6		22	32
S5		11	16
S4		5	38
S3		2	48
S2		1	24
S1			42

The basic principle is quite simple: The circuit around IC1 is a square-wave oscillator which provides clock pulses to IC5, a 14-stage binary counter. The outputs of IC5 are ANDed together via diodes D1 . . . D11 and R5. The number of outputs gated together, and which outputs those are, can be selected by means of switches S1 . . . S11. Thus by closing various combinations of switches it is possible to vary the interval which elepses before pin 6 of N3 is taken high. The output of N3 will only go low, however, if both inputs are high, i.e. if the output of N2 is also high. For this to be the case both inputs of N2 must be low and hence both inputs of N1 must be high.

When the output of N3 is taken low, the output of N4 goes high, setting the flip-flop IC6 and pulling in the relay. However if the battery voltage falls below the reference level set by P3, the output of IC3 will go low, taking the output of N3 high and resetting the flip-flop. A suitable 'threshold value' for the bettery voltage would be 11 V.

Similarly, the ambient temperature

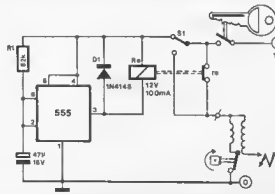


is monitored by the negative temperature coefficient resistor, R12. P2 is adjusted such that the output of IC2 goes high when the temperature falls to 0°C. Above this temperature the output of IC2 will be low, resetting flip-flop IC6.
Finally, tha remaining preset in the circuit, namely P1, is adjusted to provide the correct clock frequency. After resetting IC5, the Q8 output should go high after 11 minutes and 16 seconds.
The timing intervals provided by each of the switches S1 . . . S11 are listed in the accompanying table. Assuming, for example, that the heated windscreen is to be turned on eight hours and fifteen minutes after leaving the car, this interval can be obtained by closing switches S7, S8 and S10.

H.J.A. Roerdinkholder
(The Netherlands)

car anti-theft protection 31

The circuit described here is based on an unusuel method of deterring a possible car thief. Shortly aftar it is started en engine fault is simulated. Restarting gives the sama result suggesting that the car may be more troubla than it is worth.
The actual circuit is extremely simple. A 555 timer provides a delay of roughly 5 seconds. The normally closed contact of the relay is connected in the lead from the ignition switch to the ignition coil. Switch S1, which is used to arm the circuit, should of course be hidden.
When power is supplied to the circuit (via the ignition switch), the relay contact is initially closed and the engine will start. After the delay



period provided by the 555 has elapsed, the relay contact is opened and the ignition coil is switched out of circuit. The delay period can be altered as desired by selecting different values for R1 or C1.

B. H. J. Bennink
(The Netherlands)

32 autoranger

Although designed in the first instance for use with the universal digital meter which was published in Elektor 45, this circuit for an automatic range switch (for DC input voltages) can also be used with other meters. Input voltages between 0 and 1 V are fed directly to the output, voltages between 1 V and 10 V are attenuated by a factor of 10, whilst voltages between 10 and 100 V are attenuated by a factor of 100. Thus the output voltage fed to the meter will always lie between 0 and 1 V, regardless of the amplitude of the input voltage.

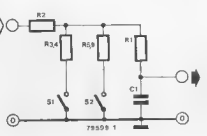
The basic principle of the circuit is illustrated by the diagram shown in figure 1. When both switches are open, the input signal is fed unattenuated to the output – always provided the meter input has a sufficiently high input impedance, which is the case with the Elektor universal digital meter. When S1 is closed, the input voltage is attenuated by a certain factor – in the actual circuit this factor is 10. If both S1 and S2 are closed, the degree of attenuation is increased still further (a factor of 100). In the autoranger circuit S1 and S2 are electronic switches which are controlled by comparators. The comparators effectively measure the input voltage level, and are biased to switch at roughly 0.96 V and 9.6 V.

Figure 2 shows the complete circuit diagram of the autoranger. The voltage divider formed by R7/R8 divides the input voltage by 3, which is then buffered by IC2. Another voltage divider network, R9 . . . R11 is connected to the output of IC2, and provides further attenuation by a factor of 10. A voltage of roughly 320 mV (depending upon the setting of P1) is present on the inverting inputs of the two comparators, IC3 and IC4. The result is that the output of IC3 swings high when the input voltage exceeds 0,96 V, and the output of IC4 does likewise when the input voltage exceeds 9.6 V. The comparator outputs control electronic switches, which are formed by MOSFETs. These are contained in IC1, which is here used in a somewhat unusual configuration; note that the positive supply voltage pin of this IC (pin 14) is left unconnected.

If the circuit of figure 3 is connected between points A and B (figure 2), the position of the decimal point in the universal digital meter can also be controlled automatically. The three outputs of the circuit in figure 3 should be connected directly to R4, R5 and R6 in the meter circuit.

J. Borgman (The Netherlands)

1

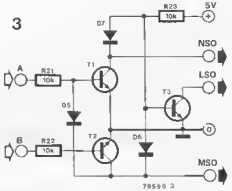


IC2 . . . IC4 = CA 3130
D1 . . . D7 = 1N4148

R2 . . . R11 = Metal oxide 1%

T1 . . . T3 = TUN

3



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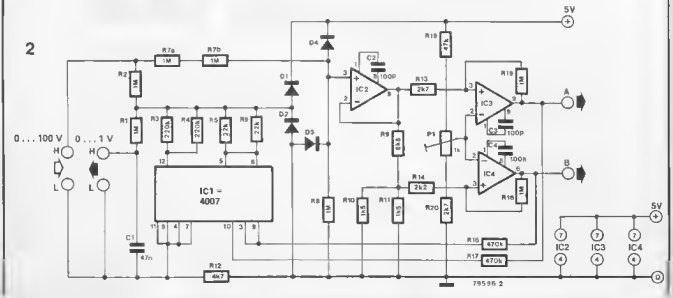


vicious chess buzzer

33

Lightning chess is often played in chess clubs, the idea being that a buzzer is sounded, usually every ten seconds or so, and the player whose turn it is to move must do so during the buzz, which lasts approximately one second. Despite the increased likelihood of a blunder by both players, it remains true that the more experienced, stronger player is still likely to defeat a weaker opponent. In fact the constraint of having to move quickly seems to exaggerate any difference in the strength of two players. The circuit described here offers the novice a new hope by providing an entirely random delay between successive buzzes. Thus there is the chance that the delays between his (strong) opponent's moves may be much shorter than those between his own. Of course the reverse is also true, but that is a risk which has to be taken!

The circuit of the 'vicious chess buzzer' is shown in the accompanying diagram. N3 and N4 form a simple squarewave oscillator with a variable duty cycle. P1, R15 and D11 determine the charge period of timing capacitor C3 (the delay between successive buzzes), whilst P2, R16 and D12 determine the discharge period (the length of the buzz). With S1 as shown in the diagram, a fixed buzz interval of from 1 to 15 seconds can be set by adjusting P1, whilst the length of the buzz can be varied as desired by adjusting P2.

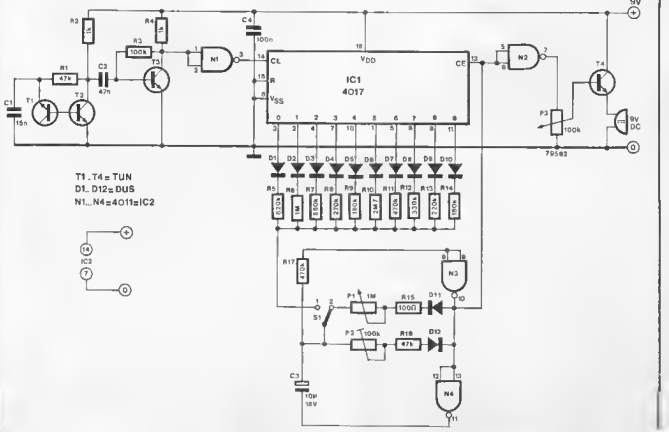
The output of N3 drives the buzzer via N2, P3 and T4. By means of P3 the volume of the buzzer can be adjusted to a suitable level.

The section of circuit described up to this point forms a 'normal' chess buzzer, however if S1 is switched to its alternative position, the delay times are randomised. The time taken to charge C3 then depends upon which Q output of IC1 happens to be high. The random element is provided by a noise generator, built round T1, T2 and T3. T1 forms a reverse-biased base-emitter junction which, in conjunction with C1 and R1, provides a random noise signal. This is amplified by T2 and T3 before being inverted, squared up and fed to the clock input of decade counter IC1. As long as the clock enable input (pin 13) of this IC is low (i.e. when the output of N3 is also low and the buzzer is sounding), the counter cycles through each of its output states. When the buzzer stops, the counter is inhibited and one of the counter outputs is held high. The resulting delay is given by the formula $T = R \times C3$, where R is one of the resistors R5 . . . R14. With the values given in the circuit diagram the maximum delay is 27 seconds, and the minimum delay 1.8 seconds – plenty of scope for the buzzer to be really 'vicious'!

The buzzer can also be used for other games (e.g. backgammon, or scrabble), in which case it may be desirable to alter the values of R5 . . . R14 accordingly.

A small 9 V buzzer was chosen to keep current consumption to a minimum and permit the use of batteries. C3 should be a tantalum type.

B. Leeming (United Kingdom)



34 cartridge life-expectancy counter

This circuit is intended to give clear warning when it is time to replace the stylus in a record-player cartridge. The unit indicates the 'playing time' that has already elapsed, using five LEDs. The first LED lights after the stylus has been in actuel use for 100 hours, and each following LED lights after a further 100 hours. After 500 hours all LEDs are lit, indicating that it is time to replace the stylus. Otherwise, after e further 100 hours the five LEDs start flashing on and off — signaling that it is now high time!

Once the stylus has been replaced, the counters are reset by briefly removing (or replacing) the battery. Power is derived from the mains when the record player is switched on. The battery is only used as a stand-by supply for the counters during 'off hours' — or in the event of a mains failure . . .

In the circuit, S is the mains switch for the record player. When this is closed, the multivibrator (N2, N3) starts to provide clock pulses to the counter chain (IC1 . . . IC3). The final IC in this chain (IC3) is a series-in/parallel-out shift register. The clock frequency and division ratio in IC1 and IC2 are chosen so that IC3 receives one pulse every 100 hours; its (parallel) outputs are used to drive the LEDs. The flashing display at 600 hours is derived from the Q4 output of IC1 (0,2 Hz).

C3, R4 and N4 are included to reset the counter chain when power is first applied — i.e. when the battery is connected. To limit the drain on the battery, it is only used to power the ICs; the LEDs are only powered when the mains supply is on.

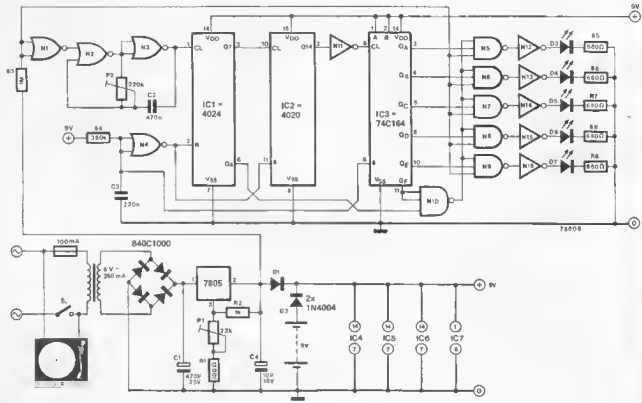
Calibration is fairly easy. The clock frequency is set (by P2) for a period time of 0.17166 s. This can be measured directly if the necessary test equipment is available; alternatively, the Q7 output of IC1 can be monitored with a multimeter: the period time at this point should be 22 seconds.

The output voltage of the stabiliser (7805) is set to 10 V by means of P1.

Editorial note

Provided it is handled with due care, a diamond stylus should last for anything up to 2000 hours. A lower clock frequency could therefore be used, giving a switching time for the LEDs of 200, 300 or even 400 hours. Furthermore, it would seem an improvement to use a nicad cell (9 V/100 mAh) instead of the battery for a stand-by supply. Trickle-cherging can be provided by including a 1 k resistor in parallel with D2.

J.G. Hemmer (France)



N1 . . N4 = IC4 = 4001
N5 . . N7 = IC5 = 4023
N8 . . N10 = IC6 = 4023
N11 . . N16 = IC7 = 4049

SHIFT-LOCK for ASCII keyboard 35

The following SHIFT-LOCK circuit should prove a useful addition to the ASCII keyboard published in Elektor 43 (November '78). The circuit is also suitable for use with most other types of keyboard which are not already provided with this facility.

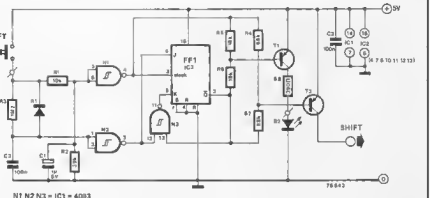
There is no need for an extra key to be mounted on the keyboard, since the original SHIFT key performs both the SHIFT and SHIFT-LOCK functions; the length of time for which the key is depressed determines which function is selected. If the SHIFT key is held down for longer than 0.2 seconds, the shift output will go low (inactive) as soon as the key is released. If, however, the key is only depressed briefly (i.e. for less than 0.2 sec), the shift output is held high (active) until pressed a second time, i.e. the key functions as a SHIFT-LOCK.

The timing for the circuit is provided by the RC constant of R3 and C2. As soon as the voltage across C2 reaches approximately 45% of the supply voltage, N2 will change the input conditions of the JK flip-flop, IC2. Assuming that the $\bar{Q}$ output is initially high, the circuit functions as follows:

Momentarily depressing the SHIFT key has no effect upon the output of N2. The J input of the flip-flop therefore remains high, and the K input low. Shortly after the key is pressed, the output of N1 goes low, taking the SHIFT output (via T2) high. When the SHIFT key is released, a positive going edge triggers the flip-flop, so that, given the state of the J and K inputs, the $\bar{Q}$ output goes low, taking the K input high, and ensuring that the SHIFT output is held high (via T1, T2). The next time the SHIFT key is held down briefly, the flip-flop is reset, i.e. the $\bar{Q}$ output is returned high, taking the SHIFT output low.

If the SHIFT key is originally depressed for longer than 0.2 seconds, the output of N2 goes low and takes the K input high, thereby holding the $\bar{Q}$ output high. The SHIFT output will go low as soon as the key is released. R1, C1 and R2 eliminate the effects of contact bounce, whilst LED D2 provides a visual indication of when the SHIFT-LOCK function is selected.

If the circuit is used in conjunction with the Elektor ASCII keyboard, the track to pin 4 of the AY-5-2376 should be broken and the circuit connected between the SHIFT key and the IC.



T. Frankemolen
(The Netherlands)

2 switches - 2 lamps - 1 wire 36

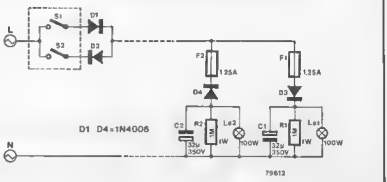
When housewiring, the addition of an extra switch and light to an existing circuit using the same power supply point would not normally cause any problems. However, the situation can arise where it is not possible to 'run' an extra cable between the additional switch and light thereby making it impractical to fit them.

The circuit described here is a simple but effective method of solving this problem by replacing the missing wire with a little ingenuity.

It will be seen from figure 1 that diodes D1 and D2 ensure that switch S1 controls lamp La1, whilst S2 controls lamp La2. The half-wave rectified mains voltage is partially smoothed by capacitors C1 and C2, so that an RMS voltage of approximately 240 V appears across the lamps, which therefore burn at normal intensity. The value of these capacitors is determined by the power rating of the lamps used. The appropriate value can be calculated by using the following equation:

$$C_X = 32 \cdot \frac{P_X}{100}$$

where C_X is the new value of the capacitor (in μF) and P_X the power rating (in W) of the corresponding lamp.



W. Richter **(Germany)**

37 frequency multiplier

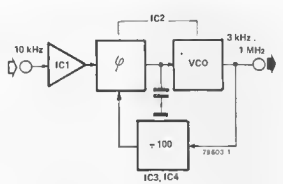
There may be occasions when it is required to measure low frequencies with a high degree of resolution. The circuit presented here is intended as a frequency multiplier for just this purpose which offers a resolution of 0.1 Hz with a fast measuring time.

A block diagram of the frequency multiplier is shown in figure 1. As can be seen, this configuration bears more than e passing resemblance to the (by now) fairly common PLL frequency syntheiser. However, in this instance it is the division ratio which is fixed and not the input (or reference) frequency. The VCO frequency is divided by 100 and then compared with the input frequency in a phase comparator. The resulting phase difference creates a DC signal which is used to correct the VCO frequency. This means that the VCO output frequency will be exactly 100 times that of the input.

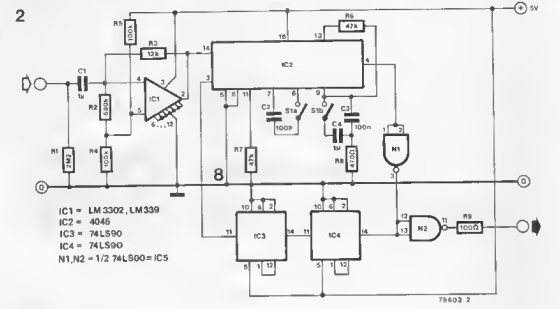
In the circuit diagram of figure 2, the input frequency is first amplified by IC1 before being fed to the phase locked loop, IC2. The VCO output is divided by 100 by the two decade counters IC3 and IC4 whereupon its phase is compared with that of the input signal in the PLL itself. The VCO output frequency is fed to the meter via the inverter formed by N2. Switch S1 is included so that the overall frequency range of 30 Hz ... 10 kHz can be split into two separate ranges, namely 30 Hz . . . 300 Hz and 200 Hz . . . 10 kHz. The input sensitivity is quoted as being around 25 mV, and the output voltage is approximately 4.5 Vp-p. Power supply requirements are 7 - 18 V at around 30 mA.

H. Rol (United Kingdom)

1



2



38 digital frequency synthesiser

A frequency range of 0.1 Hz to 999.9 kHz, a choice of CMOS or TTL output levels, and an accuracy/stability which is limited only by that of the crystal oscillator — these are the main features of the digital frequency synthesiser shown here.

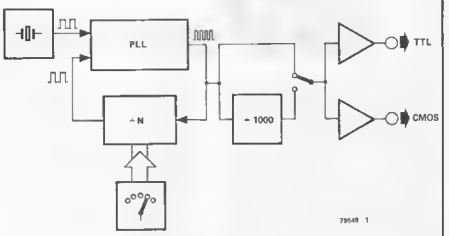
As can be seen from the block diagram in figure 1, the heart of the circuit is formed by a phase locked loop (PLL). In principle such a PLL circuit can be likened to an op-amp connected with feedback, such that the output voltage of the op-amp varies to keep the voltage at both inputs the same; the PLL circuit varies the *frequency* of the output signal, so that the frequency of both

input signals remain the same. If the output frequency is divided by a factor N, and then fed back to one of the PLL inputs, the frequency of the PLL output signal will be exactly N times that of the *other* input signal. Thus all we have to do is ensure that the latter is a stable reference signal, and we have an output whose frequency is equally stable but is N times the reference frequency.

The next step is to provide for the division factor, N, to be made variable, with the result that the frequency of the output signal can also be varied. By including a divide-by-1000 counter, which can be switched in or out of circuit, the frequency range of the output signal can be extended down to as low as 0.1 kHz. Finally, output buffers which amplify the output to both TTL and CMOS levels give the circuit a more 'universal' character.

The complete circuit diagram of the digital frequency synthesiser is shown in figure 2. The reference signal is provided by a 3.2768 MHz crystal which is divided by a factor of 2^{15} (= 32768) by IC5 and IC6, so that a signal whose frequency is exactly 100 Hz is fed to one input of the PLL IC (IC7). The frequency divider for the PLL output is formed by IC8 . . . IC11. The desired division ratio (N), and hence the output frequency, is set up on the decade switches, S3 . . . S6. The output of AND gate N10 provides the other input signal to the PLL, and due to the action of the PLL, the frequency of this signal remains constant at 100 Hz.

1



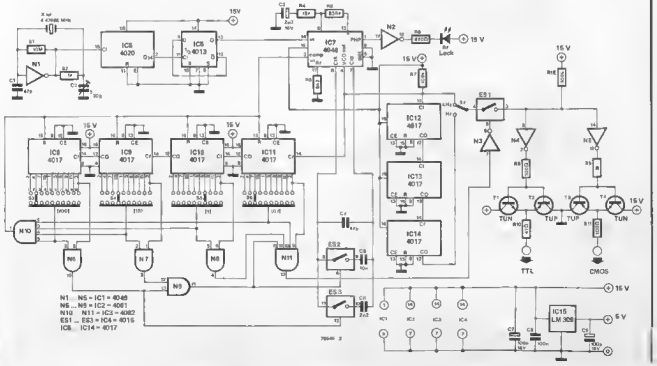
The operation of the phase locked loop is dependent upon the value of the capacitor connected between pins 6 and 7 of the IC. Since the output frequency of the PLL can be varied over a fairly wide range, it is necessary to ensure that the capacitor value can also be varied with frequency. This is done via electronic switches ES2 and ES3, which connect either one or two extra capacitors in parallel with C4. Control signals for these switches are derived, via suitable logic gating, from the decade switches, S3 . . . S6.

The divide-by-1000 counter is formed by decade counters IC12 . . . IC14. Depending upon the position of the range switch S1, the figure set up on S3 . . . S6 will be in either Hz or kHz. The output buffers are formed by means of inverters and a pair of balanced emitter followers. The outputs are short-circuit-proof. An additional electronic switch, ES1, is included to ensure that there is no output signal when the decade switches are set to 000.0. LED D1 lights up when the PLL is locked on, and thus provides a visual indication that the output frequency is correct.

The circuit requires two supply voltages: 15 V unstabilised, and 5 V stabilised. The unstabilised supply can safely be increased slightly. For example, two nine volt batteries connected in series will prove quite suitable.

R. Dürr and D. Hackspiel (Switzerland)

2



39 dwell meter

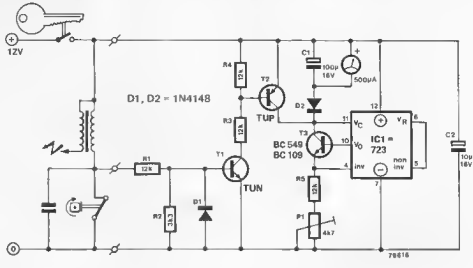
Checking and adjusting the dwell angle of a contact breaker is really no problem – provided you have a good dwell meter. By 'good' we mean that it must be accurate and linear, and work over a large range of ambient temperatures. The circuit described here meets these specifications. It is intended for use in combination with a multimeter (500 μA f.s.d.), although any other 500 μA instrument can also be used, of course. The dwell angle is measured in % (0 . . . 100%). If a reading in degrees is required, the actual reading must be multiplied by 3.6 and divided by the number of cylinders in the engine.

The circuit could hardly be simpler. The most important section is a constant-current source, consisting of T3 and a voltage-regulator IC (IC1). The extremely stable (and temperature-independent) reference voltage provided by the IC at pin 6 is connected to the non-inverting input of a differential amplifier inside the chip; the inverting input is connected to the emitter of T3. The IC will now adjust its output voltage (V_O) so that the emitter of T3 is maintained equal to the reference voltage. The result will be obvious: a constant voltage, independent of temperature, across a fixed resistance (R5 + P1) must produce an equally constant current. Since the base current of T3 is negligible, the collector current is equal to the (highly constant) emitter current. So far, so good.

The rest of the circuit either allows this constant current to pass through the meter, or else it doesn't . . . When the contact breaker is open T1 and T2 will conduct, shorting out the meter circuit. As soon as the points close, T1 and T2 will turn off. The constant current determined by T3 now flows through the meter, charging C1 at the same time. As the points open and close at rapid intervals, an average voltage is developed across C1 and this meter. This voltage is proportional to the 'duty-cycle' of the breaker points: the longer the points remain closed (the larger the dwell angle, in other words), the larger the voltage across C1 will be – giving a correspondingly higher reading on the meter.

The calibration procedure is like the circuit: simplicity itself. After connecting the supply and shorting the input (R1 to supply common), P1 is adjusted for full scale deflection of the meter (100%). After all, a shorted input corresponds to a dwell angle of 100%.

J. Becela (Germany)



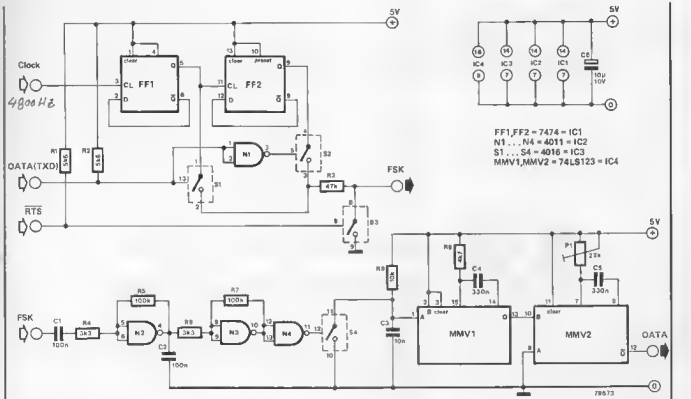
40 FSK modem

The most notable feature of this circuit for an FSK modulator/demodulator is its extreme simplicity:

– it requires only one supply voltage
– uses only 4 common ICs
– is simple to set up

The circuit conforms to Kansas City Standard (CUTS) format, i.e. logic 0 = 1200 Hz, logic 1 = 2400 Hz, and the transmission rate is 300 Baud.

The modulator circuit is quite staightforward. The clock signal is derived from the frequency of the UART, which is 16 times the baud rate (i.e. 4800 Hz). After the clock signal has been divided down by FF1 and FF2, 2400 Hz and 1200 Hz signals are available at the inputs of S1 and S2. Depending upon the logic level of the data input signal, one of these two switches is closed and a signal of the appropriate frequency is present at the modulator output. At the input of the demodulator circuit, N2, N3 and N4 form an amplifier/limiter. The actual demodulation is performed by the two re-triggerable monostable multivibrators, MMV 1 and MMV 2. The pulse duration of MMV 1 is roughly 420 μs, whilst that of MMV 2 is approximately 850 μs (depending upon the position of P1). With an input frequency of 2400 Hz, MMV 1



is continuously retriggered, so that its Q output is held high. No trigger pulses are fed to MMV 2, with the result that the $\overline{Q}$ (data) output remains high. However, with an input frequency of 1200 Hz, MMV 1 will not be retriggered before the Q output goes low, so that MMV 2 is triggered and the data output also goes low. By adjusting P1 to keep the pulse duration of MMV 2 as short as possible, the delay between rising and falling edges of the data signal can also be kept short.

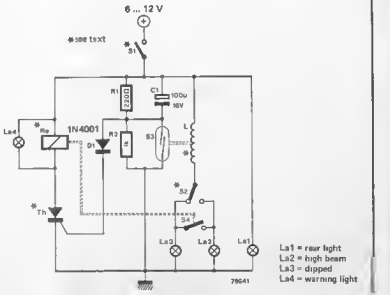
Users of the Elekterminal can take the clock signal for the modulator from either pin 17 or pin 40 of the UART. The Baud rate switch on the Elekterminal should be set to the 300 Baud position. The RTS input should only be used in conjunction with UARTs provided with such an output.

H. Stettmaier (Germany)

motorcycle emergency lighting 41

The following simple circuit should prove a useful safety aid to motorcyclists. In contrast to car drivers, motorcyclists generally only have a single headlight on their vehicle. Thus if it should fail whilst driving at night the motorcyclist is suddenly plunged into darkness and is effectively 'blind', a dangerous state of affairs, to say the least. Normally the motorcyclist would have to fumble for the dipswitch and change over from dipped to full-beam or vice-versa, depending upon which bulb or filament had failed. The circuit described here ensures the safety of the motorcyclist by performing the task automatically in the event of either bulb (filament) failing.

The headlight switch of the motorcycle is represented by S1 in the circuit diagram. Between this switch



and the dipswitch, S2, is a coil (L), consisting of 10 to 15 turns of connecting wire wound round a reed switch (S3). As soon as the headlight is switched on (whether dipped or full-beam), a current will flow through the coil, generating a magnetic field which closes the reed switch. Diode D1 is then connected via S3 to ground, with the result that the thyristor is turned off. Should the lamp or filament which has been selected by S2 now fail, the current through the coil, L, will fall, thereby opening the reed switch. Capacitor C1 will discharge via R1, and the anode of D1 will be at a positive potential, thus turning on the thyristor. The change in potential is deliberately slow, so as to ensure that should switch S3 open accidentally (as a result, e.g. of vibration, or when switching between the two positions of S2), it will have no effect upon the circuit. The thyristor pulls in the relay, Re, thereby connecting La2 and La3 in parallel. Since it is unlikely that both the dipped and full-beam bulbs should fail simultaneously, at least one lamp will be on, regardless of the position of S2. In addition, the warning lamp, La4, lights to indicate that a fault has occurred.

The circuit is suitable for both 6 V and 12 V supply voltages, and almost any type of thyristor can be used, since it is only required to switch the relay and warning lamp.

E. Wünsch (Germany)

42 automatic voltage prescaler

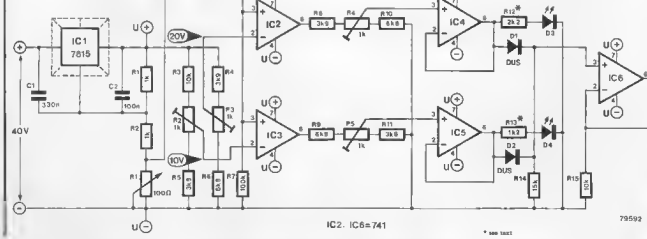
If one wants to measure a voltage which is greater than the range (full-scale deflection) of a meter, there are two things which can be done. On the one hand, the input voltage can be reduced to an acceptable value by employing a voltage divider. This is tantamount to 'compressing' the entire range of voltages to be measured. Alternatively we can arrange for the meter scale to cover only a certain portion of the total range of input voltages, depending upon the amplitude of the input signal. For example, with a voltage of 26 V, a 10 V meter will 'look at' the 20 V - 30 V range, and a reading of 6 V will be obtained. The circuit described here performs the function of 'prescaling' a 10 V meter automatically, and can be used to measure input voltages between 0 and 30 V.

With the aid of IC2 and IC3, the input voltage is compared with a reference voltage of 10 and 20 V respectively. Depending upon which comparator outputs go high, further reference voltages are fed via buffers IC4 and IC5 to diodes D1 and D2. The result is that a voltage which is equal to the greater of the two reference voltages minus the forward voltage drop of the diode, appears on the non-inverting input of IC6. The other diode remains reverse-biased. Since IC6 is connected as a voltage follower, the meter will thus show the difference between the original input voltage and the offset (reference) voltage of either 0, 10 or 20 V. LEDs D3 and D4 provide a visual indication of which scale (0 . . . 10 V, 10 . . . 20 V or 20 . . . 30 V) the meter is switched to. The brightness of the LEDs can be varied as desired by altering the values of R12 and R13.

Any type of meter with a 10 V full-scale deflection (e.g. a moving coil type provided with a suitable series resistor) can be used. However one should bear in mind that the current flowing through the meter forms a load to the remainder of the circuit. Thus the higher the impedance of the meter the better.

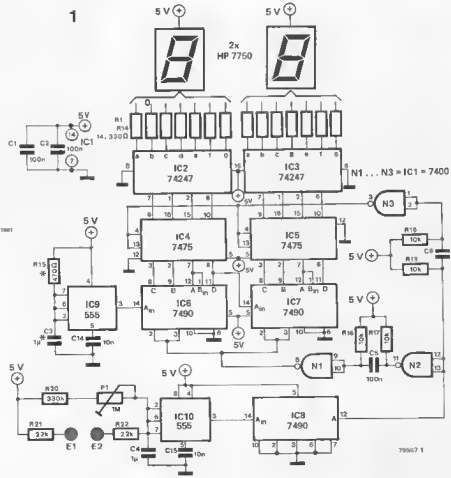
P1 is included to compensate for the fact that the op-amps cannot swing fully negative. This potentiometer is best adjusted by shorting the input of the circuit and adjusting the meter for zero deflection. To adjust the remaining potentiometers a 10 and 20 V reference voltage is required. The procedure is as follows: with an input voltage of 10 V, P2 is adjusted such that D4 is just on the point of lighting up. P5 is adjusted such that a zero deflection reading is obtained on the meter when D4 lights up. With a 20 V input, P3 and P4 are then adjusted in a similar fashion.

P. Sieben and J. P. Stevens (Belgium)



bio-control 43

1



The growing awareness of the contributory role which stress plays in causing illness has led to increased interest in various forms of 'autogenic' training as a means of promoting relaxation. In particular, different types of 'bio-feedback' circuits have become popular, the idea being that certain physiological functions (heartbeat, body temperature, brain activity) can be monitored and brought under the conscious control of the subject.

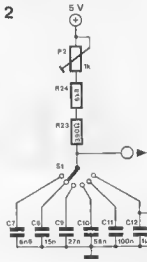
The circuit descibed here operates on the principle of monitoring skin resistance as a measure of how tense the subject is. The same approach is used in so-called lie detectors, however in that case it is the skilled interpretation of the subject's responses to a variety of both innocuous and pointed questions which is important.

The description of the circuit is as follows: variations in skin resistance (between electrodes E1 and E2) vary the frequency of the oscillator built round a 555 timer (IC10). The output of the oscillator is fed to a 7490 divider (IC8), which in turn controls the reset inputs of the counter formed by IC6 and IC7. The result is that the period between successive pulses from IC10 determines the number of clock pulses fed to this counter from a second oscillator (IC9). The outputs of the counter are decoded and displayed on a pair of 7-segment displays, thereby providing a numerical indication of the subject's relative tenseness.

The frequency of the second oscillator, which is also formed by a 555 timer, is determined by C3 and R15. By incorporating the circuit shown in figure 2, several different clock rates can be chosen, thereby allowing the sensitivity of the circuit to be varied to suit different circumstances. Initially P1 should be adjusted to a suitably 'neutral' position.

A pair of metal rings, which are slipped onto different fingers of the subject, will prove suitable sensors. The rings can be connected to points E1 and E2 by suitable lengths of wire. The current consumption of the circuit is roughly 400 mA max. To eliminate any danger of electric shock, care should be taken to ensure that the supply voltage is quite safe, ideally a battery should be used.

2



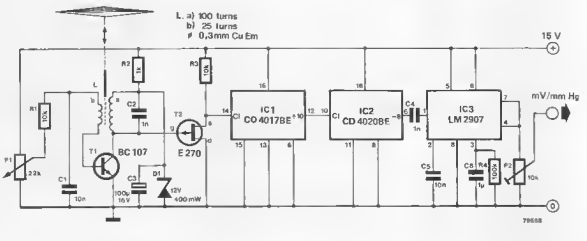
J. Mulke (Germany)

44 barometer

Barometic pressure is one of those things that is difficult to measure electronically. A sufficiently sensitive pressure sensor is not easy to obtain — unless, as in this design, you add some kind of electronic pickup to a conventional mechanical barometer.
The ferrite core of a coil is attached to the 'drum' in the barometer. As the barometric pressure changes, the core moves to and fro in the coil. Since the latter is part of an LC oscillator circuit, the ouput frequency will now depend on barometric pressure. The output from the oscillator is buffered by T2 and fed to a divide-by-ten counter (IC1), followed by a further divide-by-eight counter (IC2). The frequency has now been reduced to the point where it can be handled by a frequency-to-voltage converter, type LM 2907 (IC3). The output voltage from this IC will therefore vary with barometric pressure.
For obvious reasons, this system will only work with reasonable linearity over a limited range. Fortunately, barometric pressure doesn't vary much either (± 5%), so that a suitable choice of pressure sensor, core and coil will provide a sufficiently accurate 'barometer'.
The only real adjustment point in the circuit is P1. Initially, this is adjusted until the oscillator starts — a voltage will then appear at the output. If the oscillator frequency range is outside that of the frequency-to-voltage converter, this can sometimes be corrected by re-adjusting P1. If the frequency is too far off, however, the value of C2 will have to be changed. The preset at the output (P2) is used to adjust the output level as required. A digital or analogue millivoltmeter can be connected at this point.

Editorial note:
At first sight, there doesn't seem to be much point in stripping an existing barometer in order to connect an electrical pointer instrument instead of the mechanical pointer. However, having an electrical voltage available that is proportional to barometric pressure opens a whole range of possibilities. Just to name one: What about designing a home weather-forecasting computer?

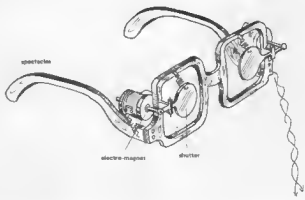
Y. Nijssen (France)



45 tv programme multiplexer

Mr Fröse has submitted an idea which could well revolutionise the viewing habits of the nation. Like many of us, he apparently has regular battles with the rest of his family over the choice of TV programmes — and has decided to do something to restore harmony in the living room. After many long winter evenings spent in his attic study, pondering on the peculiar taste in programmes of others, he has come up with the following radical solution. Although he is not yet ready to divulge all the details of his

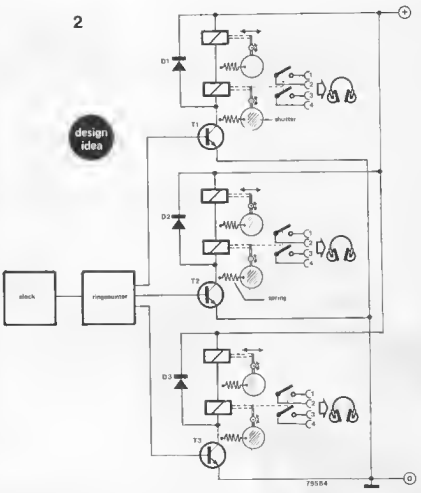
1



invention, the general principle is now free for publication.
The main point is that the TV set is not switched to just one of the channels available: all channels are selected simultaneously! To be more precise, the channels are scanned and each is displayed very briefly on the screen. In the interests of preserving the viewers' sanity, each is provided with a pair of special spectacles. These contain shutters, which are operated by electromagnets. In each pair of spectacles the shutters are only opened at the moment that the corresponding TV programme is being displayed on the screen. The basic multiplex circuit is shown in figure 2. Thus the viewer with spectacles '1' sees the first programme only; viewer '2' watches the second programme, and so on. Each pair of spectacles is accompanied by a set of headphones, which provide the sound output for the corresponding channel. In this way, several people can watch the same TV set – each following their own programme. All in all, a stroke of genius! The author is presently working on the possibility of adapting the circuit for FM radio transmissions in both mono and stereo.

W. Fröse (Germany)

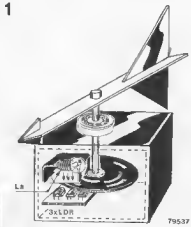
2



electronic weathercock 46

The disadvantage of most wind direction meters is the need for complicated mechanical drive systems which are necessarily prone to wear. The unit described here is intended to offer a solution to this problem. A disc which contains a number of slots is attached to the spindle of the weather vane. A light source is mounted above the disc, and a row of 3 light dependent resistors (LDRs) is situated below the disc – as shown in figure 1. Which LDRs are illuminated will depend upon the position of the disc, and therefore upon the diraction of the wind. If tha slots in the disc are correctly positioned (see figure 2), the information from the LDRs can be coded into BCD format, such that each of the eight main compass points will correspond to a particular BCD code. By means of a BCD-decimal converter, the resultant information, and hence

1



2

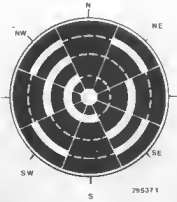
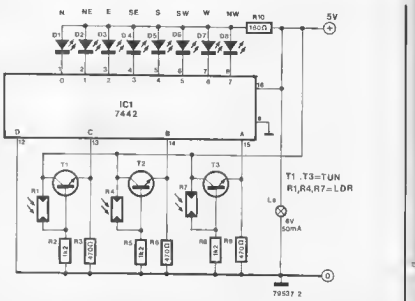


Table 1.

A	B	C	D	wind direction	LED
0	0	0	0	north	D1
1	0	0	0	north-east	D2
0	1	0	0	east	D3
1	1	0	0	south-east	D4
0	0	1	0	south	D5
1	0	1	0	south-west	D6
0	1	1	0	west	D7
1	1	1	0	north-west	D8

the direction of the wind, can then be displayed on a circle of LEDs. The 'electronics' of the unit are shown in the circuit diagram of figure 3. If no light falls upon an LDR, the associated transistor is turned off and the input of IC1 is pulled down to 0 V via the 470 Ω resistor. As soon as sufficient light falls on an LDR to turn the transistor on, however, the corresponding input of IC1 is taken high. Thus the state of the three LDRs is translated into a BCD code applied to the inputs of the 7442. Depending upon the combination of logic '0' s and '1' s at the four inputs, the 7442 takes one of its outputs low, with the result that the corresponding LED lights. The BCD code for each of the eight compass points is listed in table 1.

3

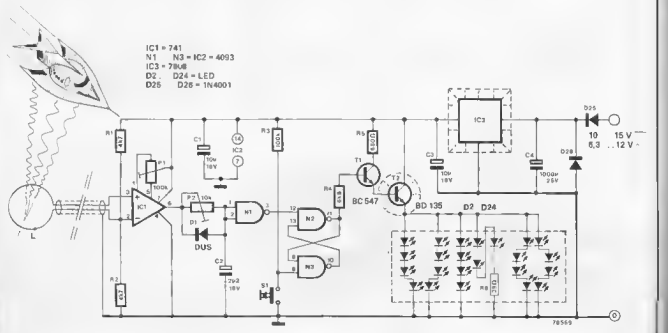


Editorial note:
If the disc should come to rest exactly between two compass points, e.g. between south and south-east, then the effect of stray light may cause the wrong code to be presented to IC1, and the NW LED will light up. Therefore, it would be better to use the 'Gray code', i.e. 000 = N; 100 = NE; 110 = E; 010 = SE; 011 = S; 111 = SW; 101 = W; 001 = NW.

D. Maurer (The Netherlands)

47 UFO detector

This somewhat 'different' circuit was sent in by one of our subscribers in the more distant sector of Vega. It was described as being an Earth type UFO detector and may find favour with those of our readers who are constantly plagued by UFO's.
The operation of the detector is based on the fact that all UFO's, regardless of type, cause sudden changes in the earth's magnetic field (or so our correspondent tells us, and he should know). These variations in magnetic intensity induce a small voltage in the search coil, L. This voltage is amplified by IC1 and used to trigger the flip-flop formed by N2 and N3, which then turns on the display formed by the array of LEDs. The brightness of the display can be varied by altering the value of R5. This may prove necessary in the event of transistor T2 having too great a gain. The original circuit used a radium



krokopaard as a search element but as these are not yet readily available on Earth (even in Tottenham Court Road) the circuit was modified for use with a coil. The diameter of the coil, which consists of roughly 5000 turns of 0.2 or 0.25 mm enamelled copper wire, is approximately 23 cm. This means that something over 3.6 km of wire is required in all. We are unable to provide the final test instructions since not too many of our readers have bicycles capable of 14,000 miles per hour. However, there is a simpler method.

A magnet is used to set up the circuit. Potentiometer P1 is first set to the mid-position and P2 adjusted to roughly two thirds of its maximum value. The magnet is then moved around near the search coil, whereupon the display should light up. The sensitivity of the circuit is adjusted by means of P1. So as to be able to detect even the smallest of UFO's, the circuit will normally be adjusted for maximum sensitivity. The optimal setting for P2 will depend upon the speed at which the UFO's are moving and should therefore be determined experimentally.

According to Mr. (?) Xantor, if one builds and uses the circuit described here it should be possible to chart the flight paths of all the UFO's which fly over one's house, and the fact that Mr Xantor's compatriots will know they are being observed could well encourage them to instigate a 'close encounter of the third kind'!

Xantor (Vega IX*)

*Earthly representative M. Muhr (Germany)

current dumping amplifier 48

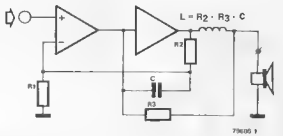
The basic principle of a current dumping amplifier has been described previously in Elektor (see Elektors 8 and 21). To recap briefly, the circuit exploits the fact that, due to the effect of the four passive components, R2, R3, L and C shown in figure 1, the non-linear characteristic of the output stage becomes unimportant. Thus it is possible to use a Class-B output stage (i.e. the output transistors are biased to their cut-off points so that there is no quiescent output current) with all the advantages and none of the disadvantages (crossover distortion) of that configuration.

The circuit shown in figure 2 functions on the above described current dumping principle. According to the designer it is capable of delivering 100 W into 4 Ω with a claimed harmonic distortion of 0.006% at 1 kHz and 60 W. If one possesses the equipment to make accurate distortion measurements, C3 can be replaced by a 22 pF variable capacitor, and the latter adjusted for minimum distortion.

The circuit also has a useful extra facility in the form of a dummy load (R9).

The output stage is driven (via driver transistors T2 and T5) by transistors T1 and T4, which are connected in series with the positive and negative supply lines respectively of IC1. In this way the slew rate of the 741 is improved. If, however, a faster op-amp is desired (e.g. the LF 357), then the value of R4 and R7 should be altered to provide the correct quiescent current for the IC, so that the output stage draws no current.

1



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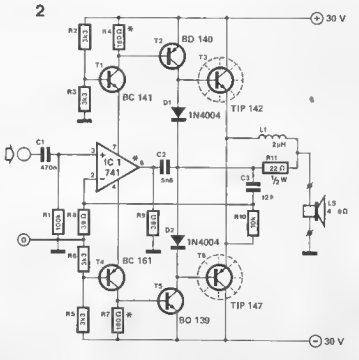
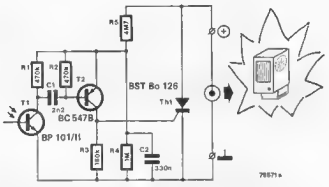


G. Schmidt (Germany)

49 slave flash



With the aid of this simple circuit a normal flash unit can be converted into a 'slave' flash. In this way it is possible to take photographs using a number of separate flash units, without getting tangled up in a confusion of cables.

The sleve flash does not require a separate supply voltage, but rather draws its current from the contact used to trigger the master flash. There is normally some 150 to 200 V on this contact, and this is divided down by R4 and R5 to provide a suitable low supply voltage. C2 is an AC-decoupling/reservoir capacitor. Since the current consumption of the circuit is not much more than several μA, the extra drain on the power supply bettery will be negligible.

When the light generated by another flash unit falls upon the phototransistor, a voltage pulse is generated across R1. This is fed via C1 to T2, where it is amplified to a level suitable to trigger the thyristor, and with it, the flash.

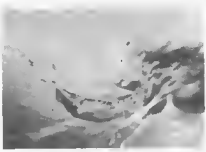
The component values have been calculated to ensure that the flash will not be spuriously triggered by, e.g. incandescent lamps, but will react only to other flash units. The circuit is sufficiently sensitive that the mester flash need not be focused on the phototransistor; it will react to the reflected light. It may be necessary, however, to shield the phototransistor from other sources of intense light.

Any 8 A/400 V thyristor should prove suitable, although it may prove necessary to increase the value of C2 slightly (since this capacitor supplies the greatest portion of the gate current). The socket for the flash unit cable can best be made using a flash extension cable.

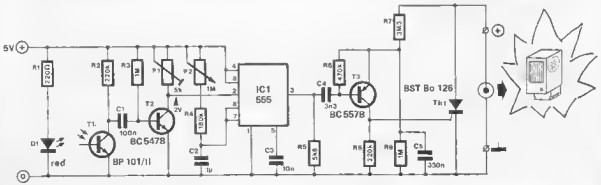
F. Schäffler (Germany)

50 photo-flash delay

One of the more specialised areas of photography is the use of ultra-short exposure times to capture events occuring at high speed. Everyone will have seen the results of this technique at one time or another: a light bulb in the process of disintegrating under the impact of a hammer, or, as in the picture shown here, a splash of water. Photographs of this type can be taken fairly simply by employing an 'open-lens' approach, i.e. the photo is taken in a darkened room and the lens of the camere is opened before the subject is illuminated. The lighting is provided by a high-speed (electronic) flash unit capable of providing extremely short exposure times.



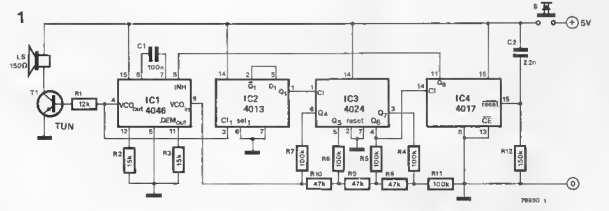
One problem with this method is determining the exect moment at which the flesh gun should be triggered. Beceuse of the extremely short time intervals involved, this can really only be done electronicelly. In the case of the picture shown here, the drop of water was sensed by a photoelectric cell, which, with the aid of tha following circuit, provided a predetermined delay before



doorbell drone 51

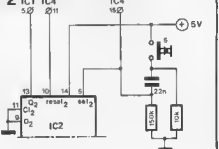
triggering the flash.
An LED (D1) and phototransistor T1 are used to form the light gate. When the light from the LED is interrupted, there is a sharp rise in voltage across R2. This is fed via T2 to the trigger input of the 555 timer (IC1). When the delay period provided by the timer has elapsed, a negative-going pulse appears at the output of this IC (i.e. pin 3), with the result that T3 and the thyristor are turned on, and the flesh is triggered.
Any 0.8 A/400 V thyristor will prove suitable, however it may be necessary to increase the value of $\frac{C5}{}$ slightly. The *DC* bias voltage on the collector of T2 should be adjusted to 2 V by means of P1.
With the aid of P2, the delay provided by the circuit can be varied between approximately 0.25 and 1.3 s. By altering several component values the range of possible delays can also be varied. The delay time is given by 1.1 x R x C2, where R is the series connection of P2 end R4. The minimum permissible value for R2 is 1 k. As one might expect, the light gate is the section of the circuit which will present the most difficulty when it comes to construction. Whatever arrangement is chosen will depend largely on individual circumstances, however the sensitivity of the circuit is greatest when the LED and phototrensistor are mounted as close together as possible. Cere should be taken to ensure that light from the LED cannot reach the lens of the camera.

F. Schäffler **(Germany)**



There seems to be no end to the variety of different sounding doorbells which people are prepared to design. Everything from the Hallelujah Chorus to the chimes of Big Ben have been simuleted for the entertainment of visiting door-to-door salesmen. However, the imaginetive resources of our readers would eppeer to be inexheustible. The circuit presented here produces a sound which is somewhet akin so that of bagpipes, and while not exactly signalling the deeth knell of original bagpipes, should prove popular north of the border.
The circuit is also intended to foil ill-mannered visitors who insist on pressing the doorbell for an annoying long time, since the bell automatically cuts out efter approximately two seconds.
As can be seen from the circuit diegram in figure 1, very little in the way of components is required to build this 'exclusive' doorbell. A 4046 phese locked loop IC (IC1) is used as a voltage controlled oscillator with a nominal frequency of around 800 Hz determined by the values of R3 and C1. The actual frequency of the oscillator is controlled by feeding the output signal to one half of a dual flip-flop (IC2) which is connected as a divide-by-two counter, and then to a binary ripple counter. The ledder network of resistors R4 ... R11 provides a staircese voltege, which is fed back to the control voltege input (pin 9) of IC1, thereby producing the 'bagpipe' effect. At the end of the count cycle IC4 takes the inhibit input of IC1 high, thus ensuring that the 'bagpipes' do not continue to sound if the bellpush is held down. R12 and *C2* automatically reset IC4 the next time the bellpush is depressed.

Editorial Note:
Although the originel circuit es shown in figure 1 will prove en effective remedy egainst over enthusiestic bell-pushers, unfortunately it does not teke into account whet will heppen if the pushbutton switch (S) is only depressed for e brief moment. Since releasing the switch interrupts the supply voltege to the circuit, the bagpipes will be cut off in their prime! To forestall a flood of letters from incensed Scotsmen we include the following possible modi-



fications. As CMOS ICs drew very little current they can be provided with e continuous supply voltage. By using the other flip-flop in IC2, the circuit can be modified to ensure that the entire 'melody' will be heard even if the bellpush is only depressed momentarily.
The circuit of figure 1 should be eltered es follows:
– switch S is repleced by e link
– C2 and R12 ere omitted
– the connection between pin 11 of IC4 and pin 5 of IC1 is broken
The circuit should then be connected es shown in figure 2.

S. Halom **(Israel)**

52 opto-transmitter for speech

Transmitting speech by modulating a beam of light isn't new. Usually, infra-red is used – as in some 'wireless' headphone systems. However, it is also possible to use a normal torch bulb. The only point to nota is that the filament must ba run at a fairly high temperature, as otherwise the response will be too slow. For this reason, the bulb must be run at almost full brightness, with a very low modulation depth – about 1%. On the other hand, this has the advantage that the high light output carries over greater distances – certainly if a so-called halogen lamp is used, as in this design.

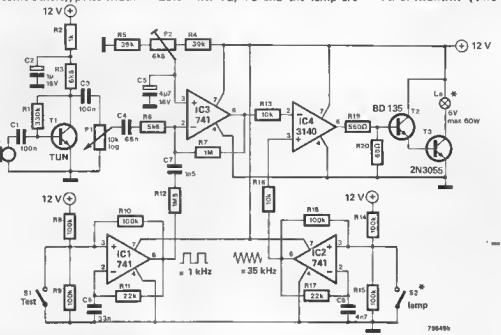
Using amplitude modulation would have the advantage that it makes for a simple receiver design. It would also have a few major disadvantages, particularly the fact that a suitable output stage for the transmitter (capable of driving a 60 watt lamp) would be rather expensive. For this reason (and some others), pulse-width modulation was chosen.

The input signal from the microphone is amplified by T1 and passed via the 'modulation depth control' (P1) to a further amplifier stage, IC3. At this point, a DC offset is added to the signal. This offset is set by P2 to obtain the correct duty-cycle of the final output signal – more on this later.

The pulse-width modulated signal is obtainad by feeding the (audio + DC) output of IC3 and a 35 kHz triangular wave-form to the two inputs of a comparator (IC4). The 35 kHz signal is produced by IC2. This opemp is used in what would normally be a multivibrator circuit (producing a square-wave), but owing to its limited slew rate the output is actually a triangular wave. The output of the comparator, IC4, is a square-wave with a duty-cycle that varies with the speech signal. The average duty-cycle is set by P2 at 25% – i.e. T2, T3 and the lamp are on for 25% of the time. The lamp can be switched off by closing S2. A 12 V car bettery can be used to powar the circuit. It should be noted, however, that a 6 V lamp must be used in that case (with any power rating up to 60 W). Why a 6 V lamp on a 12 V supply? Surely that'll give four times the nominal power dissipation in the lamp? Sura anough, it will – for a quarter of the tima, since a duty-cycle of 25% is used: the lamp is only on for a quarter of the time. And four times one quarter is one.

One part of the circuit remains to be discussed. IC1 is used as a 1 kHz multivibrator. As long as S1 is open, this signal is used to modulate the output. A useful feature when 'lining up' the transmitter and receiver.

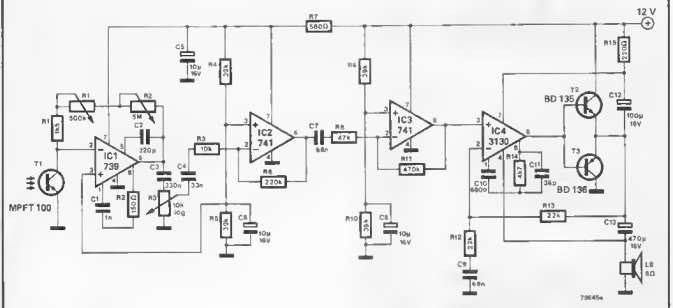
A. J. Mellink (The Netherlands)



53 opto-receiver for speech

This circuit is intended for use in conjunction with the 'opto-transmitter'. The modulated light beam is detected by a photo-transistor, T1; the output from this transistor is amplified by IC1. The overall gain of this stage can be adjusted by P1 and P2 (fine and coarse adjustment, respectively). The optimum adjustment depends on the ambient lighting; it can be found (once the transmitter and receiver are correctly aligned) by 'tuning in' the 1 kHz test tone from the transmitter. After the volume control, P3, tha signal is amplified by IC2 and IC3. The output stage is derived from an earlier Elektor circuit.

If the transmitter and receiver are to be used in a reliable communication system, some attention must ba



paid to the mechanical and optical side of the units. Some kind of reflector-and-lens system will be required both at the transmitter and at the receiver. In practice, old car headlamps have proved quite satisfactory. Both units must be mounted on a sturdy tripod or some similar adjustable base. The author claims that he has succeeded in obtaining reliable communication at distances of well over a mile – after dark, that is.

If two-way communication is required, the temptation to run a transmitter and a receiver off the same supply should be resisted. It won't work, unless the transmitter is switched off before the receiver is switched on.

A. J. Mellink (The Netherlands)

calculator as chess clock 54

With only one or two minor modifications, it is possible to adapt a calculator to increment or decrement two separate numbers and display the results simultaneously.

If we assume a calculator has an 8-digit display, two 4-digit numbers can be displayed thus:

4 3 2 1	4 3 2 1
number	number
A	B

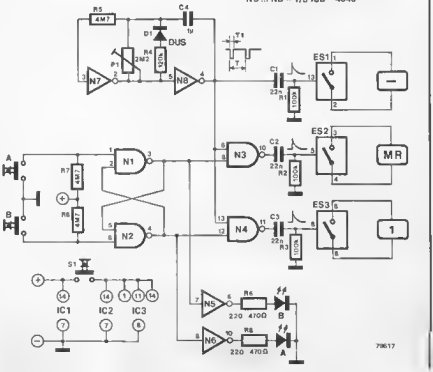
It is a simple matter to subtract (or add) '1' to either of these numbers. In the case of number 8, a straightforward subtraction is all that is required, whilst in the case of number A, the correct result can be obtained by subtracting 10000 from the 'total' number on the display. Thus:

43214321 – 10000 = 43204321

Number B remains unaltered during this operation.

With the aid of the circuit described here, this method can be used to allow the calculator to function as a chess clock, i.e. to display the amount of time each player currently has to complete the remainder of his moves. The circuit itself is

ES1 ... ES3 = 3/4 IC1 = 4016,4066
N1 ... N4 = IC2 = 4011
N5 ... N8 = 1/3 IC3 = 4049



straightforward. As long as a player is to move, the number of seconds he has left is continuously decremented by a clock generator. The only constraints on the type of calculator used is that it must have an 8-digit display and memory recall (MR) key (i.e. the contents of the memory can be recalled using only one key-stroke).

The first step is to store the number 10000 in the calculator's memory, and then to enter the number of seconds each player is to be allowed as a time limit. For example, if both players are to have 2 hours, the number 72007200 should be entered. The clock oscillator is naturally adjusted (by means of P1) to produce a clock pulse every 1 second. Next the 'subtract' key is depressed and the clock oscillator is started by pressing S1. If, for example player A is to move, each negative-going edge of a clock pulse will transfer the contents of the memory to the display, whereupon, approximately 0.1 seconds later, the positive-going edge causes the actual subtraction to be performed. When player A has moved, he presses his 'clock' button, thereby triggering the flip-flop formed by N1, N2. Each clock pulse will then cause a '1' to be subtracted from the display. The pulse duration (T1) of the oscillator must be short, since the display is interrupted during this period, however it must also be long enough to cover the time between two calculator instructions plus the time taken for C2 (C3) to discharge to a sufficiently low voltage. The time constants R1 • C1, R2 • C2 and R3 • C3 should be sufficiently long to ensure that a calculator instruction can be recognised as such. Two LEDs provide a visual indication of whose move it is.

With a suitable clock frequency the duration of the game can be displayed directly in minutes.

N. Vischer (Germany)

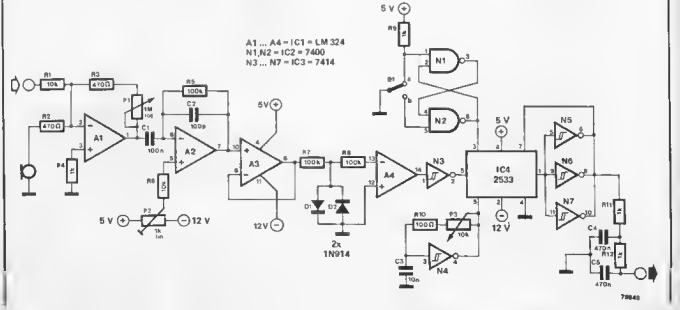
55 sound processor

Starting with, for example, a music signal, or indeed any other type of sound, the following circuit can be used to generate a variety of interesting tonal effects. The input waveform is sampled, and a small portion of the signal is stored in a memory. The signal is cycled repetitively through the memory before being read out again. In this way a new periodic signal which is obviously derived from, but completely different to, the original input signal is obtained.

A digital register is used to store the sampled portion of input signal. This means that analogue to digital conversion is necessary. The conversion process adopted here is a simple version of the delta modulator used in the digital reverberation unit published in Elektor 37. The input signal is first differentiated by A2, and then clipped by the two reverse-parallel connected diodes, D1 and D2. The signal is amplified to a suitable input level for the shift register by means of A4 and N3.

The shift register (IC4) has two inputs: pin 5 and pin 7. Which of the two inputs is used at any given moment is determined by the logic level at pin 3 of the IC, and thus by the position of switch S1. With the switch in position a) (read-in) pin 5 of the IC is the input, whilst with the switch in position b) (read-out) pin 7 is the input. In the latter case the input signal consists of an inverted version of the output signal of the shift register, so that the contents of the shift register are cycled round and round, generating a new, periodic signal at the output. This digital signal is reconverted into its analogue counterpart by an RC integrator network. The clock signal for the shift register is derived from the oscillator built round N4. The clock frequency and hence both the length of the input signal sample and the repetition rate can be varied manually by means of P3. Different types of effect can be obtained by varying the clock frequency during the read-in and read-out cycles.

A. Visser (United Kingdom)



digital contrast meter 56

When enlarging photographs, two factors are of prime importance, the required exposure time, which is determined by the density of the negative, and the contrast of the negative. The latter determines which grade of paper should be used in order to obtain a print with good overall tonal contrast. The contrast of the negative is basically the difference between the lightest and darkest portions of the exposed film. If we take the second log of this difference, we obtain the contrast ratio of the negative. Thus, for example, if the lightest part of the negative lets through 8 times as much light as the darkest part, the contrast ratio of the negative will be 3 ($2^3 = 8$). The circuit employs two light dependent resistors as sensors, and displays the contrast of the negative directly on a seven-segment display. The operation of the circuit is illustrated in the block diagram of figure 1. The amount of light falling upon the LDRs determines the frequency of the squarewave generators to which they are connected. The output of both oscillators are fed to a divide-by-sixteen counter. The pulses for the topmost counter (for the lightest portion of the negative) are counted for a period which is determined by the frequency of the signal from the lower counter. The result is that the value stored in the subsequent binary counter represents the ratio of the two clock generator frequencies, and hence the ratio of the lightest and darkest portions of the negative. The contents of the 'ratio' counter, are then fed to the $\log_2$ converter, the output of which is decoded and displayed. A measurement cycle is initiated by closing the start switch, which sets the flip-flop and resets the

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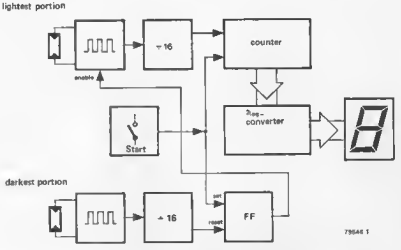

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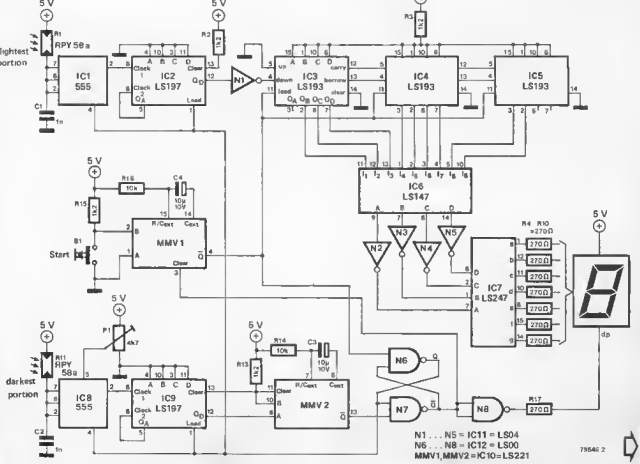


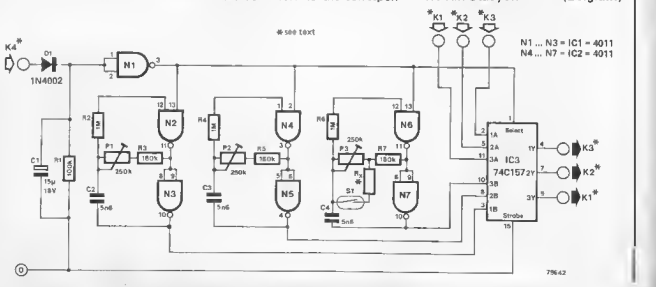
counter.
The complete circuit diagram of the contrast meter is shown in figure 2. With the exception of the two clock oscillators, in which 555 timers are used, the circuit is low power Schottky TTL. IC2 and IC9 are the divide-by-16 counters, whilst the binary 'ratio' counter consists of IC3, IC4 and IC5. This counter uses negative logic, i.e. it begins with all outputs high, and then counts down. Thus at the start of each measurement cycle, a 'load' pulse, and not as one might expect, a 'reset' pulse, is applied to the counter. The paralleled data inputs of the counter are all held high, and the pulses to be counted are fed to the 'down' input.
The reason for adopting this arrangement is the $\log_2$ converter, which also uses negative logic. This converter is formed by IC6, a decimal-8CD prlority encoder. This IC recognises the highest order bit in the input signal which is active, i.e. logic 0, and outputs the 8CD equivalent of that bit's 'weight'. For example, assume the counter holds the binary code for the number 8 (base 10). All bits will be logic 1, with the exception of I3 (remember, we are working with negative logic). IC6 recognises that the highest order bit which is logic 0, is the third bit, therefore it outputs the 8CD code for 3. As we have already established, 3 is $\log_2$ of 8, thus the conversion is complete.
The divide-by-sixteen counter, IC9, is followed by a monostable, which provides a reset pulse to the flip-flop formed by N6 and N7 at the end of each measurement cycle. The set pulse is provided by a second monostable, which is triggered by the start switch, S1. The decimal point on the seven-segment display is lit during each measurement cycle.
Since IC6 uses negative logic, its output signals must be inverted (by N2 . . . N5) before they can be fed to the 8CD-seven-segment decoder, IC7. The display is a common-anode type, e.g. HP 5082-7750, FND 557. Any type of LDR which is intended for measurement purposes, as opposed to switching applications, can be used. The type named in the circuit diagram is particularly suitable.
The circuit should be adjusted such that, as far as possible, the frequency of the two 555 oscillators is the same when identical amounts of light are falling on both LDRs.
The LDRs should therefore be laid upon a surface which is evenly illuminated. Coarse adjustment is performed by varying the values of C1 and C2, whilst fine adjustment — which in many cases will be all that is required — is carried out with the aid of P1.

J. van Dijk (The Netherlands)

57 emergency flight controller

When flying radio controlled model aeroplanes there is always the chance that a fault will occur in either the transmitter or the receiver, and that the plane will no longer obey the control signals. If one is fortunate, the model will fall near the operator, however it may equally well happen that the plane will remain in flight for a considerable distance, and that the last the unfortunate owner will see of his model is it disappearing over the horizon! The circuit described here is designed to prevent the latter possibility, and also attempts to lessen the severity of the crash, by ensuring that the model will assume a glide trajectory.
The circuit reacts to a loss of output from the receiver. When both transmitter and receiver are functioning normally, the position of the servos is determined by the transmitted control pulses. Depending upon the make of servo, a pulse width of 1.5 ms corresponds to the neutral position, whilst pulse widths of 1 and 2 ms correspond to the extreme positions of the servo. When the stream of control pulses is interrupted, the three multivibrators in the circuit set the servos to a predetermined position.
Input K4 is connected to the output of the receiver. Inputs K1, K2 and K3 are connected to the receiver servo control outputs for the elevator, rudder and engine throttle respectively, whilst outputs K1, K2 and K3 are connected to the corresponding servos. As long as control pulses are received via K4, the multiplexer, IC3, ensures that inputs K1, K2 and K3 are connected to the corresponding outputs (and servos). However when the control pulses are interrupted, the multiplexer switches to the outputs of the three oscillators. The position of P1, P2 and P3 then determine the position of the servo control horns. A mercury switch is connected across P3 (elevator control). The switch should be mounted such that it will close when the angle of descent is greater than 10°, whereupon the position of the elevator servo will be determined by the value of R_X (10 . . . 200 k).

W. van Staeyen (Belgium)



FM PLL using CA 3089 58

The following circuit should prove particularly interasting to those readers considering building thair own FM tuner. Tha novel feature of the circuit is that the well-known CA 3089 IC is not used as a conventional IF amplifier/demodulator, but as part of a phase locked loop. The resulting circuit is slightly more expensive and complicated than the 'standard' amplifier/demodulator circuits, however the results obtained ara a significant improvement on those of e 'classical' CA 3089 IF strip.

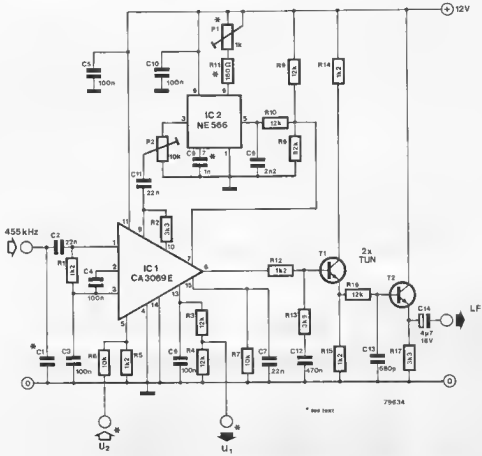
The circuit is intended as an IF amplifier/demodulator for a double conversion tuner operating at an intermediate frequency of 455 kHz. When using e PLL circuit for FM demodulation the S/N ratio of the demodulated signal is proportional to the ratio of frequency deviation/IF frequency, hence the PLL demodulator should operate at the lower IF of 455 kHz.

Briefly, the circuit functions as follows: The IF input signal is first fed to C1, which removes any high frequency signal components which might affect the operation of the PLL. The exact value of C1 will depend upon the mixar circuit which converts the 10.7 MHz output of tha front end to the desired IF frequency of 455 kHz. If the input signal is sufficiently 'clean' then lowpass filtering can be omitted. The CA 3089 amplifies and limits the IF signal to approximately 300 mV, whereupon it is fed to the on-chip quadrature detector. Output voltage U_1 can be used to drive a signal strength meter. The control voltage for the PLL VCO is taken from the AFC output (pin 7) of the IC. The voltage divider formed by R8/R9 is required to set the correct DC bias on pin 5 of IC2. Lowpass filtering of the control signal is provided by R10 and C8.

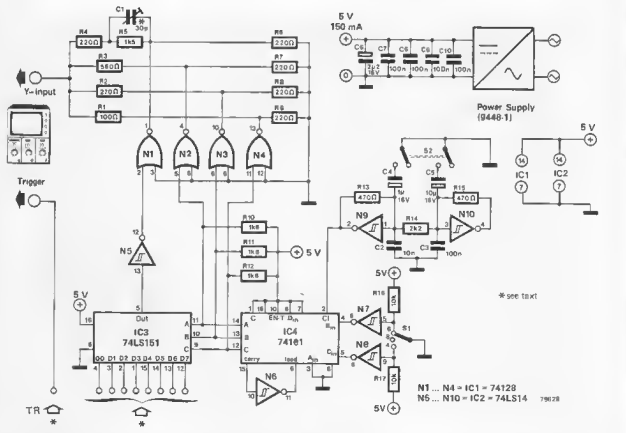
Largely for reasons of good linearity and high stability, a modern integrated circuit VCO, the NE566, was chosen. However the stability of the VCD is also significantly influenced by the associated frequency-determining components. P1 should preferably be a cermet trimmer, whilst a metal oxide rasistor should be used for R11 and a ceramic disc capacotor with extremely low temparature coefficient should ba used for C9. With the aid of a variable voltage divider (P2), tha squarewave output voltage at pin 3 of IC2 (approximately 5.4 V) is reduced to roughly 0.3 V and then fed back via C11, to the input of the quedrature detector of IC1.

The demodulated output signal is available at pin 6 of the CA 3089. If a squelch (muting) facility is required, this can be realised by feeding a positive control voltage to pin 5 of IC1, thereby suppressing the audio output. Finally, the audio signal is lowpass filtered and this output can be used with virtually any stereo decoder.

J. Deboy **(Germany)**



59 logic analyser



Although the name 'logic analyser' is generally understood to denote a quite different type of circuit, there are good reasons for borrowing the title to describe the electronic switch presented here. The switch is intended to simultaneously display the logic states of a number of test points in a digital circuit on an oscilloscope screen.

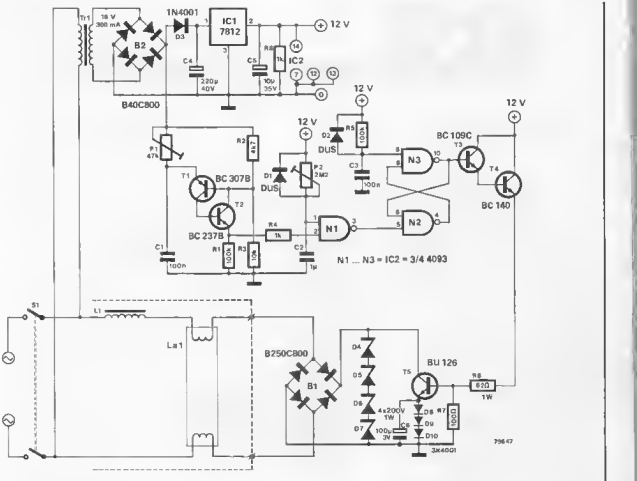
The circuit functions as follows: The oscillator formed by N9/N10 generates a clock signal with a frequency of either 1 kHz or 100 kHz, depending upon the position of switch S2. This signal is fed to a counter, IC4, which, depending upon the position of switch S1, can be preset to either '1000' (8), '1010' (10) or '1100' (12). The counter will therefore cycle through either the 8, 6 or 4 remaining output states before resetting to one of the above (preset) values. The result is that the A, B and C outputs of IC4 will count from either '000' to '111', from '010' to '111', or from '100' to '111'. The binary code present on these outputs determines which inputs are selected by the multiplexer, IC3. The multiplexer scans the inputs in turn, and transfers the input signal to the output. Depending upon the position of S1, therefore, 4, 6 or all 8 inputs will be scanned. To ensure that each input signal is displayed 'separately' on the screen, the corresponding binary code is also fed to inverters N2, N3 and N4, which, with the aid of the summing network R1 ... R4, ensure that a different DC offset is added to each signal. Thus each signal will appear at a different 'height' on the screen.

The trigger signal (TR) for the oscilloscope timebase is derived from the circuit under test. For slower scopes in particular, variable capacitor C1 can be adjusted to obtain optimal picture quality.

P. C. Demmer (The Netherlands)

60 quick starter for fluorescent lamps

An annoying disadvantage of fluorescent lamps compared to the incandescent variety is the flickering delay before they actually burst into life. This is because initially the gas in the tube is not at a sufficiently high temperature to ionise easily. Another reason is the fact that there is no control over the point on the mains waveform at which the current through the starter coil is interrupted. The following circuit is designed to



resolve these problems and ensure a flicker-free start.

When the mains voltage is applied, the filaments of the lamp, La1, are pre-warmed for a period of approximately 1 second (depending upon the position of P2). At that stage the current flows through the rectifier, B1, and transistor T5. Once the lamp has reached a sufficiently high temperature, it can be started. To ensure that the voltage induced in the choke (L1) is as large as possible, the current through the coil should be interrupted when it is at a maximum. The correct time is determined by the circuit round T1/T2. The pulse produced by T1/T2 triggers flip-flop N2/N3, with the result that transistor T5 is turned abruptly off. The resultant voltage induced across L1 ignites the pre-warmed lamp. The RC network R5/C3 ensures that the flip-flop is automatically reset at switch-on.

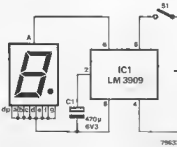
Due to its inductive nature, the voltage across the coil is shifted in phase with respect to the current through the coil (the voltage leads the current). T1/T2 must therefore provide a pulse just after the voltage has reached its maximum value. Potentiometer P1 should be adjusted until the lamp starts properly each time. The best setting for this potentiometer will depend upon the type of lamp used.

Transistor T5 dissipates little power and for so short a time that it does not need to be cooled.

D. Kraft (Germany)

61 flashing badge

Although primarily intended as a conversation piece at parties etc. the circuit described here can be used in numerous applications ranging from flashing house numbers to seat belt reminders. The circuit itself could hardly be simpler as it uses just one LM 3909 IC and a capacitor. When used as a flashing badge, the circuit is designed for use with a single HP7 (or similar) battery which can be mounted inside one half of a battery holder while the capacitor and IC are mounted in the other half. There



are a number of possibilities for the badge display itself. The author suggests the use of a line-o-light LED display or a seven-segment display (encapsulated in a suitable resin) to show the initial of the flasher!

Prospective constructors should bear in mind that the maximum output capability of the LM 3909 is around 50 mA.

L. Goodfriend
(United Kingdom)

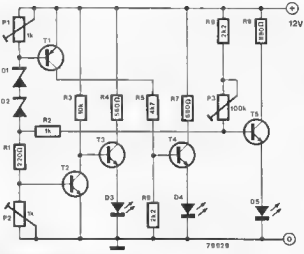
62 battery monitor

Only three LEDs are used to give an indication of the car (or boat) battery condition. The LEDs light as follows:

D3	< 12 V
D3 + D4	12 . . . 13 V
D4	13 . . . 14 V
D4 + D5	> 14 V

Preset P2 sets the voltage above which D3 goes out (13 V); P1 sets the point at which D4 lights (12 V), finally, P1 sets tha voltage above which D5 lights (14 V). The calibration procedure is rather critical, and will have to be repeated several times since the various adjustments affect each other.

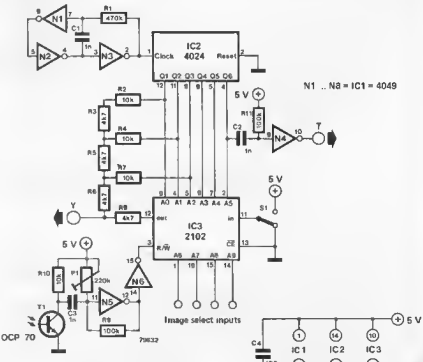
Tha photo shows the author's prototype. All components are mounted in a small plastic tube, with the LEDs at one end and a 'cigarette lighter' plug at the other. The unit can then easily be plugged into the corresponding socket on the dashboard for a quick check of battery condition. If the suggested colours are used for the various LEDs, red will correspond to 'battery low'; yellow (with or without red) indicates 'battery normal'; and green will normally light when the battery is 'on charge'.



S. Jacobsson (Sweden)

63 oscilloscope light pen

This circuit is intended to display any desired character on an oscilloscope screen. The character is produced by erasing certain dots in an eight by eight matrix with the light pen. An oscillator, formed by N1 . . . N3, provides a clock signal of approximately 2 kHz to a seven stage ripple counter, IC2. The outputs of this counter are used to address part of the memory circuit IC3. It is apparent from tha circuit diagram, that three of these outputs, together with the output of the RAM itself, are used to provide an analogue signal (Y) for tha Y input of the oscilloscopa. To enable the scope trace to be triggered at the correct time a short synchronisation pulse (T) is available from N4. The phototransistor T1 (OCP 70 or equivalent) should be mounted inside a light tube for better directional response. Once the oscilloscope is set up and the matrix display is visible, switch S1 should be set to the position shown in the diagram. Individual dots can now be erased by holding the light pen up to the required dot. The phototransistor



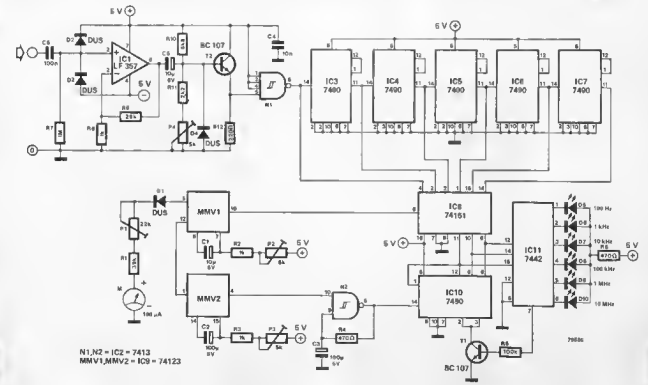
detects the arrival of the electron beam by the increase in light intensity and, once detected, provides a write pulse for the memory via N5, N6 and associated components. With S1 in the position shown, this pulse will write a '0' into the corresponding memory location.
To replace dots back into the display the original matrix can be moved up the screen whereupon a second matrix containing the missing dots will become visible. Switch S1 is then placed in the other position and the light pen again held up to the dot to be moved back into the upper matrix. It can be seen from the circuit diagram that only 64 of the possible 1024 memory locations are used and that A6 . . . A9 of IC3 can be switched to provide a total of sixteen different characters by extending the ladder network (4k7 and 10 k resistors). These address lines can also be encoded by suitable circuitry to convert the unit into a hexadecimal decoder and display, or even to provide an animated display.

A. N. Dames (United Kingdom)

analogue frequency meter 64

This circuit for a frequency meter offers six ranges: 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz and 10 MHz. Switching between ranges is performed automatically, and the display is analogue.
The input signal is first amplified to TTL level by means of IC1, T2 and N1, whereupon it is fed to a series of decade dividers (IC3 . . . IC7). Thus a signal with a frequency between 10 Hz and 100 Hz can be obtained either at the output of N1, or at the output of one of the decade counters. The analogue section of the circuit (MMV1, the moving coil meter and associated components) is designed to produce a full-scale meter deflection for an input signal of 100 Hz.
A multiplexer, IC8, is used to ensure that the correct divider output is selected. The multiplexer is clocked by counter IC10. Each of the input signals are fed to the output in turn, as long as the frequency of the output signal is lower than 10 Hz or higher than 100 Hz. If the frequency is lower than 10 Hz, then it is too low to keep the retriggerable monostable MMV2 continuously in the triggered state, with the result that the oscillator formed by N2 is started and clock pulses are fed via IC10 to the multiplexer. If, on the other hand, the frequency of the output signal is greater than 100 Hz, MMV1 remains permanently triggered, so that MMV2 no longer receives trigger pulses. This monostable thus resets, thereby ensuring that the oscillator is enabled and the multiplexer continues to cycle through its inputs. Only when the output frequency of the multiplexer is between 10 Hz and 100 Hz is the oscillator stopped, since MMV1 is not triggered sufficiently often to keep MMV2 in the triggered state. The result of stopping the oscillator is that the multiplexer in turn stops at the input which provided the signal of the appropriate frequency. LEDs D5 . . . D10 provide an indication of the range selected.
To calibrate the meter, P3 and P4 should initially be set to the mid-position, whilst P1 and P2 are adjusted for maximum and minimum resistance respectively. A 100 Hz signal (with an amplitude of greater than 1 V) is fed to the input of the circuit and P3 adjusted such that the multiplexer begins to cycle through its inputs. This can be verified by checking that the LEDs light up in turn. P2 is now adjusted until the 100 Hz range LED (D5) lights up. P1 is then adjusted for full-scale deflection on the meter. Finally, the circuit can be adjusted for maximum input sensitivity (approximately 10 mV) by means of P4.

H. Bichler (Germany)



Automatic battery charger

Recharging lead-acid batteries is often assumed to be an extremely straightforward matter. And that is indeed the case, assuming that no special demands are being made on the life of the battery. On the other hand, if one wishes to ensure that the battery lasts as long as possible, then certain constraints are placed upon the charge cycle.

Figure 1 illustrates the ideal charge current charecteristic for a normal 12 V lead-acid battary which is completely discharged. During the first phasa (A–B), a limitad charging current is used, until the battery voltage reaches approximately 10 V. This restriction on the charging current is necessary to ensure that the charger is not overloaded (excessive dissipation). For the next phase (C–D), the battery is charged with the '5-hour charging current'. The size of this current is determined by dividing the nominal capacity of the battery in ampere-hours (Ah) by 5. At the end of this period the battery should be charged to 14.4 V, whereupon the final phase (E–F) starts. The battery is charged with a much smaller 'top-up' current, which gradually would decrease to zero if the battery voltage were to reach 16.5 V.

The circuit described here (see figure 2) is intended to provide a charge cycle which follows that described above. If the battery is completely discherged (voltage < 10 V), so little current flows through D3 that T1 is turned off. The output of IC1 will be low, so that the base currents of T2 and T3, and hence the charging current, are datermined solely by the position of P1.

If the battery voltage is between 10 and 14 V, D3 is forwerd biesed and T1 is turned on. The output of IC1 still remains low, so that the charging current is now determined by both P1 and P2. If the wiper voltage of P3 exceeds the zener voltage of D1, then due to the positive faedback via R4, the output voltege of IC1 will swing up to a value determined by the zener voltage of D1 and the forward voltage drop of D2. As a result T1 is turned off and the charge current is once again determined by the position of P1. In contrast to phase A–B, howaver, the highar output voltaga of IC1 means that current through P1, and hence the charging current, is reduced accordingly.

Since D2 is forward biased, the effect of resistors R2 and R3 will be to gradually reduce the charging current still further, as the battery voltage continues to risa.

To calibrate the circuit, P3 is adjusted so that the output of IC1 swings high when the output (i.e. battery) voltage is 14.4 V.

By means of P1 the 'top-up' charge current is set to the 20-hour value (capacity of the battery in Ah divided

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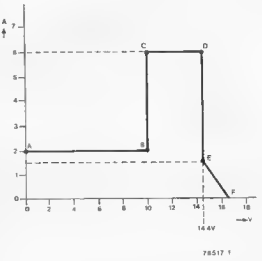

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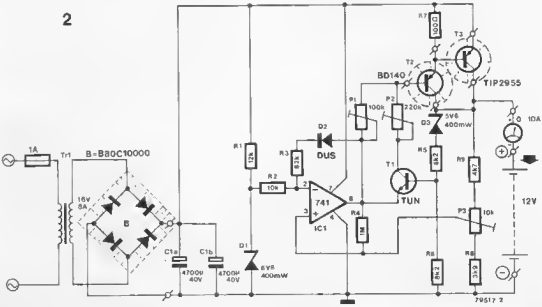
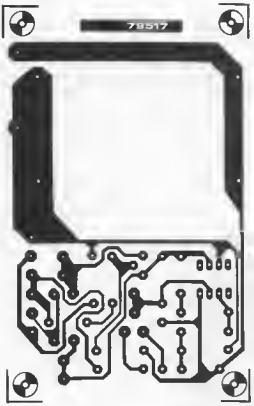
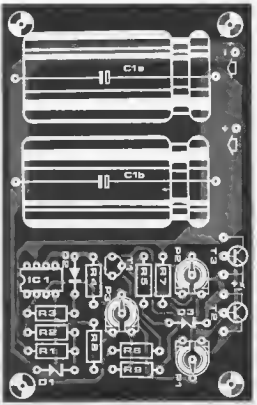






Parts list.

Resistors:
R1 = 12 k
R2 = 10 k
R3 = 82 k
R4 = 1 M
R5,R6 = 8k2
R7 = 100 Ω
R8 = 3k9
R9 = 4k7
P1 = 100 k preset
P2 = 220 k . . . 250 k preset
P3 = 10 k preset

Capacitors:
C1a = C1b = 4700 µ/40 V

Semiconductors:
T1 = TUN
T2 = BD138, BD140
T3 = TIP2955
D1 = 6V8, 400 mW zener diode
D2 = DUS
D3 = 5V6, 400 mW zener diode
IC1 = 741

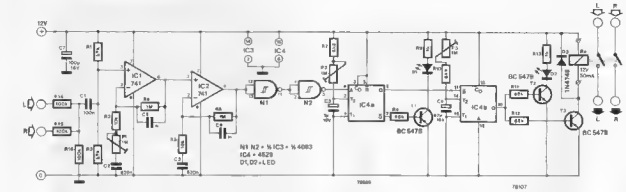
Miscellaneous:
Tr = 16 V, 8 A mains transformer
B = B80C10000 bridge rectifier
fuse = 0,5 A slo-blo

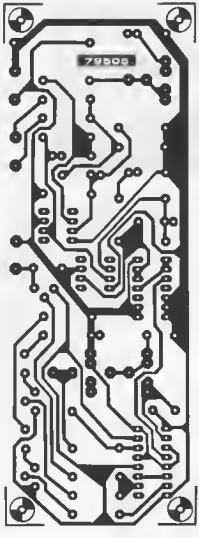
by 20) for voltages between 14.5 and 15 V. Finally, with a battery voltage of between 11 and 14 V, P2 is adjusted for the nominal (5-hour) charging current.
The initial charging current (phase A–B) is set by the value of the 'top-up' current, and depending upon the characteristics of the transistors, will be approximately 30 to 100% greater.

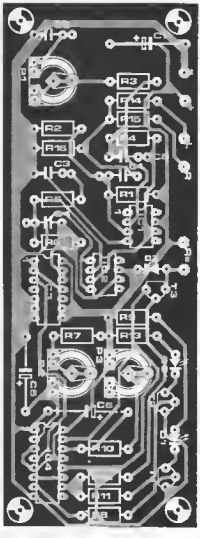
Siemens Components Report Volume XIII, No. 1 March 1978.

d.j. killer B

When we first published a circuit in last year's Summer Circuits issue which was designed to 'kill' the sound of a DJ's voice between records, little did we suspect that it would provoke such a widespread response. The circuit in question was even mentioned in a well-known daily newspaper, with several prominent DJs asked for their comments! Such is the evident popularity of the 'DJ killer' (at least among radio listeners, if not actually among the DJs themselves), that we have decided to produce a printed circuit board for it.
To recap briefly on how the circuit works:
It is possible to distinguish speech from music by virtue of the fact that distinct pauses occur in speech, whereas music is more or less continuous. The DJ killer detects these pauses and mutes the signal whilst the DJ is speaking.
The left and right-channel signals are fed into the two inputs of the unit and are summed at the junction of R14, R15 and R16. For use with a mono radio only one input is required. The summed signal is amplified and limited by two high gain amplifiers IC1 and IC2, and is then fed to two cascaded Schmitt triggers, N1 and N2. The output of N2 is used to drive a retriggerable monostable IC4a, the Q output of which is fed to the input of a second retriggerable monostable IC4b.
So long as a continuous signal is present at the input IC4a will be continuously retriggered by the out-







Parts List:

Resistors:
R1,R2,R8,R11,R12 = 68 k
R3,R5 = 10 k
R4,R6 = 1 M
R7,R10 = 6k8
R9,R13 = 1 k
R14,R15,R16 = 100 k
P1,P2,P3 = 1 M

Capacitors:
C1 = 100 n
C2,C3 = 820 n
C4,C8 = 1 n
C5 = 1 μ/16 V
C6 = 47 μ/16 V
C7 = 100 μ/16 V

Semiconductors:
D1,D2 = LED
D3 = 1N4148
IC1,IC2 = 741
IC3 = N1,N2 . . . = 4093
IC4 = 4528
T1,T2,T3 = BC5478

Miscellaneous:
relay 12 V/50 mA

put signal from N2 and its Q output will remain high. The period of IC4a is adjusted, using P2, to be somewhat less than the average duration of a speech pause, so that during such pauses IC4a will reset. This will cause IC4b to be triggered, switching off the signal for a period which is adjustable by P3. LEDs D1 and D2 indicate the output states of IC4a and IC4b and are used to set up the circuit.

To adjust the circuit P2 is first set to minimum resistance. The radio is then tuned to a station which is transmitting speech and P1 is used to adjust the sensitivity until D1 goes out during pauses. If the sensitivity is set too high then D1 will stay on continuously due to the circuit being triggered by noise, whereas if it is too low then D1 will extinguish during quiet passages of speech. The radio is then tuned to a station which is broadcasting music and P2 is adjusted until D1 stays on continuously.

Finally, the radio is tuned to a speech programme and P3 is adjusted until D2 remains permanently lit during speech.

It should of course be noted that the circuit will suppress only a pure speech signal. It will not, for example, suppress the voice of a DJ talking over the music.

R. Vanwersch

harmonic distortion meter

The following circuit is an improved version of the harmonic distortion meter published in the 1977 Summer Circuits issue. In place of transistors J-FET op-amps are used, whilst the circuit offers the choice of four switched spot frequencies as opposed to the single frequency available with the earlier version. The basic principle and operation of the circuit is the same, i.e. by applying bootstrapping to a twin-T network the Q of the filter is increased to the point where attenuation of the harmonics is eliminated. The filter thus rejects only the fundamental of the input (sinewave) signal, allowing the harmonic distortion products to be measured or examined on an oscilloscope.

In the circuit shown here, the input signal is fed via C1 directly to the twin-T network. An input buffer stage is not required. Capacitors C6 . . . C13 have a value C, where

$$C = \frac{4.82}{f}$$

(C is in nanofarads and f in kilohertz), whilst C2 . . . C5 have a value 2C. Odd values can be obtained by choosing two suitable capacitors in parallel. For example, for a 1 kHz 'notch', 4n82 can be formed by 4n7 + 120 p.

The filter is coarse tuned by P1/P3, and fina tuned by P2/P4. Inexpensive multi-turn trimmer potentiometers of the type used for station preset controls in radios and TV's can be employed. When tuning for zero fundamental, the two branches of the network (P1/P2 and P3/P4) should be adjusted alternetely.

The distortion signal is available at two outputs, D1 and D2. The signal at D2 is amplified by IC3 so that it is ten times greater than that at D1. Once the filter has been optimally tuned and no further reduction in the fundamental can be obtained, the peak-peak value of the distortion signal (D_{pp}) and the peak-peak value of the input signal U_{ipp} should be measured. The percentage distortion can then be calculated as follows:

$$\%d_{pp} = \frac{U_{Dpp} \cdot 100}{U_{ipp}} \quad \text{for D1, and}$$

$$\%d_{pp} = \frac{U_{Dpp} \cdot 10}{U_{ipp}} \quad \text{for D2.}$$

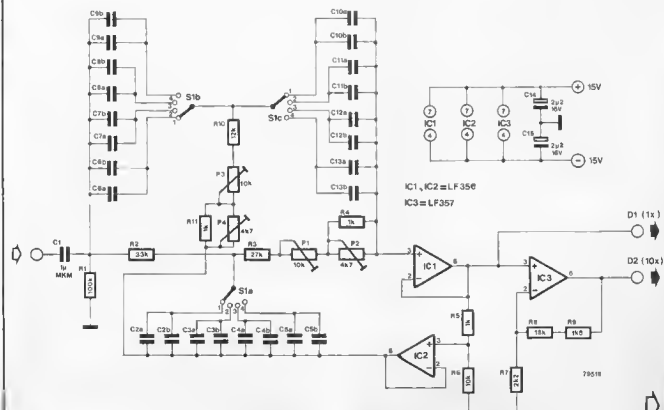
parts list

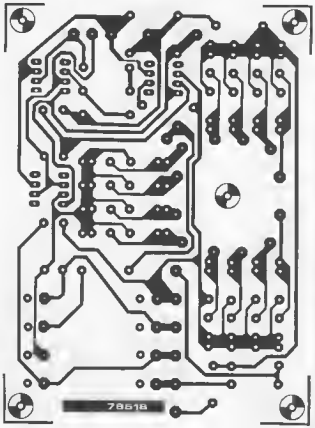
resistors
R1 = 100 k
R2 = 33 k
R3 = 27 k
R4,R5 = 1 k
R6 = 10 k
R7 = 2k2
R8 = 18 k
R9 = 1k8
R10 = 12 k
R11 = 1 k
P1,P3 = 10 k preset
P2,P4 = 4k7 preset

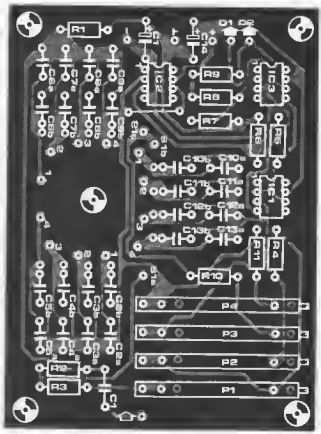
Capacitors
C1 = 1 μ (MKM)
C2a . . . C13b. see text
C14,C15 = 2μ2/16 V

Semiconductors:
IC1,IC2 = LF356
IC3 = LF356, LF357

Miscellaneous:
S1 = three-pole, multi-way switch.

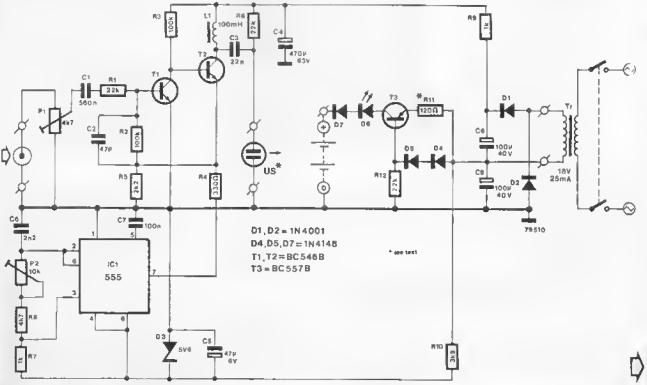


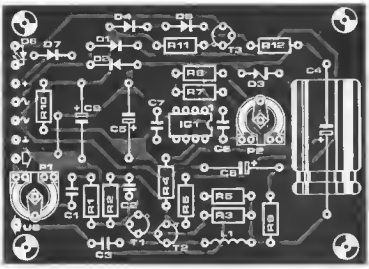


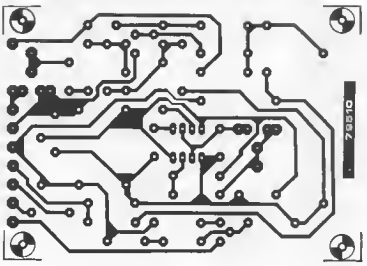


Dultrasonic transmitter for headphones

When considering constructing a 'wireless' headphones system, three basic approaches present themselves: a 'genuine' r.f. transmitter and receiver; an infra-red system employing IR LEDs and photodiodes, or an ultrasonic system. Since the first method is illegal and the second is both relatively complicated and







Resistors:

Resistors
R1,R6,R12 = 22 k
R2,R3 = 100 k
R4 = 330 Ω
R5 = 2k2
R7,R9 = 1 k
R8 = 4k7
R10 = 3k9
R11* = 120 Ω
P1 = 4k7 preset
P2 = 10 k preset

Capacitors
C1 = 560 n
C2 = 47 p
C3 = 22 n
C4 = 470 µ/63 V
C5 = 47 µ/6 V
C6 = 2n2
C7 = 100 n
C8,C9 = 100 µ/35 V

Semiconductors
D1,D2 = 1N4001
D3 = 5V6/400 mW zener diode
D4,D5,D7 = 1N4148
D6 = LED
T1,T2 = BC 107B, BC 546B or equ.
T3 = BC 177B or equ.
IC1 = 555

Miscellaneous:
L1 = 100 mH
US transducer: see text

expensive, we are left with ultrasonics, if we are looking for a reasonably simple and cheap transmitter/receiver.

Because of its inherent simplicity, amplitude modulation (AM) was chosen in preference to the qualitatively superior transmission system of frequency modulation. However providing one is reasonably ingenious in the design of the receiver, it is still possible to obtain highly acceptable quelity from an AM system. The circuit of the receiver is described in a companion article; the remainder of this article deals with the transmitter.

Apart from the supply stage, the circuit consists of only two sections: an audio amplifier stage (T1, T2) connected with negative feedback, and an astable multivibrator (IC1). Transistor T2 is switched on and off by the astable at en ultrasonic frequency. Thus at the collector of this transistor is a signal whose amplitude is varied in accordance with the input audio signal, and whose frequency is determined by the astable multivibrator. This signal is transmitted via an ultrasonic transducer.

The design of the audio amplifier stage is such (virtual earth configuration) that the astable multivibrator has very little effect upon the quality of the input signal and distortion is minimal.

The input sensitivity of the audio amplifier is about 60 mV. The modulation depth of the input signal can be varied by means of P1, whilst the frequency of the astable multivibrator, and hence of the trensmitted ultrasonic signal, can be veried between 15 and 35 kHz with the eid of P2. The optimal transmission frequency is determined in conjunction with the receiver and the type of transducers used.

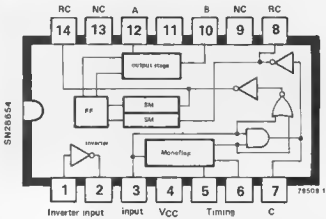
The supply stage is extremely simple. Space is provided on the printed circuit board for a current source (T3), which can be used to charge ni-cad cells in the receiver, should these be used. The charging current is 6 to 7 mA, although this figure can be increased by altering R11 accordingly. Various types of ultrasonic transducer are suitable. A more detailed discussion of this point is contained in the accompenying article on the receiver circuit.

E servo amplifier

A high quality servo amplifier can be built using only one IC and e hendful of passive components. The SN28654 (Texas Instruments) contains a pulse-width modulator and an output stege that is cepable of driving servo-motors (see figure 1).
An input pulse at pin 3 is compared to a pulse that is generated by an internal monostable multivibrator (the 'monoflop'). The resultant pulse is stretched (using RC networks and Schmitt triggers) and passed to the output stage and from there to the motor.
The complete circuit is shown in figure 2. Apart from the RC networks (R5/C4 and R8/C5) and some de-coupling capacitors, the only external components are the servo-motor and the associated servo-potentiometer. This potentiometer controls the timing of the internal monoflop, so that the motor will run until the internal pulse length corresponds to the input pulse — provided the motor is connected the right way round, of course!
The printed circuit board (figure 3) offers the option of including the inverter (between pins 1 and 2) in the circuit if required. This means that either negative or positive input control pulses can be used.
The advantages of this servo amplifier are:

- high output current: 400 mA without external transistors;
- motor control in both directions with a single supply voltage;
- adjustable 'dead zone' (determined by C3);
- power consumption less than 800 mW.

1



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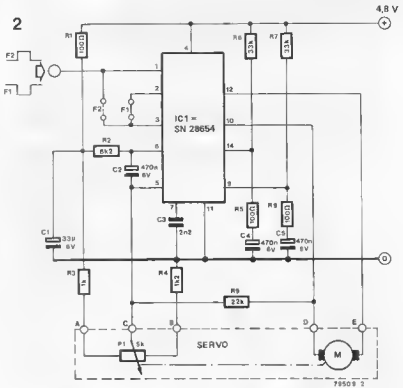

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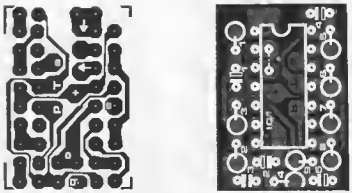


Parts list.

Resistors:
R1,R5,R8 = 100 Ω
R2 = 8k2
R3 = 1 k
R4 = 1k2
R6,R7 = 33 k
R9 = 22 k

Capacitors:
C1 = 33 µ/6 V
C2,C4,C5 = 0.47 µ/6 V
C3 = 2n2

Semiconductors:
IC1 = SN 28654

ultrasonic receiver for headphones

Before going on to describe the circuit of the receiver, there is one point worth noting. Although primarily intended for use in an ultrasonic transmission system, it is in fact much more flexible than one might think. If the ultrasonic transducer is replaced by a suitable (i.e. tunable) LC circuit, a highly sensitive 'conventional' AM receiver is obtained. The circuit can also be usefully employed as a direction finder in the 10 kHz to 30 MHz region.

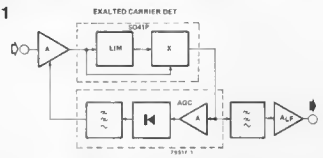
The receiver operates on the 'exalted-carrier' principle. The block diagram shown in figure 1 illustrates how this approach works. The received ultrasonic signal is first amplified (block A) before being fed to a limiter stage, which removes all traces of amplitude modulation and leaves only the carrier wave. The carrier signal is then multiplied with the non-limited AM signal in block X. Two product signals are obtained: the first is the modulation signal, and the second is a signal which has twice the frequency of the input signal. The output of the multiplier is fed to a lowpass filter which removes the high frequency modulation signal components, thus leaving the original audio signal, which can be fed via a simple amplifier stage (block A_{LF}) to the headphones.

To ensure that differences in input signal level have as little effect as possible upon the level of the audio output signal, the circuit is provided with a simple automatic gain facility (AGC). To this end the output of the multiplier is amplified, rectified and fed back via a lowpass filter as a DC control signal to the input amplifier. Thus the greater the amplitude of the input signal, the lower the gain of the input stage.

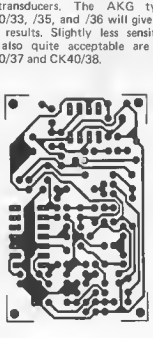
The circuit diagram of the receiver is shown in figure 2. The input amplifier is formed by an FET, type BF 256B (T1), connected in cascade with a conventional r.f. transistor (T2). The amplified input signal is fed via emitter follower T3 to an SO41P (IC1), which is a combined limiter/multiplier IC. The output of the multiplier (pin B) is in turn fed via the active lowpass filter round T5 to the audio output stage formed by a 741 (IC2). Potentiometer P1 provides a volume control.

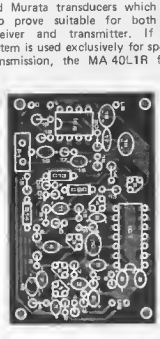
The AGC feedback loop consists of T4 (amplifier) and D1, D2 (rectifier), which provides a negative voltage which is directly proportional to input signal level; this voltage is applied to the gate of FET T1. The high input impedance (500 kΩ) and low input capacitance (5 pF) of the circuit render it suitable for use with modern electret microphone capsules as transducers. The AKG types CK40/33, /35, and /36 will give the best results. Slightly less sensitive, but also quite acceptable are the CK40/37 and CK40/38.

1



For the transmitter transducer, AKG types CK5011, CK5015 and, to a lesser extent, the CK5013, are best. In addition to the above mentioned types, there are a number of Valvo and Murata transducers which will also prove suitable for both the receiver and transmitter. If the system is used exclusively for speech transmission, the MA 40L1R from





Parts list

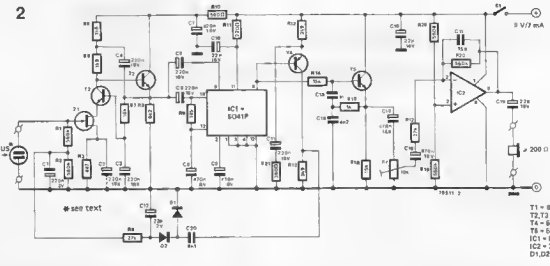
Resistors:
R1,R2,R18,R19,R20 = 560 k
R3 = 4k7
R4,R17 = 27 k
R5,R6 = 1k8
R7 = 18 k
R8 = 8k2
R9 = 1k5
R10 = 560 Ω
R11 = 220 Ω
R12,R13 = 3k9
R14,R16 = 15 k
R15 = 1 k
R21 = 390 Ω
P1 = 10 k preset

Capacitors:
C1,C2,C3,C4,C5,C6,
C11 = 0.22 µ/16 V Tantalum
C7,C8,C9,C15,C16 = 0.47 µ/16 V Tantalum
C10,C18,C19 = 22 µ/16 V Tantalum
C12 = 22 µ/3 V Tantalum
C13 = 1 n
C14,C20 = 4n7
C17 = 15 p

Semiconductors:
D1,D2 = 1N4148
T1 = BF 256B
T2,T3 = BF 494
T4 = BC 179C, BC 559C or equ.
T5 = BC 109C, BC 549C or equ
IC1 = SO41P
IC2 = 741 (MiniDip)

Miscellaneous:
us transducer (see text)

2



Murata is a good choice.
By mounting the components vertically, the printed circuit board is extremely compact. Since the circuit can be powered by a 9 V battery, one can justifiably speak of a miniature receiver. The current consumption of the circuit is only 7 mA, so that the batteries should be ensured of a relatively long life. If ni-cad cells are used, these can be recharged with the aid of the special charging circuit on the transmitter board.
In view of the wide bandwidth of the receiver, the transducer should be connected *directly* to the input of the circuit, i.e. no long leads between the two!

G frequency counter for synthesisers

A frequency counter is an extremely useful tool for tuning the voltage controlled oscillators (VCOs) of a synthesiser both quickly and accurately. To this end the author has designed a frequency multiplier which can be used in conjunction with the minicounter published in Elektor 38 (June 1978) to measure frequencies between 30 Hz and 10 kHz with much shorter gate/count times than would otherwise be the case. With a gate time of 1 s the maximum readout is 999.9 Hz, whilst with a gate time of 0,1 s the maximum frequency is 9999 Hz.
The circuit has two inputs: input 1 has a sensitivity of 1.3 V_{pp} (maximum input voltage 50 V_{pp}); input 2 has a sensitivity of 130 mV_{pp} (maximum input voltage 5 V_{pp}). The first is intended to be connected direct to the output of the VCOs, whilst the second can be used with the monitor output of an amplifier.
The input stage of the circuit is formed by two current controlled op-amps. A1 attenuates the signal at input 1 by a factor of 2, and amplifies the signal from input 2 by a factor of 5. A peak detector (D1, C2) and a comparator (A2) convert the input signal into a squarewave, which is then fed to a Schmitt trigger (A3). Flip-flop FF1 ensures that the squarewave is symmetrical.
The actual frequency multiplication is performed by means of a phase-locked loop (IC3), a dual-decade counter connected to divide by a hundred (IC4), and a flip-flop, FF2. A squarawave signal with half the fre-

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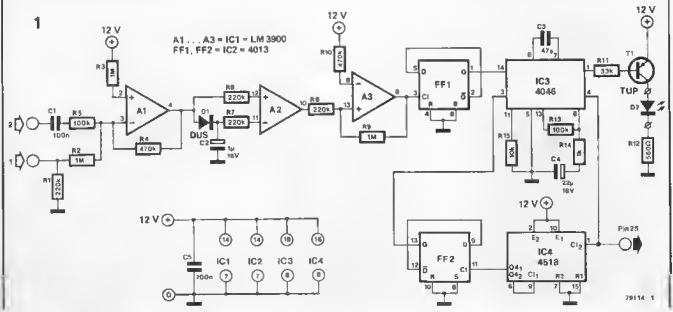

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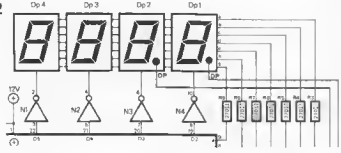


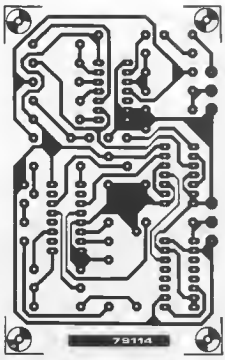
3

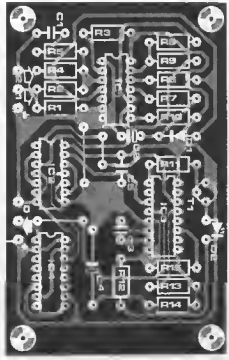
Parts list.

Resistors:
R1,R6,R7,R8 = 220 k
R2,R3,R9 = 1 M
R4,R10 = 470 k
R5,R13 = 100 k
R11 = 33 k
R12 = 560 Ω
R14 = 1 k
R15 = 10 k

Capacitors:
C1,C5 = 100 n
C2 = 1 µ/16 V tantalum
C3 = 47 p
C4 = 22 µ/16 V

Semiconductors:
IC1 = LM 3900
IC2 = 4013
IC3 = 4046
IC4 = 4518
T1 = TUN
D1 = DUS
D2 = LED





quency of the input signal is fed to one of the phase comparator inputs of the PLL, whilst the output signal of the VCO, divided 200 (by IC4 and FF2) is fed to the other input. The VCO provides an output signal with a frequency which ensures that the two comparator input signals maintain a constant phase relationship, i.e. they have the same frequency. Thus the output frequency of the PLL VCO will always be one hundred times that of the input frequency (i.e. the clock frequency of FF1). The time constant R14/C4 determines the speed at which the VCO responds to changes in the input frequency.

When the circuit is not 'locked-on', the display obtained will not be accurate. For this reason LED D2 is included; when the VCO has locked-on this LED will extinguish, thereby indicating that the meter reading is correct.

The output of the circuit is connected directly to the clock input of IC1 in the minicounter, which means that the input stage around T1 is omitted. The supply voltage can be derived from the minicounter itself

To ensure that the position of the decimal point on displays 1 and 2 (see figure 2) corresponds to the input range, several minor modifications to the minicounter board are necessary. These are shown in figure 3.

J. Naudts

autoranging peak meter

If not always for exclusively technical reasons, output level meters are a particularly popular type of circuit, especially in audio applications (power amps etc.) The circuit described here is for a moving coil meter with an autoranging facility. The meter will read from −40 to −20 dB, and from −20 dB to 0 dB; two LEDs indicate which range is selected (see figure 1). By adopting this approach the resolution of the meter is considerably improved.

The circuit diagram of the meter is shown in figure 2. The input signal is fed to an attenuator (P1) before being full-wave rectified by the circuit round A1 and A2. The output of the rectifier circuit is then fed through either S1 or S2, depending upon which switch is closed. The two switches are controlled by the comparator, A6. The state of the comparator in turn depends upon the

level of the input signal. If the voltage at the non-inverting input of the comparator is lower than the wiper voltage of P3 (i.e. if the input signal level on P1 is lower than −20 dB for sufficiently long), the output of the comparator will be low, D7 will light up, S2 will open and S1 close. A voltage 3.3 times the input voltage of A3 is then fed to the peak rectifier circuit round A4. The gain of A3 is determined by R8 . . . R11. If, however the input signal level is greater than −20 dB, the output of A6 goes high, D8 lights up, S1 opens and S2 is closed. Due to the effect of R10 . . . R12, the rectifier input voltage is attenuated by a factor of 0.33. Thus between the two switch states there is a difference in signal level of a factor of ten, i.e. 20 dB.

The printed circuit board is designed to accomodate a stereo version of the circuit. The components shown in inverted commas and the pin numbers in brackets belong to the right hand channel.

A signal generator is required to calibrate the circuit. The wiper voltage of P1 at which the maximum

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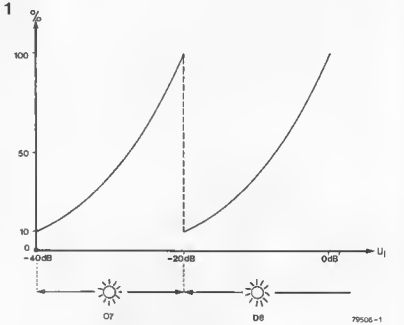
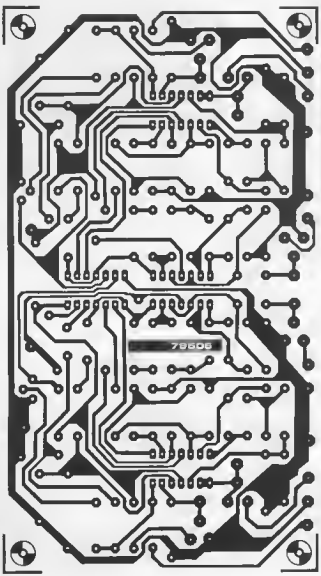
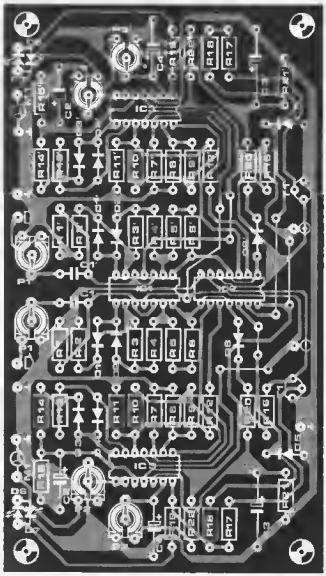


reading (0 dB) is obtained can, within reason, be selected as desired; however it is recommended that a 0 dB level corresponding to roughly 4 volts be chosen. The maximum output voltage of A5 is then approximately 1.33 V; with a 100 μA moving coil meter for M1 and M1', P2 should





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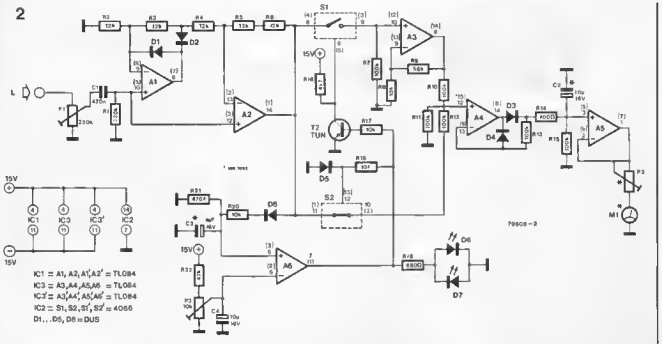
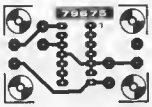


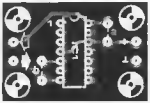
then be adjusted for a resistance value of roughly 13 k.
Potentiometer P3 should be adjusted by starting with D6 lit and a full-scale deflection on M1, and gradually reducing the input signal until at 10% of its original level, the needle suddenly jumps back up to full-scale deflection once more, D6 goes out and D7 turns on. The amplitude of the input signal should be varied very slowly, since switching between ranges takes a finite time (R20, R21, C2). If required, the value of C2 and C3 can be altered to suit the particular meter ballistics.

Based on an idea by P. de Bra

inclusive always/ exclusive never gate

With the printed circuit board design given here, it is possible to obtain an 'inclusive always' gate by mounting wire link 'a', or an 'exclusive never' gate if wire link 'b' is mounted. The circuit will operate satisfactorily with several different IC types (see parts list). For reasons of cost, it is advisable to mount defective ICs, although if good ICs are used the circuit itself will usually remedy this.





Parts list:

semiconductors:
IC1 = 7400,7401,7402,7403,7404,7405, 7406,7407,7408,7409,7410,7412,7413, 7414,7415,7416,7417,7420,7422,7425, 7426,7427,7428,7430,7432,7433,7437, 7438,7440,7450,7451,7453,7454,7460, 7470,7472,7474,7480,7481,7486,7487, 7495,74104,74105,74107,74110,74115, 74121,74122,74125,74126,74128, 74132,74164,74176,74177,74178, 74180,74183,74196,74197,74278 (or equ.).

miscellaneous:
wire link (see text).

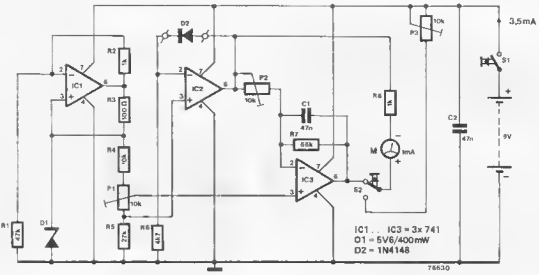
65 thermometer

The circuit shown here utilises the negative temperature coefficient of a diode to sense varietions in temperature. If a constant current is flowing through a forward-biased diode, the voltage dropped across the diode is inversely proportional to temperature.

In order to obtain a stable reference voltage, a 'super zener' configuration is used. IC1 ensures that a constant current flows through the zener diode, so that the zener voltage is uneffected by variations in the supply voltage. A 5.6 V zener was chosen for its low temperature coefficient. When the temperature of the sensor diode changes, the output voltage of IC2 varies by roughly 2 mV per °C. This voltage is emplified by IC3 end fed to the meter. The meter is calibreted for zero reading at the lower end of the desired temperature scale (e.g. 0°C) by means of P1, and for full-scale deflection at the top end of the scale by means of P2.

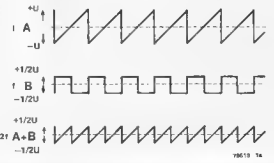
The circuit consumes relatively little current (roughly 3.5 mA), which means that it can be powered by a 9 V battery. The thermometer only draws current when a temperature reading is required (pushbutton switch S1 is depressed). Switch S2 allows the state of the battery to be monitored, and P3 should be adjusted to give a suitable deflection. However since the meter reading will also be influenced by the temperature of the sensor diode, the measurement thus obtained should only be taken as a rough indication of the battery state. With the component values shown in the diagram, the circuit hes a measurement range of roughly 50°C (depending upon the setting of P2). The range can be varied by altering the value of R7 (e.g. R7 = 33 k gives a range of 100°C). A further possibility is to reverse the meter connections, i.e. if the scale was previously 0 to 50°C, reversing the connections to the meter would give a scale of −50 to 0°C.

S. Jacobsson (Sweden)



66 sawtooths up or down an octave

The sawtooth is a favourite weveshape in electronic organs. Twelve different frequencies are required within one octave; for other octaves, frequencies are needed that are a multiple of two higher or lower. Given a sawtooth with a frequency f_o, two new sawtooth waveforms can be obtained that are one octave higher and lower respectively ($2 f_o$ and $1/2 f_o$). The principle is described here.



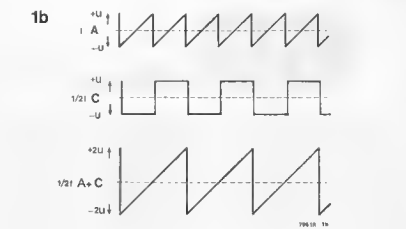
The new sawtooth is obtained by adding a symmetrical square-wave to the original wave-form. As shown in figure 1a, adding signal A (with frequency f and amplitude U) to squara-wave B (with frequency f and amplitude 1/2 U) results in a sawtooth with twice the frequency and half tha amplitude of the original. Conversely, if the squarewave is at half the original frequency and has the same amplitude as the input signal, the output will be a sawtooth at half the original frequency and twice the original amplitude – as shown in figure 1b. Obviously, the above only applies if the 'edges' of the square-wave and sawtooth coincide – in other words, if the signals are 'in phase'.

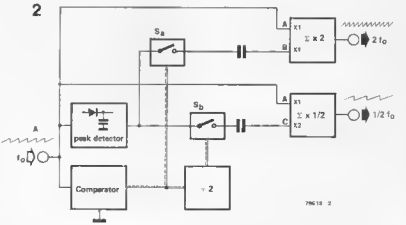
The block diagram of a suitable circuit is given in figure 2. The input signal is passed to a peak detector. This stores the peak level (+U) of the input signal; this level is passed via switch S_a to a summing circuit. Since the switch is operated (via a comparator) by the input signal, it 'chops' the peak level U at the same frequency as the input signal. After restoring the symmetry of the squarewave with respect to supply common (by adding a series capacitor), the result is a squarewave with the same frequency but half the amplitude of the input sawtooth. Add it to the original sawtooth, and what do you get? Twice the original frequency and half the amplitude.

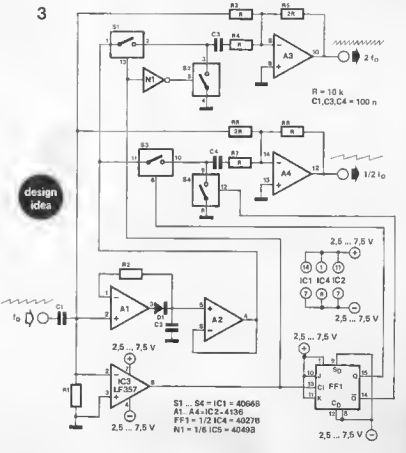
To get the other output (at half the frequency), the peak level of the input signal must be doubled (x2) and the 'chopper' frequency for the switch must be halved (÷2). Finally, if the upper summer has a gain of x2 and the lower has a 'gain' of x1/2, the sawtooths at the output will have exactly the same level as the original input signal.

A 'rough draft' of a suitable circuit is shown in figure 3. The peak detector (A1) is followed by a buffer (A2). The (electronic) switches both consist of two sections: when S1 opens, S2 closes – shorting any remaining feedthrough to ground and pulling C3 down. Flip-flop FF1 takes care of the frequency division required for the control signal to S3 + S4 (= S_b). Virtual-earth type summing amplifiers are used (A3 and A4), with a gain of x2 and x1/2, respectively.

N. Nielsen (Denmark)







67 stereo from mono

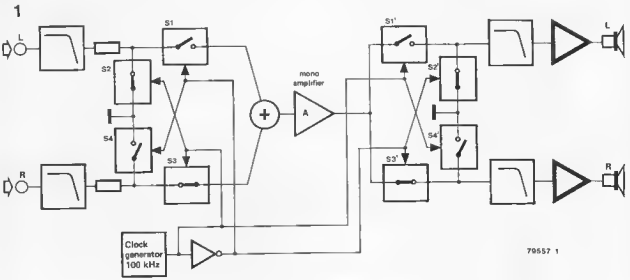
Sometimes ideas occur, which, although good in themselves, cannot be implemented because the necessary technology is not yet there. Consider, for example the possibilities if one could obtain stereo reproduction from a mono amplifier. Although the idea seems far-fetched, in principle this can be achieved by multiplexing the left and right channels, i.e. feeding the left and right channel information alternately through the mono amplifier. Figure 1 shows a design where only the preamplifier is common to both channels, whilst in figure 2 the power amp is also included.

Switching between channels is performed by means of groups of electronic switches: S1 . . . S4 at the input, and S1' . . . S4' at the output. Before the left and right channel signals are multiplexed they must first be bandwidth limited by low-pass filters with as steep as possible a roll-off. After being split back into two signals again, both channels must once more be lowpass filtered to remove the clock frequency components. In figure 1 the output filters can be active, however in figure 2 loss-free passive (LC-)filters must be used. A suitable clock frequency (switching rate) would be around 100 kHz.

There are no direct obstacles in the way of a design such as that shown in figure 1. The same is not true of the circuit in figure 2 however, since sufficiently fast low-loss power switches do not as yet exist. However that is not to say that they will not do so in the future.

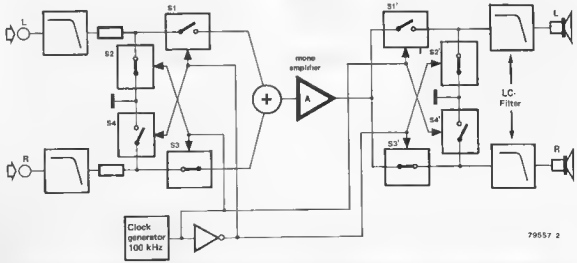
A. Jahn (Germany)

1



design ideas

2



digisplay 68

The idea itself isn't new – a similar circuit was published in Elektor, May 1976 – but the simplicity of the circuit described here lends it a special charm . . . Only three ICs and a handful of other components are required to recognise the logic levels of sixteen different signals and display them on an oscilloscope screen. The display consists of two rows of noughts and ones. This is achieved as follows. If a sine-wave is applied to the Y-input of an oscilloscope, the display depends on the signal applied to the X-input. If a sawtooth is applied, the sinewave is traced on the screen; if there is no signal on the X-input, a vertical line will be displayed; and, finally, if a sine-wave of the same frequency as the first but with different phase is applied, a circle or ellipse can be obtained. The vertical line or circle can be positioned at any point on the screen by adding a suitable DC offset to the X- and/or Y-input signals. In the circuit described here, two rows of eight lines or circles are displayed.

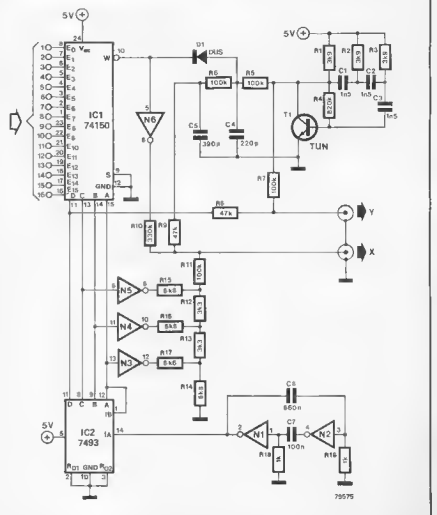
The circuit is shown in figure 1. Up to sixteen input signals are fed to the inputs of IC1. IC2 is a four-bit binary counter, and it applies binary numbers from 0 to 15 to the A, B, C and D inputs of IC1. When the number '0000' is applied, the signal at input 1 (E_0, pin 8) of IC1 is passed (in inverted form) to its output, W. As the count at the A . . . D inputs proceeds, the rest of the inputs 2 . . . 16 are also scanned in sequence and passed to the output. When a '1' is present at the selected input, the output signal from IC1 is at logic zero. The voltage at the R5/R6 junction is clamped to supply common via D1 and the output of N6 is 'high', so the X-output signal is determined by the output of IC2 and the resistor network R11 . . . R17. This signal is the 'DC component' that is required to step the display along the eight positions in one horizontal row.

The Y-output signal consists of two components. A 'DC shift' signal is taken from the D-output of IC2, to switch the display from the upper to the lower row and back, as required. Superimposed on this signal is the output from a simple RC oscillator (T1). If all 16 inputs to IC1 are at logic one (so that the W output is always '0'), the display will therefore consist of two rows of eight short vertical lines.

When the W output goes to '1', however, the voltage at the R5/R6 junction is no longer clamped to supply common by D1. R5, R6, C4 and C5 are a phase-shifting network, so the sine-wave output from the oscillator is applied to the X-output (via R9) with a phase-shift with respect to the Y-output. The result: a circle on the screen.

If the 16 inputs of IC1 are connected to the pins of a TTL IC (using a DIL test clip, for instance), the logic levels at the pins of the IC will be displayed on the screen. The upper row corresponds to inputs 0 . . . 7, the lower row to inputs 8 . . . 15. Unconnected pins are shown as 'ones'.

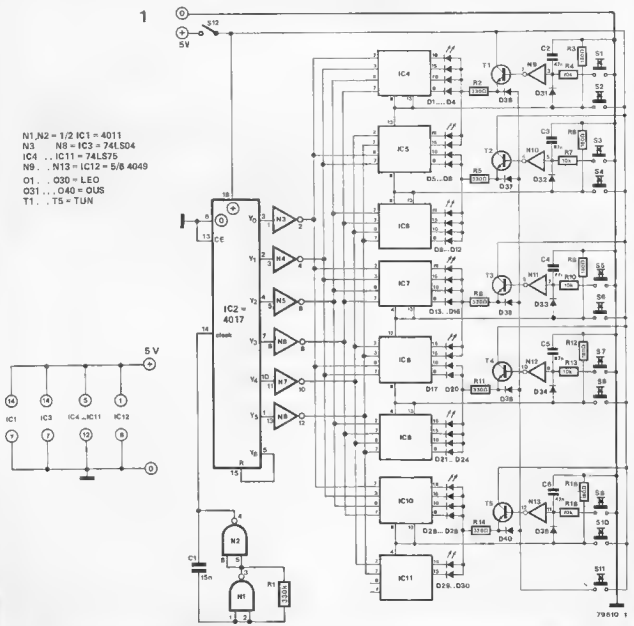
A. Kraut (Germany)



69 electronic poker dice

Most people will have played with poker dice at one time or another, but not everyone will have realised that there are considerable possibilities for the skilled player to cheat. The following circuit for an electronic set of dice should contribute to ensuring a more honest game. The five dice are replaced by five rows of six LEDs (D1 . . . D30, see figure 2) each LED corresponding to a different face of the die. For each row there is a 'throw' button (S2, S4, S6, S8, S10) and a 'set aside' button. When a 'throw' button is pressed, the result is not displayed immediately. To find out which faces of the dice have been thrown, it is necessary to press the 'shaker' button S11, which, as it were, 'uncovers' the dice, enabling the players to see them. If one has thrown, say, a pair on the first turn, by pressing the corresponding 'set aside' buttons, the two LEDs representing the pair will remain permanently lit. This is the equivalent of setting the pair of dice to one side (for all to see), before putting the remaining three dice back into the shaker and trying to improve one's score.

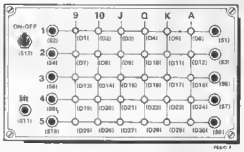
The actual circuit (see figure 1) is quite straightforward. A divide-by-six counter (IC2) is clocked by the oscillator round N1, N2. The outputs of N3 . . . N8, which are connected to S x 6 = 30 latches (IC4 . . . IC11), each go low in turn for the duration of one clock period. The outputs of the latches are connected to the display LEDs, D1 . . . D30. When one of the 'throw' buttons (S2, S4, S6, S8, S10) is pressed, the three enable inputs for the corresponding set of LEDs are taken high, with the result that the data present at that moment on the inputs of the latches are transferred to the outputs. The cathode of one LED in each set of six is pulled down virtually to ground,



and these LEDs will light should S11 now be pressed (current being supplied via S11, D36 . . . 40, R2, R5, R8, R11, R14).
If the corresponding 'set aside' button is pressed, the LEDs whose cathodes have been pulled down to earth will turn on permanently. Suppose, for example that S1 is pressed, C2, which, when the 'throw' button was pressed, charged up via D31, is now discharged. The output of N9 is thus taken high, so that T1 supplies current to the LED, whose cathode is at earth . . . . . .
There is one further point worth noting. Although it was stated that the circuit should help to ensure a more honest game, it is important that each of the 'throw' buttons are pressed in turn, and not simultaneously. The reason for this precaution is that if two or more buttons are pressed at the same time, there is an increased chance of pairs or trebles etc.

A. Vandermeelen (Belgium)

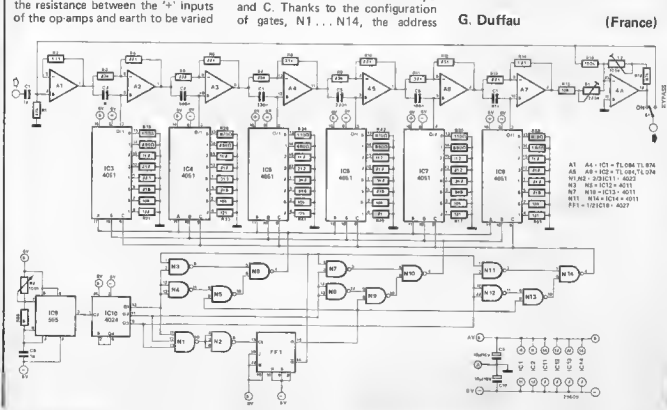
2



digitally-controlled phaser 70

Phasing is a well-known musical effect which is obtained by varying the phase relationship of a signal with respect to an original version of the same signal, whilst ensuring that its amplitude remains constant: the phase-shifted and original signals are then summed in proportions which are determined by the intensity of phasing required.
In the circuit shown here, the phase shift is provided by op-amps A2 . . . A7. The constant changes in phase are obtained by arranging for the resistance between the '+' inputs of the op-amps and earth to be varied with the aid of a low frequency modulation signal. Normally FETs are used as voltage-controlled attenuators, however they have the drawback of introducing a noise component and are not perfectly linear. The approach adopted here, although more complex, is superior. Eight resistors are switched in and out of circuit via multiplexers IC3 . . . IC8 (which thus function as single-pole, 8-way electronic switches). The multiplexers are controlled by the information present on address lines A, B and C. Thanks to the configuration of gates, N1 . . . N14, the address data continuously cycles from 000 to 111 and back down to 000 again. The clock pulses are provided by the 555 timer, IC9. The clock frequency, and hence the speed of the phasing, can be varied by means of P3, whilst P1 allows the depth of phasing to be adjusted. The overall gain of the circuit is controlled by P2.
A symmetrical supply voltage (max. ± 7.5 V) is used. In the prototype version the author used 2 x 4 1.5 V batteries to make up the 6 V supply lines shown in the diagram.

G. Duffau (France)



71 capacitance and inductance meter

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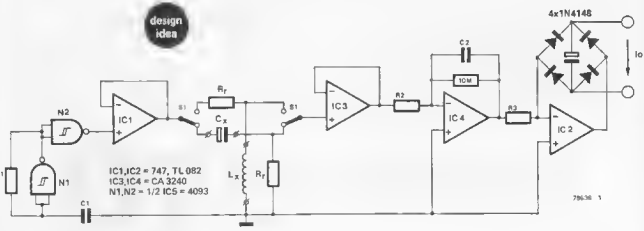
design idea



It is often very useful to ascertain the value of an unmarked or suspect capacitor or indeed to determine the value of a home-wound (or otherwise) inductor. The design idea described here is intended to fulfill both of these requirements by utilising an existing multimeter.

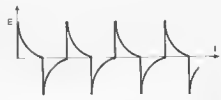
In figure 1, a squarewave is produced by N1 and associated components, buffered by N2 and IC1 and fed to one of the high pass filters Rr/Lx or Cx/Rr (see figure 2a). After being differentiated by the filter network (figure 2b) the signal is again buffered (by IC3) and then integrated by the circuit around IC4. The resultant waveform is then amplified and rectified by IC2 whereupon it can be displayed on the multimeter. The formulae for calculating the voltage at the output of IC4 (so we are told!) are:

for capacitance: $U_{out} = E \cdot \frac{RrCx}{R_3C_2}$

for inductance: $U_{out} = \frac{E \cdot Lx}{R_3C_2Rr}$

2a

2b



where E is the supply voltage. Therefore by selecting suitable range resistors Rr, and frequencies, different values of capacitors and inductors can be measured. The only proviso is that the square-wave period time (=2.5 R_1C_1) must be at least sixteen times larger than $\frac{Lx}{Rr}$ or $CxRr$, to obtain a sufficiently accurate measurement.

T. Alfredsson (Sweden)

72 nerves of steel

Behind the above title lies a well-known type of dexterity game, in which two players each attempt to pass a ring along a length of wire without touching it. The first player to reach the end of the wire is the winner. If however a player's ring should happen to brush the wire, an LED lights, indicating that he must go back to the start and begin again. The circuit incorporates an additional refinement in that, whilst one player's 'go-back-to-start' LED is lit, the other player can touch his own wire without incurring a penalty (i.e. without his own LED lighting up), thereby enabling him to speed up. However the second player must be careful, since the moment the first player reaches the start again, his LED will go out, simultaneously enabling the LED of the second player.

The actual circuit is straightforward, being based on the operation of two flip-flops formed by N1 . . . N4. At the start of the game, once both

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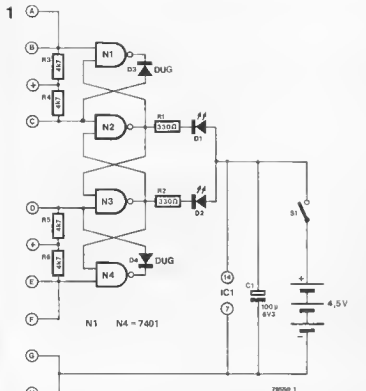

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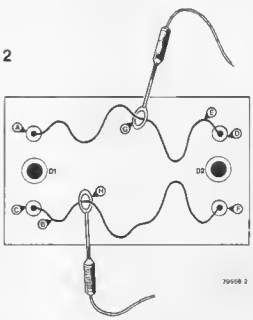

player's rings have touched the start electrodes (C and D), the outputs of N2 and N3 are high (and LEDs D1 and D2 are extinguished), whilst the outputs of N1 and N4 are low. The free inputs of N2 and N3 are also low, i.e. at a potential just above the forward voltage drop of a germanium diode (roughly 0.2 V). Assume now that player 1 touches his wire (B). The input of N1 is momentarily taken low, which takes the output of N1 high and the output of N2 low. The 'go-back-to-start' LED of player 1 thus lights up, whilst the outputs of N3 and N4 remain unchanged.

What happens now if player 2 touches the wire (with D1 still lit)? The input of N4 (E) is momentarily taken low, thus taking the free input of N3 high. Since the other input of N3 is low, the output of N3 will remain high, so that LED D2 cannot light up. This situation will only change when the first player once more touches the start electrode, taking the output of N2 high again. Figure 2 shows a sketch of a possible layout for the game. Ordinary fairly stiff copper wire can be used, and obviously the 'difficulty factor' can be varied depending upon the shape into which the wire is bent and upon the diameter of the rings.

R.J. Horst (The Netherlands)

bicycle speedometer 73

Circuits for bicycle speedometers have been fairly common (Elektor published one in last year's Summer Circuits issue No. 39/40), the difference in this particular design being the digital readout. The speed sensing is carried out by a number of magnets attached to the spokes or rim of the wheel which operate a pair of reed switches. The principle is illustrated in the drawing in figure 1. where the reed switches are shown fitted on the bicycle front forks. The main advantage that a digital display has over a moving coil meter is that of robustness in a situation where the younger generation can create a very harsh environment. Current consumption is kept to a

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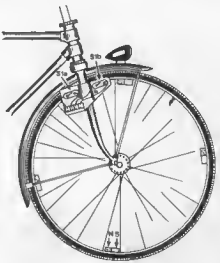
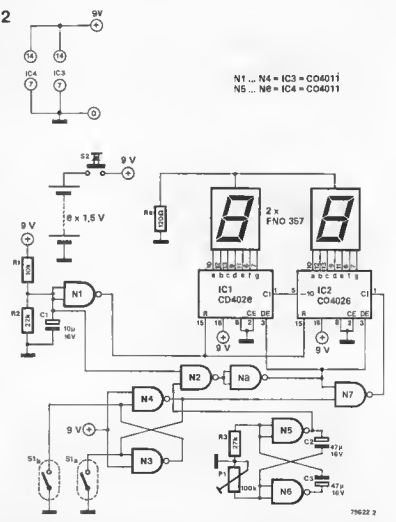


minimum by arranging for the power supply to be switched on only when e readout is required. This switch (S2) should ideally be mounted on the handlabars (i.e. using an electric bicycle horn button or similar). The circuit diagram for the digital speedometer is shown in figure 2. The principle behind the circuit is uncomplicated: The pulses from the reed switches are fad to a counter (IC1, IC2) for a predetermined langth of time. The counter is then inhibited and the count decoded and displayed. Dacoding and display driva is parformed by the counter itself. N3 and N4 serve to eliminate contect bounce from tha read switches, S1a and S1b, whilst the count pulses are fed to IC1 via N7. The meesurement period is determined by the circuit round N5, N6, and can be varied by adjusting P1. The meter can therefore be calibreted with the aid of this preset. The charge time of capacitor C1 will ensure that the counters are reset by N1 before a new count cycle starts. Gate N2 prevents a count cycle starting before the reset is cleared. In view of the high current consumption of LED displays, a continuous readout is not feasible. A 'push-button'-type display was therefore chosen, i.e. each time S2 is depressed the speed of the bicycle at that particular moment is displayed. This approach also means that the components which would have been required to ensure that the counter is automatically resat after each count can be dispansed with.

In principle any number of magnets can be employed, however in order



to avoid excessively long count periods, a minimum of three is recommended. The circuit should be calibrated (i.a. P1 adjusted for the desired count period) with the aid of an existing speedometer.

P. de Jong (The Netherlands)

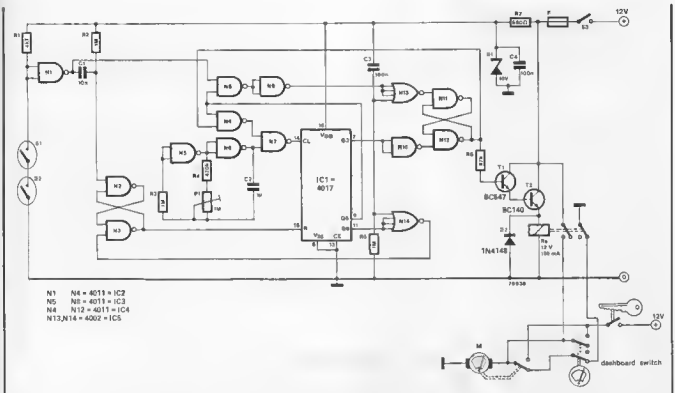
74 automatic windscreen clearer

The designar of this circuit must have had fraquant occasion to becoma annoyed at the various pamphlats, posters and advartising 'bumph' which is left undar tha windscreen wipers of parkad cars, for he has come up with a radical antidote – an automatic windscreen clearar. Unfortunately this inganious device has one slight drawback, eny meter-maid or passing policamen who tries to laave a parking ticket under the wipers might well be less than pleased to see the ticket being repaatadly pushed off the windscreen (although perhaps some of our readers will find this prospect an added attraction).

The circuit reacts to the windscreen wipers being lifted off the windscreen by switching on the wiper motor, with the result thet the offending piece of paper is swept away. To detect when the wipers are lifted up, two reed switchas are mounted on the inside of tha windscreen et the point whera the wipers come to rest. A small magnet attached to each wiper holds the switches closed under normal conditions. However, when one of the wipers is lifted off the windscreen, the corresponding switch opens, and the flip-flop formed by N2 and N3 removes the inhibition on the decade counter, IC1. The latter starts to count clock pulses from the clock oscillator (N5, N6), and after the third pulse the Q3 output goes high, with the result that the second flip-flop, formed by N11 and N12, turns on T1 end T2. The ralay Re, is then pulled in, thareby switching on the wipers.

After a further five clock pulses, the Q8 output of IC1 going high inhibits the clock signal via N4 and N7. Gates N8, N9 and N13 now ensure that the second flip-flop causes the relay to drop out (T1 and T2 are turned off) the moment both raad switches era closed. IC1 restarts to count, and upon the next clock pulse, the Q9 output goas high, causing the first flip-flop (N3, N4) to reset the counter.

When power is applied, C3 and R5 ensure that the two flip-flops are automatically reset. The length of time the wipers are switched on is



determined by P1, and can be varied as desired. The extra break contact in the relay prevents any difficulties arising in the event of wipers being turned on when the circuit is operating. The circuit can only be used with wiper motors having an internal switch (wired in parallel with the manual switch) that opens to bring the wipers to rest. Fortunately, these are the most commonly used type. To deter even the most persistent of pamphleteers, one could even go so far as to use the circuit to switch on the windscreen washer as well as the wipers!

E. Stamberger **(Austria)**

75

noise level meter

There are many potential applications nowadays to justify the use of a noise level meter — for instance, monitoring the sound output at dances, discos etc. The unit described here was designed primarily to establish the noise level produced by model engines. It has five switched ranges from 70 dB to 120 dB in 10 dB steps and is readable to ½ dB. The prototype was found to be accurate to ± 1 dB.

The circuit for the noise level meter is shown in figure 1. The sound signal is picked up by the micro-

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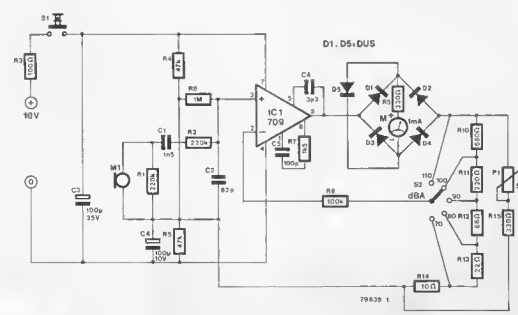
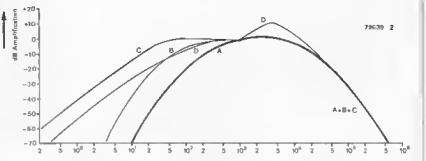


phone M1 and filtered by the network C1, C2, R1 and R2. These components, together with the capacitance of the microphone and the input impedance of the amplifier, ensure that the frequency response of the system is corrected to suit the internationelly standardised 'A' weighting curve shown in figure 2. This 'weighted' signal is then fed to the operational amplifier A1, the gain of which can be altered by S2 to provide five noise ranges.

The AC output of the op-amp is then rectified by diodes D1 . . . D4 and fed to the meter via resistor R9. As this rectifier is included in the feedback loop the meter reading remains linear over the entire scale. Diode D5 is included to limit the current through the meter to a safe value, thereby reducing the risk



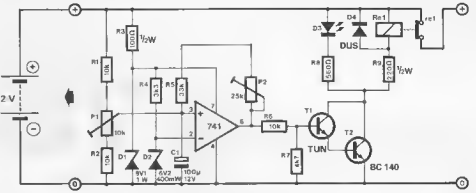
2

of damage if a 'loud' noise is measured on a 'quiet' range. Components C5, C6 and R7 are included to provide frequency compensation and to prevent instability.

Under normal operation the circuit will only draw about 2 mA, so it can be powered by two PP3 (or similer) betteries. The push-button switch S1 ensures that the circuit is not inadvertently left on. The meter should be calibrated in dBs and should have a full scale deflection of +10 (normal log scale).

P. Barnes (United Kingdom)

76 automatic battery charger



Automatic battery chargers are not particularly cheap, however the protection they afford against overcharging and possible battery damage is highly desirable. The circuit shown here is intended to provide an inexpensive alternative to the commercially available fully automatic chargers. The idea is to take a simple battery charger and incorporate an add-on unit which will automatically monitor the state of the battery and cut off the charge current at the desired point, i.e. when the battery is fully charged.

The circuit basically consists of a comparator, which monitors the battery voltage with respect to a fixed reference value. If the battery voltage exceeds a presettable maximum level, a relay is actuated which interrupts the charge current. If the battery voltage falls below a lower threshold value, the relay is released switching the charge current back in. The comparator is formed by a 741 op-amp. The supply voltage of the op-emp is stabilised by R3 and D1, and is thus unaffected by variations in the battery voltage. The reference voltage, which is fed to the inverting input of the op-amp, is derived from this stabilised supply via R4 and D2. The reference voltage is compared with e portion of the battery voltage, which is taken from the voltage divider, R1/P1/R2. As the battery voltage rises, et a certain point (determined by the setting of P1) the voltage on the non-inverting input of the op-amp will eventually exceed that on the inverting input, with the result that the output of the op-amp will swing high, turning on T1 and T2, pulling in the (normally-closed) contact of the relay and interrupting the charge current to the battery. LED D3 will then light up to indicate that the battery is fully charged.

To prevent the battery being reconnected to the charger at the slightest drop in battery voltage, a portion of the op-amp output voltage is fed back via P2 and R5 to the non-inverting input. The op-amp thus functions in a fashion similer to a Schmitt trigger, the degree of hysteresis, i.e. the battery voltage at which the op-amp output will go low again, being determined by P2.

The circuit is best calibrated by using a variable stabilised voltage as an 'artificial battery'. A voltage of 14.5 V is selected and P1 adjusted such that the relay just pulls in (opens). The 'battery' voltage is then reduced to 12.4 V and P2 adjusted until the relay drops out. Since P1 and P2 will influence one another, the procedure is best repeated several times.

A final tip: if the charge current is too large to be switched by the relay, the circuit can still be used by connecting the relay in the primary of the battery charger transformer.

H. Heere (The Netherlands)

5-minute chess clock

77

In games of speed chess, where each player has only 5 or 10 minutes to complete all his moves, mechanical chess clocks leave something to be desired in terms of accuracy, especially when both players have only 30 or 40 seconds left. The author of the circuit decribed here offers a solution to this problem by employing LEDs to provide an unequivocal display which counts off the time remaining in multiples of 10 seconds. The clock uses two counters, one for player A and one for player B. By bridging a set of touch contacts each player can stop his own counter and start his opponent's. The state of each counter is displayed on a circle of 30 LEDs (see figure 2). In a 5-minute game S1 is set to position 1, whereupon each LED lights up in turn for (300 seconds/30 =) 10 seconds. With S1 in position 2, the time limit is increased to 10 minutes per player, i.e. each LED lights up for 20 seconds.

If a player exceeds his time limit, then LED D40 (A) or D40' (B) lights up. The counters can be reset for the start of a new game by pressing S2. LEDs D35 and D36 provide a visual indication of who is to move.

Assuming player B has just made a move on the board, he presses TAP switch B, which takes the output of N1 (which together with N2 forms a set/reset flip-flop) high. The output of N2 goes low, causing counter A (IC2, IC3, IC4) to start counting the clock pulses provided by N3 and N4; counter B is inhibited until TAP switch A is touched. Since D31 is now reverse biased, D35 will be turned on and off via D32 at a rate

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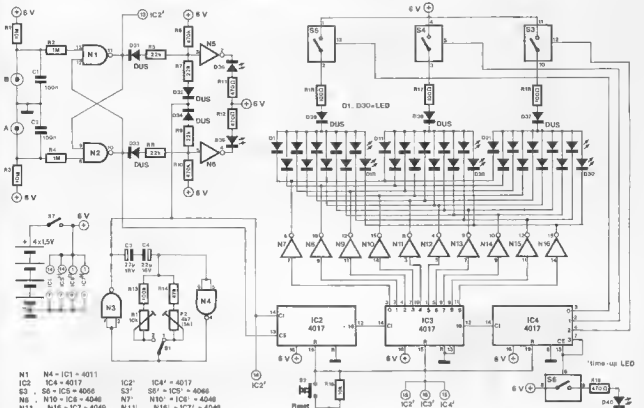

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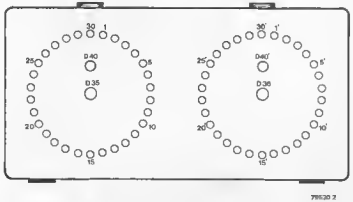


equel to the clock frequency. D33 is forward biased, pulling the input of N6 low, so that D36 will be extinguished.

The circuit can be powered by four 1.5 V batteries or by ni-cads. The current consumption is approximately 45 mA. P1 and P2 can be calibrated using a known accurate timebase; each LED should light up for 10 seconds with S1 in position 1 and twenty seconds with S1 in position 2.

S. Woydig (Germany)

78 emergency break

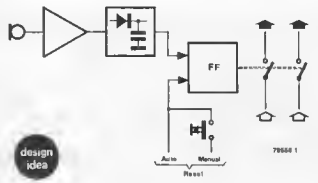
design idea

If one's stereo system is pumping out too many watts, then there is always the danger that either one's loudspeakers or relations with the neighbours will suffer as a result. One obvious solution is to turn back the volume control. However, Mr. Ziemssen has come up with a more drastic suggestion: disconnect the speakers automatically whenever the output signal exceeds a preset maximum level.

The basic principle of the circuit is illustrated by the block diagram of figure 1. The sound level is monitored by a microphone, the output of which is amplified and rectified, before being fed to a flip-flop which disconnects the speakers (or interrupts the audio signal path at some other point). A second flip-flop input is desirable to reset the circuit when the audio signal falls back to an acceptable level (and also to ensure it assumes the proper state on power-up). The author originally submitted a detailed circuit design (see figure 2), however it suffered from the disadvantage of falling to provide an automatic reset facility, and — rather uneconomically — used TTL. However the basic idea behind the circuit remains valid.

K. Ziemssen (Germany)

1



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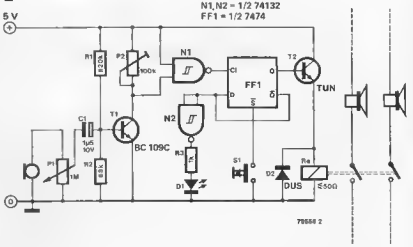
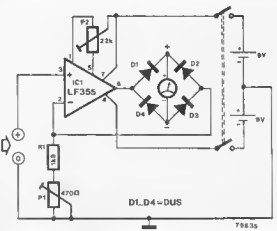


79 voltage trend meter

The advantages of a digital multimeter are sufficiently well known that they do not need to be repeated here. However there are situations where it is useful to determine whether the quantity being measured is increasing or decreasing, particularly if it is subject to sudden fluctations. An op-amp connected as an AC amplifier is particularly suited to this task.

Most simple DVMs contain an LSI chip with an input sensitivity of 200 mV and an extremely high input impedance. A suitable op-amp is the LF 355 used as a voltage-current converter, which has an input impedance of 10^{12} Ω.



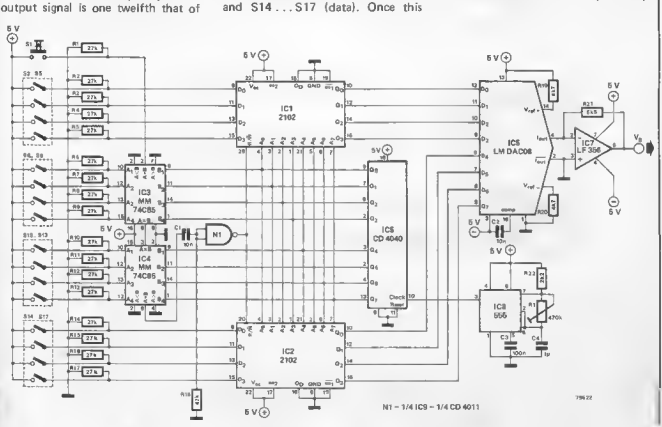
The circuit shown here is designed for an input voltage of 200 mV and a current through the moving coil meter of 100 μA. For other input voltage and/or output currents the trimmer potentiometer P1 and resistor R1 should be altered accordingly.
The op-amp requires two supply voltages (positive and negative) between 5 and 18 V. In view of the nominal current consumption of the circuit (several milliamps), these can easily be provided by two 9 V batteries.
The calibration procedure is quite straightforward. With the input short circuited, P2 is adjusted for a meter reading of zero volts. A 200 mV signal is then fed to the input, and P1 adjusted for the corresponding reading on the meter.
If the meter has a scale of e.g. 0 . . . 3/30, then by calibrating the moving coil meter to read '2' for a maximum reading (with e.g. 200 mV in) on the DVM, an 'overload' range up to 300 mV can be obtained. In the above case, with a constant current of 100 μA through the analogue meter, the value of R1 should be increased to 2k7.
The circuit functions in a similar fashion for both current and resistance measurements. The DVM is connected in parallel with the analogue meter.

H. Ehrlich (Germany)

programmable digital function generator 80

The circuit shown here will generate pre-programmable periodic waveforms. The waveform is stored digitally in two 256 x 4 bit RAMs which are connected in parallel to form a single 256 x 8 bit memory. The output waveform is obtained by repeatedly cycling through the contents of each of the 256 memory locations. The resulting digital signal is fed to a D/A converter and finally to a lowpass filter (not present in the circuit described here) to remove the clock frequency components. The address bus is clocked via an 8-bit binary counter by the clock oscillator IC8. The frequency of the output signal is one twelfth that of the clock frequency.
The circuit is programmed as follows: A single period of the desired waveform is divided into 256 discrete parts, each part having an address, starting with 00000000 and finishing with 11111111. The peak to peak amplitude of the waveform is also divided into 256 discrete levels, which are quantified digitally (00000000 for the lowest level and 11111111 for the highest level). Thus a list of addresses with corresponding data to be read into the RAMs is obtained. These addresses and data are set up on DIL switches S6 . . . S13 (addresses) and S2 . . . S5 and S14 . . . S17 (data). Once this has been done (open switch = 0), switch S1 is momentarily depressed, thereby enabling the digital comparators IC3 and IC4. As soon as the address generated by IC8 and IC5 corresponds to the address set up on S6 . . . S13, the output (pin 6) of IC4 goes high. The monostable formed by C1, R18 and N1 then produces a short write pulse on the R/$\overline{W}$ input of IC1 and IC2, causing the data set up on the data switches to be written into memory. The above procedure is then repeated for the remaining 255 memory locations.

C. Rohrbacher (France)

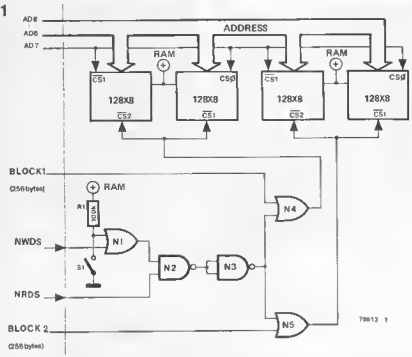


81 pseudo PROM

When developing programs for microcomputers a single mistake can have disastrous consequences. A particularly aggravating occurrence is when a section of program, which was considered to be safely tucked out of harm's way in a different part of RAM, has been inadvertently written over. The simple circuit shown here offers a handy solution to this problem, namely a Read Only switch for RAM. With the aid of this switch the Write signal is inhibited, so that data can only be read out of RAM.
With the circuit shown in figure 1 four 128 x 8 bit RAMS, i.e. two ¼ k blocks, are protected by the Read Only switch. Naturally the circuit can be extended to cover larger blocks of memory.
IF CMOS RAMs are used, then a further interesting possibility is to provide a battery back-up power supply. Since the power consumption of CMOS memories is so low, a normal 4,5 V battery would be sufficient to power the circuit for several days. A suitable battery buffer circuit is shown in figure 2. The state of the battery can be checked by means of switch S2; below a battery voltage of 3.9 V the LED will be completely extinguished. In actual fact CMOS ICs will work with supply voltages as low as 3 V, so the gradual loss of battery voltage should present no problems.
As well as eliminating the possibility of accidentally altering the contents of a section of RAM, the above circuit allows one to preserve a program or section of program for several hours or more without having to use a cassette dump routine.

J.F. Courteheuse and A. Monnier (France)

1



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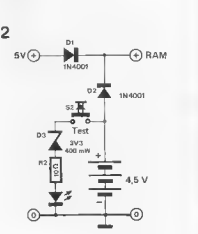
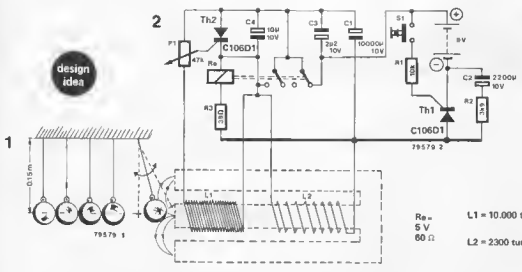


82 non-stop Newton's cradle

Most people will have seen the desktop ornament/toy known as a 'Newtons cradle' (see figure 1), which consists of usually five steel balls suspended in a row from a pair of threads. When one of the end balls is lifted and then released so that it falls back and strikes the next ball, the energy of the impact is transmitted through the other balls, with the result that the ball on the opposite end of the row swings up. It then in turn falls back, energy is again transmitted through the row, and the first ball swings up, and so on. The energy losses of the system are fairly high, and after a number of oscillations the balls are returned to rest. The idea behind the circuit described here, is to compensate for the natural energy losses of the system, so that it continues to oscillate indefinitely (i.e. until the circuit is disconnected or the batteries run out!).
If, for the moment we ignore the energy losses, the frequency at which the system oscillates will be:

$$f = \frac{1}{2\pi \cdot \sqrt{\frac{l}{g}}}$$

design idea

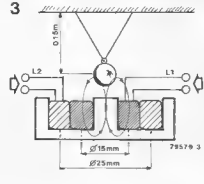


where l is the length of the thread and g is the force of gravity (9.81 m/s²). Thus with a length of 0.15 m, the fundamental frequency of the system will be approximately 1.3 Hz. In order to compensate for natural energy losses, the magnetic field system shown in figure 2 has been designed. Together with the accompanying circuit, the idea is that a magnetic force is applied to one of the end balls in the cradle. If the circuit is powered by 6 1.5 V cells (manganese-alkali), the cradle should continue to oscillate for roughly 5 days without interruption.

To set the circuit in operation, switch S1 should be pressed immediately before or after the end ball is set in motion, thereby triggering thyristor Th1 via resistor R1. Capacitor C1 then charges up, as does C4. As soon as a ball enters the field of the permanent magnet, a voltage is induced in coil L1, turning on thyristor Th2; the trigger point of the thyristor is determined by P1. The relay connected in the cathode of Th2 pulls in, so that current flows through coil L2, and an additional magnetic field is created which repels the ball. As soon as the ball leaves the magnetic field, the voltage induced in L1 collapses and Th2 is turned off. The process then repeats itself at the natural frequency of the system.

If the ball is stopped, no charge current will flow to C1, with the result that C2 will discharge. If the discharge current is smaller than the holding current of Th1, the latter turns off and circuit switches off. Figure 3 shows a cross-section of the coil and magnet system. L1 (10,000 turns of enamelled copper wire, 0.01 mm diameter, 1 k) and L2 (2300 turns enamelled copper wire, 0.4 mm diameter, 25 Ω) are wound on a permanent magnet core, and enclosed in transformer laminations. Any readily available alternative type of thyristor can be used.

3



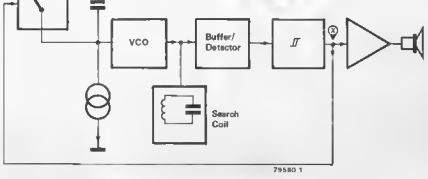
K. Bartkowiak (Germany)

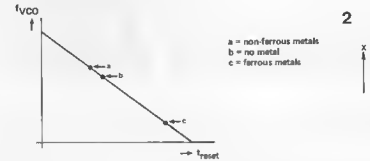
metal detector 83

Most metal detectors suffer from one sort of drawback or another, perhaps the most serious being the tendency of the oscillator frequency to drift. For this reason the author has sought an entirely new approach, the basic principle of which is described here. A capacitor, C, is charged by a current source, so that the frequency of a VCO is varied by a linearly decreasing voltage. The search coil of the detector (LC tuned circuit) is connected to the output of the VCO. As the frequency of the VCO signal approaches the resonant frequency of the coil, the output voltage of the buffer/detector increases, until, at the resonant frequency itself, it

1

design idea

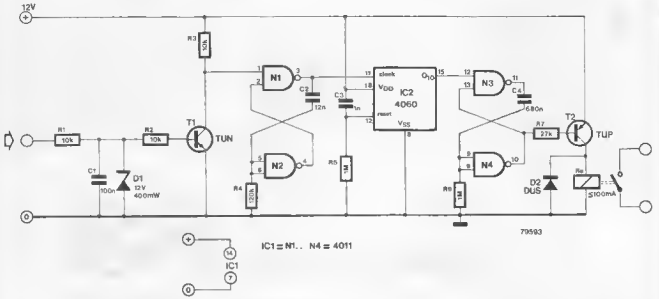




axceads the threshold level of the Schmitt trigger. This causes the switch (e.g. a thyristor) to close, thereby discharging C, and e new cycla begins.
Figure 2 shows the relationship between the reset time and the resonant frequency. When the search coil is held near metel objects the inductance of the coil, end with it the resonant frequency of the tuned circuit, is varied.
The output signal of the Schmitt trigger is amplified and fed to a loudspeaker to provide an audible indication of the circuit heving 'detected' something.

M. Kimberley-Jennings
(United Kingdom)

84 varispeed windscreen wiper delay circuit



In most windscreen wiper delay circuits the wiper speed is independent of the speed of the car. However the faster the car trevels, the more rain falls on the windscreen, therefore, ideally, the shortar the delay should be. A variable delay circuit could be controlled by a sensor mountad in the spaedometer cable. However this approach would be fairly complicated. The simpler solution adopted hare, is to derive the control signals from the contact breaker, so that the wiper speed is varied in accordance with the engine speed.
The input of the circuit is connected to the contact breaker; when the contacts open, the full battery voltage appears across the input, with the result that T1 provides a short output pulse. The resultant pulse stream is used to trigger the monostable multivibrator formed by N1 and N2. The frequency of the multivibrator is then divided by ten by the counter, IC2. The output of the counter is fed to a second monostable, N3/N4, which provides an output pulsa duration of approximately 0.5 s. Depending upon the speed of the engine, the time between successive pulses will be between roughly 10 and 40 seconds. Thus trensistor T2 is regularly turned on for a short period, causing the wiper relay to pull in and the wipers to perform a single sweep.
By arranging for a capacitor of roughly 2.2 μF to be switched in parallal with C4, tha wipers can be mede to perform a double sweep evary cycle.
The zener diode D1 is included to protect the circuit from excessively large surge voltages appearing across the contact breakers, whilst diode D2 protects T2 against the back EMF induced by the relay. Prefarably, the holding current of the relay should not exceed 100 mA; if that is the case, however, a transistor with a higher output currant capability should be used.

D. Laues **(Germany)**

IR lock 85

The following circuit is intended as an infra-rad lock for house doors, garaga doors, atc. Sinca the 'key' is almost impossible to copy, it should provide an affectiva obstacla to unwanted visitors.

Figure 1 shows the infra red transmittar. An astable multivibrator, formed by NAND gates N1 . . . N3, drives an output transistor, T1, which turns the infra-red emitter diode on and off at a frequency which can be varied by means of P1.

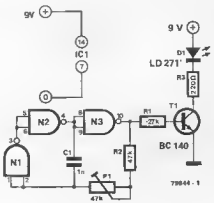
The receiver circuit is shown in figure 2. Light pulses received by the phototransistor T1 are amplified by IC1 and fed to an LC circuit tuned to roughly 23 kHz. The filtered output signal is rectified by D1 and fed to op-amp IC2, which is connected as a Schmitt trigger. The trigger threshold is set by zener diode D4 to 2.4 V. The unfiltered output of IC1 is also fed to a second Schmitt trigger, (IC3). The output of this op-amp (point 1) will remain high as long as the voltage level at its input is 2.4 volts or greater regardless of the frequency of the received signal.

Assuming point 1 is high, a positive going edge at the output of IC2 (point 2) will 'turn the lock' as follows: when point 2 goes high, the output of N1 also goes high, and with it the input of monostable multivibrator MMV1. However, since this monostable is triggered by a negative going edge, tha output state of the monostabla remains unchanged, i.e. the Q output remains low. The positive going edge at point 2 is also transferred to tha trigger input of MMV2, which since it is triggered by positive going pulses, turns on the Darlington pair T3/T4 and pulls in the ralay. Thus for the pulse duration of MMV2 the lock is 'opened'.

If the modulation frequency of the transmitter signal deviates from 23 kHz, only point 1 will be high; point 2 will go low, with the result that, via N1, tha negativa going edge will trigger MMV1. Thus for tha pulse duration of MMV1 -- which is several minutes -- MMV2 cannot be triggerad. Evan if the modulation frequency is subsequantly corrected, since one input of N5 is held low, tha lock cannot be opened durlng this period. If a flip-flop is used in placa of a relay, the circuit could, for exampla, be used to switch a car alarm system on and off.

H.J. Urban **(Germany)**

1



N1 ... N3 = 3/4 IC1 = 4011

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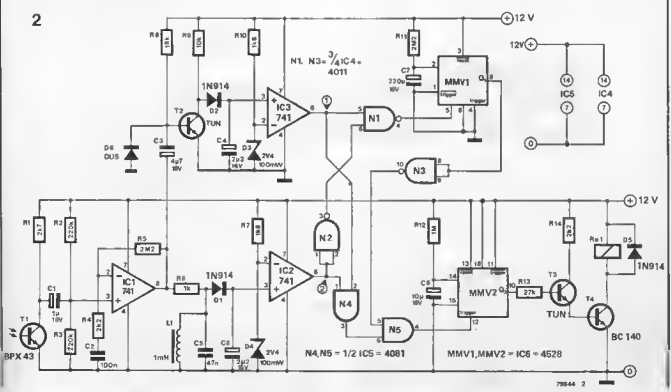
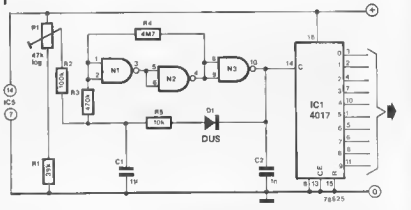


86 sequencer

The following design for a sequencer, which will generate a 10 note analogue waveform, is distinguished by its relative simplicity. To control a synthesiser two types of signal are required: a gate pulse to trigger the envelope shaper (ADSR), and a control voltage for the voltage controlled oscillators (VCOs).
The VCO voltages are generated as follows. An oscillator, formed by N1, N2 and N3, clocks a decade counter (IC1). Each output of the counter is connected to an analogue switch (as shown in figure 2), the input voltage of which can be varied by means of a potentiometer. The outputs of all the switches are joined together, so that an analogue waveform, composed of 10 discrete voltage levels, is generated at this point. The frequency of the resultant signal can be varied by means of P1.
The gate signal for the ADSR is derived from the clock signal, however since each synthesiser places different demands on the type of gate pulse required, no circuit is given.
Readers may wish to experiment with extending the circuit. One possibility is to include a monostable multivibrator (at the clock input of IC1), which allows one to cycle through the analogue waveform step by step. Each of the preset voltage levels on the inputs of S1 . . . S10 are then compared with a reference voltage. If a shorter cycle (i.e. less than 10 steps) is required, the appropriate output of IC1 should be connected to the reset input (pin 15).

J.C.J. Smeets (The Netherlands)

1



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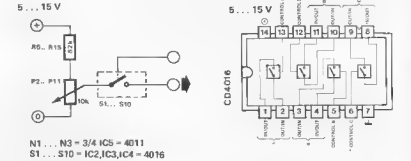
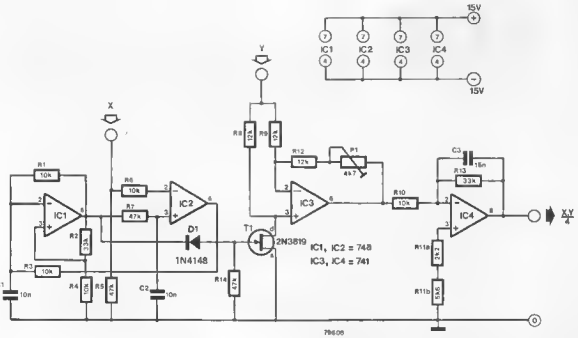


87 four quadrant multiplier

Multiply X and Y and you get XY – all very simple and straightforward – at least on paper. But what if X and Y are analogue voltages, which may be of either polarity? How does one go about multiplying two such quantities? The following circuit for a 'four quadrant multiplier' – a circuit which will multiply two input voltages and ensure the product is of the correct polarity – shows one way of approaching this problem.
Basically the circuit generates a squarewave signal, whose duty-cycle is proportional to one of the input signals and whose amplitude is proportional to the other. The average value of the squarewave, and hence the value of the product voltage, is obtained by lowpass filtering.
The squarewave generator is formed by IC1, R1, R2, R4 and C1. The output of IC1 is lowpass filtered by R7 and C2, then compared with the input voltage, X. The duty cycle of the squarewave is modulated via the output of IC2, R3 and C1, whilst the amplitude of the output signal of IC1 is held constant. The output of IC1 is also used to control the FET switch, T1. When this switch is 'closed' i.e. T1 is turned on, a voltage equal to –Y is present at the output of IC3; assuming P1 is correctly adjusted, this op-amp then functions as an inverting amplifier. If T1 is turned off, i.e. the switch is 'open', IC3 is connected as a non-inverting amplifier. Thus at the output of IC3 will be a squarewave voltage with an amplitude which is proportional to Y, a duty-cycle proportional to X, and whose average value is proportional to XY. The latter is obtained by the lowpass filter formed by IC4, R10, R13 and C3. The turnover frequency of this filter is approximately 330 Hz. The circuit will quite happily multiply analogue signals with frequencies which are an order of magnitude lower than the turnover point



of the two lowpass filters. The author has used the circuit for correlation measurements on very low frequency EEG signals.
The adjustment of P1 is necessary since, when conducting, T1 has a significant resistance. With an input voltage X = 0 (input grounded) and Y = + 6 or − 6 V, P1 should be adjusted for minimum output voltage of IC4 (roughly ± 40 mV).

P. Creighton (United Kingdom)

simple synthesising of PPM's by using LED's

88

Circuits for synthesising peak programme meters by using light emitting diodes are certainly not new, but the design shown here offers simplicity and flexibility and is especially suited for multi-channel equipment.
As can be seen from the block diagram in figure 1 the circuit consists of a master section and one or more channels. The master section provides a logarithmic voltage reference for the analogue bus (A) together with the timing circuitry for multiplexing the display. The circuit for each channel consists of a full-wave rectifier and a comparator which enables the display. The circuit for the master section is shown in figure 2. A clock oscillator is formed by N1/N2 which should be adjusted to approximately 50 kHz by P1. The oscillator is buffered by N3 which drives a binary (up/)down-counter IC1. The output of the binary counter is decoded by IC2 to form the digital system bus (B). Pin 1 of IC2 is used to drive an analogue switch to charge up capacitor C2. During the count from 15 to 1 the switch is off and C2 is discharged

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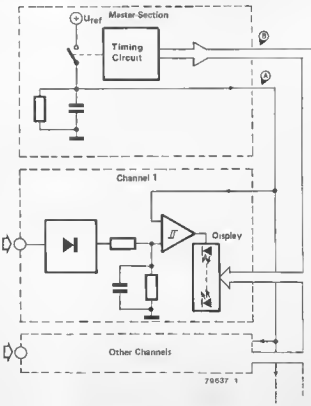
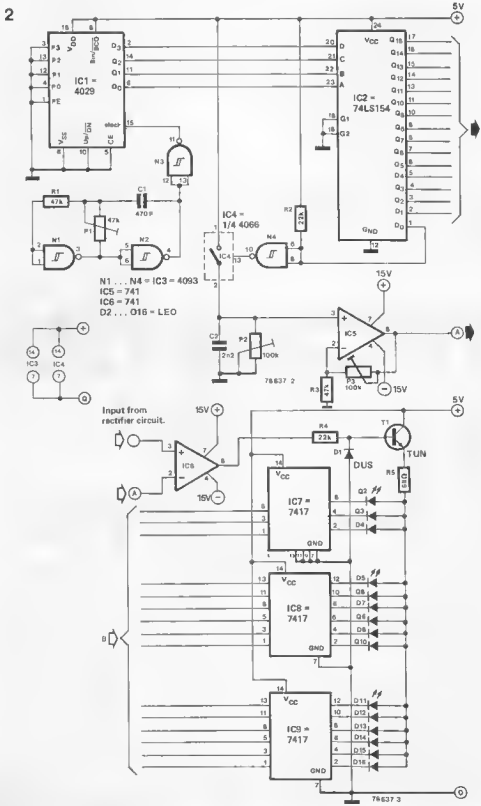
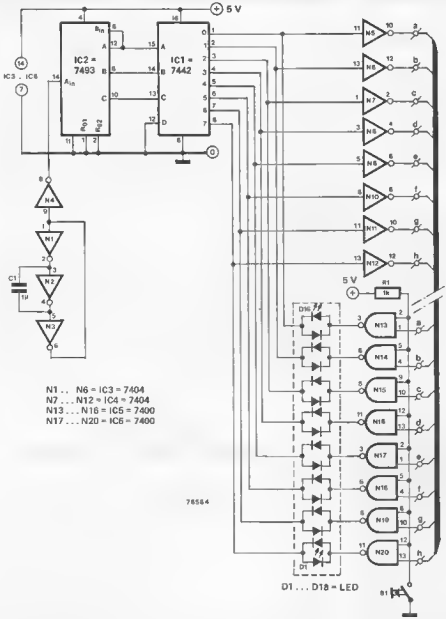


through the preset potentiometer P2. This decaying voltage is then amplified and buffered by IC5 and fed to the analogue bus.
The rectifier section of this PPM synthesiser is not shown here, but readers are referred to Elektor 24 (April 1977) for a suitable circuit. Once rectified the input signal is compared with the voltage on the analogue bus by IC6 as shown in figure 3. When these two voltages are the same the output of IC6 will go high turning on transistor T1 thereby enabling the data on the digital bus to be displayed on the LED's via buffers IC7 . . . IC9.
The unit is calibrated by applying 12 V DC to the rectifier input and adjusting P3 until all the LED's are just turned on. The input voltage is then altered to 0.48 V and P2 is adjusted until only one LED is on. The unit is then ready for use. The master section as shown is capable of driving up to five channels, but if more are required then the buses will have to be buffered accordingly.

J. Andersen (Denmark)



ribbon cable tester 89



For microcomputer enthusiasts and anyone working with large scale digital circuits, a ribbon cable tester can prove a useful aid.

The circuit described here will simultaneously test 8 cores, with the facility for extending this to 16. A clock oscillator (N1 . . . N3) drives a 4-bit counter (IC2). Three of the counter's outputs are used to clock a BCD-decimal decoder (IC1). The outputs of the decoder each go low in turn for the duration of a certain clock period. The outputs are connected via inverters N5 . . . N12 to a set of terminals, to which one end of the ribbon cable is attached. The other end of the cable is connected to the inputs of gates N13 . . . N20. Between the outputs of these gates and the outputs of IC1 8 pairs of reverse-parallel connected LEDs (D1 . . . D16) are inserted.

The odd-numbered LEDs will light up only if the corresponding NAND output is low and the corresponding output of IC1 is high (87½% of the time). The even-numbered LEDs on the other hand, will light up only if the NAND outputs are high and the outputs of IC1 are low (12½% of the time).

If there is a break in one of the cores, the corresponding NAND output will be low and the associated LED will light up. If the core is intact, then the LED will be extinguished, since the logic levels on either side of the LED change state simultaneously.

The circuit will also check for shorts between cores, since in that case the anode of an even-numbered LED will be high, whilst the cathode will be low, causing the LED to light up. Note that series resistors for the LEDs are not necessary (see 'driving LEDs from TTL, circuit 72, Summer Circuits issue 1978). If no cable is connected, the odd-numbered LEDs will light up. Switch S2 functions as a lamp test for the even-numbered LEDs.

For a 16-core version of the circuit a 74154 should be used in place of IC1 (the D-input is of course used), whilst the number of inverters, NAND gates and LEDs is doubled.

J.J. van der Weele
(United Kingdom)

90 µP-programmable speed controller for model railways

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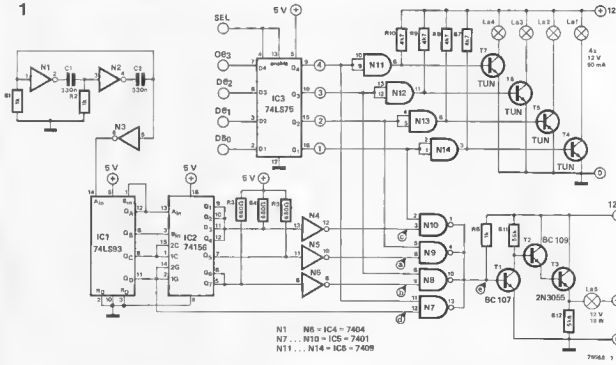

In the world of model railways, electronics is playing an increasingly important role, and it is only a matter of time before the microprocessor becomes a standard component in any large layout. The design described here brings this prospect nearer to becoming a reality. With the aid of the following circuit a µP can be used to automatically control the speed of a train. The speed of the train is controlled by varying the pulse width of the squarewave supply voltage of the motor. The squarewave signal is generated by the oscillator N1/N2, and fed to a 4-bit binery counter. The counter outputs are in turn fed to a 1-of-8 decoder. The decoder outputs are connected together such that at points a . . . d there are four squarewave signals, whose pulse widths are in the ratio 1 : 2 : 4 : 8 respectively (see figure 2). By combining one or more of these waveforms a choice of 16 different duty cycles (0, 1, 2, 1+2, 4, 1+4, etc.) can be obtained.

Which duty cycle is selected is determined by NAND gates N7 . . . N10; the output state of these gates is in turn determined by the information present on the data bus (DB0 . . . DB3) of the microprocessor system. Between the µP data bus and

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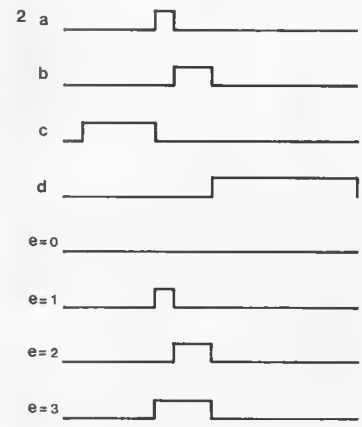

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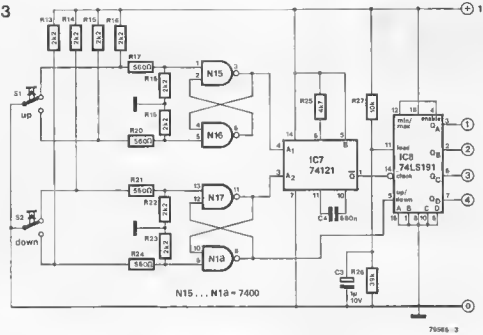
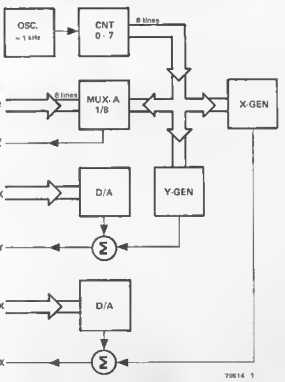


the NAND gates is a 4-bit latch (IC3). Information is only transferred from the data bus to the gates when a select pulse is received.
The waveform selected by the μP is amplified by T1/T2/T3. Lamp L5 protects the circuit from excessive current in the event of a short on the track, whilst lamps La1 . . . La4 indicate the speed of the train in binary code.
If a μP system is not available, the 'manually-operated' processor circuit shown in figure 3 can be used instead. The circuit performs the same basic function as a μP, with the exception that the 'brainwork' is done by the hobbyist himself. By pressing either S1 or S2 the speed of the train can be increased or reduced in single steps. If the circuit of figure 3 is used, then IC3 in figure 1 can of course be omitted.

W. Pussel (Germany)

7-segment displays on a scope 91

1



With the aid of the following circuit a seven-segment display can be generated on an oscilloscope screen. The height and width of the digits can be independently varied, and a decimal point can be provided on either side of the display.
As is apparent from the block diagram of figure 1, the circuit comprises the following sections:

- an oscillator which clocks an 8-output ring counter.
- a multiplexer which switches the 7-segment signal to the Z or $\overline{Z}$ input of the scope
- X and Y signal generators which are controlled by the output of the ring counter.
- two D/A converters which translate the digital codes representing the X and Y deflection of the scope beam into analogue values.

The X and Y deflection signals shown in figure 2 are derived via capacitors C1 and C2 in the circuit diagram of figure 3. The voltage across these capacitors is controlled via MOS switches S1/S3 and S2/S4 by the outputs of N1 . . . N4. The

emplitude of the deflection signal is largely determined by the clock frequency. T3 and T4 are connected as source followers and function as buffers.

IC1 decodes the pattern of enebled segments. The deflection signal shown as a dotted line in figure 2 (period 7) returns the spot to its original position. This pulse is used to generate the decimal point by connecting output 7 of IC1 to, on the one hand S5 and S8, and on the other hand, via an inverter formed by T2, to S6 and S7. The position of the spot is determined by the offset voltage which is adjusted by means of trimmer potantiometers R7 and R15.

The D/A converted code for the position of the display is fed to the X and Y position inputs. Tha setting of trimmer potentiometers R6 and R14 determines the gap between digits.

As far as the D/A converter is concerned its construction will depend upon, for exampla, whether the digitised display signals are coded in binary or in decimel, are inverted or normal. If tha Y-POS input is not required, R14 can be omitted and S7/S8 connection can be used as an output. The clock frequency end multiplex fraquency should not hava a common division ratio.

The multiplexer section of the circuit is formed by switches S9 . . . S16. In contrast to AND/OR gates, these permit a decoder with either 'active-low' or 'active-high' outputs to be used. In the case of IC1, tha outputs ara active-high; if the reverse is tha case, R1 should be connected to ground; the output signals will then be inverted.

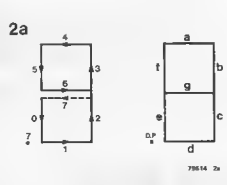
The reset signal for IC1 can be used as a clock signel for an internal multiplexer (if the MPX input is not desired), or to scen the addresses of a memory. A 1-bit shift register is required for leading zero blanking via the RBO pins of the BCD-7-segment decoder.

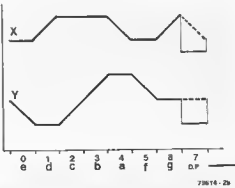
Among other things, the circuit can be employed to display the position of the calibration mark of wobbulators and frequency analysers.

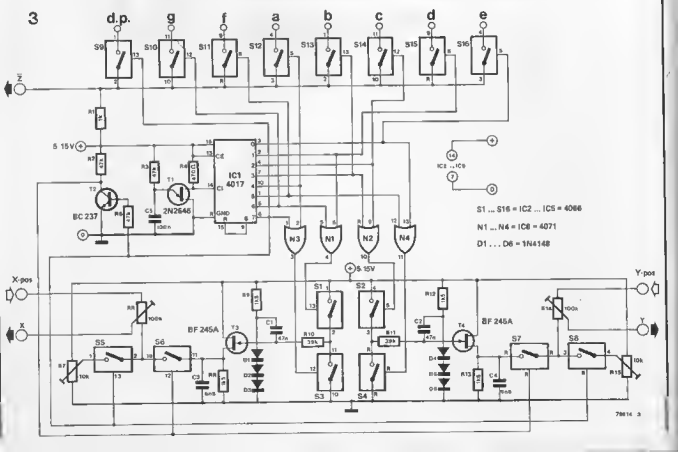
The supply voltage can be anywhera between 5 and 15 V. The emplitude of the output signals et S5/S6 and S7/S8 is approximately 1 V. The load impedanca for R6 and R14 should be 1 MΩ.

In order that the edges of tha switching signal cannot ba detected, any amplifier connected to the output must have a high slew rate.

F. Kasparec (Austria)







pH meter circuit for DVM 92

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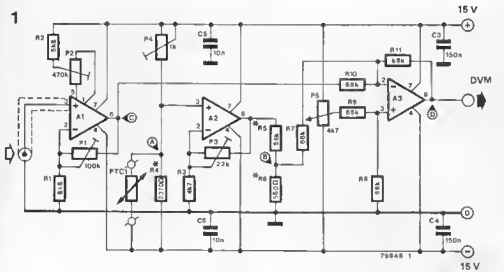

To accurately measure the concentration of hydrogen ions (pH value) in a solution, a 'glass electrode' is often used in chemistry laboratories. The electrode is constructed on the principle of a galvanic cell, and the output voltage of the electrode is proportional to the pH value of the solution to be measured. The temperature of the solution considerably affects the pH value, thus a pH meter is effectively a temperature compensated millivoltmeter.

The circuit shown employs an op-amp (A1) to amplify the output voltage of the electrode. The input impedance of the circuit is thus equal to that of the op-amp, which is $10^{12}\ \Omega$, so that there is negligible loading of the electrode. The positive temperature coefficient (PTC) resistor TSP 102 (Texas) compensates for the effect of variations in the temperature of the solution. Together with the shunt resistor of exactly 2370 Ω, which should be made up of several metal film resistors (e.g. 2k2 + 150 Ω + 10 Ω + 10 Ω), the resistance of the PTC varies linearly with temperature.

The voltage at point A is amplified by op-amp A2, the output of which is divided by R5/R6 such that it varies the total output voltage by just the right amount. Op-amp A3 is connected as a combined summing and differential amplifier and provides the output voltage for the DVM, which displays the pH value of the solution directly. Trimmer potentiometers P1 and P3 set the gain of the input stage while P2 ensures that A1 is correctly biased.

The calibration procedure for the circuit is as follows:

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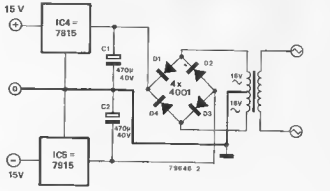

1. With the inputs short-circuited P2 is adjusted for zero volts at point C.
2. Again with the inputs shorted, potentiometer P5 (wirewound type) is adjusted such that 7 volts are present at point D.
3. Trimmer potentiometer P4 (spindle type) is adjusted such that, with the PTC at a temperature of 25° C, zero volts are present at point A.
4. A glass electrode, which is suspended in a solution with a pH of 7, is connected to the input of the circuit. P5 is then adjusted until a reading of 7 volts is obtained at point D (note that the temperature of the solution should be 25° C)
5. The glass electrode is suspended in a solution with a pH value of 4 and trimmer P4 (spindle type) is adjusted for a reading of 4 volts at point D. Once again the temperature of the solution must be 25° C.
6. Heat the solution to approximately 70° C, and with the PTC suspended in the solution check to see that a reading of 4 volts is still obtained. If necessary, readjust P3.
7. Repeat the above procedure from point 3 onwards.

The high input impedance of the circuit renders it sensitive to r.f. pick-up, hum etc, and it should therefore be well-screened, preferably by mounting it in a metal case. The connections to the PTC must be water, acid and alkali proof.

The accuracy of the circuit depends upon a stable supply voltage (± 15 V), and upon the accuracy of the reference solution used during calibration (not to mention the accuracy of the DVM).

Glass electrodes are available commercially, and are supplied with instructions on how they should be used.

Th. Rumbach (Germany)

93 robot with reflexes

This robot is an example of a simple cybernetic model, i.e. it will take whatever manoeuvres necessary to navigate its way around any obstacles placed in its path. The robot will continue to travel in a straight line until it bumps into an obstruction of some sort, it then changes direction to avoid the object in its way; if it becomes completely stuck, all the drive motors are switched off.
The sensors used to detect obstacles

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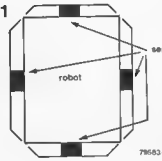

take the form of switches. During construction care should be taken to ensure that these react to contact over the entire length of each side, hence some sort of bumper arrangement such as that shown in figure 1 should be adopted.
When an impact occurs, the switches detect on which side it is, and the information is fed as a four-bit code to a latch (IC3). The outputs of the latch trigger a 555 timer (IC2). For

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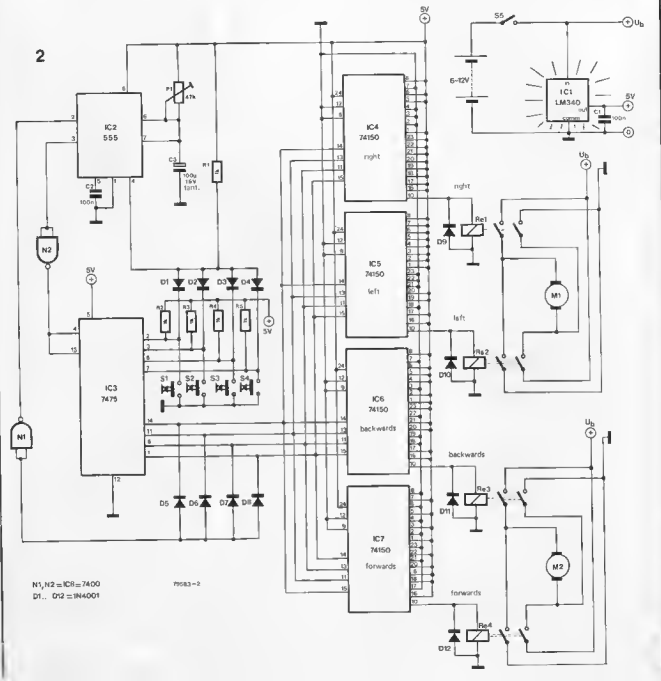


the period of the delay provided by the timer, this code is stored on the latch outputs, thus giving the robot time to take evasive action. The 4-bit code serves as an address for the four data-selectors (IC4 . . . IC7), which function as a look-up memory. The address information determines which of the data-selector outputs are enabled, and hence which of the four relays are pulled in. If a second collision occurs during the timer period, the latter is reset and a new code is fed to the latch. Once the timer delay has elapsed, the latch outputs go to 0000 and the robot continues on its way. The accompanying table lists the various evasive manoeuvres the robot takes for each of the latch codes.

Potentiometer P1 should be adjusted such that the robot has sufficient time to just clear the obstruction. With 0000 on the outputs of the data-selectors both motors are stopped. If desired one can arrange for this state to be detected and an alarm to sound.

Table.

latch outputs				data-selector outputs				
right	left	back-wards	for-wards	right	left	back-wards	for-wards	Direction
0	0	0	0	0	0	0	1	forwards
0	0	0	1	1	0	1	0	backwards and to the right
0	0	1	0	0	0	0	1	forwards
0	0	1	1	0	0	0	0	stop
0	1	0	0	1	0	0	1	forwards and to the right
0	1	0	1	1	0	1	0	backwards and to the right
0	1	1	0	1	0	0	1	forwards and to the right
0	1	1	1	0	0	0	0	stop
1	0	0	0	0	1	0	1	forwards and to the left
1	0	0	1	0	1	1	0	backwards and to the left
1	0	1	0	0	1	0	1	forwards and to the left
1	0	1	1	0	0	0	0	stop
1	1	0	0	0	0	1	0	backwards
1	1	0	1	0	1	1	0	backwards and to the left
1	1	1	0	0	0	0	1	forwards
1	1	1	1	0	0	0	0	stop

M. Blencowe (United Kingdom)

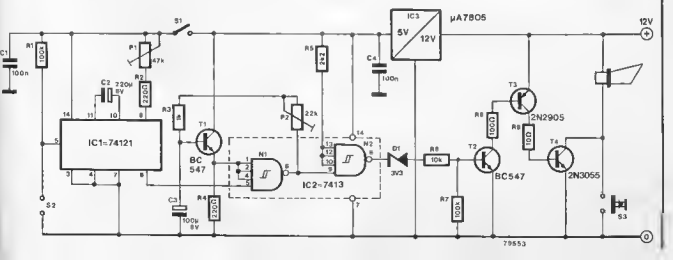
94 car collision alarm

With the overcrowding that is a common feature of most car parks nowadays, the chances of coming back to one's car and finding a dent in the bumper or one of the wings are quite considerable. It is particularly galling if the culprit has made off without acknowledging his guilt and leaving behind his name and address. The following circuit is designed to attract the attention of passers-by in the event of someone bumping into your car. Hopefully the guilty party will then be unable to escape in anonymity, and will be compelled to own up to his mistake.

First of all a suitable sensor, which will detect an impact to the car, must be constructed. One idea is to suspend a small weight from a spring inside a tin or jar lined with a conductive material (e.g. silver paper). Normally the weight and the tin will be isolated from one another, but if the car is subjected to a reasonably violent impact, the two will touch. The sensitivity of the sensor can be adjusted by shortening or lengthening the spring. One word of warning: if it is made too sensitive, it may react to severe gusts of wind!

The circuit of the alarm is shown in figure 1. The sensor is mounted in place of S2. As soon as the two contacts are shorted, and assuming S1 is closed, the monostable multivibrator, IC1, is triggered, with the result that its output goes high. The period of the monostable can be varied between 0.5 and 10 seconds by means of P1. As long as the output of the monostable remains high it will enable the oscillator built around N1, T1 and associated components. The oscillator frequency can be adjusted by means of preset potentiometer P2. The output of the oscillator is fed via N2 to the amplifier section built around T2 . . . T4 and hence to the outside world via the car horn: T4 is connected in parallel with the existing horn button (S3). Note that in some cars the horn is only operative when the ignition is turned on. In that case, the supply connection to the horn will have to be modified — it must be transferred to a (fused) connection that is always 'on'.

M. Haest (Belgium)



95 aircraft sound and 'hijack' effects generator

The circuit described here was designed to fulfill the need for a jet airliner sound effects generator in a school play which involved an attempted hijack. The unit had to be capable of producing a number of typical jet noises as heard from the insida of the aircraft – start-up, idle, take-off, in-flight, approach, landing and raverse thrust conditions – together with tyre squeal on landing and machine-gun fire.

To simulate the sound of a jet engine both the roar from the 'hot end' of the engine and the whistle from the compressor (whose pitch varies with engine speed) are required. The engine roar is obtained by feeding white noise through a band pass filter which emphasises frequencies around 800 Hz. Transistor T1 and the zener diode D1 form the white noise generator whose output is fed to IC1, the band pass filter. The volume of the roar can be altered by potentiometer P1.

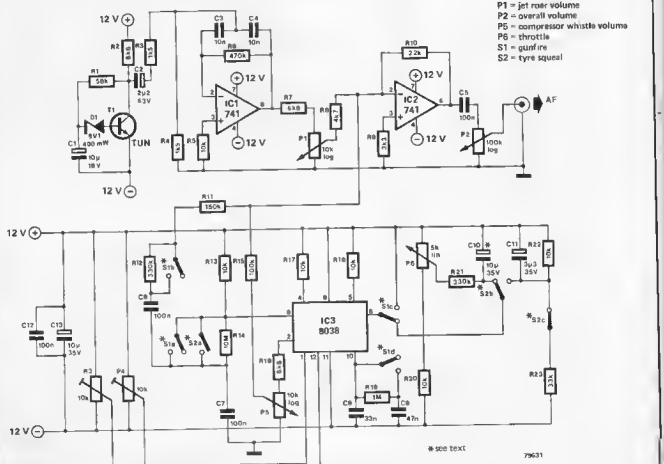
The whistle is derived from the sine-wave output of the 8038 waveform generator IC3 whose frequency range is set by C8 and is typically between 10 Hz and 10 kHz. Tha actual frequency is determined by the throttle control P6 which is connected to the FM input of IC3 via switches S1c and S2b, while the whistle volume is controlled by potentiometar P5. Engina inertia (lag in response to throttle demands) is realistically imitated by the integrating network R21/C10. C10 should be a low-leakage type – if available, a 10 μ paper capacitor would be a good choice.

Both these signals, the engine roar and compressor whistle, are then summed by IC2 and passed to the external amplifier through the overall volume control P2. By varying the settings of these controls all of the above mentioned jet engine sounds can be realised. The purity of the sinewave signal can be adjusted by potentiometers P3 and P4.

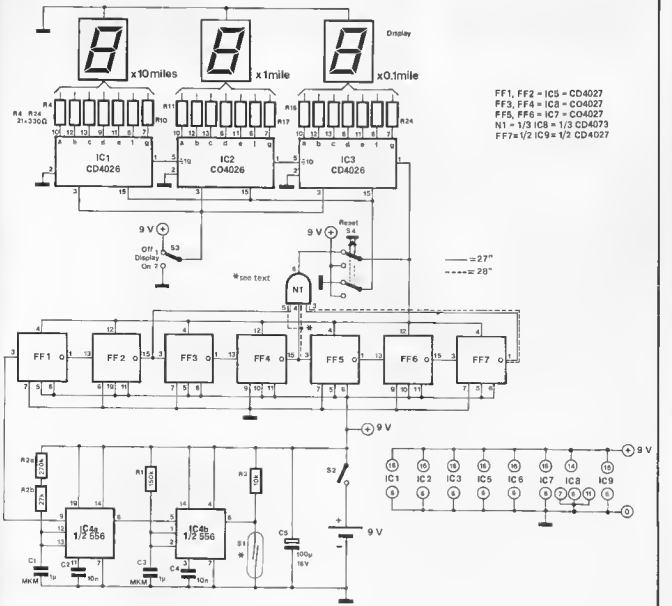
The gunfire effect is obtained from the squarewave output of IC3 when switch S1 is closed. By closing this switch the squarewave is allowed to pass through to the summing amplifier and the FM input of IC3 is taken high to give minimum frequency whilst the frequency range itself is also decreased by the addition of C9 in parallel with C8. Resistor R19 is included so that C9 is always kept charged to the average voltage across C8 to prevent a 'chirp' when S1 is first closed.

The tyre sqeal effect is also obtained from the squarewava output of IC3. When switch S2 is closed the squarewave is enabled, and the FM input of IC3 is initially taken to a potential which gives a high frequency output via the potential divider R22/R23, but as R23 is now disconnected capacitor C11 will discharge to the positive supply rail and the frequency of the squarewave output will fall rapidly.

M. J. Walmsley (United Kingdom)



digital milometer 96



Mechanical mileage recorders for bicycles have been commonly available for a large number of years, however there are several advantages to be gained from adopting an electronic approach: robustness, improved readability thanks to a digital readout, and 'friction-free' operation.

The distance travelled is measured by counting the number of wheel revolutions. Each complete revolution is sensed by means of a small magnet attached to one of the spokes. The magnet actuates a reed switch mounted at the appropriate height on the front forks of the bicycle.

In the circuit diagram the reed switch is represented by S1. Each time the magnet passes the switch, the latter closes momentarily, triggering the two 555 timers (IC4a, IC4b) and providing a pulse to the divider formed by FF1 . . . FF7 and N1. The output of N1 in turn produces a pulse every tenth of a mile. These pulses are fed to the three decade counters/decoders IC1 . . . IC3 which are connected in cascade. The maximum count is therefore 99.9 miles.

With a 27" wheel, a pulse every tenth of a mile corresponds to 74 revolutions (connections to N1 shown as unbroken lines), whilst in the case of a 28" wheel 72 revolutions (dotted connections to N1) are required.

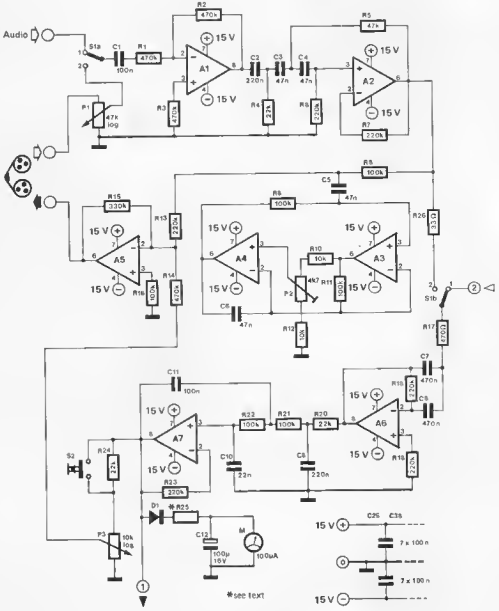
The current consumption of the circuit is 130 mA with the displays enabled (S3 in position 1) and 30 mA with the displays switched off (S2 in position 1). A 9 V battery (6 x 1.5 V) will provide a suitable power supply. Alternatively one could consider using ni-cad cells which are recharged via the dynamo. Of course the circuit no longer functions 'friction-free' in that case.

R. Kuijer (The Netherlands)

97 tape-slide synchroniser

Slide shows can be improved greatly by providing them with accompanying music and spoken comment from a tape. One way of changing the slides automatically at the correct moments is to record trigger pulses on an additional track on the tape. However, that requires an additional tape head (unless you make do with mono sound), which can prove rather complicated. The circuit described here uses 30 Hz pulses, recorded on the normal sound track — simplifying matters considerably. The circuit works as follows. During

1a



A1 ... A7 = IC4 ... IC10 = 741
N1,N2 = IC11 = 7413
N3,N4,N6,N12 = IC12 = 7400
N7,N8,N10,N11 = IC13 = 7400
N13,N14 = IC14 = 4001
N5,N9,N15,N16 = IC15 = 7402

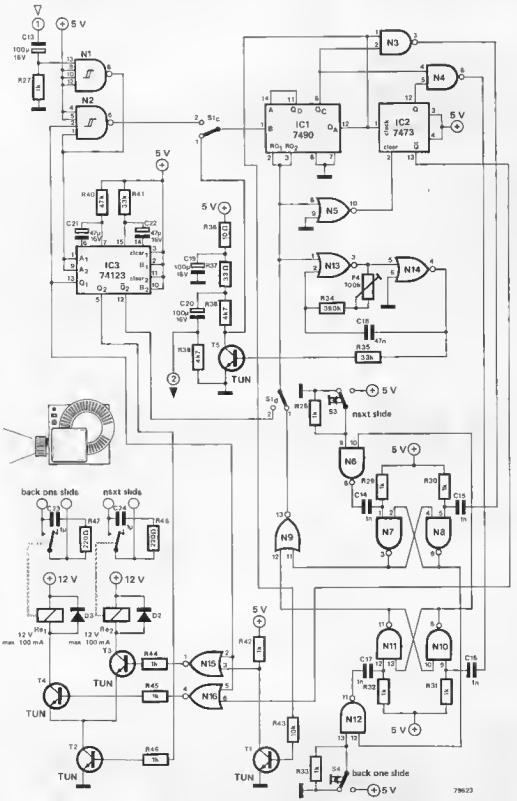
79023

recording, S1 is switched to position 1. The music and speech signal is fed through a buffer stage (A1), a 30 Hz high-pass filter (A2), a 30 Hz notch filter (A3, A4) and a summer (A5) to the tape recorder input. A 30 Hz oscillator (N13/N14) is enabled by operating either S3 (next slide) or S4 (back one slide). S3 triggers a flip-flop (N7/N8), starting the oscillator and enabling the counter (IC1); the oscillator pulses are fed through T5 to this counter. After 7 pulses, IC1 resets the flip-flop.

Operating S4 produces the same result, with one difference: in this case the flip-flop (N10/N11) is reset after 12 pulses have been counted. The pulses are passed through a band-pass filter (A6) and a low-pass filter (A7) to the summer (A5). During playback (S1 in position 2), the 30 Hz burst is filtered out and 'squared up' by N1 and N2. Each pulse triggers an MMV (IC3) that enables counter IC1 for 500 ms. During this period, the 30 Hz pulses are counted and Re1 or Re2 pulls in — depending on the final count. A second MMV (the second half of IC3) causes the relay to drop out again after 200 ms.

The calibration procedure is as follows. S1 is switched to position 1 (record) and the oscillator frequency is adjusted (with P4) for maximum output from A7. (Note that the oscillator will run continuously if S3 and S4 are both held down.) Turn P3 right down, make a temporary link from the output of A7 to the audio input (S1a), and adjust P2 for

1b

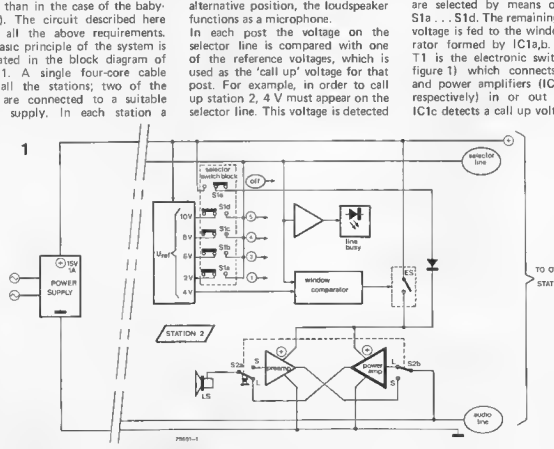


minimum output from A5. A suitable value for R25 should now be selected, so that the meter (M1) reads approximately ¾ scale; the exact indication can be marked on the scale.
Connect the tape recorder, and set the correct recording level for the normal audio signal. Disconnect the 'normal' audio, depress S2, S3 and S4 and adjust P3 for 'full modulation' (sometimes indicated as '0 dB'). Release S2 and record a short 30 Hz 'reference tone' at the start of the tape. The actual program can now be recorded, operating S3 and S4 as required to change the slides; the 30 Hz pulses will be recorded at −10 dB.
For playback, S2 is set to position 2. The initial reference tone can be used to adjust P1 so that the meter gives the same ¾ scale reading as befora. If the system is used in conjunction with e really good hi-fi installation, the 30 Hz pulses may be audible. In that case, the amplifier can be connected to the output of A5 so that the pulses are filtered out. The only disadvantage is that P3 must then be turned right down, so that it will have to be re-calibrated before the next recording.

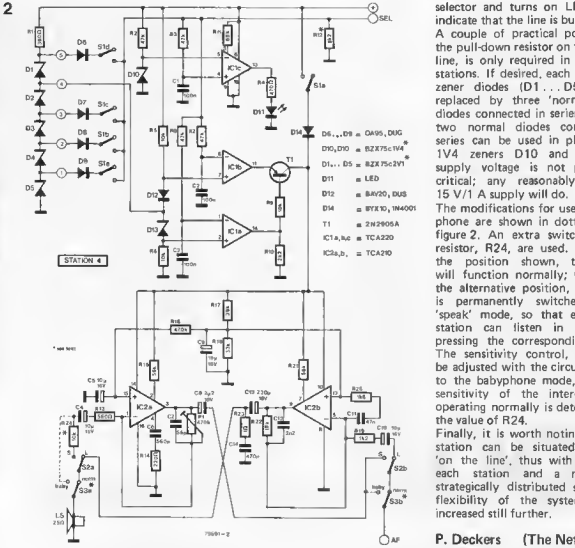
A. Hamm (United Kingdom)

98 flexible intercom system

The criteria for a good domestic intercom system are as follows: First of all, it is essential that each station can call up any other station in the house, without having to route the signal via a 'central' or master station. Secondly, there should be as few wires as possible between each station. Thirdly, the system should be capable of being used as a babyphone, without interfering with normal operation. Finally, there should be no possibility of 'listening in' to stations (other than in the case of the babyphone). The circuit described here fulfils all the above requirements. The basic principle of the system is illustrated in the block diagram of figura 1. A single four-core cable links all the stations; two of the cores are connected to a suitable power supply. In each station a number of reference voltages (U_{REF}) are derived from the supply line. When one of the switches S1a . . . S1d is operated, the corresponding reference voltage appears on the 'selector line'. At the same time switch S1e is closed (all five switches are mounted in an interlocking group), switching in the preamp and power amp. With the 'speak/listen' switch S2a,b in the position shown, any signal appearing on the 'audio line' is fed via the power amp to the loudspeaker. With S2 in the alternative position, the loudspeaker functions as a microphone.
In each post the voltage on the selector line is compared with one of the reference voltages, which is used as the 'call up' voltage for that post. For example, in order to call up station 2, 4 V must appear on the selector line. This voltage is detected by means of a window comparator, which controls an electronic switch (ES), turning on the amplifiers of the station in question. As soon as a voltage above 2 V appears on the selector line, an LED will light at each post to indicate that the line is busy.
The actual circuit is fairly straightforward (see figure 2). The five reference voltages are derived via the five zener diodes D1 . . . D5 which are connected in series. The call up voltages for the other four stations are selected by means of switches S1a . . . S1d. The remaining reference voltage is fed to the window comparator formed by IC1a,b. Transistor T1 is the electronic switch (ES of figure 1) which connects the pre- and power amplifiers (IC2 a and b respectively) in or out of circuit. IC1c detects a call up voltage on the



2



selector and turns on LED D11 to indicate that the line is busy.

A couple of practical points: R12, the pull-down resistor on the selector line, is only required in one of the stations. If desired, each of the 2V1 zener diodes (D1 . . . D5) can be replaced by three 'normal' silicon diodes connected in series; similarly, two normal diodes connected in series can be used in place of the 1V4 zeners D10 and D14. The supply voltage is not particularly critical; any reasonably stabilised 15 V/1 A supply will do.

The modifications for use as a baby-phone are shown in dotted lines in figure 2. An extra switch, S3, and resistor, R24, are used. With S3 in the position shown, the station will function normally; with S3 in the alternative position, the station is permanently switched to the 'speak' mode, so that every other station can listen in simply by pressing the corresponding button. The sensitivity control, P1, should be adjusted with the circuit switched to the babyphone mode, whilst the sensitivity of the intercom when operating normally is determined by the value of R24.

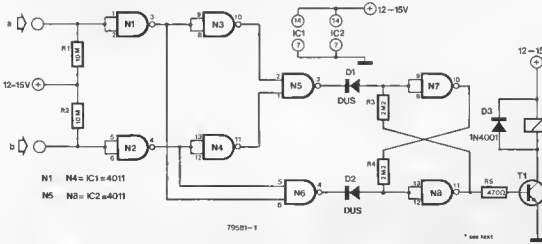
Finally, it is worth noting that each station can be situated anywhere 'on the line', thus with a plug on each station and a number of strategically distributed sockets the flexibility of the system can be increased still further.

P. Deckers (The Netherlands)

fermentation rate indicator 99

When making one's own wine, the fermentation rate can for the most part be estimated by counting the number of times the level of the (sterilising) liquid in the air-lock rises and falls as a result of the CO_2 which is produced. Towards the end of the fermentation process however, the level tends to 'jitter' somewhat, so

1

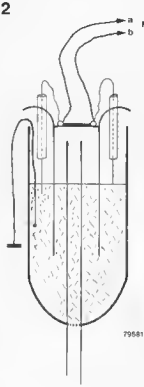


that accurate measurements are not possible. One solution to this problem is to employ two electrodes, one of which is mounted higher than the other – see figure 2. The difference in height between the two should be greater than that by which the level of liquid fluctuates (approximately 2 mm).

The circuit shown in figure 1 is designed to produce an output pulse only if both electrodes are suspended in the liquid, after previously having been clear of the liquid. Enamelled copper wire, 0.3 mm in diameter is used for the electrodes. Insulating sleeving is pushed over the wire, whilst an earth connection is also suspended in the liquid.

As is apparent from the circuit diagram, the input of inverters N1 and N2 are held high via pull-up resistors R1 and R2 when neither of the electrodes is in contact with the liquid. The output of the OR-gate formed by N3, N4 and N5 is therefore low, as is the output of the set-reset flip-flop N7/N8. The output of NAND gate N6 is high.

2



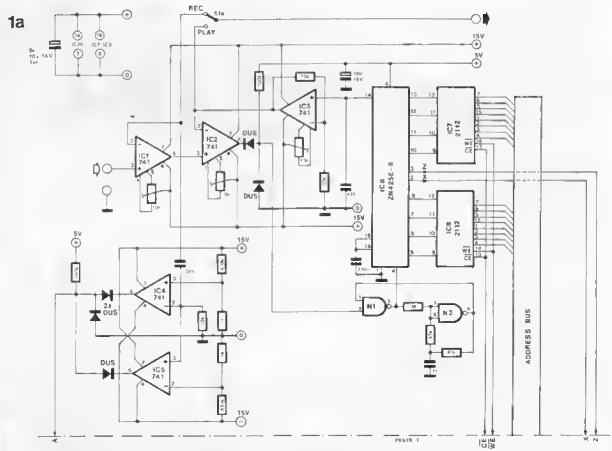
If the level of the liquid in the fermentation lock rises to cover the lower of the two electrodes, the output of the corresponding inverter will go high. This has no effect upon the output of the NAND gate, but the output of the OR-gate will be taken high also. Due to the effect of diode D1, however, the set-reset flip-flop remains in its original state. Should the liquid level fall, the only result will be that the output of the OR-gate is returned low once again. Only if the level rises still further to cover the second electrode will the output of N6 go low and the flip-flop be triggered, turning on T1 and feeding a pulse to the counter (Re). Since the flip-flop can only be triggered by '0' logic levels via D1 and D2, both electrodes must clear the liquid before the flip-flop is reset and another pulse can be counted.

Any normal 12 V impulse counter can be used.

J. Ryan (Ireland)

100 256-note sequencer

1a

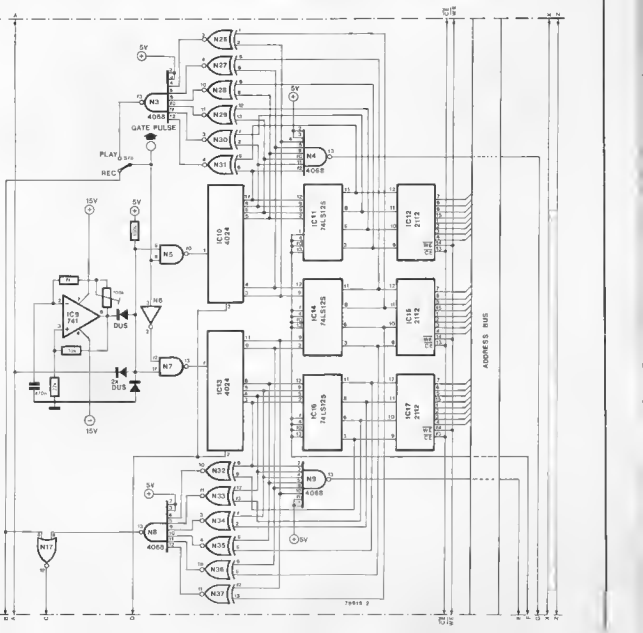


The sequencer is intended to be used in conjunction with a voltage controlled synthesiser. It can store a sequence of up to 256 notes which can then be played back automatically.
The sequence of voltages produced by the keyboard circuit of the synthesiser are fed to an 8-bit A/D converter and then stored. The length of the note and the length of rests between notes are also encoded with the aid of a clock generator and two counters. When the stored sequence of notes is to be played back, the 8-bit data word corresponding to the keyboard voltage level is read out of the memory and re-converted back into an analogue voltage by a D/A converter. Similarly, the note and rest length data are decoded to ensure that the original melody is obtained.
The above approach offers the following advantages over other systems which employ an 'encoded keyboard'.

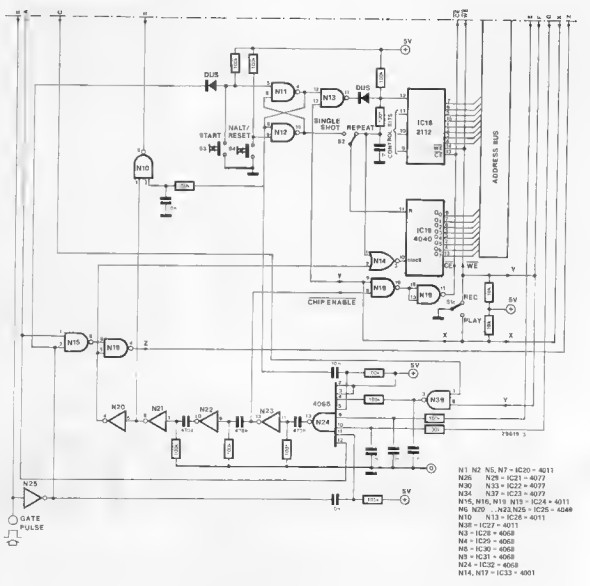
1. The existing keyboard does not need to be modified.
2. An 8-bit A/D converter is cheaper than an encoded keyboard.
3. By using a 2-way converter (A/D and D/A) the original sequence of notes can be reproduced with a high degree of accuracy.

The circuit functions as follows:
To store a sequence of notes, switch S1 is set to the 'record' position; the memory is simultaneously switched to the 'write' mode. When one of the synthesiser keys is pressed, the keyboard gate pulse sets flip-flop N11/N12, taking one of the data inputs of IC18 low and setting the address counter, IC19. The gate pulse also triggers a dynamic shift register formed by N20 . . . N24. This shift register performs a number of functions: resetting IC10 (the 'note counter') and IC13 (the 'rest counter'), resetting the AD-D/A converter, ZN425, enabling the memory IC18, and clocking the address counter. The result of these control signals are that the first memory location remains empty.
The keyboard voltage is digitised by the ZN425. IC10 counts clock pulses provided by IC9 for the duration of the note. When the key is released, IC10 again counts the clock pulses from IC9, this time to time the rest. When the next key is pressed the store cycle is initiated, and the previously obtained information is written into the second memory location. Of course one cannot always use the keyboard gate pulse to determine the length of a note, especially if playing 'legato'. For this reason a detector (IC4, IC5) is included which determines when the keyboard voltage changes. The detector consists of a differentiating network followed by a window comparator, which provides a negative pulse when the voltage level alters. When either IC10 or IC13 reach their maximum count (6 bits), the

1b



1c

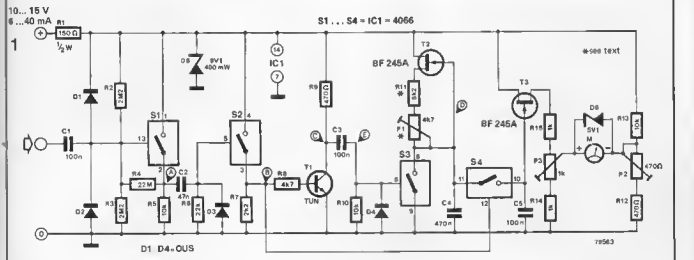


output of N4 or N9 goes low starting a new store cycle and resetting the counters. In this way either a note or rest can be programmed into two or more memory locations.
It was stated that the first memory location remains empty. However if one wishes to start the sequence of notes with a rest, this location can be filled by pressing S3, which triggers ICs 10, 13 and 18 independently of the keyboard gate pulse. IC13 then counts clock pulses until a key is pressed, whereupon the above-described reset and store cycles write the 6-bit data word corresponding to the rest into the first memory location of ICs 12 and 15.
To playback the sequence of notes stored in memory, switch S1 is set to the 'play' position, switching the memory to the 'read' mode and the ZN425 to D/A conversion.

To regain the note and/or rest length information, IC10 is clocked until its output state corresponds with the data outputs of IC12 and IC15. During this period the gate pulse output remains high, and only goes low when the two sets of data coincide; clock pulses are then fed to IC13 until its output state coincides with the data outputs of ICs 15 and 17, whereupon the memory addresses are systematically scanned by IC19 and the stored data read out to the D/A converter.
The output (pin 12) of IC18 goes high when the replay sequence is finished. If the sequence of notes is to be repeated, (S2 is switched to the 'repeat' position) the address counter 'wraps round' and begins again with the lowest address. The unused pins of IC18 can be employed as extra control inputs and connected (via suitable buffers!) to VCOs, filters, etc.
Two final remarks:
Portamento and/or (coarse and fine) voltage controls should be connected after the sequencer.
The A/D · D/A converter will accept the output of a 3-octave keyboard. A 4-octave keyboard can be used if the feedback resistor of op-amp IC3 is increased from 10 kΩ to 18 kΩ.

T. Emmens (United Kingdom)

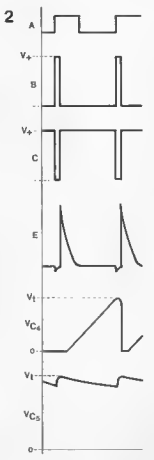
frequency to voltage converter for multimeter 101



Most frequency measurements are carried out by means of a digital frequency meter or else on an oscilloscope. However both these instruments are relatively expensive, and thus not often 'standard equipment' for the hobbyist. One way to measure the frequency of a signal without investing in specialised equipment is to use a frequency-voltage converter, which can then be 'plugged in' to an ordinary multimeter. That is the function of the circuit described here. A meter with a 5 V range should be used; the conversion ratio is linear, assuming the scale is calibrated in ms (1 V = 5 ms).

The circuit is built round a quad analogue switch IC, type 4066. The squarewave signal at point A is switched via S1 to the differentiating network, C2/R6. The resulting pulses are then fed via S2 on the one hand to the inverter formed by T1, and on the other hand to S4. The result is that S3 and S4 open and close alternately, i.e. S3 is open when S4 is closed, and vice-versa. Assuming that S4 is closed, capacitor C4 will be charged linearly by the constant current source T2. The charge is transferred via S4 to storage capacitor C5. S4 and C5 thus function as a sample and hold circuit. If now S4 is opened, S3 will close; capacitor C4 will discharge via S3 to ground, and a new measurement cycle will begin. Depending upon the characteristics of the FET, T3, the sample and hold circuit will increase the voltage by approximately 2 V. Thus a maximum charge voltage of around 6.5 V is possible.

The circuit is calibrated as follows: With the input unconnected, the wiper of P2 is turned to the positive end stop (junction of P2 and R13). A DC voltage of 6.5 V is applied to the gate of T3, and P2 is adjusted for full-scale deflection on the meter. Potentiometer P4 is adjusted for zero reading on the meter with 0 V on the gate of T3. A known frequency is then fed to the input of the circuit (e.g. 50 Hz mains signal from a doorbell transformer), and P2 is then fine tuned for a reading of 20 ms.



The pulse diagram in figure 2 illustrates the signals obtained at points A . . . E in the circuit, and across C4 and C5. With the component values shown in the circuit diagram, the meter will display frequencies between 40 and 2000 Hz (0.1 V = 0.5 ms = 2000 Hz).

Different frequency ranges can be obtained by altering the value of components R11, R12 and C4 accordingly.

The appropriate values can be calculated by using the formula;

$$U_{C4} = \frac{I_{C4}}{C4 \cdot f_{in}}$$

where $I_{C4} = \frac{U_{R11} + U_{P1}}{R11 + P1}$

Finally one or two specifications:

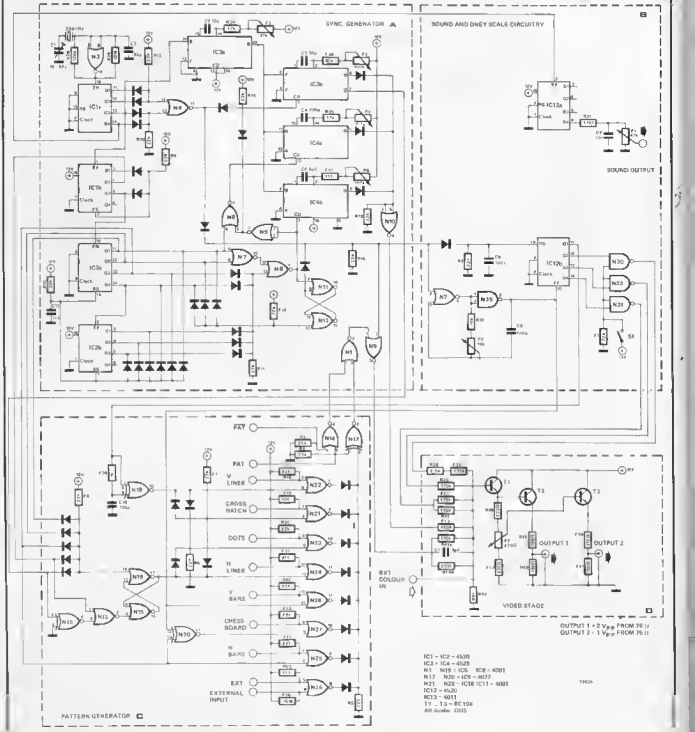
supply voltage:	10 . . . 15 V
current consumption:	5 mA
input impedance:	1 MΩ
input sensitivity:	minimum 1.5 V pp

F. Kasparec (Austria)

102 video pattern generator

When setting up a television set, a video pattern generator is a very useful instrument to have at hand. While circuits for video pattern generators are by no means rare, they often suffer from overcomplexity or use of uncommon components. The design offered here, however, although using a large number of components, is neither complex nor are the components difficult to obtain.

As can be seen the design splits neatly into a number of parts the first of which is the Sync. generator (section A) which provides all the necessary timing pulses. The output of the crystal oscillator built round N3 is divided by 16 by IC1a to provide the line frequency. The field frequency is obtained from counters IC1b, IC2a and IC2b, which divide the line frequency by 625. The outputs of these counters are gated together to select three timers (IC3b, IC4a and IC4b) which provide the line sync pulse, the field sync pulse and the equalisation pulses after being triggered by IC3a (the front porch delay). The enable signal for IC3b is also gated with the 12 μs line blanking interval (from N4) to ensure that it is triggered at line



frequency. The bistable N11/N12 produces the field blanking interval which is reset after 25 lines by IC2a. Both blanking pulses and the output from the pattern generator are gated by N9 to provide a blanked video drive to the mixer stage.
The output from the mixer can be fed to a suitable UHF TV modulator (see Elektor 42, October 197B).

Sound output

The sound output circuitry is shown in section B. The Q4 output of IC1a is divided by sixteen in IC12a to produce a 977 Hz signal at its Q4 output. This signal is then attenuated by R31 and P1 and filtered by C7 to produce a more pleasent sound.

Grey scale

The grey scale is produced by a gated oscillator built around N2/N29 and a binary counter IC12b. During line and field blanking intervals the oscillator is inhibited and IC12b reset to zero to ensure that each new line is correctly positioned. The outputs of the counter are inverted by gates N30 . . . N32 to give a grey scale of descending height. To select the grey scale the other inputs of gates N30 . . . N32 are taken high, i.e. by operating switch S1.

Pattern generator

The pattern generator (section C) provides a selection of eight basic black and white patterns which can be selected by a rotary switch.

Vertical lines.

The output of the grey scale counter (IC12b) is connected to gate N19 which gives a short output pulse each time the input changes state giving 15 vertical lines.

Horizontal lines.

A horizontal line is produced after every 20 TV lines at the output of the bistable N15/N16. The gating on the input ensures that the line is one TV line long between line sync pulses. Fourteen horizontal lines are thus produced.

Crosshatch.

This is simply the vertical and horizontal lines ORed together.

Dots.

These are produced by ANDing the vertical and horizontal lines together.

Vertical Bars.

This is the output of the grey scale oscillator and gives sixteen bars.

Horizontal bars.

The output Q3 of the field counter IC2a gives thirteen horizontal bars.

Chessboard.

This is the output from the horizontal and vertical bars when connected to the EXclusive NOR gate N20.

External.

Provision has been made so that an external pattern can be connected to the system via gate N26.

As can be seen the eight patterns are connected to gates N21 . . . N28. By taking the unused input of these gates low the required pattern can be selected. Gates N14 and N17 allow the inverted or normal pattern to be selected.
The number of patterns can be increased by selecting several basic patterns together (vertical bars with horizontal lines) or more complex patterns can be produced by using the binary outputs of IC12b.

Video stage.

Section D shows the circuit of the video stage of the pattern generator. The logic inputs are mixed together by the resistor network R38 . . . R45. The composite video signal is then buffered by T1 which drives transistors T2 and T3 to provide two different output levels. The output of T3 can be adjusted by potentiometer P3. Capacitor C11 is included to sharpen the vertical edges.

P. Needham (United Kingdom)

audio sectioner 103

Many phonetic research applications may benefit from the use of an audio system with a repeating loop. Additionally, a sectioning device is often desirable — allowing only a desired sagment of the material recorded on the loop to be passed to the output.
The system described here uses two tape recorders with remote control capabilities. The Master recorder holds an ordinary reel of tape on which the material for analysis has been recorded. The second, or Slave, tape recorder has no reels, but an endless tape loop of the desired length. A length of 3 seconds has been used for convenience, but the electronics of the Sectioner could be modified to allow for any length.
Using a remote control panel in the Sectioner, the operator may play or rewind the tape on the Master tape recorder. During the 'listen' mode, the material is automatically recorded onto the loop of the Slave recorder.
By switching to the 'repeat' mode, the operator can make the loop repeat endlessly, while the Master recorder is stopped.
In the 'repeat' mode, the Sectioner may be made to function. This device 'chops' out the undesired portions at the begining and end of the loop, leaving only the desired portion in a 'window' in the loop. The lead and lag controls (which define how much is chopped at the beginning and end of the loop, respectively) are infinitely adjustable, so that the window may be of any length and at any point in the loop.
The material which is chopped is not erased, and the lead and lag controls may be subsequently readjusted for a wider or narrower window. Additionally, the material on the entire loop may be played back without changing the lead and lag control settings, so that the sectioned and unsectioned loops may be easily compared.
The material on the Master tape recorder (in the 'listen' mode) or on the loop (in the 'repeat' mode) may be played back through any audio amplifier and/or may be fed directly into an oscilloscope, oscillograph, spectrum analyzer, or other instrument. The chopping is accomplished electronically, and no detectable click is produced, so auditory or instrumental analysis are not marred by the noise of switching.
A special circuit makes it easy to produce visual displays on an oscilloscope. It ellows the oscilloscope sweep to be triggered just before the beginning of the 'window'.
As shown in figure 1, the Sectioner itself (enclosed in dotted lines) contains an oscillator and a tone decoder. The output from the latter triggers electronic timers (lead and lag) which create the 'window'.
When the 'listen' mode switch is pressed, the following sequence of operations occurs:
1. The Master tape recorder (that

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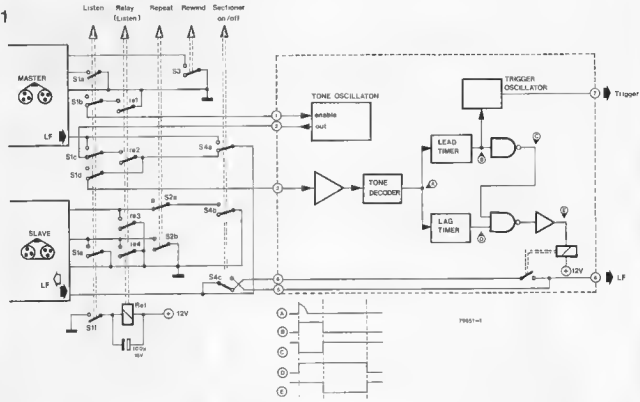


containing the pre-recorded reel) starts in the playback mode (S1a).
2. Voltage is applied to the relay (S1f).
3. The Slave tape recorder (that with the loop) starts in the record mode (re3, re4).
4. The Tone Generator is inhibited (S1b).
5. The Tone Decoder is inhibited (S1d).
6. The audio signal from the Master tape recorder is recorded on the Slave tape recorder (S1c, re2, S4a).

When the 'repeat' mode switch is pressed, the following sequence of operations occurs:

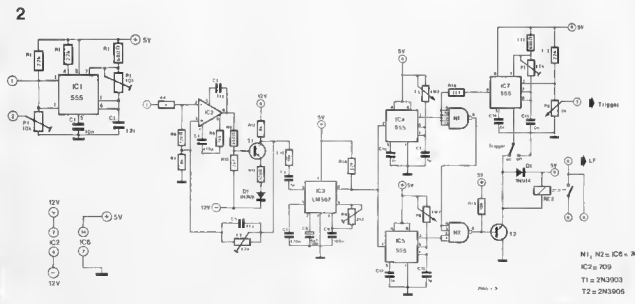
1. The Master tape recorder stops (S1a).
2. Voltage is removed from the relay (S1f) but the relay remains energized while the capacitor (across its pins) discharges.
3. During the discharge time (approximately 100 milliseconds), the Slave tape recorder continues in a record mode (re3, re4). A tone from the Tone Generator is recorded on the loop (S1c, re2). The Tone Generator is keyed by applying a ground connection (S1b, re1).
4. After the delay (100 milliseconds), the relay de-energizes, thus the Slave tape recorder is switched from a record mode to a playback mode (S2b). Simultaneously, the Tone Generator is inhibited (re1) and its output is disconnected (re2). The audio output from the Slave tape recorder is fed to one pole of the Sectioner On/Off switch, and to the input of the decoder network (S4a, S1d).

The operator may rewind the master reel by pressing the rewind mode switch, and during this time the following sequence of operations occurs:

1. The Slave tape recorder stops (S1e, re4, S2b all open).
2. The relay is de-energized (S1f).

Should the operator wish to by-pass the Sectioner and use the two tape recorders only, the mode selector switches retain their functions, and the 'Sectioner On/Off' switch pro-

2



vides the necessary circuit changes:
1. S4a by-passes the 'listen' mode contacts and relay pin connections, so that the audio signal goes from the Master tape recorder directly to the Slave tape recorder.
2. S4b by-passes the relay pin connections and enables the Slave tape recorder to be operated in the record mode.
3. S4c permits the operator to monitor the recorded audio signal of the loop.
   It is by operating this switch in the 'repeat' mode that the operator can compare the 'window' with the 'full loop', providing the Sectioner was turned On while the loop was recorded.

The circuit of the Sectioner is shown in figure 2. The signal from the loop is amplified (IC2, T1) and fed to the tone decoder (IC3). The inherent phase-lock-loop qualities of the decoder ignores all signals other than its pre-tuned pure tone. When this signal is present, the decoder provides a saturated switch to ground. This ground condition triggers the lead and lag timers (IC4 and IC5) simultaneously.

The output logic of the timers is independent of the input waveform and is controlled by the time constant of Rt•Ct: any change in the value of the potentiometers (P5 and P6) will change the position of the beginning (lead) and end (lag) of the window.

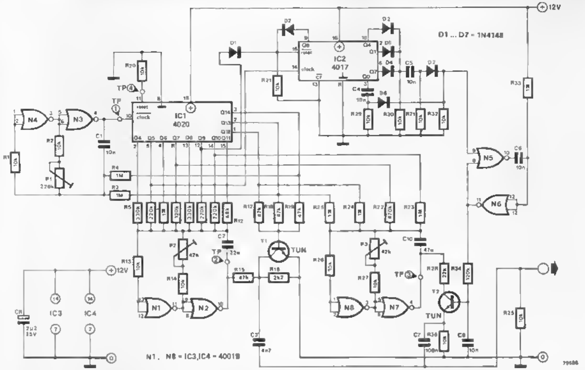
The output of the lead timer is inverted (N1) and used to inhibit N2. When the 'lead' time expires, the output of N1 goes 'high' so that the output of N2 changes to 'low', creating the window. Transistor T2 now conducts and the relay pulls in. With the loop signal present at one contact of the relay, and the output jack on the other contact of the relay, the sectioned audio signal is available.

With the Synchronized Trigger switch in operation, the circuit at rest, the level at the emitter of T2 is 'high' and the oscilloscope trigger oscillator is inhibited. Upon conduction of the transistor, the level at pin 1 goes 'low' and the oscillator is keyed on. This condition allows the operator to trigger the visual display in synchronism with the sectioned signal.

The tone oscillator (IC1) is enabled in the same way: by taking pin 1 high or low, the oscillator is turned off or on as required.

R.D. Fournier (Canada)

electronic horse 104



The term 'electronic horse' is actually something of a slight exaggeration, for the circuit described here will not really carry you off into the sunset after a shoot-out at the O.K. corral. What it will do is imitate the sound of a horse carrying you off into the sunset. The circuit both 'neighs' and 'clip-clops' (throw away those old coconuts), and should prove an amusing diversion at parties or a useful special effects unit for amateur dramatics.

The circuit functions as follows: oscillator N3/N4 is the clock generator for a frequency divider (IC1). The two audio oscillators N1/N2 end N7/N8 are modulated by the outputs of the divider via resistor networks to produce 'neigh' and 'hoof' sounds respectively. To ensure that they do not sound too artificial, the clock generator is also modulated by the frequency divider. The pauses between successive 'neighs' are provided by transistor T1.

The frequency counter IC2, diode network D3 . . . D6, the one-shot N5/N6 and transistor T2 ensure the correct rhythm between hoof beats.

The circuit is calibrated as follows:
- test point TP4 is connected to + supply (12 V)
- connect a frequency meter between test point TP1 and earth, then adjust P1 to a frequency of 1350 Hz
- adjust the frequency at test point TP2 (by means of P2) to 1550 Hz
- adjust the frequency at test point TP3 (by means of P3) to 400 Hz
- break the connection between TP4 and + supply.

Heigh-ho Silver!

J.M. Carreras (Spain)

105 programmable melody generator

No, the circuit described here is not just another 'doorbell', it is intended primarily for use in electronic toys, musical car horns etc. Simple melodies of up to 25 notes can be stored in memory via the eight programming switches.

Two 256 x 4 Bit random access memory (RAM) ICs (IC1 and IC2 in figure 1) comprise the melody generator memory, IC1 stores the 'octave' data while IC2 stores the 'note' data. The address counter, IC3, is clocked by the astable multivibrator formed by the gates N1/N2,

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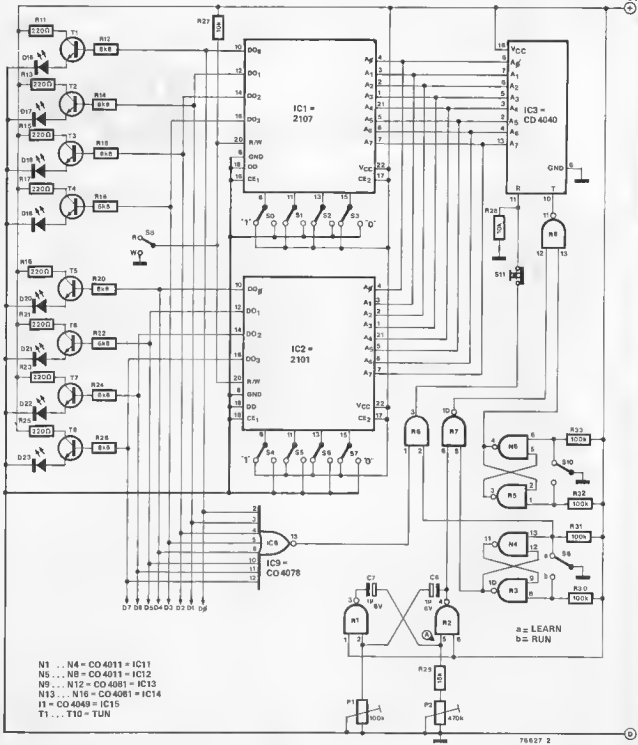


Table 1.

note	note number binary D7	D6	D5	D4	decimal	master oscillator frequency (Hz)
C#	1	1	1	1	15	8870
C	1	1	1	0	14	8372
B	1	1	0	1	13	7902
A#	1	1	0	0	12	7459
A	1	0	1	1	11	7040
G#	1	0	1	0	10	6645
G	1	0	0	1	9	6272
F#	1	0	0	0	8	5920
F	0	1	1	1	7	5588
E	0	1	1	0	6	5274
D#	0	1	0	1	5	4978
D	0	1	0	0	4	4699
C#	0	0	1	1	3	4435
C	0	0	1	0	2	4186
B	0	0	0	1	1	3951
–	0	0	0	0	0	–

Table 2.

octave number binary D3	D2	D1	decimal	frequency of note A (Hz)
1	1	1	7	3520
1	1	0	6	1760
1	0	1	5	880
1	0	0	4	440
0	1	1	3	220
0	1	0	2	110
0	0	1	1	55
0	0	0	0	–

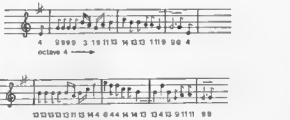
as long as the Run/Learn switch, S9, is in the Run position. Potentiometers P1 and P2 provide coarse and fine adjustment of the replay speed (tempo) of the melody respectively. If the AMV fails to start however, point A should be taken briefly to the +5 V rail.

The basic frequency of the note generator (IC8 in figure 2) is determined by which of the preset potentiometers P3 . . . P17 is selected by the decoders IC4 and IC5. Table 1 lists the frequencies obtained from the data at the inputs of the decoders. The output of the note generator is divided by IC7 to provide the correct note for the particular octave which is selected (on the basis of input data) by counter IC6. The selected note can be sustained by means of transistor T9, depending on the data present at DØ, while the decay time of the note is determined by capacitor C6.

Programming a tune is carried out by setting the Read/Write switch, S8, to the Write (W) position, and the Run/Learn switch, S9, to the Learn position. The data to be stored is set up on switches SØ . . . S7 whereupon the single-step switch S10 is operated to transfer this data into memory one step at a time. At the beginning of every program, addresses Ø and 1 should receive 'zero' data to ensure that the melody does not start off on its own. This is accomplished by setting switches S0 . . . S7 to '0' and pressing S10 twice. Upon replay the zero data word is detected by the NOR gate IC9 and fed to the reset input of IC3 via the AND gate N9. As this 'zero' data interrupts the count cycle, it can also be used to shorten the melody i.e. the full 256-bit cycle need not be used.

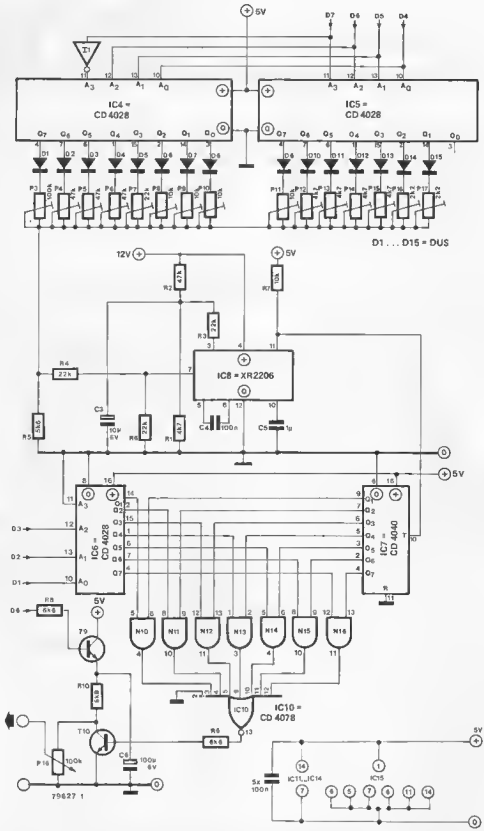
The 'note' and 'octave' data are programmed on switches S1 . . . S7 with reference to tables 1 and 2. Initially, for each note, switch SØ is set to '1' and the preset data written into memory when S10 is operated. If the note is to last for longer than

Table 3.



address	note	D7	D6	D5	D4	D3	D2	D1	D0	remarks
0	–	0	0	0	0	0	0	0	0	stop; wait for
1	–	0	0	0	0	0	0	0	0	start key
2	4	0	1	0	0	1	0	0	1	1st note
3	4	0	1	0	0	1	0	0	0	
4	9	1	0	0	1	1	0	0	1	2nd note
5	9	1	0	0	1	1	0	0	0	
6	9	1	0	0	1	1	0	0	1	3rd note
7	9	1	0	0	1	1	0	0	0	
8	9	1	0	0	1	1	0	0	1	4th note
9	9	1	0	0	1	1	0	0	0	
10	9	1	0	0	1	1	0	0	1	5th note
11	9	1	0	0	1	1	0	0	0	
12	13	1	1	0	1	1	0	0	1	6th note
13	11	1	0	1	1	1	0	0	1	7th note
14	9	1	0	0	1	1	0	0	1	8th note
15	11	1	0	1	1	1	0	0	1	9th note
16	13	1	1	0	1	1	0	0	1	
17	13	1	1	0	1	1	0	0	0	10th note
18	13	1	1	0	1	1	0	0	0	
19	13	1	1	0	1	1	0	0	0	
•									•	
•									•	
•									•	
•									•	
84	13	1	1	0	1	1	0	0	0	
85	13	1	1	0	1	1	0	0	0	
86	13	1	1	0	1	1	0	0	0	
87	13	1	1	0	1	1	0	0	0	
88	4	0	1	0	0	1	0	1	1	
89	4	0	1	0	0	1	0	1	0	note '4' in
90	4	0	1	0	0	1	0	1	0	octave 5!
91	4	0	1	0	0	1	0	1	0	
92	13	1	1	0	1	1	0	0	1	
93	13	1	1	0	1	1	0	0	0	
94	9	1	0	0	1	1	0	0	1	
95	9	1	0	0	1	1	0	0	0	
96	11	1	0	1	1	1	0	0	1	
97	11	1	0	1	1	1	0	0	0	
98	11	1	0	1	1	1	0	0	1	
99	11	1	0	1	1	1	0	0	0	
100	9	1	0	0	1	1	0	0	1	
101	9	1	0	0	1	1	0	0	1	
102	9	1	0	0	1	1	0	0	0	
103	9	1	0	0	1	1	0	0	0	
104	9	1	0	0	1	1	0	0	0	
105	9	1	0	0	1	1	0	0	0	
106	–	0	0	0	0	0	0	0	0	end

2



one clock pulse, then S10 is pressed again. If, however, the note is to die away then SØ is set to '0' before operating S10. To program the next note SØ is switched back to '1'. When the full program has been entered, a zero data word is placed into the final memory location.

To replay the melody, switches S8 and S9 are placed in the Read and Run positions respectively and Switch S11 (the start switch) operated. An example of how to program the melody generator is given in table 3.

Finally some specifications:

Supply voltages:
5 V/200 mA } stabilised
12 V/ 10 mA }
number of program steps: 256
maximum duration: approximately 4 minutes
minimum duration: approximately 15 seconds
clock frequency: 1 . . . 15 Hz, adjustable by P2
15 basic notes, selected by S4 . . . S7
7 octaves, selected by S1 . . . S3
note sustain, selected by SØ

R. Pfister (Switzerland)

chorosynth 106

Low-cost chorus/string synthesiser

The inherent sophistication of a synthesiser such as the Elektor Formant means that, on the one hand it is a comparatively expensive instrument, and on the other hand that it requires considerable skill and practice to utilise its potential to the full when playing live. For readers with a limited budget who are particularly interested in stage work, the Chorosynth offers an attractive alternative.

The Chorosynth contains four voltage controlled oscillators (VCOs) as the basic tone generators (see figure 1). Three of the VCOs are tuned to the same pitch, whilst the fourth is tuned to a fifth higher. An interval of a fifth corresponds to a frequency ratio of 2:3, i.e. with a basic note f1 = 1000 Hz, the fifth, f2 = 1000 · 3/2 = 1500 Hz.

By tuning the fourth VCO to a higher pitch, the harmonic structure of the resulting output signal is enriched, providing a fuller, less artificial sound.

The outputs of the VCOs are fed to 4-bit binary counters which function as octave dividers. From each of the outputs of VCOs 1 . . . 3, the dividers produce 4 notes with a common interval of an octave (16', 8', 4', 2'), whilst from the output of the fourth VCO, the twelfth ($2^2/_3$) and larigot ($1^1/_3$) are produced.

The waveforms at the outputs of the octave dividers are symmetrical squarewaves, suitable for synthesising brass sounds. By feeding the outputs to pulse shapers in the form of NAND gates, three squarewaves with a duty-cycle of 25% are obtained. These form the basic input waveforms for the string filters.

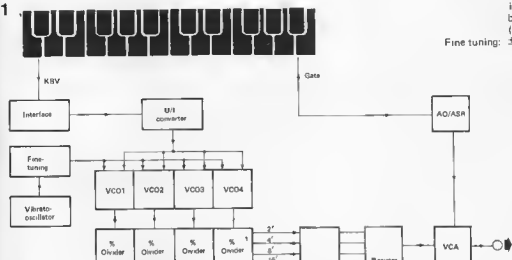
Four chorus switches allow chorus effects to be obtained with each register or 'stop', whilst voicing filters provide a choice of string or woodwind sounds. Altogether a

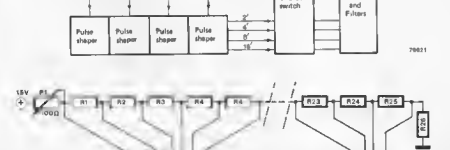
Chorosynth
Technical details:

Range:	Tenor C to G^5 (130 Hz to 6 kHz)
Keyboard:	Printed circuit board with stylus; renge C^1 to C^3, monophonic
Registers:	Cello 16' (S10) Bassoon 16' (S14) Viola 8' (S9) Clarinet 8' (S13) Violin 4' (S8) Clarinet 4' (S12) Violine 2' (S7) Flute 2' (S11) Twelfth $2^2/_3$' (S6) Larigot $1^1/_3$' (S5)
Effects:	Chorus 16' (S4) Chorus 8' (S3) Chorus 4' (S2) Chorus 2' (S1)

Additional controls:

Glissando:	(Portamento, P2)
Vibrato:	Depth and rate (P8 and P9)
Envelope shaper:	Attack/decay or attack/sustain/release, selectable by S15; attack and decay times independently variable between 1 ms and 10 s (P10 and P11)
Fine tuning:	± 4 semitones (P7)





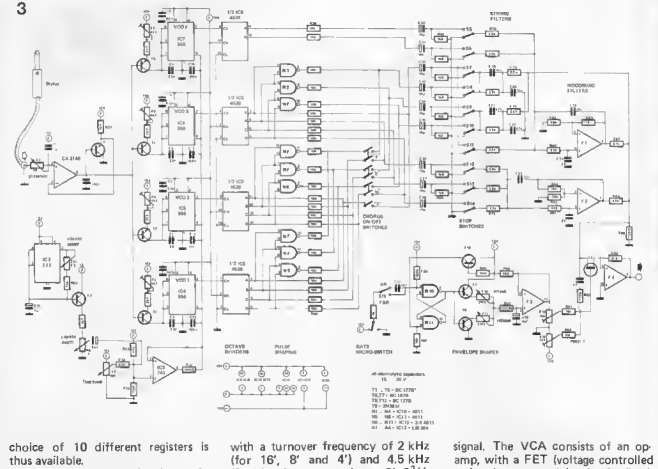
2. OCTAVE KEYBOARD (PCB-type)

Table 1.

Keyboard divider resistors
"+" = series connection
// = parallel connection

R1 = 68 Ω
R2,R3 = 10 Ω
R4,R5,R6 = 12 Ω
R7 = 27 Ω // 27 Ω
R8,R9 = 27 Ω // 33 Ω
R10 = 15 Ω
R11 = 33 Ω // 33 Ω
R12 = 18 Ω
R13,R14 = 39 Ω // 39 Ω
R15 = 39 Ω // 47 Ω
R16 = 22 Ω
R17 = 12 Ω + 12 Ω
R18 = 10 Ω + 15 Ω
R19 = 27 Ω
R20 = 56 Ω // 56 Ω
R21 = 15 Ω + 15 Ω
R22 = 10 Ω + 22 Ω
R23 = 33 Ω
R24 = 39 Ω // 470 Ω
R25 = 39 Ω // 1k5
R26 = 1k8

3



choice of 10 different registers is thus available.

The circuit diagram is shown in figures 2 and 3. The VCOs are formed by 555 timers. The output voltage of the keyboard turns on transistors T2 . . . T5, charging the frequency-determining capacitors C2 . . . C5, and hence the pitch of the oscillator output signals.

Ideally T1 . . . T5 should have the same U_{be} characteristic. In theory, therefore, it would be best to employ a transistor array, however in practice it is sufficient to use individual transistors of the same type (preferably from the same batch).

Since the oscillators have a linear voltage-frequency characteristic, the keyboard tuning resistors must form a logarithmic potential divider. The appropriate values (listed in table 1) can ell be made up using resistors from the E12 series. With 1% tolerance resistors, a tuning accuracy of 1% of a semitone is obtained, however 5% resistors will also prove suitable, since the chorus effect by and large obscures any slight mistuning.

The keyboard is tuned by means of P1, whilst the VCOs are tuned by P3 . . . P6.

S1 . . . S4 are the chorus switches, which provide a separate chorus effect for each register. The tone filter circuits are comparatively simple. Passive highpass filters whose top-end response is slightly rolled off by C30 and C32 provide the voicing for strings. The woodwind filters are active lowpass elements with a turnover frequency of 2 kHz (for 16', 8' and 4') and 4.5 kHz (for the three top registers, 2', $2^2/_3$', and $1^1/_3$'). The lower registers thus have a greater proportion of higher harmonics, which improves the musical tone.

For reasons of cost, a simple printed circuit board which is played with the aid of a stylus, was chosen as a keyboard. The board is mounted on a microswitch, which provides a gate pulse each time one of the key contacts is touched. The gate signal triggers the AD/ASR (attack-decay/attack-sustain-release) envelope shaper: the type of envelope contour obtained is selected by switch S15. With this switch in the AR position, the positive going edge of the gate signal triggers the flip-flop formed by NAND gates N10/N11, turning on T7 and charging capacitor C38 via the attack control, P10. As soon as the voltage on C38 reaches approximately 13.5 V, T10 turns off and the flip-flop is reset. The capacitor then starts to discharge via the release control, P11, and transistor T8.

With the ASR envelope contour selected, the flip-flop remains set as long as the gate signal is present, i.e. as long as a note is held (sustained) on the keyboard. Only when the key is 'released' can T10 reset the flip-flop and C38 discharge (release).

The output of the envelope shaper circuit controls a simple VCA (voltage controlled amplifier), which in turn determines the dynamic amplitude characteristics of the output signal. The VCA consists of an op-amp, with a FET (voltage controlled resistor) connected in the feedback loop. The VCA has two adjustment points:

P12 determines the minimum gain, and is adjusted such that, under quiescent conditions (i.e. no keyboard output voltage, all registers switched in), no output signal is audible. A note is then 'struck' and held (S15 set to ASR!), whilst P13 is adjusted for, first of all, maximum volume, then slightly less than maximum volume.

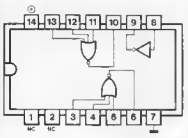
A certain amount of care is needed in the construction of the Chorosynth. Particular attention should be paid to decoupling the VCOs, so that they do not synchronise and the chorus effect is lost. Screened signal leads and a metal case which is connected to circuit earth is also recommended.

The prototype of the Chorosynth has been used live on stage by the author with considerable success, both as a solo instrument and to provide string accompaniment. Although the Chorosynth is no replacement for a full-scale modular synthesiser, it does fill the gap between synthesiser and organ. A particularly interesting possibility as far as organists are concerned is to use the Chorosynth with separate keyboard as an alternative to a small preset or string synthesiser.

J.D. Mitchell (United Kingdom)

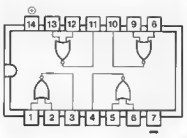
DUAL 3 INPUT NOR GATE PLUS INVERTER

4000



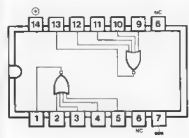
QUADRUPLE 2 INPUT NOR GATE

4001



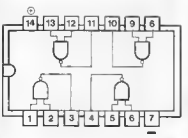
DUAL 4 INPUT NOR GATE

4002



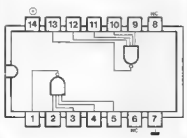
QUADRUPLE 2 INPUT NAND GATE

4011



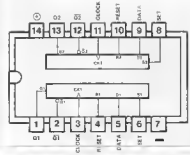
DUAL 4 INPUT NAND GATE

4012



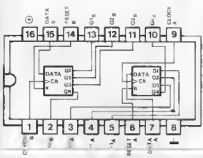
DUAL D FLIP FLOP

4013



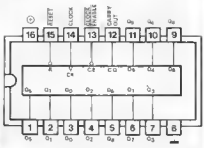
DUAL 4 BIT STATIC SHIFT REGISTER

4015



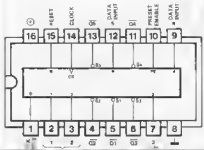
DIVIDE BY 10 SYNCHRONOUS COUNTER

4017



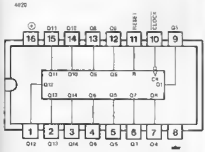
SYNCHRONOUS PRESETTABLE DIVIDE BY N COUNTER

4018



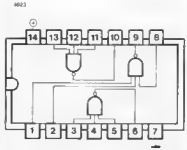
14 BIT BINARY RIPPLE COUNTER

4020



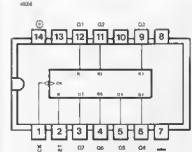
TRIPLE 3 INPUT NAND GATE

4023



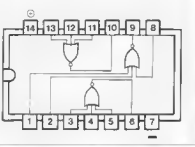
14 STAGE BINARY RIPPLE COUNTER

4024



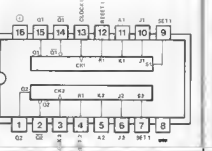
TRIPLE 3 INPUT NOR GATE

4025



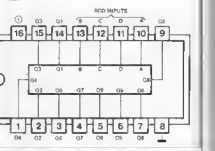
DUAL JK FLIP-FLOP

4027



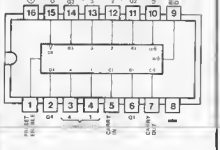
BCD TO DECIMAL DECODER

4028



SYNCHRONOUS PRESETTABLE BINARY/BCD-DECADE UP/DOWN COUNTER

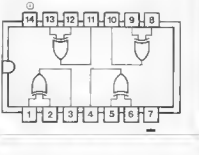
4029



QUADRUPLE 2 INPUT EXCLUSIVE OR GATES

4030

4070 low power TTL compatible (fan out = 2)

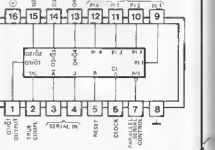


4034

8-BIT

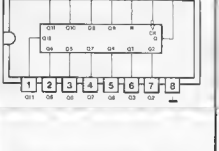
PARALLEL IN/PARALLEL OUT

SHIFT REGISTER



12-BIT BINARY RIPPLE COUNTER

4040

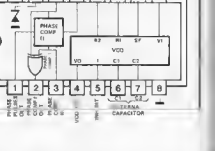


DUAL CLOCKED "D" LATCH

4042

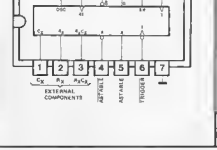
MICROPOWER PLL

4046



MONOSTABLE/ASTABLE MULTIVIBRATOR

4047

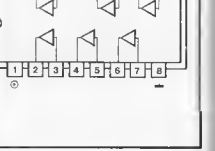


HEX INVERTING BUFFER

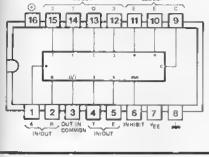
4049

HEX BUFFER

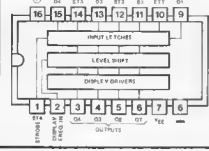
4050



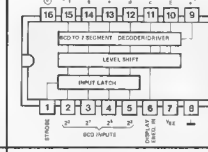
8 CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER
4051



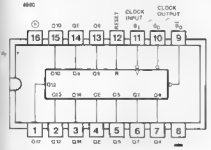
LCD DRIVER
4054



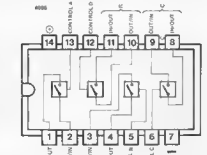
BCD TO 7 SEGMENT DECODER/DRIVER
4056



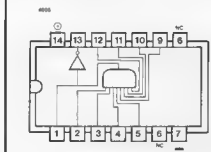
1 BIT BINARY RIPPLE COUNTER AND OSCILLATOR
4060



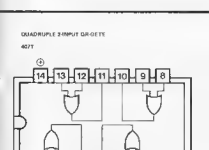
QUAD BILATERAL SWITCH
4066



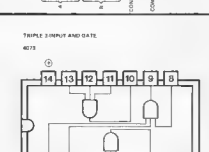
8 INPUT AND/NAND GATE
4068



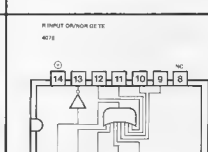
QUADRUPLE 2-INPUT OR-GATE
4071



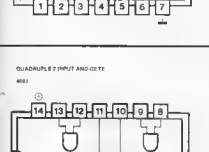
TRIPLE 3-INPUT AND GATE
4073



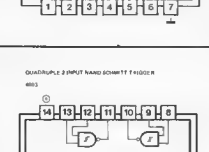
8 INPUT OR/NOR GATE
4078



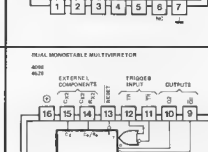
QUADRUPLE 2 INPUT AND GATE
4081



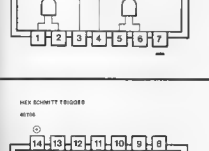
QUADRUPLE 2 INPUT NAND SCHMITT TRIGGER
4093



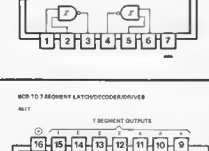
DUAL MONOSTABLE MULTIVIBRATOR
4098
4528



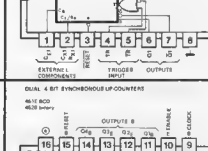
HEX SCHMITT TRIGGER
40106



BCD TO 7-SEGMENT LATCH/DECODER/DRIVER
4511

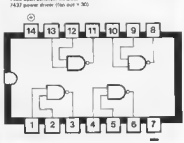


DUAL 4 BIT SYNCHRONOUS UP-COUNTERS
4510 BCD
4516 binary



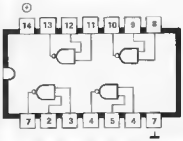
QUADRUPLE 2-INPUT NAND GATES

7400
7401 open collector outputs
7437 power driver (fan out = 30)



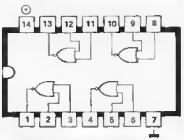
QUADRUPLE 2-INPUT NAND GATE WITH OPEN COLLECTOR OUTPUT

7401



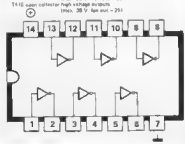
QUADRUPLE 2-INPUT NOR GATES

7402
7428 power driver (fan out = 30)



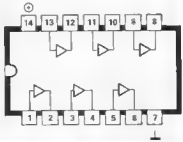
HEX INVERTERS

7404
7405 open collector outputs
7406 open collector high voltage outputs
(max. 30 V, fan out = 25)
7416 open collector high voltage outputs
(max. 30 V, fan out = 25)



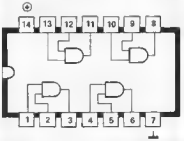
HEX BUFFER-DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS (max. 30 V, fan out = 25)

7407



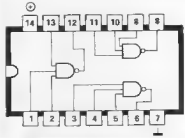
QUADRUPLE 2-INPUT AND GATES

7408
1409 open collector outputs



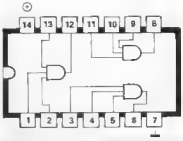
DUAL 4-INPUT AND GATES

7410
7412 open collector outputs



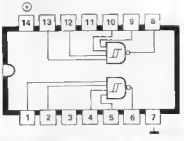
TRIPLE 3-INPUT NAND GATES

7411



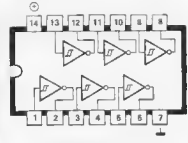
DUAL 4-INPUT NAND SCHMITT TRIGGER

7413



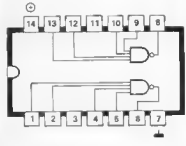
HEX SCHMITT TRIGGER INVERTER

7414



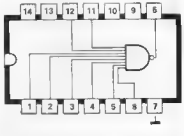
DUAL 4-INPUT NAND GATES

7420
1648 power driver (fan out = 30)



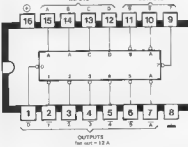
4-INPUT NAND GATES

7420



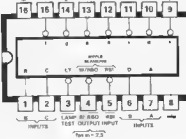
BCD TO DECIMAL DECODER/DRIVER WITH OPEN COLLECTOR OUTPUTS (max. 30 V)

7445



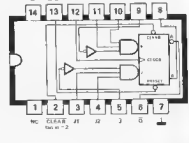
BCD TO 7 SEGMENT DECODER/DRIVER

7447

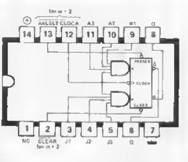


AND GATED J-K MASTER/SLAVE EDGE TRIGGERED FLIP FLOP WITH PRESET AND CLEAR

7470

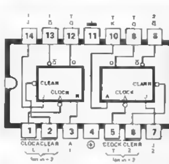


AND GATED J-K FLIP FLOP WITH PRESET AND CLEAR



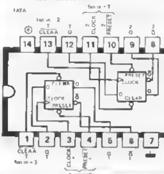
DUAL J-K FLIP FLOP WITH CLEAR

7473



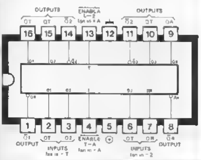
DUAL D TYPE POSITIVE EDGE TRIGGERED FLIP FLOP WITH PRESET AND CLEAR

7474



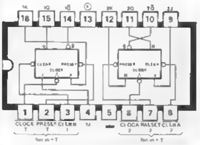
4 BIT BISTABLE LATCH

7475



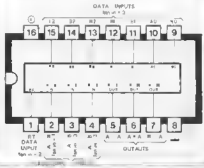
DUAL J-K MASTER SLAVE FLIP FLOP WITH PRESET AND CLEAR

7476



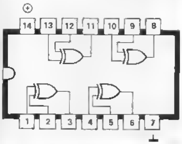
4 BIT COMPARATOR

7485



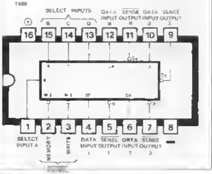
QUADRUPLE 2 INPUT EXCLUSIVE OR GATE

7486



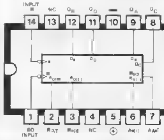
64-BIT READ/WRITE MEMORY

7489



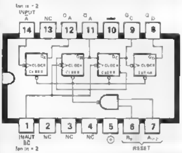
DECADE COUNTER

7490



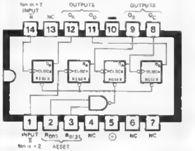
DIVIDE BY TWELVE COUNTER

7492



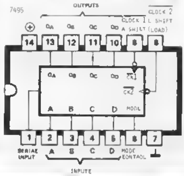
4-BIT BINARY COUNTER

7493



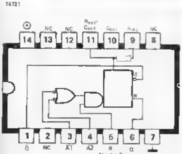
4-BIT PARALLEL IN PARALLEL OUT SHIFT REGISTER

7495



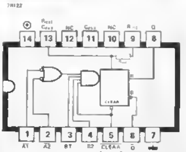
MONOSTABLE MULTIVIBRATOR

74121



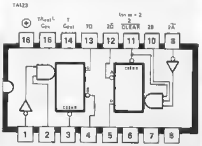
RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

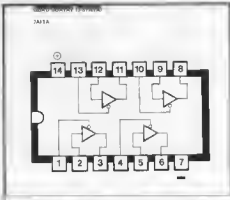
74122



DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

74123

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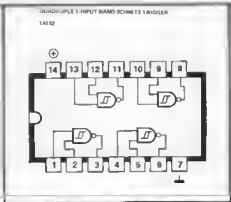
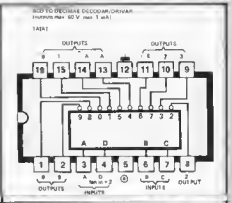
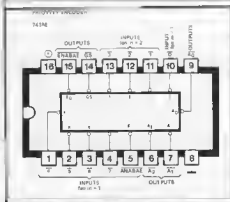

QUADRUPLE 2-INPUT NAND SCHMITT TRIGGER
74132


BCD TO DECIMAL DECODER/DRIVER
74141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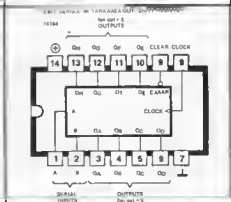
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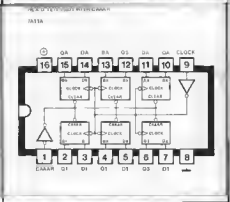
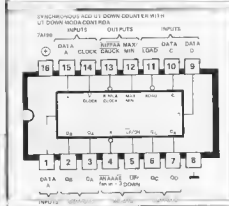

74193A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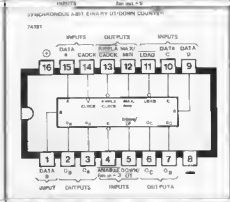
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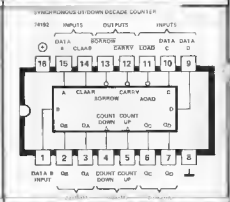
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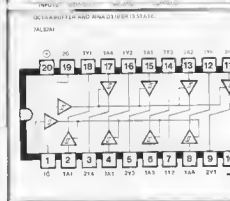
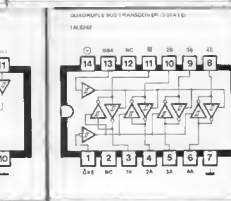
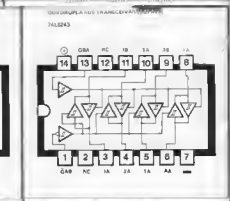

74LS241


74LS242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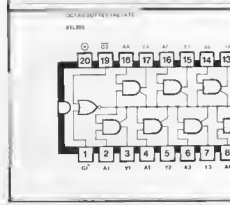
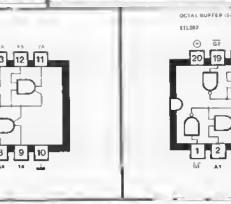
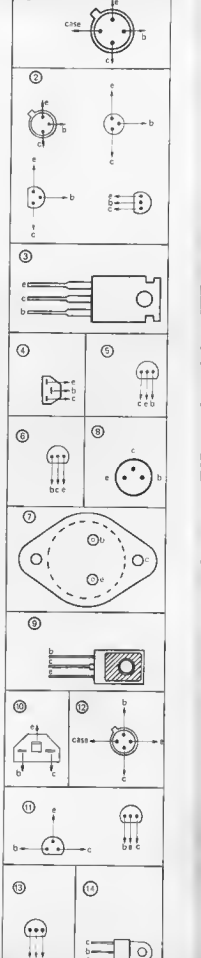

81LS95


81LS97

Type	PNP = P NPN = N	U_{CEO} (Volt) 0 = < 20 00 = 25-40 000 = 45-80 0000 = 66-80 00000 = > 85	$I_{C(max)}$ (mA) 0 = < 50 00 = 55-100 000 = 105-400 0000 = 405 2 A 00000 = > 2 A	P_{max} (mW) not cooled 0 = < 300 00 = 305-1000 cooled 00+ = 1 10 W 000+ = 10-35 W 0000+ = > 40 W	h_{FE} (min) 0 = < 20 00 = 25-50 000 = 55-129 0000 = > 125	case nr	comments	
TUN	N	0	00	0	000			
TUP	P	0	00	0	000			
AC126	P	0	00	00	0000	2		
AF239	P	0	0	0	0	1	grounded base	f_T = 700 MHz
BC107	N	000	00	0	000	2		
BC108	N	0	00	0	000	2		
BC109	N	0	00	0	0000	2	low noise	
BC140	N	00	0000	00+	00	2		
BC141	N	000	0000	00+	00	2		
BC160	P	00	0000	00+	00	2		
BC161	P	000	0000	00+	00	2		
BC182	N	000	000	0	0000	2		
BC212	P	000	000	0	000	2		
BC546	N	0000	00	00	0000	2		
BC556	P	0000	00	00	000	2		
BD108	N	00	00000	00++	00	7		
BD139	N	000	00000	00+++	0	7		
BD132	P	000	00000	00+++	00	9		
BD137	N	000	0000	00+	00	9		
BD138	P	000	0000	00+	00	9		
BD139	N	0000	0000	00+	00	9		
BD140	P	0000	0000	00+	00	9		
BDY20	N	000	00000	00+++	0	7		
BF180	N	0	0	0	0	1	grounded base	f_T = 675 MHz
BF185	N	0	0	0	00	12	grounded base	f_T = 220 MHz
BF194	N	0	0	0	000	10	grounded emitter	f_T = 260 MHz
BF196	N	0	0	0	000	10	grounded emitter	f_T = 200 MHz
BF199	N	00	0	00	000	11	grounded emitter	f_T = 550 MHz
BF200	N	0	0	0	00	1	grounded base	f_T = 240 MHz
BF254	N	00	0	0	000	11	grounded emitter	f_T = 260 MHz
BF257	P	00000	00	00	00	2	grounded emitter	f_T = 90 MHz
BF494	N	0	0	0	000	11	grounded emitter	f_T = 260 MHz
BFX34	N	000	00000	00	00	2	grounded emitter	f_T = 70 MHz
BFX89	N	0	0	0	00	1	grounded emitter	f_T = 1000 MHz
BFY90	N	0	0	0	00	1	grounded emitter	f_T = 1000 MHz
BSX19	N	0	0000	0	000	2		
BSX20	N	0	0000	0	000	2		
BSX61	N	000	0000	00	000	2		
HEP51	P	00	0000	00	000	1		f_T = 150 MHz
HEP53	N	00	0000	00	000	1		f_T = 200 MHz
HEP56	N	0	00	00	000	5		f_T = 750 MHz
MJE171	P	000	00000	00+	00	9		
MJE180	N	00	00000	00++	00	9		
MJE181	N	000	00000	00++	00	9		
MJE340	N	00000	0000	00++	00	9		
MPS A05	N	000	0000	00	00	13		
MPS A06	N	0000	0000	00	00	13		
MPS A09	N	0000	0	00	000	13		
MPS A10	N	00	00	00	00	13		
MPS A13	N	00	000	00	0000	13		
MPS A16	N	00	00	00	0000	13		
MPS A17	N	00	00	00	0000	13		
MPS A18	N	000	000	00	0000	13		
MPS A55	P	000	0000	0	00	13		
MPS A56	P	0000	0000	0	00	13		
MPS U01	N	00	00000	00+	00	14		
MPS U05	N	000	00000	00+	00	14		
MPS U56	P	0000	00000	00+	00	14		
MPS2926	N	0	00	00	00	13	f_T = 300 MHz	
MPS3394	N	00	00	00	0000	13		
MPS3702	P	00	000	00	000	13	f_T = 100 MHz	
MPS3706	N	0	0000	00	000	13		
MPS6514	N	00	00	0	0000	13	f_T = 480 MHz	
TIP29	N	00	0000	00++	0	3		
TIP30	P	00	0000	00++	0	3		
TIP31	N	00	00000	00+++	0	3		
TIP32	P	00	00000	00+++	0	3		
TIP140	N	000	00000	00+++	0000	7	Darlington	
TIP142	N	00000	00000	00+++	0000	7	Darlington	
TIP2955	P	000	00000	00+++	0	3		
TIP3055	N	000	00000	00+++	0	3		
TIP5630	P	000	00000	00+++	0	3		
2N696	N	000	0000	00	0	2		
2N706	N	0	0	0	0	2		
2N914	N	0	0000	00	00	2		
2N1613	N	000	0000	00	00	2		
2N1711	N	000	0000	00	000	2		
2N1983	N	00	0000	00	000	2		
2N1984	N	00	0000	00		2		
2N2219	N	00	0000	00	00	2		
2N2222	N	00	0000	00	00	2		
2N2925	N	00	00	0	0000	13		
2N2955	P	00	00	0	0	2	= MJE2955 TIP2955t	
2N3054	N	000	00000	00++	00	7		
2N3055	N	000	00000	00+++	0	7		
2N3553	N	00	0000	00+	0	2	f_T = 500 MHz	
2N3568	N	000	0000	0	000	13		
2N3638	P	00	0000	0	000	13		
2N3702	P	00	000	00	000	13		
2N3866	N	00	000	00+	0	2	f_T = 700 MHz	
2N3904	N	00	000	0	00	13		
2N3905	P	00	000	00	000	13		
2N3906	P	00	000	00	000	13		
2N3907	N	000	0	0	000	13		
2N4123	N	00	000	0	00	13		
2N4124	N	00	000	0	000	13		
2N4126	P	00	000	0	000	13		
2N4401	N	00	0000	00	0	13		
2N4410	N	0000	000	00	000	13		
2N4427	N	0	000	00+	0	2	f_T = 700 MHz	
2N5183	N	0	0000	00	000	2		

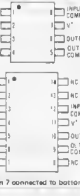


OPAMPS, COMPARATORS

703

NOTE Pin 4 connected to case

709



NOTE Pin 7 connected to bottom of package

NOTE Pin 4 connected to case

741 (835,844)

TAA 861 (A)

LM3900

1458 (5558)

SN 76131 = TBA 231 = µA 239

324

CA 3080

NOTE Pin 4 is connected to case

CA 3094

NOTE Pin 4 is connected to case

CA 3130

NOTE Pin 4 is connected to case

339 (3302)

NOTE: All IC's shown top view, unless otherwise stated.

SPECIAL TYPES

CA 3086 = CA 3046

555

556

1310

VOLTAGE REGULATORS

L 129/L 130/L 131

µA 78..

TBA 625 (829, 830)

LM 309 H, µA 78 M..

LM309K

723 (550)

NOTE On metal can, pin 5 is connected to case

SG 3501 (SG 4501)

LM 325 (LM 1525/LM 2525)

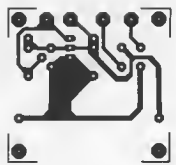
78L voltage regulators

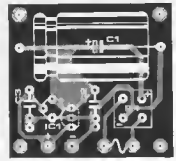
Low-power IC voltage regulators of the 78L series are now so cheap that they represent an economic alternative to simple zener stabilisers. In additon they offer the advantages of better regulation, current limitng/short circuit protection at 100 mA and thermal shutdown in the event of excessive power dissipation. In fact virtually the only way in which these regulators can be damaged is by incorrect polarity or by an excessive input voltage. Regulators in the 78L series up to the 8 V type will withstand input voltages up to about 35 V, whilst the 24 V type will withstand 40 V. Normally, of course, the regulators would not be operated with such a large input-output differential as this would lead to excessive power dissipation.

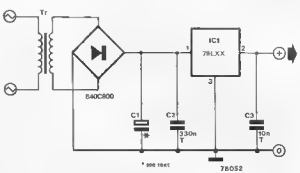
A choice of 8 output voltages is offered in the 78L series of regulators, as shown in table 1. The full type number also carries a letter suffix (not shown in table 1) to denote the output voltage tolerance and package type. The AC suffix denotes a voltage tolerance of ± 5%, whilst the C suffix denotes a tolerance of ± 10%. The letter H denotes a metal can package, whilst the letter Z denotes a plastic package. Thus a 78L05ACZ would be a 5 V regulator with a 5% tolerance in a plastic package.

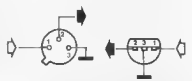
All the regulators in the 78L series will deliver a maximum current of 100 mA provided the input-output voltage differential does not exceed 7 V, otherwise excessive power dissipation will result and the thermal shutdown will operate. This occurs at a dissipation of about 700 mW; however, the metal-can version may dissipate 1.4 W if fitted with a heatsink.

A regulator circuit using the 78L ICs is shown in figure 1, together with the layout of a suitable printed circuit board. The minimum and maximum transformer voltages to obtain the rated output voltage at a current up to 100 mA are given in table 1, together with suitable values for the reservoir capacitor, C1. The capacitance/voltage product of these capacitors is chosen so that any one of them will fit the printed circuit board without difficulty.









LM78L05ACH	LM78L05CH	LM78L05ACZ	LM78L05CZ
LM78L06ACH	LM78L06CH	LM78L06ACZ	LM78L06CZ
LM78L08ACH	LM78L08CH	LM78L08ACZ	LM78L08CZ
LM78L10ACH	LM78L10CH	LM78L10ACZ	LM78L10CZ
LM78L12ACH	LM78L12CH	LM78L12ACZ	LM78L12CZ
LM78L15ACH	LM78L15CH	LM78L15ACZ	LM78L15CZ
LM78L18ACH	LM78L18CH	LM78L18ACZ	LM78L18CZ
LM78L24ACH	LM78L24CH	LM78L24ACZ	LM78L24CZ

Parts list

Capacitors:
C1 = see text and table
C2 = 330 n
C3 = 10 n

Semiconductors:
IC = 78LXX (see text and table)
B = 40 V/800 mA bridge rectifier

Table 1

$I_{max.}$ = 100 mA

U_{out}	type	$U_{tr.}$ (RMS) min.	$U_{tr.}$ (RMS) max.	C1
5 V	78L05	6.4 V	9.6 V	1000 µ/16 V
6 V	78L06	7.3 V	10.3 V	1000 µ/16 V
8 V	78L08	9.6 V	12.0 V	470 µ/25 V
10 V	78L10	11.0 V	13.4 V	470 µ/25 V
12 V	78L12	13.1 V	15.2 V	330 µ/25 V
15 V	78L15	15.2 V	17.3 V	330 µ/25 V
18 V	78L18	17.5 V	19.5 V	330 µ/35 V
24 V	78L24	21.9 V	23.7 V	330 µ/35 V

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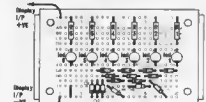
Look at the diagram and select R1, this is a resistor with a value between 120 to 270 ohm. Plug it into holes X20 and D20, now take LED 1 and plug it into holes E20 and F20. Do the same with the Diodes e.g. plug D7 into holes G7 and G10.



YOU WILL NEED

EXP. ANY EXPERIMENTOR BREADBOARD
D1 to D15 — Silicon Diodes (such as 1N914)
R1 to R6 — From 120-270 ohm resistors ¼ watt.
LED1 to LED6 — Light emitting diodes.

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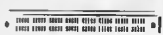

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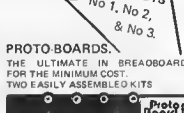

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