

elektor

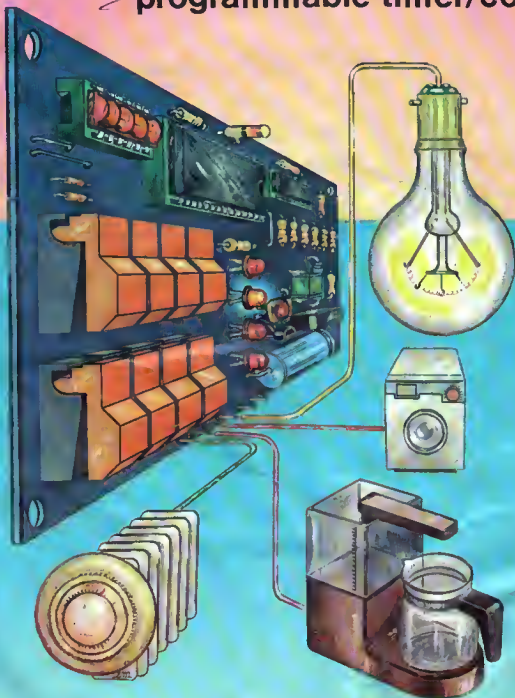
49
May 1979

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Surinder Singh

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Volume 5

Number 5

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What is a TUN?

What is 10 n?

What is the EPS service?

What is the T0 service?

What is a missing link?

Semiconductor types

Very often, a large number of equivalent semiconductors exist with different type numbers. For this reason, 'abbreviated' type numbers are used in Elektor wherever possible:

- '741' stand for μ A741, LM741, MC741, MIC741, RM741, SN72741, etc.
- 'TUP' or 'TUN' (Transistor, Universal, PNP or NPN respectively) stand for any low frequency silicon transistor that meets the following specifications:

| | |
|-----------|---------|
| UCEO, max | 20V |
| IC, max | 100 mA |
| hfe, min | 100 |
| Ptot, max | 100 mW |
| fT, min | 100 MHz |

Some 'TUN's are: BC107, BC108 and BC109 families; 2N3856A, 2N3859, 2N3860, 2N3904, 2N3947, 2N4124. Some 'TUP's are: BC177 and BC178 families; BC179 family with the possible exception of BC159 and BC179; 2N2412, 2N3251, 2N3906, 2N4126, 2N4291.

• 'OUS' or 'DUG' (Diode Universal, Silicon or Germanium respectively) stands for any diode that meets the following specifications:

| | | |
|-----------|-----------|-------------|
| UR, max | 25V | DUG |
| IF, max | 100mA | 35mA |
| IR, max | 1 μ A | 100 μ A |
| Ptot, max | 250mW | 250mW |
| CD, max | 5pF | 10pF |

Some 'DUS's are: BA127, BA217, BA218, BA221, BA222, BA317, BA318, BAX13, BA761, IN914, 1N4148.

Some 'DUG's are: OA85, OA91, OA95, AA116.

• 'BC107B', 'BC237B', 'BC547B' etc refer to the same 'family' of almost identical better-quality silicon transistors. In general, any other member of the same family can be used instead.

BC107 (-8, -9) families:
BC107 (-8, -9), BC147 (-8, -9), BC207 (-8, -9), BC237 (-8, -9), BC317 (-8, -9), BC347 (-8, -9), BC547 (-8, -9), BC171 (-2, -3), BC182 (-3, -4), BC382 (-3, -4), BC437 (-8, -9), BC414

BC177 (-8, -9) families:
BC177 (-8, -9), BC157 (-8, -9), BC204 (-5, -6), BC307 (-8, -9), BC320 (-1, -2), BC350 (-1, -2), BC557 (-8, -9), BC351 (-2, -3), BC212 (-3, -4), BC512 (-3, -4), BC261 (-2, -3), BC416.

Resistor and capacitor values

When giving component values, decimal points and large numbers

of zeros are avoided wherever possible. The decimal point is usually replaced by one of the following abbreviations

p (pico-) = 10^{-12}

n (nano-) = 10^{-9}

μ (micro-) = 10^{-6}

m (milli-) = 10^{-3}

k (kilo-) = 10^3

M (mega-) = 10^6

G (giga-) = 10^9

A few examples:

Resistance value 2k7: 2700 Ω .
Resistance value 470: 470 Ω .

Capacitance value 4p7: 4.7 pF, or 0.000 000 004 7 F. ...

Capacitance value 10n: this is the international way of writing 10,000 pF or .01 μ F, since 1 n is 10⁻⁹ farads or 1000 pF.

Resistors are $\frac{1}{2}$ Watt 5% carbon types, unless otherwise specified.

The DC working voltage of capacitors (other than electro-

lytic) is normally assumed to be at least 50 V. As a rule of thumb, a safe value is usually, approximately twice the DC supply voltage.

Test voltages
The DC test voltages shown are measured with a 20 k Ω /V instrument, unless otherwise specified.

U, not V

The international letter symbol 'U' for voltage is often used instead of the ambiguous 'V'.

'V' is normally reserved for 'volts'. For instance: $U_b = 10 V$, not $V_b = 10 V$.

Mains voltages

No mains (power line) voltages are listed in Elektor circuits. It is assumed that our readers know what voltage is standard in their part of the world!

Readers in countries that use 50 Hz should note that Elektor circuits are designed for 50 Hz operation. This will not normally be a problem; however, in cases where the mains frequency is used for synchronisation some modification may be required.

Technical services to readers

• EPS service. Many Elektor articles include a layout for a printed circuit board. Some — but not all — of these boards are available ready-etched and predrilled.

The 'EPS print service list' in the current issue always gives a complete list of available boards.

• Technical queries. Members of the technical staff are available to answer technical queries relating to articles published in Elektor

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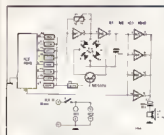
• Missing link. Any important modifications to, additions to, improvements on or corrections in Elektor circuits are generally listed under the heading 'Missing Link' at the earliest opportunity.

Supplement:
BASIC (part 3), an
introduction to a simple
computer language.



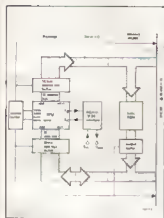
The desire to have a distinctive 'sound' is not restricted to musicians. People are also getting tired of old-fashioned doorbells, and even gongs and chimes ere by no means unique. In this issue, a random tune doorbell and a musical doorbell are described; next month we will extend the range with a fully programmable doorbell.

(p.5-17 and p. 5-47)



'Cheep cheeper' was also considered as title for the simple sound effects generator. However, this name doesn't quite do justice to a unit that can produce so many recognisable and unrecognisable noises!

(p. 5-32)



The BASIC microcomputer card contains three relatively independent sections: a fully buffered and self-contained CPU, a NIBL interpreter in ROM and a standard interface. Adding one 4 K RAM card converts it into a complete microcomputer.

(p. 5-34)



This month's cover illustrates the possible uses of the programmable timer/controller; control of lighting and (central) heating, domestic appliances such as washing machines and cookers, coffee percolator or early-morning tea, etc. In general: automatic switching of equipment at fixed, preset times.

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| programmable timer/controller | 5-08 |
| The circuit described is a versatile timer/controller, capable of switching 4 separate outputs on or off at 4 pre-programmed times every day. The circuit is ideally suited for the control of domestic appliances such as cookers, central heating, intruder alarms (to be switched on at night) etc., or can be used as a straightforward 24 hour 'radio-snooze-alarm' clock. | |
| switching mains-powered equipment | 5-13 |
| If mains powered equipment is to be switched on and off by electronic circuits like the timer/controller, something more is required: an (electronic) relay. Four examples of this type of reliable and silent electronic relay are described. | |
| random tune doorbell (A. Houghton) | 5-17 |
| delay lines (2) | 5-18 |
| Having dealt with reverberation and echo in a previous article (see Elektor 46, February 1979) we now take a look at how delay lines can be used to achieve a wide variety of interesting special effects such as double tracking, vibrato, phasing, chorus etc. | |
| CAPITALS from the ASCII keyboard | 5-24 |
| When programming in BASIC, only capitals are required. This option can be selected by adding one switch on the ASCII keyboard. | |
| interface for μPs | 5-25 |
| The specifications for a serial interface between computer and terminal are given by the so-called RS232C and V 24 standards—among others. Only a few components are required for a 'standard' interface. The circuit described in this article can be used in conjunction with both the Elektor SC/MP system and the popular KIM 1. | |
| sweep generator (L. Kõroen) | 5-28 |
| Determining the frequency response of an amplifier normally requires a series of carefully conducted test measurements, a large supply of graph paper, and plenty of patience. However if one possesses an oscilloscope, there is a way of displaying frequency response curves upon its screen—provided one also has the instrument described here, namely a sweep generator. | |
| simple sound effects | 5-32 |
| Using only two CMOS ICs, a wide range of sounds can be produced—varying from an American police siren to the twittering of birds. | |
| BASIC-microcomputer | 5-34 |
| It seems safe to assume that the 'BASIC microcomputer' is the cheapest home-construction computer ever described that can be programmed using a higher programming language. The BASIC computer consists of not more than two Euro-card-sized printed circuit boards! | |
| NIBL-E (O. Hendriksen) | 5-43 |
| A BASIC interpreter for the SC/MP has been available for some time. However, this can only be used in systems where page 0 is available for storing the interpreter program. In the Elektor SC/MP system, part of page 0 is used for the monitor program. Even so, an adapted version can be incorporated into the Elektor system—es described in this article. | |
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SELEKTOR

Our remarkable sense of pitch

(Dr R. A. Henson*)

To hear or sing even the simplest of tunes we need a sense of pitch. Our ability to judge it consistently is remarkable, but investigating how we do it is far from simple. Although we have quite a lot of information about the way the ear responds to sounds at various frequencies, we know very little yet about the subsequent central processing by the nervous system and the brain.

The pitch of a sound means its position on a scale of frequencies. Pitch sense is involved in perceiving all complex sounds; for example, human speech has its set of pitches. In this article the way pitch relates to music is considered. In general, the pitch of a tone depends on its fundamental frequency, which determines whether it stands high or low on the musical scale. We tell one tone from another by their different fundamentals. Music is made up of a succession of tones and combinations of tones that are perceived, analysed and coded by the nervous system in ways to be explored, but questions of tuning and scales and how well we can hear them must be dealt with first.

Orchestral pitch is agreed nowadays as 440 Hz for A', that is, the note A above middle C. It became necessary to agree this internationally because different pitches were used in different places and because a progressive heightening of pitch in the 19th century led to A' as high as 461 Hz in some places. Musical scales are sets of pitches arranged in such a way that they contain a maximum of consonances, where various tones blend pleasingly, and a minimum of dissonances, where they do not. Tuning in 'equal temperament' has

held the field in western music for three centuries because, unlike the earlier 'perfect temperament', it makes possible the use of all 24 keys (C major, C minor, C sharp and so on) without retuning. In equal temperament the octave is divided into 12 logarithmically equal steps of frequency, each to a frequency 5.9 per cent greater than the step below. The steps, called semitones, are each divided into 100 further equal steps or cents, and an octave covers 1200 cents. This method of tuning is imperfect and less accurate than the earlier forms. As Balbour, the eminent American composer and organist wrote, 'all players and singers are playing false most of the time ... these are errors of equal temperament.'

Have we an inbuilt tuning system?

Training and early exposure to musical stimuli make this question impossible to answer with assurance. However, we can say that the western musician's internal pitch scale corresponds to equal temperament but with a slight tendency to sharpen all notes relevant to the tonic or keynote; the target pitch for notation is a shade sharper than equal temperament.

Normal Capability

How much of the normal range of frequencies is actually heard depends on the age of the hearer and also on what is meant by 'hearing' a frequency. Some organ pipes are felt rather than heard. The figures commonly given are 16-20 000 Hz for young people and 20-16 000 Hz for adults. Hearing is most sensitive for frequencies between 1000 and 3000 Hz, being much reduced in the extreme lower and higher ranges. People's ability to discriminate in pitch ranges from those who are tune- or tone-deaf to those with absolute pitch sense. Though it is highly developed in

some, there is no experimental evidence that they can do better than discriminate between quarter tone intervals consistently. The ability to detect small changes of frequency diminishes sharply above 4000 Hz.

Some writers speak of tone 'height' and tone 'chroma'. Tone height means pitch, whereas tone chroma indicates the colour or the way in which a tone affects a listener. It has been suggested that tone chroma plays a part in pitch identification, but Roederer** believed that there was no psycho-acoustic foundation for the notion, because all intervals are equal in the tempered scale; only the pitch is different. Maybe this is a metaphysical question, but there must be few musicians who would agree that C major sounds the same as E flat major. A sense of relative pitch is necessary for hearing or singing a simple tune. Most of us perceive and remember music in terms of changing sequences of pitch rather than in orchestral or other pitch values. Absolute or perfect pitch is the ability to name a sounded note or identify its frequency, or to do both this and to sing a given note accurately straight off. Possessors of absolute pitch appear to have an inbuilt pitch grid against which to measure incoming sounds, though there may be considerable lability or flexibility in the pitch reference points from day to day, for example, at the menstrual periods.

There has been a prolonged debate about whether absolute pitch is innate or acquired, but the present majority view is that both heredity and environment play their parts. Early training is needed for the development of absolute pitch, and important requirements probably include lengthy exposure to sounds of constant frequency and single, critical pitch experiences. Absolute pitch may be the normal manner in which we deal with frequency, but this is trained out of us by our musical environment, which depends on relative pitch. Certainly, absolute pitch can be learned in early childhood, but while pitch perception can be improved in adults by training, no one has been able to train adolescents and older people who had little original ability in pitch-naming. It is likely that highly developed pitch-naming almost always derives from reinforcement of a child's behaviour by an adult.

Perfect pitch is an advantage in some aspects of practical musicianship, but it also carries handicaps. For example, a singer has to transpose consciously when a key is changed. Interestingly, all

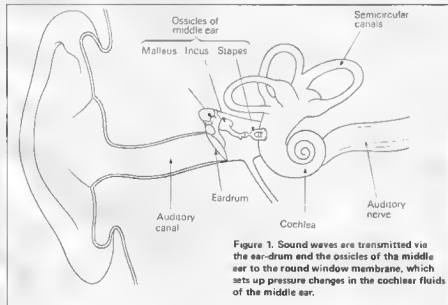


Figure 1. Sound waves are transmitted via the ear-drum and the ossicles of the middle ear to the round window membrane, which sets up pressure changes in the cochlear fluids of the middle ear.

* Neurological Department, the London Hospital.

** J. G. Roederer, Professor of Physics at the University of Denver, Colorado, USA.

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normal people can retain information on absolute pitch for periods ranging from ten seconds to a few minutes, but the information is then discarded.

Pitch Perception

Musical notes must be sounded for at least two or three cycles before their frequencies can be precisely determined. The ear and the brain are more susceptible to the pitch changes of a melody than to blurred acoustic patterns, such as a *glissando* by a pianist. Problems of tuning and intonation must also be taken into account. Electroacoustic analysis has shown that professional violinists and woodwind players deviate slightly from equal temperament in tuning or playing their instruments, and these deviations differ from one player to the next. In other words, they do not all play the same frequency for given notes. Fortunately, the auditory processing mechanism of the ear ignores minor fluctuations in pitch so that we place tones clearly in their right category. When fluctuations are larger the tone may seem out of tune, with the appearance of beats of one frequency against another, or be perceived as the next semitone or tone above or below the desired pitch. Considerations of this sort brought the suggestion that pitch may be defined operationally as the subjective correlate of each one of the auditory events contained in a musical performance.

The Peripheral Analyser

The capacity of the human ear to analyse sound waves is truly remarkable. Perception of musical sound depends on several factors, including identification of the pitch, duration, intensity and rhythm of a series of tones, and this requires an efficient peripheral analyser of the sound waves produced. Here we are concerned solely with the problem of pitch perception. Many theories of pitch discrimination have been advanced over the past hundred years, but even now a unified solution escapes us. Current knowledge and views appear to add up to what follows. Sound waves are transmitted from outside via the ear-drum and the ossicles of the middle ear to the round window membrane, which sets up pressure changes in the cochlear fluids of the inner ear. The sound receptors of the cochlea are the inner hair cells, disposed along the basilar membrane. These cells are activated by a travelling wave which always passes throughout the membrane from the base to the apex of the cochlea. The travelling wave has its greatest amplitude at a point determined by the frequency of the sound stimulus. High frequencies cause vibrations in a small part of the base of the cochlear parti-

tion; low frequencies set the whole membrane into vibration. The place where the inner hair cells are activated may well account for the perception of high frequencies, and this idea is supported by the fact that people with disease at the base of the cochlea are deaf to high tones. But this theory does not explain how we perceive low tones, and it has been suggested that low frequencies are represented by the rate of nerve impulses engendered by the stimulus. The cochlear nerve fibres, which join the ear to the brainstem, cannot carry more than 500 to 600 impulses per second, and this led to a 'volley' theory. This was that groups of fibres could carry frequency information, so that the stimulus frequency is represented in the combined pattern of nerve impulses produced. This idea is acceptable in a general sense, but there are objections to it on physiological grounds, especially where frequencies over 3000 Hz are concerned. Perhaps place and frequency and patterns in time all play their parts in pitch perception. Harmonics may help in identifying the fundamental of lower tones, for if a set of overtones is sounded, without the fundamental, the listener's ear supplies it and he hears it just the same.

Second Mechanism

This first stage of analysis by the basilar membrane is not enough to account for the fine degree of pitch discrimination achieved by the human ear. Studies on the mechanical tuning of the basilar membrane have shown that it acts as a heavily damped, broadly tuned structure; on the other hand, recent recordings of the activity of a single auditory nerve fibre have shown that the tuning here is sufficiently fine to meet psychophysical requirements. There must be a second mechanism inside the cochlea to account for the difference in tuning between the two structures, and it has been suggested that the olivocochlear bundle, which runs from the brainstem to the inner ear, is involved in it. With higher intensities — for example, the orchestral *fortissimo* — the neural tuning of the cochlea is broad, and it seems that there must be a further tuning mechanism within the nervous system to deal with loud sounds. Single auditory neurons have their own best frequencies, but they can also respond to neighbouring frequencies; that is to say, the frequencies that neurons respond to overlap. Looking at how the system works, an arrangement of this type would be essential to ensure the transition from one sound to another that listening to music demands; it would also contribute towards the appreciation of loudness. Psychophysical studies suggest that fre-

quency selectivity is achieved in man by the equivalent of a bank of overlapping filters, a system that would separate the individual components of a complex signal for analysis. Psychophysical measurements, known as critical bands, have been used to find the effective bandwidths of the human auditory system. It appears that these critical bands range from 200 Hz wide at 1 kHz to 2 kHz wide at 10 kHz. Such a mechanism could explain why we hear the normal differences in tuning or sounding of instruments or voices as the same note or tone. Tonal material that is not relevant to the task on hand is inhibited, a process called tuning or sharpening. The exquisite sensitivity of the human ear is shown by the way in which we can separate simultaneously-heard tones with shared harmonics. So far we have been unable to sort out the mechanisms that produce these psychophysical effects. A central pitch processor should transform incoming nervous impulses bearing information on pitch into patterns, so that all stimuli of the same periodicity are represented in the same way. This would produce individual sensations for different pitches. We have already seen the need for an auditory system capable of categorical assessment and of dealing with tones of neighbouring frequency or shared harmonics. The nervous system meets this need in ways we do not understand. The auditory system must integrate stimuli presented to both ears, and its ability to do this is shown by the way harmonic components of a tone fed simultaneously into both ears combine so that the subject hears the fundamental.

Conventional neuroanatomical and neurophysiological studies have given little information about central pitch processing, although the complex pathways of hearing in the brainstem have been thoroughly described. Auditory nerve fibres from both inner ears stream up the brainstem on both sides after their first relay point in the cochlear nuclei. It appears that these fibres relay at four or more points in the brainstem nuclei before they reach the auditory cortex of the brain.

The final relay is in the thalamus, and from it auditory radiation flows to the auditory cortex. Apart from the complexity of the nuclei and linking tracts, investigations are made difficult because if anaesthetics are used; then evoked auditory responses in man and experimental animals are not normal, but, of course, more of these abnormal responses are obtained under anaesthesia than otherwise. In general, however, we can say that the organization that the cochlea imposes on frequency is maintained through the nuclei of the brainstem to the thalamus and auditory radiation. Experimental work on the cat

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has shown that there is systematic cochlear representation in the primary auditory cortex, but opinions differ on whether the techniques used show the true state of affairs at this level.

The Auditory Cortex

The primary auditory cortex, that is the part of the brain solely concerned with input from the cochlear system, lies on an area surrounded by secondary cortex. In animals, this secondary cortex also appears to generate some systematic representation of pitch frequencies. The auditory cortex differs in some respects from other parts of the cortex, but the nerve cells are disposed in the usual columnar arrangement. Many of these cells are finely tuned and the number activated increases with sound intensity. The nerve cell population is not uniform, nor would we expect it to be because of the complicated input, carrying various information about sounds heard. Descending pathways from the cortex pass to those nuclei in the brainstem concerned with hearing. These pathways can be expected to shape and control pitch input by inhibiting and amplifying signals to ensure, among other things, that dominant frequencies prevail. There is evidence from observations on people with brain damage from strokes that humans can distinguish pure tones of different frequency without the intervention of the auditory cortex. But such patients cannot recognize complex sounds.

We do not know how the brain deals with auditory input. On general principles we may presume that incoming nervous impulses are analysed for such variables as pitch, duration, rhythm, intensity, sequence and location. This analysis is not confined to the cells in the immediate area of projection; neighbouring groups and columns of cells are also involved. After analysis comes synthesis. Within the cortex new pitch experiences, arriving as coded patterns of nerve impulses, are matched against the old, and the incoming stimuli are compared and contrasted with each other.

Further consideration of central pitch processing would involve discussion of psychological and psychophysical ideas which are beyond the scope of this article. However, we may conclude with the thought that many factors are involved in pitch discrimination, including semantic memory, musical memory, prediction and set and bias. Progress in our knowledge of the ways in which peripheral analysis of pitch takes place can be expected in the next few years. Solution of the problems of central pitch processing is likely to take much longer.

(Spectrum 156)

Cassette Recorder with a brain

Cassette decks used to be low-fi, easy-to-operate machines. You just popped in a cassette, hit the Record button and set the level. Over the years, however, they've been progressively upgraded; new types of tape have been introduced; noise reduction systems have been added. The result: cassette decks are now hi-fi — but they are anything but easy to operate. . . .

One of the main problems is the vast difference from tape to tape. Modern decks have an array of buttons that select the (hopefully) optimum bias setting and equalisation characteristics for various types of tape (Fe, CrO₂, FeCr, etc.). In practice, even this isn't enough to get the best out of the system, owing to the differences between even nominally identical tapes. A difference in sensitivity of one or two dB between, say, two CrO₂ tapes may not seem much — but if some kind of noise reduction system is used, any errors of this type will be aggravated. So what do you do? Add more buttons? Or, worse still, add continuous controls? For most users, this would make matters worse instead of better — the chance of finding the 'correct' setting will decrease in proportion to the number of controls.

JVC have come up with a better solution: enlist the aid of our new-found friend, the microprocessor! In their new top-of-the-line cassette deck, the KD-A8E, top quality recordings can be made after an initial twenty-second alignment procedure that is carried out by the machine itself, fully automatically. After a cassette has been inserted,

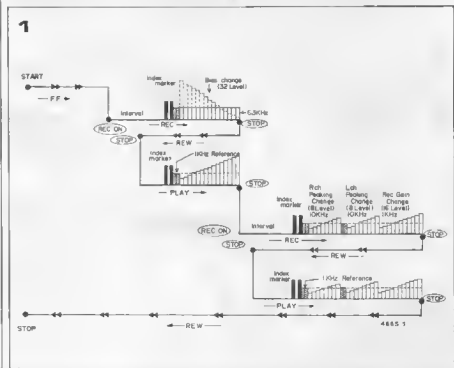
the so-called BEST system (for 'Bias, Equalisation, Sensitivity and Total') first selects the optimum bias setting for that particular tape. It then proceeds to select the correct equalisation and sensitivity settings for a flat 0 dB frequency response out to 10 kHz — worst case, that is, using standard tape!

What it does

Having loaded a cassette and operated the 'computer start' button, the sequence of (automatic) operations are as shown in figure 1. The first thing is to get past the tape leader and into the tape proper, so: 'Fast Forward Wind' for 1.5 seconds.

The machine now switches to Record. After erasing 2.5 seconds worth of tape to leave a gap, two 'index markers' are recorded: 60 ms pulses at -5 dB. A 1 kHz reference signal is then recorded at -15 dB, followed by a 6.3 kHz signal at the same level. During recording of this 6.3 kHz signal, the bias level is reduced in 32 steps — each step lasting 60 ms — from 30% above the 'average' bias level to 30% below. Now, the tape is rewound to the blank section and the test sequence is played back; the 'optimum' bias setting is the one that is found to give identical levels for the 1 kHz reference and the 6.3 kHz test signals.

During this bias setting procedure, the noise reduction circuits are by-passed and the frequency equalisation is set at an average level for that particular kind of tape. It is now time to 'fine-tune' this equalisation. A further test section is recorded, consisting of two index markers, the 1 kHz reference signal and



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a set of 10 kHz test signals. As these 10 kHz sinewaves are recorded, first right channel only and then left channel only, the equalisation for the corresponding channel is increased in eight steps. Finally, it is useful to set the recording sensitivity at the 'standard 0 dB' level — if only to make sure that noise reduction systems work properly! — and so the 1 kHz signal is recorded in sixteen level steps. The tape is now rewound and played back. The equalisation settings for both channels that give equal levels for the 1 kHz reference and 10 kHz test signals are selected; the 1 kHz test signals are compared with the original signal level to select the sensitivity setting that gives 0 dB overall gain. Finally, the machine winds the tape back and signals that it's 'ready to go'.

How it does it

As stated earlier, the whole system works under microprocessor control. The 'program' is illustrated in the flow chart (figure 2); most of it should be clear from the description given above. Starting at the top, the computer first wants to know whether or not its assistance is required. If the 'automatic flag' is not set, the bias, equalisation and sensitivity are simply set at 'nominal' levels, as in any normal cassette recorder. Assuming, however, that the flag is 'on' and the 'computer start' button is operated, the sequence of events described earlier is initiated: Fast Forward wind; RECORD gap, markers, 1 kHz reference and 6.3 kHz test with varying bias; REWIND and Play, Bias Select. At this point, a step is introduced that has not yet been mentioned: Error detection.

In the description given so far, we have blithely assumed that an 'optimum setting' for the various parameters will always be found. In practice, of course, this need not always be the case: the first section of tape may be damaged (causing severe drop-outs) or the tape characteristics may be outside the range of automatic adjustment. If this happens, the machine first checks whether this is its first try; if so, it repeats the whole procedure without first rewinding — so that the test signals are recorded on a new section of tape. If an error again occurs, it gives up and lights a flashing 'error indicator'. Assuming that no error has occurred the bias is then correctly set — the next step is to record the equalisation and sensitivity test signals. The optimum settings are then selected; once again, if an error is detected the machine will have one further try.

If the setting-up procedure has been completed without problems, the machine will rewind the tape and indicate that calibration is complete.

2

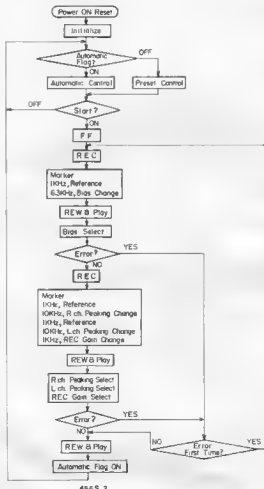


Table 1

SPECIFICATIONS

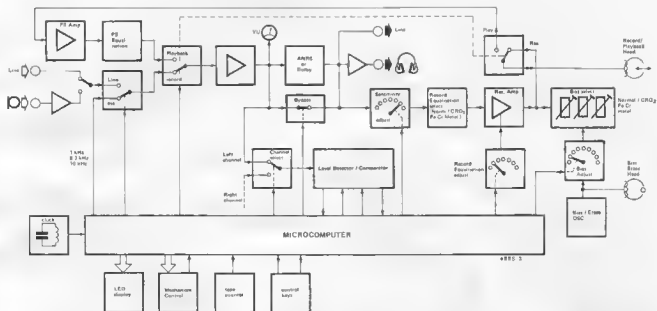
• Frequency Response (Recording/Playback at -20 VU)

| | |
|----------------------------|--|
| (Normal tape) | 15 Hz — 17,000 Hz (30 — 12,500 Hz ± 1 dB) |
| (SA/C/O ₂ tape) | 15 Hz — 18,000 Hz (30 — 12,500 Hz ± 1 dB) (at 0 VU: 25 — 8,000 Hz ± 3 dB) |
| (Metal tape) | 15 Hz — 18,000 Hz (30 — 12,500 Hz ± 1 dB) (at 0 VU: 25 — 12,500 Hz ± 3 dB) |

- Signal to Noise Ratio : 58 dB (ANRS — off)
- Wow & Flutter : 0.035% (WRMS)
(IDIN 45 500 : 0.14%)
- Channel Separation : 35 dB
- Crosstalk : 65 dB
- FF/Rewind Time : 80 sec.
- Total Harmonic Distortion : 1.2%
- Third harmonic Distortion : 0.5%
(0 VU, 1 kHz, UD Tape)
- Dimensions (W x H x O) : 450 x 120 x 395 mm
- Weight : 11 kg

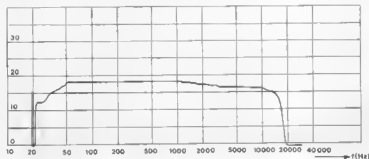
SELEKTOR

3

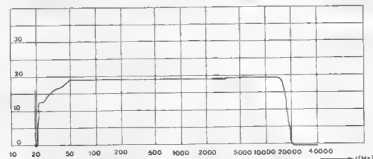


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4a



4b



Block diagram

In the same way that the flow chart gives a brief outline of the program, a block diagram will give some idea of the hardware involved (see figure 3). The switches and trimming potentiometers normally used are replaced by or supplemented with electronic circuits that are controlled by the microcomputer. Of the sections shown in the simplified block diagram, only a few require further explanation.

- ANRS or Dolby. This refers to the noise reduction circuit: ANRS is JVC's own version; Dolby is Dolby. . . .
- Recording equalisation select and Bias select. These sections are controlled by a three-way switch on the front panel. The first position is correct for both normal and most high-performance tapes (CrO₂, SA, XL-II, etc.); the second and third positions are for FeCr and metal tape, respectively. The corresponding equalisation characteristics are reasonably accurate for the various types of tape.
- Tape counter. Rapid and relatively precise 'tape position' information is obtained from a Hall device mounted on the mechanical tape counter; its output is fed to a counter in the microcomputer.

Results

The main specifications are given in table 1. It must be realised that these are 'guaranteed worst-case specs' — not just 'what you may achieve if you're lucky enough to use an ideally suited tape'

A single test may serve to illustrate this. In figure 4a, the frequency response of a standard tape is shown — as obtained with the preset equalisations and sensitivity adjustments. As can be seen, the response in this case is 2 dB down at 3 kHz and 4 dB down at 15 kHz. Not bad? Figure 4b shows the response that can be obtained with the same tape — after the computer has done its job!

It might be argued that the same result could be obtained with more accurate preset adjustment. Not so. As shown in table 2, the recording sensitivity at 1 kHz can vary by as much as 2.6 dB for 'high quality' tapes, and this can have a distinctly noticeable effect on the frequency response if a noise reduction system such as Dolby or ANRS is used. Furthermore, the variation in frequency response for 12.5 kHz signals with respect to the 1 kHz level may vary by as much as 4.7 dB for nominally 'identical' tapes. Even if the effect of a noise

Table 2
Sensitivity and frequency characteristics of tapes

| Tape No. | Sensitivity | Freq. Response |
|---------------------|-------------|----------------|
| Normal 1 | -0,4 | 0 |
| 2 | -0,7 | -0,2 |
| 3 | -0,1 | +0,1 |
| 4 | -0,8 | -0,7 |
| 5 | 0 | -1,6 |
| 6 | -0,7 | +1,7 |
| 7 | -0,7 | +0,1 |
| 8 | +0,6 | +3,1 |
| 9 | 0 | +2,8 |
| Deviation | 1,4 | 4,7 |
| CrO ₂ 10 | +0,9 | -1,5 |
| 11 | -1,2 | +0,2 |
| 12 | +0,9 | -1,6 |
| 13 | +1,4 | +1,1 |
| Deviation | 2,6 | 2,5 |

reduction system is disregarded, it is impossible to guarantee a response within ± 1 dB if only preset adjustment is used!

One final point. The full and honest specifications, as presented by JVC, may appear less than sensational in some aspects. The frequency response at 0 VU, for instance, seems rather poor; however, when recording 'normal music' this is irrelevant — the -20 VU response is more important for high frequencies. Similarly, distortion and signal-to-noise ratio (without ANRS!) may seem marginal, but they are in fact quite good for a compact cassette system. As J. Moorer put it at the recent AES convention in Brussels, when addressing representatives of the recording industry (amongst others).

"If we could get more on the tape, you would reduce the track width or the tape speed, wouldn't you? You've been doing it for years!" True enough — witness the compact cassette.

Victor Company of Japan (JVC)
Limited,
European liaison office
Kiestrasse 20
6 Frankfurt/M.90
West Germany. (465 S)

The shape of things to come?

A fully decoded 256 x 4 bit non-volatile (!) random access memory has been announced by General Instrument Microelectronics Ltd. This RAM/EAROM, designated the ER1711, is intended for applications where data is constantly changing and must be protected in case of a power failure. The device operates normally as a RAM with a 1.5 micro-second cycle time. When powering down, a single negative pulse applied to the Erase/Write control line

SELEKTOR

enters the entire contents of the 1024 bit memory into associated on-chip EAROM cells. All stored data is retained for 72 hours minimum after a 1 millisecond write pulse, or 30 days minimum after a 10 millisecond write pulse. Data can be recalled (restored into the RAM cells) by means of a power-up sequence followed by a bulk erase of the EAROM cells (a positive pulse on the Erase/Write control line).

The FR1711 is directly compatible with 4-bit microprocessors and typical applications include protection of process control state variables during power interruptions, in-machine and motor control to hold set points and feedback data, navigation equipment to hold constantly varying time and position data and cash registers for holding constantly changing cash totals. The FR1711 is available in both ceramic or plastic 22 pin dual-in-line packages.

General Instrument Microelectronics Ltd,
Regency House,
1-4 Warwick Street,
London W1R 5WB, U.K.

(465 S)

broadcast system which allows a computer to put together human speech. The system has been adopted by the UK Civil Aviation Authority and will be used to transmit in-flight weather reports from the summer of next year. Marconi says it has recorded the voice of one of its executives, Colonel John West, reading a range of standard weather report phrases, words and figures. These are converted into digital form and stored in a computer bank. When the computer is fed the latest telex report it automatically produces and arranges the sequence of words, phrases and figures needed to create a human voice report. Marconi, which has more than 20 years' experience in voice digitization for military use, believes this technique will be adopted for much wider use. For example, practically all broadcast announcements at airports and main-line railway stations could be constantly updated and issued by automation.

(470S)

15 kHz is enough for Golden Ears!

Everyone 'knows' that 20 kHz bandwidth is necessary for top-quality audio reproduction. Is it, though? For some time now, 'necessary bandwidth' has been the subject of heated discussions in the professional audio world.

The main reason for the sudden interest is the advent of digital audio. In digital systems, the audio signal must be 'sampled', and the sampling frequency determines the bandwidth. The sampling frequencies proposed vary between 32 kHz and 54 kHz - corresponding to theoretical audio bandwidths between 16 kHz and 27 kHz. At this point, the battle is joined. . .

Proponents of 32 kHz (broadcasting authorities, in particular) maintain that 'nobody heard the difference when we experimented with digital audio at a 32 kHz sampling rate'. 'No great trick', say the opponents, 'you've been using sharp 15 kHz low-pass filters for years'. Manufacturers of digital audio recorders introduce a new consideration: 'We can't sell digital recorders unless they at least equal the specs of conventional analog equipment. A bandwidth of well over 20 kHz is therefore essential'. At last year's AES convention in Hamburg, several groups announced that they were going to run tests to find the true bandwidth requirement for top-quality audio. This year, in Brussels,

the results of some of these experiments were reported.

One typical test series can be briefly described as follows. A special test signal, containing harmonics at almost full level to well over 25 kHz, was reproduced via suitable loudspeakers (ionophones). A group of critical listeners (recording engineers and other 'Golden Ears') were used as Guinea pigs. Several low-pass filters were evaluated, with cut-off frequencies of 15 kHz, 18 kHz and 20 kHz, with filter orders varying from 7th to 13th order and with and without group delay correction. Two loudspeakers were used; the signals could be the same (both filtered or both unfiltered) or one signal could be the original and the other after filtering.

The test subjects were asked to determine, by A-B comparison, whether or not there was any difference in the two signals. Note that no attempt was made at quality evaluation; the only question was: 'Can you hear any difference between the two signals?'. Since the only possible answers are 'yes' and 'no', random guesses would produce 50% accuracy. A 'significant' difference in this type of test is generally taken as more than 75%.

The results were perhaps somewhat surprising. . . Even with the 'worst possible' filter combination (15 kHz cut-off, 13th order, no group delay correction and two of these filters used in cascade), the percentage of 'correct' answers was only 62% for the most critical section of the test group. The percentage for the whole group was only 57%!

The conclusion drawn is that, even with a 15 kHz filter, differences will only be heard in extreme cases; signals with an extremely strong high-frequency content; a sufficiently broadband loudspeaker; listeners with exceptionally good hearing; and, finally, the possibility of direct signal comparison. An unlikely combination. . . It will be interesting to see the reaction in professional audio circles to these claims. Will it be ready acceptance ('OK, that's settled'), dogmatic refutation ('I don't believe it') or a call for further tests? It is interesting to note that at least three groups have already reached very similar conclusions: a representative of the broadcasting authorities, a record manufacturer and a manufacturer of digital audio tape recorders who has also introduced a digital audio disc system. . .

Based in part on AES preprint 1449, presented at the 62nd AES convention: 'What bandwidth is necessary for optimal sound transmission?'. G.H. Plenge, H. Jakubowski and P. Schöne.

UK system will operate in 1980

Britain's Marconi space and defence systems company believes it has found the answer with a new automatic

(468 S)

programmable timer/controller

The circuit described here is a versatile timer/controller, capable of switching 4 separate outputs on or off at 4 pre-programmed times every day. The circuit is ideally suited for the control of domestic appliances such as cookers, central heating, intruder alarms (to be switched on at night) etc., or can be used as a straightforward 24 hour 'radio-snooze-alarm' clock. Almost all the work is performed by a single IC, so that the circuit is both compact and relatively inexpensive.

The heart of the circuit is formed by the MM57160 standard timer and controller (STAC) chip from National Semiconductor. This IC is designed for use in timing applications where up to 4 separate outputs are required to operate at up to 4 user-programmed times. Thanks to direct display drive capability and on-chip keyboard scan facility, very little in the way of external hardware is required to provide a complete timer/controller system. The main features of the IC are summarised in table 1. An interesting facility is the provision of valid day programming, which allows control outputs to be inhibited on certain days (weekends, for instance).

Circuit design

The circuit diagram of the timer/controller is shown in figure 1. Timing is derived from the 50 Hz mains frequency at the secondary of the transformer and shaped by N1, N2 and N3. Mains transients are suppressed by the interference filter R1/C1. During the positive half cycle of the 50 Hz input signal C2 is rapidly discharged by N1. The capacitor takes much longer to charge up again, however, since this can only occur via R3, which is roughly 1000 times greater than R2.

The condition of each of the four outputs of the timer/controller chip (IC1) is indicated by a LED. Each output has a current capability of 20 mA but buffers are included to increase the maximum load current to 400 mA. It must be remembered that the use of the buffers inverts the output levels i.e. if the control output is low (0V) then the buffer output will be high (equal to + supply). This should be borne in mind when programming the system.

A stabilised power supply is provided, using a 78L08 regulator IC. Components R7 and C3 are included to ensure that the timer is reset upon switch-on. Initial conditions are: (real time) clock to 00:00; all set point times to 00:00 and all outputs off; all days valid; and the IC in the real time clock mode.

Programming

Programming is carried out using push button switches having up to three different functions and these are summarised in table 2.

Set point times (switching times) are loaded as follows:

- The DATA ENTRY switch is momentarily depressed to take the system from the real time clock mode to the data entry mode, whereupon one of the set point times is displayed and its outputs status indicated on the decimal points of the display. If the data entry mode is selected immediately after power-up, the display will show 00:00, with the decimal points off.

- To examine the next set point, the ADVANCE SET POINT switch is depressed. The four set point values are stored in a revolving stack, so that four advances will cause the stack to roll round to the original value.

- Set point times are loaded or altered using the SET HOURS and SET MINUTES switches. When depressed, these switches increment the hours displays from 0-23 and the minutes displays from 0-59 at a rate of one per second.

- Next, the SET STATUS switch is used to program the output(s) to be activated at the set point times. When the SET STATUS switch is initially depressed the first decimal point is turned on, signifying that output 1 will be activated at this time.

- If this is the only output to be activated, the ADVANCE SET POINT switch can be depressed to go on to the next set point.

- If, however, output 2, 3 or 4 is to be activated, the SET STATUS switch should be pressed again to advance to the subsequent outputs. Each advance turns off the previous decimal point (and output).

- If more than one output is to be activated, e.g. 2 and 4, the HOLD STATUS switch is used to hold number 2 decimal point on before the SET STATUS switch advances through 3 to number 4. Thus using the SET STATUS and HOLD STATUS switches it is possible to program any combina-

Table 1.

- 24 hour real-time clock with 4-digit display
- 4 control outputs
- 4 programmable set point times with repeat every 24 hours
- valid day programming to skip certain days if desired
- manual mode to verify programming
- each output can switch up to 400 mA

Figure 1. Complete circuit diagram of the timer/controller. If desired, the output buffers N4...N7 may be omitted.

tion of outputs to be activated at each set point.

- If an error is made during programming, operating the SET STATUS switch from position 4 will clear all data (including that set by HOLD STATUS), whereupon the correct information can be re-entered.

- The programmed information can be verified by using the MANUAL switch, which, when depressed in the data entry mode, transfers the decimal point status to the outputs, activating the appropriate relay, solenoid, etc. The system is returned to the real-time clock mode by depressing the DATA ENTRY switch a second time.

- To examine and alter the valid day information, the DAY MODE key is depressed, whereupon the current day

is displayed in the left-most display digit and the validity of the day in the right-most digit. A valid day is signified by '1', an invalid day by '0'. When depressed in the day mode, the SET DAY switch advances to the next day. The validity information can be altered by the SET STATUS switch. To return to the real-time clock mode the DAY MODE switch is pressed a second time.

- With the aid of the HOLD STATUS/DEMO switch it is possible to rapidly cycle through the entire programmed sequence. When this switch is pressed in the real-time clock mode, the clock advances at a rate of one hour per second, i.e. a 24 hour day can be verified in 24 seconds, whilst a 7-day week requires less than 3 minutes to check.
- To set the real-time clock to the cor-

1

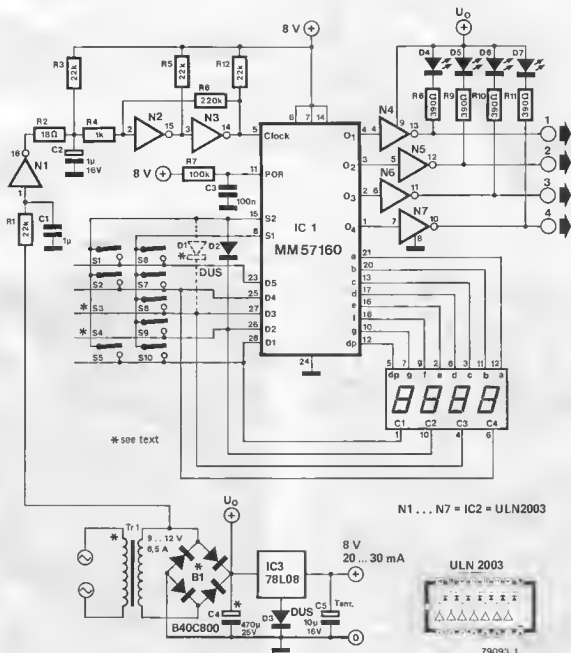
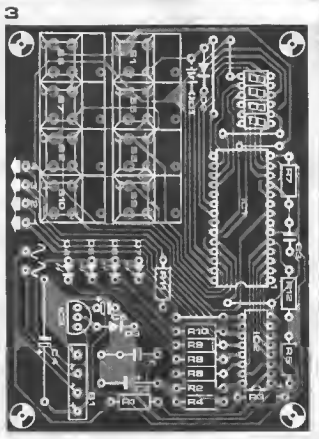
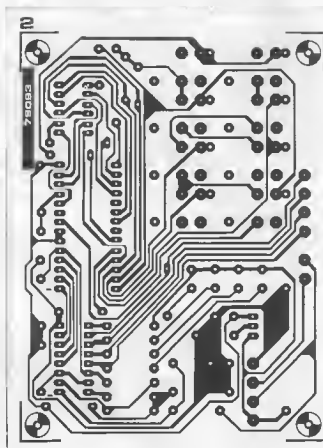


Table 2.

| KEY NO. | KEY SWITCH NAME | FUNCTION | | |
|---------|--------------------------------------|---|--|--|
| | | REAL-TIME CLOCK MODE | DATA ENTRY MODE | DAY MODE |
| 1 | MANUAL/ REMOTE TRANS- DUCER | Remote transducer input; forces output 1 ON, outputs 2-4 OFF until next valid set point after switch is off | Manual verification mode; allows data to be transferred to outputs 1-4 | (None) |
| 2 | HOLD STATUS/ DEMO | Allows rapid demonstration of sequence by advancing clock at rate of 1 hr/sec | Holds output N ON while programming advances to output N + 1, N = 1-4 | (None) |
| 5 | DATA ENTRY | Places unit in the data entry mode | RETURNS UNIT TO THE REAL-TIME CLOCK MODE | (None) |
| 6 | ADVANCE SET POINT/ RESET TIME | Resets time of day to 00.00 without changing set points but resets all days to valid | Advances display to the next set point so that it may be verified or altered | (None) |
| 7 | DAY MODE | Places unit in the day mode | (None) | RETURNS UNIT TO THE REAL-TIME CLOCK |
| 8 | SET STATUS | (None) | Controls programming of outputs; resets output N to "0" (unless preceded by HOLD key) and advances to output N + 1 | Alternates action key; changes day from valid ("1") to invalid ("0") and vice-versa |
| 9 | SET MINUTES | Advances minutes display of real-time clock | Advances minutes display of selected set point | (None) |
| 10 | SET HOURS/ SET DAY | Advances hours display of real-time clock | Advances hours display of selected set point | Advances display to next day—must be set to current day before returning to real-time clock mode |



Parts list

Resistors:

R1, R3, R5, R12 = 22 k
 R2 = 18 Ω
 R4 = 1 k
 R6 = 220 k
 R7 = 100 k
 R8, R9, R10, R11 = 390 Ω

Capacitors:

C1 = 1 μ (Siemens)
 C2 = 1 μ /16 V
 C3 = 100 n
 C4 = 470 μ /25 V*
 C5 = 10 μ /16 V, tantalum

Semiconductors:

D1*, D2, D3 = DUS
 D4... D7 = LED
 IC1 = MM57160 (National)
 IC2 = ULN 2003 (Sprague), XR 2203 (Exar),
 MC 1413 (Motorola) R.S. No. 307-108,
 IC3 = 78L08

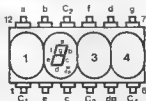
Miscellaneous

S1, S2, S5... S10 = Digitist pushbutton switch
 HP 5082-7414 display or equivalent
 T1 = transformer, 9 V*
 B1 = bridge rectifier, 840C800*

* see text

4

HP 5082-7414



79033 4

5



79033 6

rect time the SET HOURS and SET MINUTES switches are used. The clock time can be reset to zero by pressing the ADVANCE SET POINT switch in the real-time clock mode. The set point times remain unaffected by this operation, however it should be noted that it also resets the valid day information (i.e. all days are valid).

• Finally, the MANUAL/REMOTE TRANSDUCER switch provides a facility for external inputs. When pressed in the real-time clock mode, the programmed data is ignored, and output 1 is switched on whilst outputs 2...4 are turned off. On valid days this condition is maintained until the next set point time. On non-valid days all outputs are turned off as soon as the switch is opened.

Construction

For ease of construction a printed circuit board (figures 2 and 3) is available from the Elektor print service. Since the display is made entirely of plastic it may be unwise to solder it directly to the board but it can be mounted in an IC socket. The pin-out details for the display are given in figure 4 for those readers who may already possess a suitable type. It is often possible to pick up second-hand calculators and to extract the

displays from them, thereby saving money. The only condition is that the display must be common cathode. If the pin-out of the display is not known, it is possible to determine it by using a multimeter switched to a resistance range and checking each of the pins in turn to see which segment they light up. Use a discrete LED first to check that the meter is set to the right range.

Like the Beatles, some readers may have an application for an 8-day week cycle. This facility can be selected by wiring a switch in series with diode D1, or D1 can be mounted directly on the printed circuit board. Similarly diode D2, if removed from the board will enable the timer to be used with a 60 Hz mains frequency supply.

The choice of transformer, bridge rectifier and smoothing capacitor is determined by the maximum current consumption of the circuit, which in this case is 4 x 400 mA = 1.6 A. However, if the load current of each output is known to be less than the maximum, it is a simple matter to calculate the desired transformer current ratings.

As a rule of thumb the value of the electrolytic can be calculated on the basis of 2000 μ F per amp. The values shown in the circuit diagram for the

Figure 2. Track pattern of the printed circuit board for the timer/controller (EPS 79093). As can be seen there are a considerable number of connections to the displays and to the keyboard. The use of a printed circuit board reduces the amount of work and increases the reliability of the circuit.

Figure 3. Component overlay of the printed circuit board. Diode D1, (see text) is shown in dotted lines. If a different type of display is used, then it may not fit on the board, in which case separate connections will be necessary.

Figure 4. Pin-out of the HP 5082-7414. The segments are indicated by the small letters, whilst C1, C2 etc. stand for the cathode of the first display, second display, and so on.

Figure 5. Layout of the keyboard.

power supply components are sufficient to drive several relays (12 V/20 to 50 mA). The relays, like the LEDs and their resistors, can be connected to the unbalanced supply (positive end of C4).

One should check to ensure that the stabilised supply is satisfactory. With a voltage between 8 and 9.5 V trouble-free operation should be guaranteed. There is in fact no need for the supply voltage to exceed 8 V, and if one measures a voltage of more than 8.6 V, diode D3 can safely be omitted. However if for some reason the voltage regulator provides less than 8 V, the diode must be included.

Upon switch-on the displays should show '0000'. If this is not the case then pin 11 of IC1 should be grounded providing an additional reset pulse. If the display still refuses to reset then there is a fault in the circuit (defective IC, bad solder joint, etc.).

It may at first sight appear that programming the timer is rather a complicated process. However with a little practice it is possible to enter and check (using the DEMO and MANUAL switches) a program extremely quickly. The following sample program should help to familiarise prospective users with program entry and operation.

M

To illustrate how the timer/controller can be programmed, assume that it is required to perform the following operations:

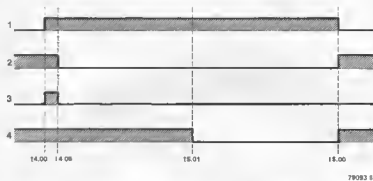
1. Output 1 should turn on at 14.00 and turn off at 16.00 each valid day.
2. Output 2 should turn off at 14.05 and turn back on at 16.00 each valid day.
3. Output 3 should turn on at 14.00 and turn off at 14.05.
4. Output 4 should turn off at 15.01 and turn on again at 16.00.
5. Valid days are Monday to Friday inclusive. Saturday and Sunday are invalid days.
6. The current day is Monday, the time is 13.00.

From the above information we can construct the following 'truth table'.

| time | 01 | 02 | 03 | 04 |
|-------|----|----|----|----|
| 14.00 | 1 | 1 | 1 | 1 |
| 14.05 | 1 | 0 | 0 | 1 |
| 15.01 | 1 | 0 | 0 | 0 |
| 16.00 | 0 | 1 | 0 | 1 |

The states of each output are illustrated in the timing diagram.

To load the above program into the chip memory the following sequence of key strokes is used.



79032 5

This timing diagram illustrates the changes in output states at the four set point times.

| SWITCH DEPRESSED | DISPLAY | REMARKS |
|-------------------|----------|--|
| DATA ENTRY | 0000 | Initial display |
| SET HOURS | 1400 | Switch is depressed until first set point time is displayed. |
| SET STATUS | 1.400 | Set point 1 at 14.00 (2 p.m.), output 1 ON |
| HOLD STATUS | 1.400 | Hold output 1 ON |
| SET STATUS | 1.4.00 | Output 2 ON |
| HOLD STATUS | 1.4.00 | Hold output 2 ON |
| SET STATUS | 1.4.0.0 | Output 3 ON |
| HOLD STATUS | 1.4.0.0 | Hold output 3 ON |
| SET STATUS | 1.4.0.0. | Output 4 ON |
| ADVANCE SET POINT | 0000 | All the above status information is stored in memory, and at 14.00 hours all four control outputs will be turned on. |
| SET HOURS | 1400 | Switch is depressed until second set point time (hours) is displayed. |
| SET MINUTES | 1405 | Switch is depressed until correct set point time (minutes) is displayed. |
| SET STATUS | 1.405 | Set point 2 at 14.05 hours (2.05 p.m.), output 1 ON |
| HOLD STATUS | 1.405 | Hold output 1 ON |
| HOLD STATUS | 1.4.05 | Output 2 ON |
| SET STATUS | 1.4.0.5 | Output 2 OFF, output 3 ON (second decimal point is extinguished, third decimal point turns on) |
| SET STATUS | 1.405. | Output 3 OFF, output 4 ON |
| ADVANCE SET POINT | 0000 | The status information for the second set point is stored. |
| SET HOURS | 1500 | Switch is depressed until third set point time (hours) is displayed. |
| SET MINUTES | 1501 | Third set point time (minutes) is displayed |

| | | |
|-------------------|--------|---|
| SET STATUS | 1.501 | Set point 3 at 15.01 hours (3.01 p.m.), output 1 ON. No other output is required so the next step is simply to store this status information. The status information for the third set point is stored. |
| ADVANCE SET POINT | 0000 | Switch is depressed until fourth set point time is displayed. |
| SET STATUS | 1.600 | Set point 4 at 16.00 hours (4.00 p.m.), output 1 ON |
| SET STATUS | 16.00 | Output 1 OFF, output 2 ON |
| HOLD STATUS | 16.00 | Hold output 2 ON |
| SET STATUS | 16.0.0 | Output 3 ON |
| SET STATUS | 16.00. | Output 3 OFF, output 4 ON. Output 2 and 4 are now programmed to turn on at the fourth set point. All that remains is to transfer this status information to memory |
| DATA ENTRY | 0000 | Current status information stored in memory, return to real-time clock mode. It would also have been possible to press the ADVANCE SET POINT switch, in which case the first set point and status would have appeared (i.e. 1.4.0.0.) |
| DAY MODE | 1 1 | The timer is now programmed with valid day information. The first digit indicates the day, the second digit represents status information |
| SET DAY | 2 1 | Also valid day |
| SET DAY | 3 1 | Also valid day |
| SET DAY | 4 1 | Also valid day |
| SET DAY | 5 1 | Also valid day |
| SET DAY | 6 1 | A non-valid day, therefore . . . |
| SET STATUS | 6 0 | |
| SET DAY | 7 1 | This should also be a non-valid day, so . . . |
| SET STATUS | 7 0 | |
| SET DAY | 1 1 | Return to current day |
| DAY MODE | 0000 | Return to real-time clock mode. |

The program can be checked by pressing the DEMO switch. As soon as this switch is depressed the clock will advance at a rate of 1 hour per second, lighting up the output LEDs in accordance with the

program. Remember, however that because of the buffers the LEDs will indicate the inverse of the chip output states. Finally, the clock can be set to the correct current time using the SET HOURS switch.

switching mains-powered equipment

Electronic relays

The programmable timer/controller, described elsewhere in this issue, is not really complete. It cannot be used to switch aquarium lighting and heating, for instance — not directly, that is. If mains powered equipment is to be switched on and off by electronic circuits like the timer/controller, something more is required: an (electronic) relay.

The programmable timer/controller will often be required to switch mains-powered equipment. One possibility would be to use the old and trusty mechanical relay, but this does have certain disadvantages. Being mechanical, the relay is relatively slow and prone to wear. Furthermore, it is rather bulky. For these reasons, it makes sense to use an up-to-date electronic replacement: the triac.

In industrial applications, the tendency is to use what is known as a 'solid state relay': a triac with associated electronics. Four examples of this type of reliable and silent electronic relay are described here.

The circuits are described in order of sophistication; each one can be used to replace mechanical relays, and even the simplest circuit is an improvement.

Optocoupling for safety.

There are two main reasons for using relays: a small control current can be used to switch a large load current, and the load is electrically isolated from the control circuit. This 'electrical isolation' refers to the fact that no current can flow from the load back to the control circuit. In other words, even if the load is connected to the mains it is still safe to touch the control circuit.

In a mechanical relay, isolation is given by the fact that the relay coil is not connected to the relay contacts. When it comes to the more up-to-date electronic version, this simple safety precaution is often omitted: the control circuit is connected direct to the triac and, with it, to the mains.

In most applications, it is advisable to restore the isolation between the two parts of the circuit. Some way must be found to transmit the control signal to the triac without any actual electrical connection. The obvious transmission medium, nowadays, is light. If the control circuit is arranged to light an LED and a photo-transistor is used to trigger the triac, electrical isolation can be maintained. When LED and photo-transistor are mounted in one package, the complete unit is known as an opto-coupler.

Synchronous or asynchronous?

Switching the mains voltage can be done in several ways. At this point, our main interest is the difference between synchronous and asynchronous switching. Synchronous switching refers to the fact that the load is turned on or off at the zero-crossing of the mains voltage (or current). This has the advantage that interference pulses are reduced to a minimum. By now, everyone will have heard (or at least heard of) the horrible radio and TV interference that inferior lighting dimmers can cause!

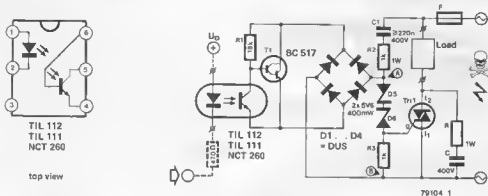
Theoretically, synchronous switching has one draw-back: the load is not switched on or off immediately. The circuit must 'wait' for a zero-crossing. However, since zero-crossings occur every 10 milliseconds, it is rare indeed for this to be a problem. Nobody is going to worry about an aquarium heater being turned off 10 ms late! The only reason why synchronous switching has not become standard practice is that the control circuit it requires is more expensive...

Circuit 1: simplicity itself.

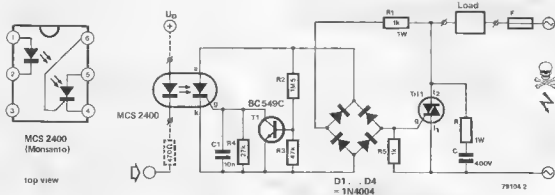
A simple, reliable circuit for a solid state relay is given in figure 1. In this circuit, the load is not turned on at the zero-crossing of the mains, but it is switched off in synchronism. As in virtually all triac circuits, synchronous turn-off comes free: the triac turns off when the current through it drops below a certain minimum value, the so-called hold current.

The link to the timer/controller — or whatever other control circuit is used — consists of an opto-coupler. When sufficient current is passed through the LED, the photo-transistor will conduct. This, in turn, causes the 'darlington transistor' T1 to turn off, so that very little current can flow through the bridge circuit. (Note that two BC107s in cascade can be used instead of T1). In effect, the bridge circuit no longer forms a 'short' between points A and B, so that the voltage between these points can rise above the 'zener' voltage determined by D5 and D6. Depending

1



2



on the phase of the mains voltage, one of these diodes will be forward-biased (giving a 'normal' forward voltage drop of approximately 0.7 V) and the other will be reverse-biased. No matter what the phase, the voltage across the two diodes will therefore be just over 6 V. The triac now receives gate current (via these two diodes, R2 and C1), so it turns on — switching on the load. If the LED in the opto-coupler is not driven, the photo-transistor will turn off. As the voltage between points A and B rises after a zero-crossing of the mains, T1 will now turn on. This limits the voltage to two 'diode drops', two 'base-emitter drops' and the saturation voltage of T1 — about 3 V in all. Not enough to cause the zener diodes to conduct, so no gate current flows to the triac. The load is switched off.

In this circuit, the load is turned on when a current of 5 mA or more flows through the LED in the opto-coupler. The connection to the programmable timer/controller is shown in dotted lines: the anode is connected to the positive supply and the cathode to one of the four control outputs via a 470 Ω resistor.

The resistor R and capacitor C, connected across the triac, are especially important when switching inductive loads. The values depend on the type of load, as explained elsewhere ('RC network').

An improvement: synchronous switching

As explained above, it is usually better to switch the load at the zero-crossing of the current through the triac. In this way, interference 'spikes' can be reduced to a minimum. Turning off at the zero-crossing is no problem, as we have already seen: the triac takes care of this. Turning on is a different matter. Some way must be found to ensure that the triac is switched on when the voltage across it is zero — or 'as near as makes no muchness'. To put it another way: the triac must not be turned on halfway through a (mains) period, when the voltage is nowhere near zero.

The circuit shown in figure 2 takes care of this. In this case, the link to the control circuit is an opto-coupler consisting of an LED and a photo-thyristor. The gate current for the triac flows through R1, the diode bridge and

this photo-thyristor; the thyristor is turned on when it is illuminated by the LED — provided its gate is not shorted by T1. During most of the mains period, the voltage across the bridge circuit is sufficiently high to turn on T1: the voltage has to be less than about 20 V for T1 to turn off. Only at this point — close to the zero-crossing — can the photo-thyristor be triggered, turning on the triac. On the other hand, once the thyristor is triggered T1 cannot turn on, so that gate drive to the triac will not be interrupted.

When more than 10 mA is passed through the LED in the opto-coupler, the load will be switched on at the next zero-crossing. The connections to the programmable timer/controller are again shown in dotted lines; the values for the series connection of a resistor and a capacitor across the triac can be found from the separate explanation (see 'RC network').

Continuous drive for small loads

Both of the circuits described so far are reliable, provided the load is sufficient. One of the characteristics of triacs, however, is that they 'extinguish'

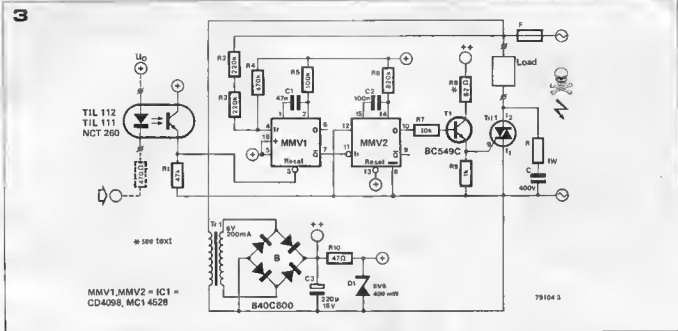
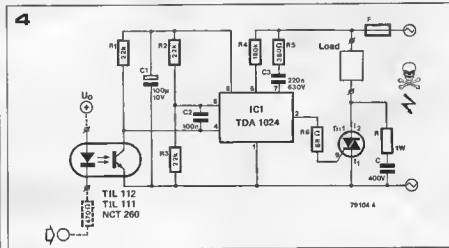


Figure 1. A straightforward electronic relay. The load is not switched on during the zero-crossing of the mains waveform — except by sheer chance.

Figure 2. An improved circuit that provides mains-synchronous switching.

Figure 3. A rather more complicated circuit is required for switching small loads. Gate current for the triac is maintained during the whole 'on' cycle.

Figure 4. A specially designed IC, the TDA 1024, can also be used. Broadly speaking, this circuit does the same as that shown in figure 2.



(cease to conduct) if the current passed through them falls below a certain value, known as the 'hold current'. This is not always a disadvantage: in the two circuits described above it is this characteristic that ensures that the load is turned off at the zero-crossing of the current. It does, however, become a drawback when the load is so small that the load current is less than the hold current. Fortunately, a triac will always conduct if its gate current is sufficient — regardless of whether the main current is sufficient to 'hold' it. For small loads, therefore, the gate current must be maintained for as long as the triac is to remain 'on'. This can be achieved as shown in figure 3, using two monostable multivibrators in a CMOS IC. The first monostable (MMV 1) provides 1 ms pulses at the positive-going zero-crossings of the mains waveform; the necessary trigger pulses are derived from the mains by means of R2, R3 and R4. Note that two resistors in series are used, so that only half the mains voltage is dropped across each — ¼ watt resistors cannot normally withstand more than about 250 V. For output pulses to be produced, the 'reset'

input must be high; this is the case when the photo-transistor in the opto-coupler is conducting.

The output pulses from the first monostable are used to trigger MMV 2. This second monostable provides 35 ms output pulses — equal to almost twice the period time of the mains waveform. These pulses are used to turn on T1, providing gate current to the triac so that the load is switched on.

When no current flows through the LED in the opto-coupler, the photo-transistor will block, causing the reset input of MMV 1 to go 'low'. No further pulses will be produced, so that at the end of the current 35 ms pulse T1 and the triac will cease to conduct, switching off the load.

The CMOS IC and transistor in this circuit require a low, positive supply voltage. When the load is to be switched on, gate current must be supplied continuously (approximately 100 mA). This effectively rules out the use of a series resistor and diode to derive the supply voltage from the mains: some 20 W would be dissipated in the resistor! For this reason, a small transformer and bridge rectifier are used. The 'raw'

supply (approximately 9 V) is used for T1; the supply to the CMOS IC and photo-transistor is stabilised with a zener diode.

The transformer secondary voltage is not particularly critical. If it is significantly more than 6 V, however, the values of R8 and R10 should be increased accordingly. Certain types of triacs may prove to require an exceptionally high gate current or be satisfied with an exceptionally low current, in which case the value of R8 can be modified. Nine times out of ten the value given should be correct.

It should be noted that both the primary and the secondary side of the power supply are connected to the mains! Under no circumstances should the same supply be used for another circuit — the control circuit, for instance. The complete circuit shown must be seen as an isolated unit: the 'only' connections to the 'outside world' are the mains and load connections and the drive to the LED in the opto-coupler. The connection to the programmable timer/controller has already been described; the RC series-connection across the triac is discussed elsewhere.

Finally: a special IC

A special integrated circuit for triac control is available from Philips; the TDA 1024. It was used in the 'solid-state thermostat' described in last year's 'summer circuits' issue; a modified circuit for opto-coupler drive is given here (figure 4).

When the photo-transistor in the opto-coupler is illuminated, the IC starts to produce mains-synchronous pulses to trigger the triac. The width of the pulses is determined by R4; with the value given, a pulse width of approximately 150 μ s is obtained. When switching small loads (a 40 W lamp, say) it is advisable to increase the value of R4 to the maximum permissible (820 k) so that the pulse width becomes 650 μ s. The gate current is equal to 6 V divided

by the value of R6; approximately 90 mA with the value shown. Since the trigger pulses are quite short, the supply to the IC can be derived from the mains via a dropper resistor and capacitor (R5 and C3). The advantage of using a capacitor is that the phase shift leads to a much lower power dissipation.

Constructional notes

The most important thing to watch in this type of circuit is the electrical safety. Every part of the circuit, with the exception only of the connections to the LED in the opto-coupler, is connected to the mains. Careful construction is therefore a must.

The choice of triac is determined mainly by the maximum load current. In some

cases, switch-on surges can occur that are several times the nominal load current - particularly when switching motors, but to a lesser extent also if the load consists of incandescent lamps or heaters. The triac must obviously be rated accordingly. The same applies to the fuse, F; a 'slo-blo' type is preferable. Adequate cooling is required for the triac. Note that the heatsink will also be connected to the mains, unless a mica insulating washer is used.

Where resistor 'wattage ratings' or capacitor working voltages are specified, these should be adhered to - of course. Capacitor C should also have a working voltage of at least 400 V. In all other cases, $\frac{1}{4}$ W resistors and 'normal' capacitors can be used.

The RC network

In each of the circuits, an RC network is connected across the triac. This network is intended to prevent the triac turning on at the wrong moment, or even being damaged. Two things must be prevented in any triac circuit: an excessively high voltage across the triac and an excessively rapid increase in this voltage.

Too high a voltage simply causes the triac to 'break down'. Triacs are commonly rated at 400 V, and 630 V types are also available. At first sight, 400 V seems an ample rating. However, when one considers that the peak voltage on a 245 V mains supply is approximately 346 V and that variations in the nominal supply voltage of $\pm 10\%$ are quite possible, the safety margin becomes alarmingly small.

The second point, an 'excessively rapid increase in the voltage across the triac', is perhaps less obvious. Most triacs can withstand a voltage increase at a rate of 200 volts per microsecond; a faster increase may cause the triac to turn on. One way to limit the rate of change would be to connect a 'fat' capacitor across the triac. However, if the triac is then triggered at a point where the capacitor is charged, the heavy surge current would almost certainly damage the triac. For this reason, a series resistor *must* be included. The minimum value can be calculated from the maximum voltage and current rating; for a 6 amp triac, for instance:

$$R = \frac{V_{\max}}{I_{\max}} = \frac{346}{6} \approx 58 \Omega$$

A further point to watch is the effect of an (even partly) inductive load. The RC network across the triac and the RL network formed by the load together represent a series RLC circuit. If this resonant circuit is insufficiently damped (damping $d \leq 1$) oscillation can occur - with the triac switching on and off at a frequency determined by the RLC network. At the same time, the voltage can swing up to above the maximum rating of the triac... When selecting the resistance value, therefore, the damping in the resonant circuit must

also be estimated. If all resistances are taken together as R_{tot} and the inductances are summed in the same way, the damping is given by:

$$d = \frac{R_{\text{tot}}}{2\sqrt{\frac{L}{C}}}$$

Since the whole idea is to damp out voltage spikes with a capacitor, it is logical to use a 'fat' one. In practice, 47 n... 100 n/400 V... 630 V will normally be used. The series inductance of mains wiring and load can be estimated as 100 μ H in most applications (barring truly inductive loads). If the load consists of, say, a 60 W lamp (with a resistance of 1 k) and a 56 Ω resistor is used for R, the damping will be:

$$d = \frac{1056}{2\sqrt{\frac{100 \cdot 10^{-6}}{47 \cdot 10^{-9}}} \approx 11.7$$

Adequate. No problems are to be expected until the load resistance becomes less than about 36 Ω (equivalent to a good 1600 W). If loads in excess of this are to be switched, a larger capacitor value will be required. The maximum rate of voltage increase occurs if the triac is triggered at the peak of the mains voltage. In the example given, it is equal to:

$$\frac{dV}{dt} = \frac{RV}{L} = \frac{56 \cdot 346}{100 \cdot 10^{-6}} \approx 193 \text{ V}/\mu\text{s}$$

This is just within the safe limit.

The problems associated with inductive loads can be illustrated with a simple example. Let us assume that a fluorescent lamp with its associated ballast is to be switched. Common values for the resistance and inductance of the ballast are 200 Ω and 1 H, respectively. The damping is therefore approximately equal to:

$$d = \frac{250}{2\sqrt{\frac{1}{47 \cdot 10^{-9}}} \approx 0.03!$$

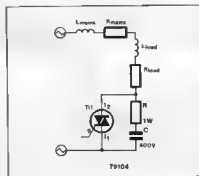
The result? Oscillation, and the lamp will refuse to go out. The obvious remedy is to increase the value of R, the minimum value (for $d = 1$) can be calculated as follows:

$$R_{\min} = d \cdot 2\sqrt{\frac{L}{C}} = 1 \cdot 2\sqrt{\frac{1}{47 \cdot 10^{-9}}} \approx 10 \text{ k}$$

The rate of change must be checked with these new values:

$$\frac{dV}{dt} = \frac{10 \cdot 10^3 \cdot 346}{1} = 3.46 \text{ V}/\mu\text{s}$$

Perfectly safe.



Summary

For 'normal' loads (incandescent lamps, heating elements etc.) up to 1 kW, a 6 A triac can be used. In this case, a safe value for R is 56 Ω /1 W and a good capacitor value is 47 n/400 V. There is no harm in playing it safe: the capacitor value can be increased to 100 n and the working voltage to 630 V if desired. For 10 A triacs (loads up to 1600 W), the resistance value can be decreased to 39 Ω , provided a 100 n capacitor is used. The same values can be used for 15 A triacs; 27 Ω and 150 n or 220 n are also permissible in this case.

When switching fluorescent lamps (note that 'dimming' is not possible with these circuits!) the value of R will have to be increased considerably - to over 10 k. If other 'odd' loads are to be switched, the corresponding values for R and C can be calculated as described above.

random tune doorbell

(A Houghton)



The circuit diagram of the 'random tune' doorbell is shown in figure 1. As can be seen, it basically consists of two squarewave generators, a counter, and a current controlled oscillator. The frequency of the first squarewave generator (N1/N2) can be varied between approx. 12 and 900 Hz, whilst that of the second generator (N3/N4) is roughly 1 kHz. The counter, IC3, is enabled when the clock enable input is taken low. However due to the integrating effect of C3/R4, the negative going edge of the first squarewave enables the counter for only a brief period. The count is only incremented when a positive going edge from N3/N4 coincides with a negative pulse from N1/N2.

The doorbell thus functions as follows: When the pushbutton switch S1 is in the open position, pin 15 (reset) of IC3 is high and the counter is inhibited. If S1

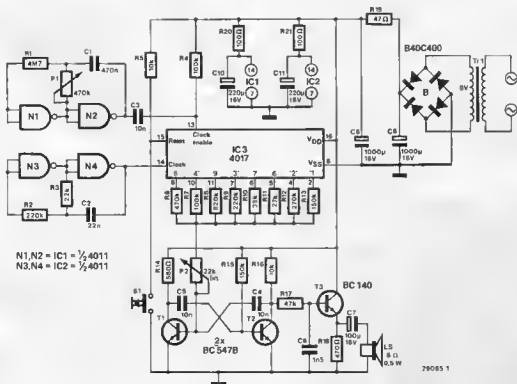
is pressed, then the first time that a clock enable- and clock pulse coincide, the counter will increment to '1'. The counter will remain in this state until a clock pulse again coincides with a clock enable pulse, whereupon the counter is once more incremented. Thus each of the counter outputs is taken high in turn.

The outputs are commuted via resistors R6 ... R13 and fed via P2 to the current controlled oscillator T1/T2. Thus the value of whichever output resistor is high, together with the setting of P2, determine the pitch of the oscillator signal. The result is a semi-random tune, in which the length of each note is dependent upon the length of time between clock-enable and clock pulses coinciding.

In order to introduce a pause between successive cycles of the counter, output

0 of the counter is left floating. Similarly, by leaving output 5 (pin 1) unconnected, each 'phrase' will consist of two groups of four notes, separated by a rest. Thus the 'tune' will always have a certain basic 'shape', regardless of variations in the length of successive notes. In order to eliminate the possibility of the two squarewave generators influencing one another, i.e. tending to synchronise, it is advisable to use separate 4011's for each.

1



delay lines (2)

Having dealt with reverberation and echo in a previous article (see *Elektor* 46, February 1979) we now take a look at how delay lines can be used to achieve a wide variety of interesting special effects such as double tracking, vibrato, phasing, chorus etc. Such applications are of particular interest to the amateur musician since they can be implemented using relatively short delay lines and hence at comparatively low cost. The article is rounded off with a look at the contribution of delay lines to studio recording techniques and sound reinforcement systems.

Unlike reverberation and echo, such effects as vibrato, phasing, flanging, chorus and string ensemble can be obtained using comparatively short delay lines. In practice, a single bucket-brigade memory is often all that is required. As we shall see, most of the effects mentioned above are achieved by varying the frequency at which the audio signal is clocked through the delay line, however there is one commonly used technique where this is not the case.

Automatic Double Tracking (ADT)

The block diagram of figure 1 illustrates the simplest application of a short delay line, in which the audio signal is delayed by approx. 1 to 5 ms and then summed with the direct signal. The result is that a solo voice or instrument is made to sound 'fuller' or stronger, since the human ear is unable to distinguish between the original and delayed signals and has the subjective impression of increased volume. The actual increase in signal amplitude, however, is considerably smaller than the perceived increase in volume (which can be anything up to 6 dB); thus there is no danger of equipment overload on signal peaks. If several double tracking elements are connected in cascade, a multiple voice effect is obtained, this being the first step towards 'chorus'.

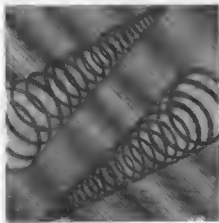
Chorus

True chorus effect is obtained when the delay time is not constant, but is subject to small variations. In the case of both digital delay lines and analogue 'bucket-brigade' memories the delay time is determined by the clock frequency and by the length of the delay line. Thus the delay time can be varied by using a voltage controlled oscillator as clock generator, which is modulated by a low frequency random voltage generator (see figure 2a). In practice more than one delay line is used. The circuit shown in figure 2b consists of 4 delay lines, each of which is independently varied by a random clock signal. The principle of chorus generation is to simulate the effect of a multiplicity of sound sources - as are present in a voice or string section of an orchestra.

Although a group of instruments may be required to play the same note, due to variations in the phase relationship of each sound the human ear perceives that several instruments are present. These phase discrepancies are caused by slight differences in the mechanical construction of similar instruments, differences in the musicians' technique and in the different path lengths which the sounds must travel to the listener or recording microphone. Thus randomly varying the length of the delay lines ensures that the phase relationship of the output signals is constantly changing, thereby producing a multiple image effect. For simulation of complex orchestral sounds, in particular those of stringed instruments, the arrangement of figure 2c is used. The modulation signals of the clock generators (VCOs) are periodic, not random, and are locked out-of-phase with one another. The result is that whilst the delay time of one line will be increasing, the delay time of another will be decreasing, and vice-versa. As the length of the delay lines are varied, so is the phase relationship of the signals at the output. A second 'fast' modulation signal superimposed on the clock frequencies has the effect of further enhancing the pattern of phase differences and produces a rich, heavily textured sound composed of an apparent multiplicity of separate instruments.

Vibrato and Phasing

If a periodic clock frequency signal is used instead of a random clock signal, vibrato and phasing can be obtained. Figure 3a shows a basic circuit for vibrato, whilst 3b illustrates how phasing can be achieved. As can be seen the basic difference in the two circuits is that the vibrato signal is taken directly from the output of the delay line, whilst in the case of phasing, the delayed and direct signals are summed. Vibrato essentially involves alternately speeding up and slowing down the sampled signal as it progresses through the delay line. Since the rate at which the signal enters the delay line is different from that at which it exists, the result is variations in the pitch of the



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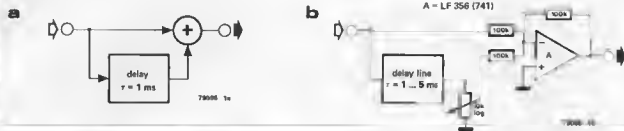
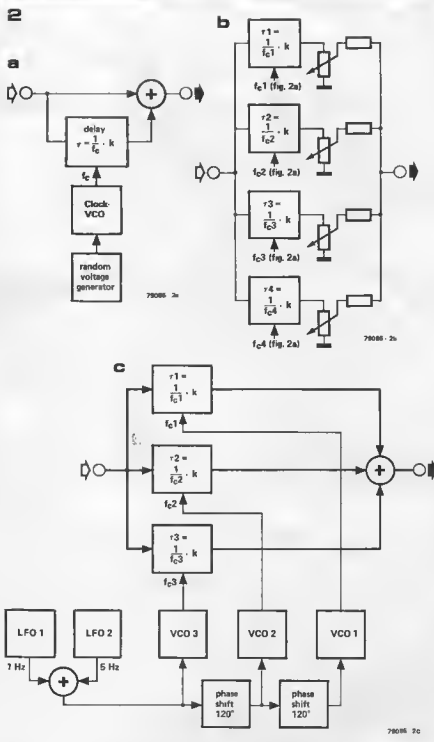


Figure 1. Basic principles of ADT - automatic double tracking. A very slightly delayed version of the audio signal is summed with the original. The result is that the signal is intensified, without a significant increase in signal amplitude. Figure 1b shows a practical circuit for such an arrangement.

Figure 2a. Block diagram of a basic chorus generator. By randomly varying the clock frequency of the delay line the changing phase relationships between the direct and delayed signals produces the effect of a multiple sound source similar to that of a voice choir.

Figure 2b. In practice more than one delay line is normally used. In the circuit shown here, there are four delay lines, the clock frequencies ($f_{c1} \dots f_{c4}$) of which are independently varied by separate random voltages.

Figure 2c. For string ensemble effects a multiple phasing unit of the type shown here is used. The principle involved is similar to that of the circuit in figure 2b, however in contrast to the above circuit the clock frequencies of the delay lines are modulated by periodic (not random) signals. In fact two modulators are used, one 'fast' and one 'slow', and the modulation signals to each VCO are held in a fixed out-of-phase relationship. When the outputs of the delay lines are summed, the periodic variations in the delay time of each line lead to highly complex phase patterns which lend the resultant sound a rich, vibrant quality characteristic of a string section.



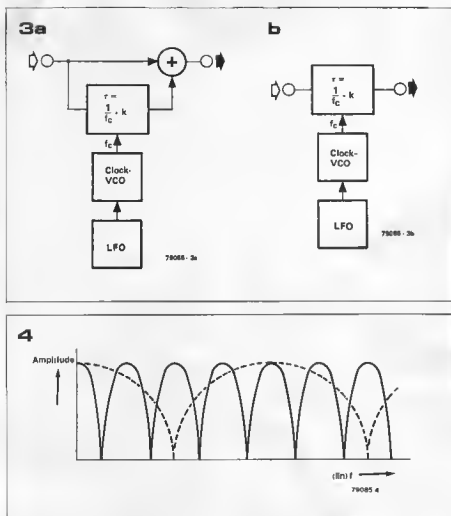


Figure 3. Basic circuit arrangement for phasing (3a) and vibrato (3b). In both cases the clock frequency of the delay line is modulated by a low frequency oscillator. The difference between the two effects is that for phasing, the delayed and direct signals are summed. The result of the shifts in phase between these signals is that the response of the sum signal exhibits a series of attenuation notches which are swept up and down the audio spectrum. The vibrato signal consists simply of the output of the delay line. The variations in phase of the delayed signal amount to frequency modulation, i.e. the pitch of the signal is periodically varied about a centre frequency.

Figure 4. Varying the clock frequency of the delay line has the effect of varying the distance between successive attenuation notches in the signal's response. It is this which produces the characteristic phasing effect.

Figure 5a. Block diagram of a frequency modulator which can be used as the basis for a special effects unit providing phasing, vibrato, chorus, ADT etc.

Figure 5b. Circuit diagram of a frequency modulator using the TDA 1022. The circuit is based on a manufacturer's application note (Mullard).

Figure 5c. Circuit of a suitable lowpass input filter for use with delay lines. The turnover frequency of the filter is 15 kHz and the filter roll-off is 24 dB per octave.

signal, i.e. frequency modulation. Relatively short delay times are used (approx. 5 ms), which means that high clock frequencies are possible and hence input signals with a wide bandwidth can be processed in this way.

The modulation rate is normally in the region 5 to 10 Hz. The modulation depth (i.e. the extent to which the signal frequency is shifted up or down) of the vibrato signal is determined by the average delay time of the delay line, the modulation depth of the clock signal and the rate of modulation (vibrato frequency). Thus with a delay time of e.g. 5 ms, a variation in clock frequency of $\pm 5\%$ about an average value, and a vibrato frequency of 10 Hz, the signal frequency will vary by $\pm 3.14\%$. As a comparison, the musical interval of one semitone corresponds to a frequency change of just under 6%.

Phasing is an effect which is extremely popular with many musicians, and one which is very difficult to describe! Many people liken it to the effect of passing the sound through a long tunnel, or describe it as a 'wooshing' effect, the music seeming to 'breathe' in and out in a regular rhythm.

This highly individual sound is obtained by summing the direct and delayed signals. At frequencies where the delay is equal to an odd number of half periods of the signal frequency the

direct and delayed signals will be 180° out of phase and therefore cancel. Conversely, at frequencies where the delay time is equal to an even number of half periods, the two signals will be in phase and reinforce. The result is a series of attenuation notches in the response of the signal at the odd harmonics of the fundamental. The process is the equivalent of passing the audio signal through a comb filter. The distance between successive notches is inversely proportional to the delay time, and is in fact equal to $\frac{1}{\tau}$, where τ is the delay time. Thus with $\tau = 10$ ms, the frequency response of the output signal will exhibit a notch every 100 Hz. By cyclically varying the delay time (by low frequency modulating the clock oscillator) the distance between successive peaks in the response is also varied (see figure 4), and it is this which produces the characteristic phasing effect. Delay times for phasing are normally between approx. 1 and 20 ms, whilst the modulation signal from the low frequency oscillator is generally a sine wave or triangle, with a frequency between roughly 0.05 Hz (i.e. one complete cycle every 20 seconds) and 1 Hz.

Frequency Modulator for Chorus, Phasing and Vibrato

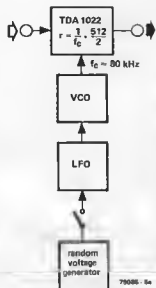
Figures 5a and 5b show the block diagram and circuit diagram respectively of

a frequency modulator using the TDA 1022 bucket-brigade memory. This circuit forms the basis of an audio effects unit for chorus, phasing and vibrato. A simple VCO built round two BC 337 (or BC 107) transistors provides the clock signal, whose frequency can be modulated by means of a separate sine wave oscillator. The frequency of this vibrato oscillator can be varied between 0.5 and 7 Hz by means of a 100 k potentiometer. The modulation signal is fed to the VCO via an emitter follower, whose emitter resistor is formed by a potentiometer (intensity) thus allowing the modulation depth to be varied.

A random voltage circuit is included in order to provide aperiodic phasing/vibrato (chorus effects). The random voltage is derived by amplifying and low pass filtering the noise voltage of a 13 V zener diode (more commonly available 12 or 13 V, 0.4 W zeners can also be used). When switched into circuit, the random voltage controls the vibrato oscillator, which in turn controls the VCO. The intensity of the random voltage modulation can also be varied by means of a potentiometer (random intensity).

Figure 5c shows the circuit of a suitable lowpass filter to limit the bandwidth of the audio input signal. As was explained in the first part of the article, since the clock frequency must be at least twice

5a



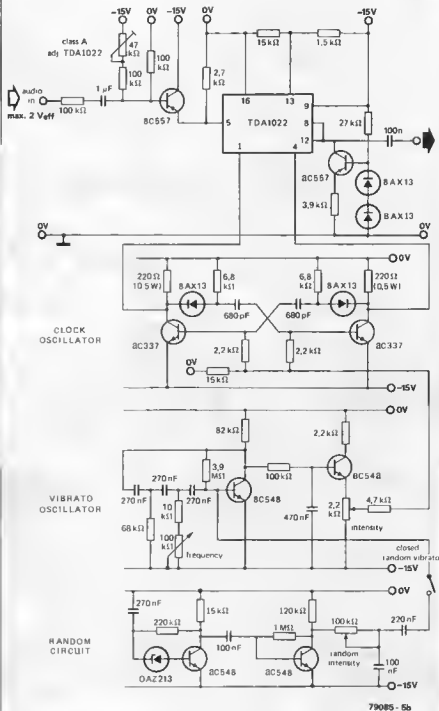
the maximum signal frequency, there is a trade-off between delay time (which of course is determined by clock frequency) and signal bandwidth. The filter shown here has a turnover frequency of 15 kHz and a filter slope of 24 dB per octave.

The circuit of an audio effects unit for phasing, vibrato and chorus using the above frequency modulator is shown in figure 5d. Potentiometers P1 and P2 determine the relative proportions of direct and delayed signal mixed at the output. If the delayed signal only is fed to the output, vibrato is obtained. As a rule fairly fast vibrato, i.e. a modulation frequency of several Hertz, is best, whilst the modulation depth (clock frequency deviation) should be kept low. If the direct and delayed signals are mixed, either chorus or phasing is the result, depending on whether a random or periodic modulation signal is used. A gradual transition from vibrato to phasing can be obtained by slowly increasing the amount of direct signal summed with the delayed version. The above circuit can also be used for ADT. With the vibrato intensity turned right down a constant delay time of approx. 3.2 ms is obtained. Mixing direct and delayed signal will then produce the double tracking effect.

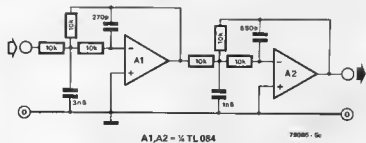
Stereo phasing

For multi-channel effects, the add-on

5b



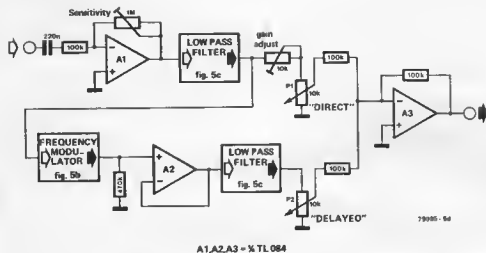
5c



A1, A2 = 1/2 TL084

79085-5c

5d



79085-54

circuit of figure 6 provides three separate output signals. Output I gives the sum of the delayed and direct signals, at output II is the direct signal minus the delayed signal, whilst at output III is the delayed signal minus the direct signal. Stereo phasing, chorus and ADT are obtained by taking either outputs I and II or I and III as the stereo signal pair. In case of vibrato, obviously all three outputs will give the vibrato signal, with output II being inverted with respect to outputs I and III. Any of the three outputs can in principle be used to provide a mono signal, however it is normal to use the sum signal at output I.

Sound reinforcement systems and studio work

With the aid of delay lines it is possible to exploit two interesting psycho-acoustic phenomena related to the time taken for sound waves to travel through free air.

The Haas effect and the law of the first wavefront

According to the theory of Dr Haas, a blindfold listener will determine the source of a sound not by amplitude, but on a 'first arrival basis'.

If for example the same signal is fed to two loudspeakers of a stereo system, delaying the signal to the left channel speaker by several milliseconds will give the listener the impression that the music is originating almost entirely from the right channel speaker. Even if the volume of the left channel signal is increased to several times that of the right channel, the listener will continue to be deluded into thinking the sound is coming exclusively from the right-hand speaker. The increase in left channel volume only affects the listener's impression of overall loudness of the

signal; it has little or no effect on the perceived direction.

The use of electronic delay lines allows the sound technician to focus the listener's attention on a particular sound source by ensuring that the other signals are delayed. When recording orchestral music delay lines are often used to counteract the effect of different path lengths between individual instruments and the microphones. Thus when recording a large orchestra using one main stereo microphone (for good transparency and resolution) supported by a series of secondary microphones to pick up instruments further removed from the main microphone (e.g. second violins), the latter tends to pick up the sound of distant instruments *after* the more closely positioned microphone. Due to the Haas effect this can lead to falsification of the desired stereo image, a problem which is only partially resolved by lowering the level of the secondary microphone. The ideal solution is to employ delay lines to equalise the path lengths.

A similar technique can be used when recording an orchestra with a main microphone close to the body of the orchestra and one or more secondary microphones positioned further back in the hall to capture reverberation. At distances of greater than 15 m between main and secondary microphones, the time taken for signals to reach the two can differ by more than 50 ms. Path length differences of this order can produce intrusive echoes. By employing delay lines the main microphone signal can be held back to reduce the period between direct and reverberation signals to acceptable levels.

In the case of P. A. systems used in large halls or in the open air, excessive path

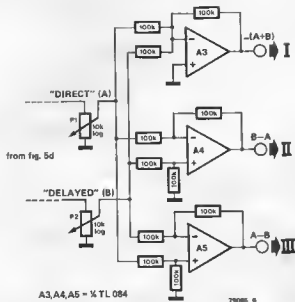
Figure 5d. Block diagram of a complete audio effects unit. In addition to input and output lowpass filters and the frequency modulator of figure 5b, the circuit includes an input amplifier with variable sensitivity (A1), a buffer amplifier (A2), and an output mixer (P1, P2, A3), which allows the direct and delayed signals to be summed in any desired proportion. The relative proportions of the two signals determine the tonal character of the resultant sound.

Figure 6. Stereo effects can be obtained by extending the output mixer circuit to provide two difference outputs.

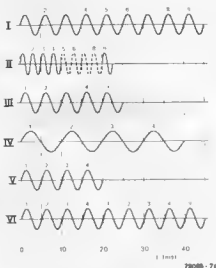
Figure 7a. Illustration of how a variable speech processor expands or compresses the time domain of a signal, allowing it to be reproduced at other than normal speeds without altering the pitch of the signal.

Figure 7b. Block diagram of a variable speech processor.

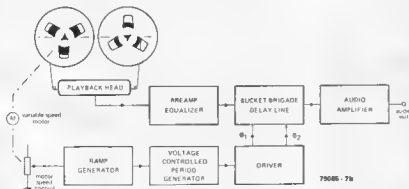
6



7a



7b



length differences between signals from different loudspeakers can also cause the intelligibility of the speech signal to be impaired. Here again delay lines can be used with advantage to reduce the interval between direct and reverberation signals reaching the listener to below the crucial 50 ms mark. The ideal interval between successive signals is in the region of 20 ms, since the effect is then similar to that of double tracking, i.e. the listener 'integrates' the two sounds and subjectively experiences a slight increase in the volume of the signal.

In the case of loudspeaker installations which do not incorporate delay lines, the first signal to reach the listener will be that from the loudspeaker closest to him, which normally will not be situated in the line of sight between himself and the person speaking into the microphone. Thus, due to the first wavefront principle, he will see the speaker in front of him, but will hear him from the side, a phenomenon which can often have a slightly disconcerting effect.

The problem can be overcome by using a small loudspeaker at the front of the stage or hall to reproduce the direct signal, and delaying the signal to the remainder of the loudspeakers sufficiently to ensure that their signals reach the audience after the signal from the front loudspeaker. If a suitable delay time is used the output of the front loudspeaker can be considerably smaller than that of the others. Once again, with a delay of approx 20 ms between successive signals the listener perceives them as simultaneous and the intelligibility of the speech signal is improved.

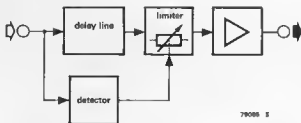
Variable Speed Control, Level Control and Anti-Click Units

Variable speed control is a process which allows recorded speech to be replayed at faster or slower speeds, without affecting the pitch of the signal.

As every owner of a variable speed tape recorder knows, playing back a recording at a higher than normal speed produces a high-pitched twittering sound, whilst lower speeds give an incomprehensible deep grumbling noise. Variable speed control prevents these changes in voice pitch. Signal I in figure 7a shows 9 cycles of a 200 Hz sine wave recorded at normal speed. When replayed at twice the recording speed the signal frequency is doubled to 400 Hz (signal II). Variable speed control 'stretches' the first four cycles of signal II to twice their 'length' i.e. the time domain of the signal is compressed. The result is signal III, which has the original frequency of 200 Hz. Cycles 5...8 of signal II (shown dotted) are suppressed. The informational content of these 4 cycles is in fact superfluous, which means that the intelligibility of a speech signal is unaffected by replay at twice the original speed.

When replaying at half the original speed the opposite occurs. The original

8



79005 1

signal is slowed down to a frequency of 100 Hz (signal IV). The section of signal containing the first four cycles is compressed into half its original period (signal V), the resulting 'hole' or time gap is filled by repeating the first four cycles, which have been specially stored for this purpose (signal VI). Since the pitch and speech rhythms (at half their normal speed) of the original signal are preserved, the extra information is not important.

In practice the speech signal is processed by feeding it through a bucket brigade memory and continuously varying the clock frequency. A simplified block diagram of a variable speech processor is shown in figure 7b. A sawtooth generator, the frequency of which is determined by the speed of the tape recorder, is used to modulate the clock generator of the delay line. In the case of faster than normal playback the sawtooth ramps negative. During each period of the sawtooth the clock frequency is continuously varied from a maximum to a minimum value. The lower the clock frequency, the longer each successive sample takes to travel through the delay line. The result is that the time domain of the output signal is extended (its frequency is reduced), whilst leaving the shape of the waveform unaffected. Since all the frequency components of the original signal were 'slowed' by the same relative proportion, the harmonic structure and therefore the tonal character of the signal are preserved.

In the case of speech expansion (the time domain of the speech signal is expanded by playback at a slower than normal speed) the opposite occurs. The sawtooth ramps positive and the clock frequency varies from an initial minimum to a maximum value, with the result that the pitch of the signal is increased.

The variable speech processor can also be used to falsify the pitch of signals played at their correct speed, i.e. real-time pitch shifting. Thus by expanding the time domain of the speech signal the effect is of increasing its frequency and pitch, a trick which can be used for cartoon voices etc. Conversely, by compressing the time domain of the speech signal its frequency can be lowered. This technique is useful in un-

Figure 8. Basic principle of a level control circuit incorporating a delay line. The detector monitors the input signal for overloads, and as soon as a signal peak is detected, activates the limiter circuit. The delay line ensures that the gain reduction occurs before the input signal reaches the limiter, thereby preventing initial transient distortion. The same principle can be used for click suppressors etc.

scrambling the voice signals of divers working in helium-filled atmospheres.

Finally, two closely-related applications of delay lines in specialised studio equipment: level control units and click eliminators. In both cases the principle involved is the same, an audio signal is monitored for a particular irregularity. In one case it is signals above a preset maximum level, and in the other case a particular type of noise or distortion (clicks or pops caused by scratches, old recordings etc).

Delay lines are used to give the control circuits sufficient time to respond to signal overloads or noise transients. The basic arrangement is illustrated by the block diagram of figure 8. The input signal is fed to a delay line and to a detector circuit which controls the limiter or noise suppression circuit. Since the signal fed to the detector circuit is undelayed in the case of e.g. a signal overload, gain reduction sufficient to prevent overshoot will have occurred before the delayed signal (and signal peak) arrive at the limiter. Due to the reduction in the cost of bucket brigade memories, click suppressors are now a feasible proposition for the amateur, who can make more or less noise-free recordings of old records which previously were 'unlistenable-to'.

CAPITALS from the ASCII keyboard

BASIC made easy

The ASCII keyboard (Elektor, November 1978) is more versatile than may appear at first sight. Some readers have commented that a 'shift-lock' would be useful, particularly when it is used for programming in BASIC. In actual fact, we can go one stage further: an 'upper-case lock'!

In the ASCII code, capitals and lower-case letters are distinguished by the value of the sixth bit (S6 on the character generator). For capitals, this bit is logic '0'; for lower-case letters it is logic '1' (see table 1 in the original article).

The character generator used, the AY-5-2376, not only provides the usual 7-bit ASCII code; it has an eighth output (S8). Although this is not made clear in the data sheet, S8 can be used instead of S6. The result is all that could be desired: the shift key operates normally for numerals, punctuation marks etc. — but only CAPITALS are printed when a letter key is operated!

This facility can be extremely useful — for instance, when programming in NIBL. The 'shift' key need only be used when special symbols are required; it is no longer required for printing text.

A single-pole change-over switch can be added as shown in the figure.



79109

interface for μ Ps

The specifications for a serial interface between computer and terminal are given by the so-called RS232C and V 24 standards — among others. Although these standards are in widespread use, this is not to say that all (micro-) computers include the corresponding interface.

Only a few components are required for a 'standard' interface. The circuit described in this article can be used in conjunction with both the Elektor SC/MP system and the popular KIM 1.

The main difference between computer- and RS 232C/V24 signals is the definition of the signal levels. Within a computer system it is common practice to use TTL levels, with logic '0' corresponding to 0 V and logic '1' to +5 V. The interface standards are rather different: logic '0' may be anything between +5 V and +25 V, and logic '1' is 'defined' as between -5 V and -25 V. Note the level inversion: positive voltages for logic '0' and negative voltages for logic '1'! The supply voltages in the SC/MP system are +5 V and -12 V, so it is 'logical' to use these levels for '0' and '1' respectively.

No negative supply voltage is available in the KIM 1 system, so an additional

power supply must be added (giving a voltage between -5 V and -25 V). Two positive voltages are present (+5 V and +12 V). Either of these could be used for the positive logic level, but the higher voltage is to be preferred since it gives better noise immunity. The only disadvantage is that the power dissipation is higher in this case.

SC/MP interface

The input/output software for the SC/MP normally uses the sense B input and flag \emptyset output for serial data transfer. A suitable interface for these connections is shown in figure 1.

The input interface (figure 1a) consists

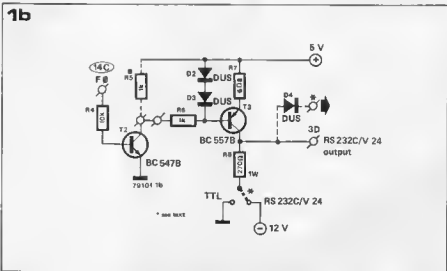
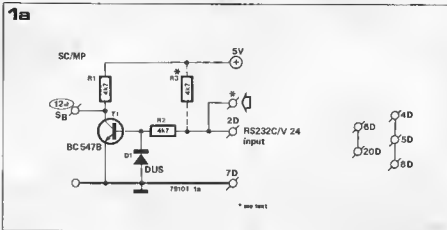
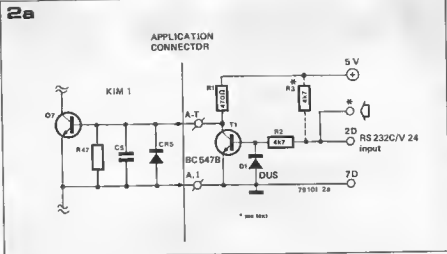


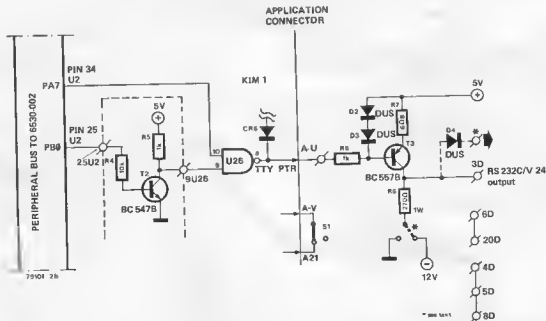
Figure 1. Interface for the SC/MP system. The input side is given in figure 1a, and the output in figure 1b.

Figure 2. Modified communication interface for the KIM 1 microcomputer. Input and output sections are given in figures 2a and 2b, respectively; the relevant sections of the KIM circuit are also shown.

Figure 3. Multi-purpose printed circuit board for the communication interface (EPS79101). The track layout is given in figure 3a; figure 3b is the component layout for use with the Elektor SC/MP system and figure 3c is for use with the KIM.



2b



of four components. A diode (D1) and resistor (R2) limit the input signal, after which the transistor performs the conversion to TTL levels. Resistor R3 is not required if the input signal conforms to the official standards. However, the interface can also be fed from an optocoupler or open-collector gate; in either of these cases R3 can be used as pull-up resistor.

The output side of the interface is slightly more complicated. The TTL levels from the SC/MP must be converted to +5 V and -12 V. A low output impedance is a must, since lines of up to 10 m (30') are quite common. Furthermore, the circuit must be short-circuit proof.

Figure 1b gives the circuit. A current source (T3) is used to obtain the low output impedance; it has the added virtue of being short-circuit proof. A second transistor (T2) is included as an inverter, to obtain the correct logic level relationship between the flag \emptyset output and the interface output. Resis-

tor R5 is not strictly necessary: it improves the switching characteristic of the interface, giving sharper edges. The second output, via diode D4, can be used to drive the LED in an optocoupler. The output current will have to be reduced in that application, by increasing the value of R7 to 15 Ω . The same circuit can also be used for buffering the flag \emptyset output, without altering the levels. In that case R8 should be connected to supply common instead of negative supply. The printed circuit board (figure 3) is designed to cater for all possible applications.

KIM interface

Only a few modifications are required if the interface is to be used in conjunction with the KIM 1. The TTY (teletype) interface in the KIM system will also have to be modified slightly.

The serial data input is no problem: the same circuit can be used. The only difference is that the value of R1 (in

figure 1a) must be reduced to 470 Ω to cope with the heavier load requirement. The circuit is therefore as shown in figure 2a; it can be connected to the KIM's 'application connector' as shown. For the serial output, some minor surgery on the KIM board is required. The TTY output on the KIM is intended for teletypes with a so-called current loop, but if it is to be used with the interface described here the polarity of the signal after the output gate must be inverted. Transistor T2 on the interface board is used for this, as shown in figure 2b. The track between PB \emptyset (pin 25 of U2) and pin 9 of U26 on the KIM board must be broken, after which T2 can be wired in series as shown. The signal at output A-U on the application connector now has the correct polarity to drive the current source (T3 on the interface board).

The printed circuit board

All the options described, both for

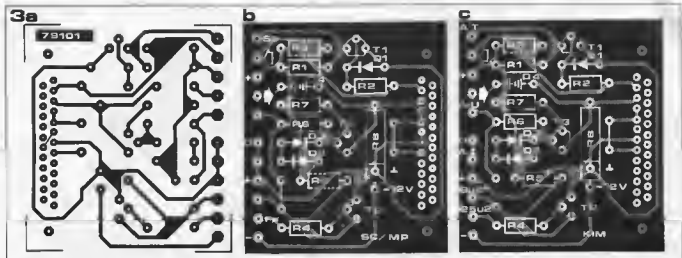


Table 1

MEMORY-DUMP ROUTINE BY D. HENDRIKSEN

```

0C00 C4 0C 35 C4 00 31 C4 0C 37 C4 86 33 C4 0C 36 C4
0C10 95 32 C4 0D CB FD C4 0D 3E 8F 80 C4 0A 3E C4 20
0C20 3E 35 01 40 35 40 1C 1C 1C 1C 01 C3 80 3E 35 01
0C30 40 35 40 D4 0F 01 C3 80 3E 31 01 40 31 40 1C 1C
0C40 1C 1C 01 C3 80 3E 31 01 40 31 40 D4 0F 01 C3 80
0C50 3E C4 20 3E C4 10 CB FE C4 20 3E C1 00 1C 1C 1C
0C60 1C 01 C3 80 3E C5 01 D4 0F 01 C3 80 3E BB FE 9C
0C70 E5 BB FD 9C A1 C4 0C CB FF 08 08 08 BB FF 9C F9
0C80 00 90 8F 05 0C 00 30 31 32 33 34 35 36 37 38 39
0C90 41 42 43 44 45 46 01 C4 64 8F 06 06 DC 01 07 C4
0CA0 09 C8 20 C4 F0 8F 02 B8 1A 98 10 40 D4 01 C8 14
0CB0 01 1C 01 06 DC 01 E0 0C 07 90 E8 06 D4 FE 07 3E
0CC0 90 D4 00 00 00 00 00 00 00 00 00 00 00 00 00

```

Parts list

Resistors:

R1 = 4k7 (470 Ω)
R2 = 4k7
R3 = 4k7*
R4 = 10 k
R5 = 1 k* (1 k)
R6 = 1 k
R7 = 608 or 15 Ω *
R8 = 270 Ω /1 W

Semiconductors:

T1, T2 - BC107B, BC547B or eq.
T3 - BC177B, BC557B or eq.
D1 ... D3 = DUS
D4 = DUS*

* see text.

Where values for SC/MP and KIM differ, the values for the KIM are given in brackets.

SC/MP and KIM systems, can be mounted on the p.c. board shown in figure 3. The component layout for use with the SC/MP system is given in figure 3b; figure 3c corresponds to use in a KIM system.

A so-called modem connector can be used, if required. The mounting holes for the connector correspond to those of the p.c. board, so that the complete unit can then be mounted with only two bolts. The only thing to watch, in this case, is that the components must be mounted as nearly flush with the board as possible - there will not be much room between the board and the panel on which it is mounted! An alternative is to use a right-angle modem connector, so that the board can be mounted horizontally.

Software

The monitor program for the KIM 1 already includes a teletype routine. The selection between a hexadecimal

keyboard or teletype input is made by a wire link on the 'application connector'. In this case, since the TTY input is required (even if it is actually used by the Elektorterminal), the wire link (or a switch) between pins A-V and A-21) on the connector must be included.

In the Elektor SC/MP system, no provision was made for connecting a teletype. However, only small programs will be required to obtain the necessary functions. As an example, a memory-dump routine is given in table 1. By means of this program, the memory contents will be printed out in hexadecimal - starting at a specified address.

The length of the block is determined by the number of lines specified for the print-out. When the complete block has been 'dumped' the processor goes to the 'HALT' mode; operating the HALT-reset key causes a further block to be printed out, etc. The 'modify' routine is used to enter the new start address in memory locations 0C01 (upper address byte) and 0C04 (lower address

byte). In the same way, the desired block length can be stored in location 0C13. The program itself is started at 0C00.

The program listing given in table 1 was actually printed using this memory-dump routine, as can be seen from the three underlined data bytes.

The transmission rate is 300 baud. \blacksquare

sweep generator

Determining the frequency response of an amplifier normally requires a series of carefully conducted test measurements, a large supply of graph paper, and plenty of patience. Wrestling with peak-peak values, RMS voltages, dBs, logarithms etc. can prove to be something of a chore, and it is all too easy to make mistakes which 'distort' the final results. However if one possesses an oscilloscope, there is a way of displaying frequency response curves directly upon its screen — provided one also has the instrument described here, namely a sweep generator.

(L. Köppen)

Sweep generators are not usually part of the basic equipment of amateur electronics enthusiasts, for the simple reason that such an instrument is normally too expensive. However if we are content with an instrument which will provide relative results (which is often more important than the measurement of a quantity with absolute accuracy), then there is no reason why a sweep generator should not be included in the test equipment of every hobbyist.

Why sweep?

What exactly is a sweep generator? The simplest way to answer this question is to look at how one would normally set about measuring the frequency response of an amplifier. The usual measurement set-up is illustrated in figure 1.

The amplifier under test is provided with an input signal from a low frequency sine-wave generator. The amplitude of the amplifier output signal is measured on an AC voltmeter. We now ensure that the amplitude of the input signal is held constant, and measure the amplitude of the output signal for a number of different input frequencies. The results are plotted on graph paper, with frequency along the horizontal axis and amplitude (voltage) along the vertical axis. In this way the frequency response of the amplifier is immediately apparent — how flat it is, at what frequency it starts to roll off, etc.

With this arrangement, each time we wish to make a new measurement the frequency of the sine-wave generator must be increased by hand. It would of course be much simpler if, in some way, this could be done automatically. This would also allow a continuous increase of the frequency (instead of in discrete steps), thereby ensuring that we are not jumping over small dips or peaks in the response. Thus what is required is a signal whose frequency increases continuously. In other words, a sweep generator.

Figure 2 illustrates how a sweep generator is used to display the frequency response of an amplifier on an oscilloscope.

The sweep generator actually provides two signals: the above described input signal for the amplifier, and a voltage which varies with the frequency of the

input signal. The latter signal, designated X, is used to control the horizontal deflection of the oscilloscope (X amplifier). The vertical deflection of the spot is determined by a voltage which is proportional to the amplitude of the amplifier output signal. This is obtained simply by rectifying and smoothing the amplifier output signal. The result of such an arrangement is that the frequency response of the amplifier is displayed directly on the scope screen, with amplitude along the vertical axis, and frequency along the horizontal axis.

Not linear, but logarithmic

As most readers will no doubt know, it is generally the case that a logarithmic scale is used for the frequency axis in such graphs. The question is, how to ensure a logarithmic relationship between the frequency of the sweep generator signal and the external timebase input signal (X). One answer is to increase the frequency of the sweep signal linearly, whilst that of the X signal is increased logarithmically. However a better solution is to let the X voltage increase linearly, and increase the frequency exponentially (with time). In this way there is a logarithmic relationship between frequency and X voltage, whilst the horizontal deflection of the scope will remain constant. This means that the brightness of the trace will also remain constant, and more importantly, affords the possibility of using the (linear) timebase generator of the scope (as not every scope has an X-input).

It should be noted that the vertical axis of the response ought to have a logarithmic scale as well, a facility which is not provided by the circuit described here. Strictly speaking, however, the provision of a logarithmic Y axis is not among the functions of a sweep generator; its job is simply to provide the necessary input signals for the measurement procedure. A suitable circuit (with p.c. board) was published in *Elektor*, January 1978: the peak programme meter.

Basic circuit

The basic design of the sweep generator is illustrated by the block diagram of figure 3.

An asymmetrical squarewave oscillator is used to trigger a sawtooth generator, which provides the control voltage for the X input of the scope. The X-voltage is also used, via an exponential converter, to control a VCO, resulting in a signal with a frequency exponentially related to the X-voltage. The block diagram is completed by buffers for the various output signals.

The sweep generator has two outputs, the first offers a choice of sinewave or triangle waveforms, whilst the second provides a squarewave. Although triangle and squarewave signals are not generally employed to determine the

frequency response of circuits, they are useful in a number of other applications.

The circuit also contains a 'manual' switch, which allows the frequency of the generator to be continuously varied by means of a potentiometer, rather than automatically swept up and down the frequency range.

The circuit in detail

The complete circuit diagram of the sweep generator is shown in figure 4. As can be seen, the circuit contains a number of switches which function as fol-

lows:

- S1 - sweep inhibit
- S2 - sweep/manual
- S3 - sinewave/triangle
- S4 - frequency range
- S5 - output attenuator

A more detailed description of these functions will be dealt with later in the text.

An asymmetrical squarewave oscillator is formed by the circuit round T1 and T2. The output of this oscillator is attenuated by R6 and R7 then limited by diodes D1 and D2 which are connected in 'reverse-parallel'. This signal is then used to trigger the sawtooth generator

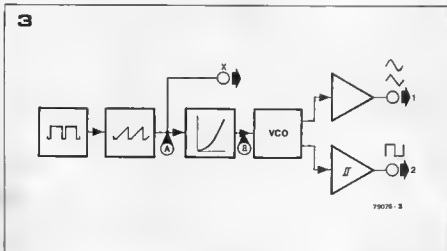
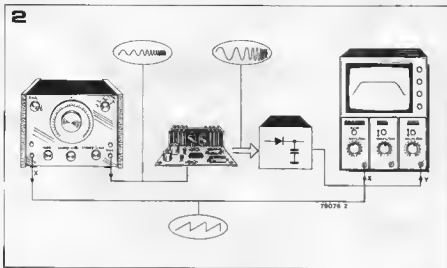
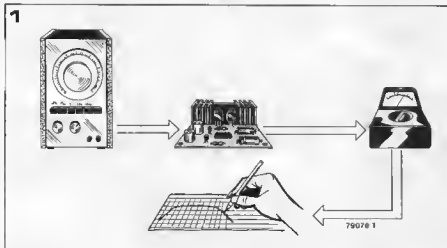
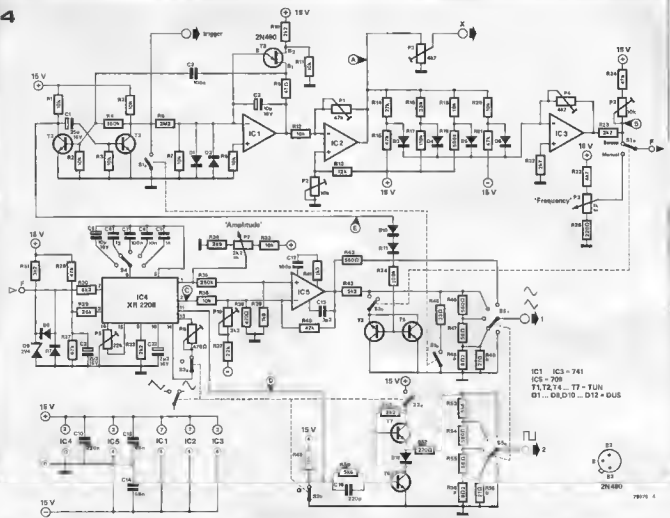


Figure 1. This figure illustrates the basic set up for measuring the frequency response of an amplifier, using a low frequency generator and an AC voltmeter.

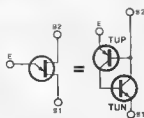
Figure 2. With the aid of a sweep generator and an oscilloscope the same measurement can be carried out virtually automatically. The sweep generator provides a sinewave output signal, the frequency of which increases continuously, and a sawtooth signal which is used as an external timebase input for the scope.

Figure 3. Block diagram of the sweep generator. In order to provide a logarithmic frequency scale, the circuit ensures an exponential relationship between the instantaneous value of the sawtooth and the VCO frequency.

4



5



consisting of IC1 and the unijunction transistor (UJT) T3. When the voltage on C3 reaches a certain value, T3 turns on, with the result that the voltage at the output of IC1 ramps negative. The period of the sawtooth is approximately 10 seconds, which may appear rather long. However it is important that the frequency of the sawtooth is much lower than that of the lowest VCO signal. After being amplified and inverted by IC2 the sawtooth waveform is used as the external timebase signal for the scope. The peak-peak value of the voltage at point A is 16 V.

The next step is to derive an exponentially related voltage from this sawtooth, and so this end a diode-resistor matrix, consisting of D3... D6 and R14

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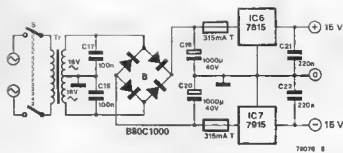


Figure 4. Complete circuit diagram of the sweep generator. The exponential converter consists of a diode-resistor matrix.

Figure 5. The unijunction transistor for the sawtooth generator can, if desired, be replaced by two separate transistors.

Figure 6. Circuit of a suitable power supply for the sweep generator.

... R21 is used. Basically the matrix forms a voltage divider network in which the size of the input voltage (i.e. A) determines which resistors are included in the divider chain. As with all exponential converters, the diode-resistor matrix provides only an approximation to an exponential signal, however the advantage of this arrangement is that it possesses excellent temperature stability.

The output of the matrix is amplified by IC3. The exponential characteristic can be adjusted by means of P4 and P5 — the procedure will be described later in the article. Assuming P4 and P5 are correctly adjusted, a signal which is synchronous with the sawtooth and which increases exponentially with time will

be present at point B.

Oscillator

The actual sweep signal is generated by IC4, a function generator type XR 2206. A detailed description of this IC was contained in Elektor 33 (January 1977).

The input of the IC is protected against excessively large voltages by diodes D7 ... D9 and R31.

The IC has two outputs which provide a signal of the same frequency. Depending upon the position of S3, the output at pin 2 (point C) will be a triangle or sine-wave, whilst pin 11 (point D) provides a symmetrical squarewave. The range switch, S4, provides five frequency ranges (1-10 Hz, 10-100 Hz, 100-1 kHz, 1-10 kHz and 10-100 kHz). The amplitude of the triangle/sinewave output can be varied by means of potentiometer P7.

With S2 in the 'sweep' position, the oscillator frequency is controlled by the output of the exponential converter. In the manual position, the circuit functions as a conventional function generator, the frequency of which can be adjusted by means of P6.

The sinewave/triangle output is buffered by IC5. This op-amp must be capable of rapidly handling large input signals, therefore a 709 is used, since it has a higher slew rate than the 741 (IC1 ... IC3). The control voltage which determines the amplitude of the sinewave/triangle signal is fed not only to pin 1 of IC4, but also via R35 to the non-inverting input of IC5. This compensates for the effect of the control voltage on the DC component at point C. The buffered sinewave/triangle is fed to a voltage divider. By means of S5 the amplitude of the output signal can be varied in 20 dB steps. The circuit is short-circuit proof in all positions of the switch.

The reverse-parallel connected transistors T4 and T5 form a voltage controlled limiter. When the voltage at point E goes high, T4 and T5 receive base current and conduct on negative and positive half cycles of the waveform respectively, so that the sinewave/triangle is limited to the saturation voltage of these transistors. This step ensures that the signal is suppressed during the flyback of the sawtooth. For this reason the voltage at point E is derived from the squarewave oscillator which triggers the sawtooth generator.

The XR 2206 also provides a squarewave output (from pin 11), which is buffered by the circuit round T6 and T7. Although this circuit looks rather unusual, it is basically a discrete equivalent of the totem-pole output of TTL ICs. Because of the effect of D12, when T6 is turned on the voltage at the base of T7 is lower than that at the emitter, i.e. T7 is turned off. On the other hand, when T6 is turned off, D12 is reverse biased and the base of T7 is at a higher potential than the emitter, so that T7 is

turned on.

The squarewave output is also provided with a switchable attenuator, however, unlike the sinewave/triangle output, there is no suppression of the signal during the flyback of the sawtooth, since there is basically little point in using the squarewave signal in the 'sweep' mode.

Trigger output

In addition to the X-output and the two function generator outputs, the circuit is also provided with a trigger output, which can be used if the oscilloscope does not have an external timebase input. The signal at the trigger output remains high for the duration of the sweep, and should thus be fed to the sync input of the scope. The trigger output can also be used for the Z-input of scopes which have such a facility, ensuring that the trace is blanked during flyback of the sawtooth.

S1 is a pushbutton switch, which, as long as it remains depressed, inhibits the sweep. If the button is pressed during a sweep, the cycle is interrupted and the signal at output 1 is suppressed.

S3 switches between sinewave and triangle waveform at output 1. At the same time it also switches the squarewave signal in and out. The squarewave is only present when S3a is in the triangle position. This prevents pulse spikes being superimposed upon the sinewave output because of crosstalk between the two outputs.

Construction

Care is required in the construction of the sweep generator. Of particular importance is the circuit around IC5, since, in order to obtain a high slew-rate, this op-amp is somewhat under-compensated. This means that it may well exhibit a tendency to oscillate and to counteract this effect R38 has been included. Capacitors C14 and C15 should be mounted as close to the IC as possible.

For potentiometer P6, used to vary the frequency when the generator is used in the manual mode, it may be advantageous to use a multi-turn type with slow motion drive, thus permitting accurate adjustment.

Should the unijunction transistor prove difficult to obtain in certain areas, the following alternatives are offered: 2N492, 2N1671, 2N2418, 2N2420, 2N2422, and a further possibility is the TIS 43. In addition it is also possible to replace the UJT by two separate transistors as shown in figure 5.

The sweep generator requires a power supply which can provide + and - 15V at 300 mA. A suitable circuit is shown in figure 6 and this can be built on the EPS 9968-5 printed circuit board.

Calibration

The sweep generator has eight preset po-

tentiometers, and before beginning the calibration procedure they should all be set to their mid-positions. The same also holds for the control potentiometers, P6 (frequency) and P7 (amplitude). S5 should be set for minimum attenuation, and S2 to 'manual'. With S3 in the 'triangle' position, there should be both a triangular waveform at output 1 and a squarewave at output 2. With S2 in its alternative position the squarewave should be absent.

By means of P7 it should be possible to vary the amplitude of the triangle waveform by at least a factor of 10. Should this not be the case, then a smaller value should be chosen for R33. Similarly, with the aid of P8 it should be possible to vary the frequency by a factor of 10. If this is not the case, both R25 and R26 should be reduced.

The symmetry of the triangle and sine waveforms can be adjusted by means of potentiometer P8, whilst the distortion factor of the sinewave can be reduced to a minimum by adjusting P9. For both these procedures an oscilloscope is necessary.

Once the sweep generator has been given five minutes to warm up, P10 can be adjusted to give a DC voltage level of 0 V (offset voltage) at output 1 (triangle/sinewave). When setting the amplitude level with P7 this offset voltage should remain at zero volts, however the value of R35 can be altered if it is found that it does vary.

Having set up the function generator and output stages the adjustment of P1 ... P5 will complete the setting-up procedure. The amplitude of the sawtooth at point A should be adjusted to 16 V peak-peak by means of P1, whilst P2 is used to ensure that the sawtooth is symmetrical about 0 V. Should it prove necessary, the sawtooth can be attenuated by P3 before it is fed to the X-input of the scope.

P4 (amplitude) and P5 (DC voltage level) are adjusted such that the exponential voltage at point B varies between +2.75 V and +0.54 V. It will be apparent that P5 also influences P4. Once these two potentiometers have been adjusted the sweep generator is ready for use.

The performance of the circuit - particularly in view of the relatively low cost - is excellent. Within the frequency range of 5 Hz to 100 kHz the amplitude of the sweep signal is constant ± 0.25 dB; below 5 Hz the amplitude increases slightly. The frequency characteristic of the generator is also extremely stable, and the zero voltage setting at output 1 exhibits very little temperature drift.

simple sound effects

We have, somewhere in the Elektor laboratories, a sound effects department, although the exact location has yet to be discovered. There was a widely held opinion that it was found during the last Christmas office party but this was eventually discounted because a) the noises were too lifelike and b) it was not possible to simulate them electronically! We usually associate their normal products with the dying shrieks of tortured cats, horrifying howls and a whole assortment of plops, bangs, whistles etc. However on the odd occasion they do produce sounds suitable for publication and, to prove that this department really does exist, here is their latest circuit design.

The original design for this rather clever sound effects unit was built into a 19inch rack mounting cabinet which unfortunately tended to overheat to an alarming degree (see 'workshop heater' in *Elektor* number 184) and lacked a little on portability. Further research resulted in the following circuit which uses only two CMOS ICs and is very cheap to build. Despite its modest dimensions it will produce a range of sounds from that of an American police siren to one closely resembling the 'twittering' of birds.

Sounds simple?

As is apparent from the block diagram of the circuit (figure 1), the basic principle is extremely straightforward. The output of a twelve-bit binary counter is converted into an analogue voltage which is used to control a VCO. As the binary output of the counter increases, the control voltage ramps positive, until the counter resets and the voltage falls to zero, whereupon the count resumes and the control voltage once again starts to ramp positive, and so on. The waveform of the control voltage is thus a periodic sawtooth. The VCO produces the actual output signal of the circuit, whose pitch is determined by the instantaneous amplitude of the sawtooth control voltage. An output buffer amplifier ensures that the signal is sufficiently large to produce an audible tone when fed to a loudspeaker. The highly individual nature of the resultant sound is due to an unusual feedback configuration. The output signal of the VCO is not only used as the output of the circuit, but as the clock input of the binary counter. Thus the rate at which the counter steps through each count cycle depends upon the pitch of the output signal. In other words, the higher the sound, the faster it varies in pitch. The result is a repetitive *beep-beep* sound which starts each phrase at a low frequency and rises exponentially to a maximum pitch.

Circuit diagram

The circuit diagram of the sound effects generator is shown in figure 2, and as can be seen, it consists of only a couple of readily-available CMOS ICs and a few

assorted resistors and diodes.

IC2 forms the 12-bit binary counter. The binary value of the 8 lowest order bits (i.e. those bits which change state most frequently) is converted into an analogue voltage by means of resistors R1...R8. The VCO consists of a simple CMOS oscillator (built round N1 and N2) the RC time constant of which is varied by using transistor T1 and a diode bridge as a voltage-controlled resistor. As the control voltage fed to the base of T1 increases, more current is passed through the diodes, with the result that their dynamic resistance falls. The initial frequency of the oscillator is set with the aid of preset potentiometer P1, which is connected in parallel with the diode network.

The squarewave output of the VCO is fed both to the clock input of IC2 and to an output buffer. The latter is formed by four of the remaining inverters of IC1 connected in parallel.

Construction

A printed circuit board has been provided for the circuit (see figure 3). As can be seen, due to the low component count, the board can be kept very small. The loudspeaker can be any inexpensive 8 Ω type capable of handling 500 mW. The supply voltage of the circuit can lie between 4.5 and 10V; at the lowest supply voltage the current consumption of the circuit is only 5 mA, which means that a 4.5 V battery could be used, thereby rendering the circuit portable. Note that the volume of the output signal is determined by the supply voltage level: the higher the supply voltage the louder the sound.

The pitch of the output signal can be adjusted by means of P1. Since the pitch directly determines the rate at which the pitch changes, reducing the resistance setting of P1 not only increases the pitch of the output signal but also causes it to increase more quickly. At the minimum resistance settings of P1 the resultant sound somewhat resembles that of a chirping bird.

The value shown for P1 in the diagram (1 M Ω) is chosen to give the maximum adjustment range. However, if desired any value from 10k to 1M may be used, with or without fixed series resistors.

1

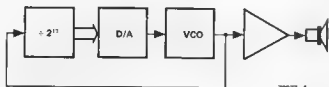


Figure 1. Block diagram of the simple sound effects generator. The output of a binary counter is converted into an analog voltage which is used to control a VCO. The output of the VCO forms both the output signal of the circuit proper and the clock signal of the counter.

Figure 2. Complete circuit diagram. Two CMOS ICs and a handful of discrete components are all that is required to produce an interesting range of sound effects.

Figure 3. Printed circuit board for the sound effects generator, on which all the components, with the exception of the loudspeaker, can be mounted. The circuit can be battery-powered if so desired (EPS 79077).

Parts list

Resistors:

R1, R9 = 820 k
 R2 = 470 k
 R3 = 220 k
 R4 = 100 k
 R5 = 47 k
 R6 = 22 k
 R7 = 12 k
 R8 = 5k6
 P1 = preset potentiometer, 1 M
 (see text)

Capacitors:

C1 = 120 n
 C2 = 100 μ /16 V

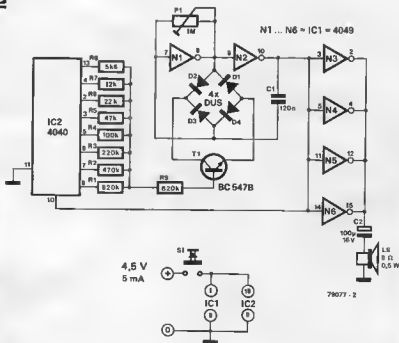
Semiconductors:

IC1 = 4049
 IC2 = 4040
 T1 = BC 547B, BC 107B or equ.
 D1 ... D4 = DUS

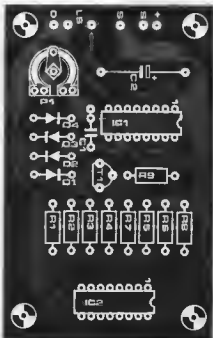
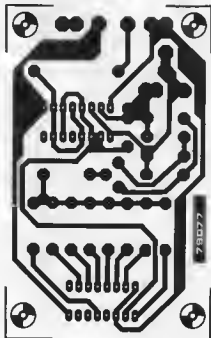
Miscellaneous:

LS = loudspeaker, 8 Ω /500 mW
 S1 = pushbutton

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3



BASIC microcomputer

A SC/MP μ P with BASIC interpreter

It seems safe to assume that the 'BASIC microcomputer' is the cheapest home-construction computer ever described that can be programmed using a higher programming language.

The SC/MP is a popular and readily-available microprocessor. Two further good reasons for using it in this microcomputer are that it can readily be incorporated into the Elektor SC/MP system, and that a Tiny BASIC interpreter for this μ P is available in ROM (Read Only Memory).

The BASIC computer card described in this article contains three circuits that can be used as more or less independent units. The processor section is a fully buffered end self-contained 'CPU card' with provisions for DMA (Direct Memory Access) and multiprocessing.

The memory section is also fully independent, and contains the BASIC Interpreter (NIBL-ROM) and the address decoder.

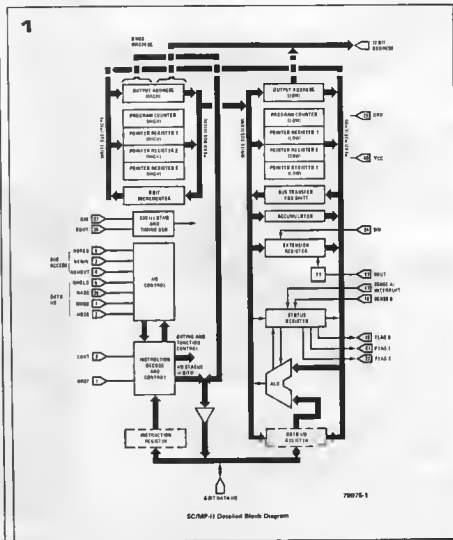
Communication with the 'outside world' (the Elektterminal, for instance) is taken care of by the third section: the interface.

To be fully operational, the computer requires at least one 4K RAM card (RAM = Random Access Memory), as described in Elektor, March 1978. The basic BASIC computer therefore consists of not more than two Eurocard-sized printed circuit boards!

The main advantage of a higher programming language is that there is no need to know the exact details of how the 'inside' of the computer works. A minor disadvantage is that a more sophisticated in- and output unit ('terminal') is required, with an alphanumeric keyboard. In other words, a keyboard that is similar to that of a typewriter. Furthermore, a serial data flow ('bit by bit!') between computer and terminal is normally required. The Elektterminal with ASCII keyboard (Elektor, November and December 1978) meets these requirements, and this unit or a

Figure 1. Functional block diagram of the INS 8060.

Figure 2. Block diagram of the BASIC microcomputer/CPU card.



similar terminal must be used in conjunction with the BASIC computer.

Programming in BASIC is easily learned, but it is not so easy to explain all the details in a few pages. For this reason, no attempt will be made in this article to explain how to program in NIBL (National's Industrial BASIC Language). The BASIC course, which started in the recent March issue of Elektor, must suffice. It explains BASIC in general and, as required, deals with NIBL in particular. Obviously, it was written with this BASIC microcomputer in mind!

For this article, software is a side issue. The primary concern is the microcomputer hardware.

However, as stated at the outset: if the aim is to program in BASIC, there is no real need to know how the computer works. Most of the following article would therefore appear to be superfluous: certainly if one has some experience in programming in BASIC, the components can simply be mounted on the board and, (after a quick glance at the summary of NIBL statements and commands) everything's ready to roll. However, NIBL not only offers the possibility of programming in (Tiny) BASIC; it also provides for immediate addressing of the hardware. For this reason, it can be useful to know a little bit about the actual circuit...

Bird's-eye view of the CPU

The SC/MP (Simple Cost-effective Micro Processor) is an 8-bit μ P, with all essential functions integrated on a single chip. As is apparent from the block diagram (figure 1), the SC/MP (type number INS 8060) contains four 16-bit registers: the program counter and three pointer registers. These 'pointers' play an important part in the (auto-) indexed addressing of the memory and input/output units.

The (8-bit) extension register is of particular interest, since it offers a serial in- and output facility with a minimum of fuss. The cassette interface in the Elektor SC/MP system makes full use of this possibility. A UART (Universal Asynchronous Receiver/Transmitter), as used in the Elektor terminal, can also be made redundant by utilising the SIN and SOUT connections.

The status register can also be used for serial transfer of data. The three 'flag' connections can be used as outputs; 'sense A' and 'sense B' are both serial inputs. In fact, NIBL uses Flag 0 and Sense B as serial data out- and input respectively.

The INS 8060 can address 64k bytes of memory. This requires 16 address lines, 12 of which are brought out direct via pins of the IC. The four remaining

MSB's (Most Significant Bits) are applied to four lines on the databus during the NADS (Negative Address Data Strobe, on pin 39). If these four bits are left unused, the SC/MP can address only 4096 bytes of memory. This 4K memory is called a 'page'; the four MSB's can therefore be used to address 16 pages of memory. The SC/MP will not, of its own accord, 'turn to a new page'. This requires an explicit instruction in the program. When programming in BASIC, nothing could be simpler: for example, the 'statement' PAGE = PAGE + 1 causes the μ P to proceed to the next page.

DMA and multiprocessing

The SC/MP has an extremely useful facility, absent in many other μ Ps: all the outputs used for writing into memory etc. employ so-called Tri-state logic. This means that they can not only be made 'hard' logic 1 or 0; a third state is also possible, where the outputs are 'floating' with a high output impedance. In this third state, the processor no longer has any effect on the address- and databus: as far as any other units are concerned it is no longer 'on-line'! Another microprocessor can then take over (multiprocessing), or a terminal can be used for immediate access to the memory. The latter option is normally referred to as DMA, for Direct Memory Access. It is not really the intention that the (human) operator should proceed to 'walk around inside the memory'; the main advantage of DMA is that it can save a considerable amount of (computer-) time when transferring large blocks of data from the memory to peripherals - floppy disc, for instance.

Instruction set

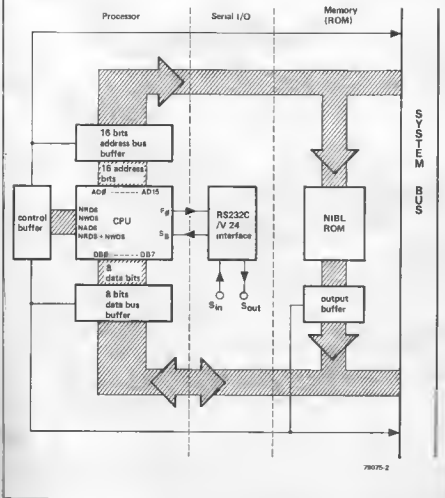
The SC/MP recognises 46 instructions, divided into nine groups; these instructions can be used in up to five different addressing modes. A detailed description of the complete instruction set, with all its variation capabilities, is way outside the scope of this article. It would require pages and pages (both magazine and human memory) and, moreover, it would be rather pointless. After all, this computer can be programmed in BASIC!

Detailed information is provided by the manufacturer, in the documentation listed at the end of this article. This not only explains the instruction set, but also contains full details on how to program in machine language and provides detailed technical information.

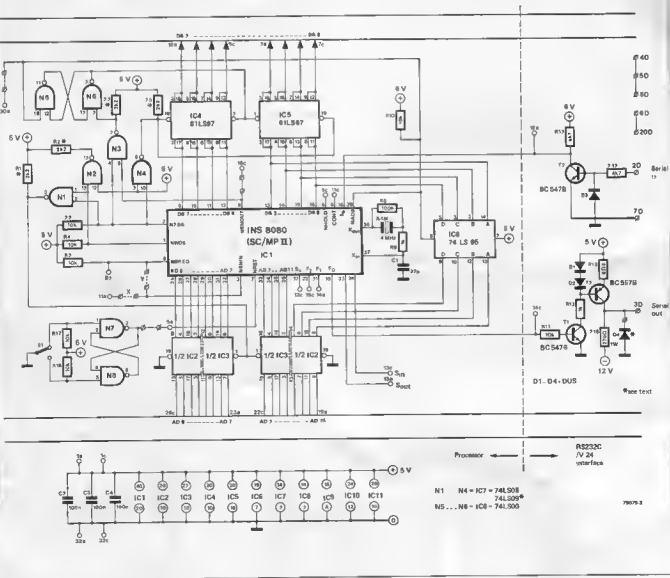
Block diagram

The BASIC card consists of three relatively independent sections. In fact, it doesn't really do justice to this design to call it a 'BASIC card', since its uses are by no means limited to a mere BASIC

2



3



computer. Right from the start, the intention was to produce a design with a minimum component count and maximum flexibility for different applications. The final result is all that we had hoped for.

The BASIC card is virtually a complete microcomputer: only the program memory must be added. The minimum memory requirement is 2048 bytes (sufficient for approximately sixty program lines), or half a 4K RAM card (EPS 9885). Obviously, any other 'memory' with the same capacity (or more) will do instead.

As illustrated in the block diagram (figure 2), the p.c. board contains three distinct sections. The most important of these is the processor section, consisting of the CPU and associated buffer circuits for the address bus, data bus and the main control signals. These buffer circuits make it possible for the CPU to work with extensive memory and peripheral systems. In short, this section is the ideal heart of a larger system.

A small but useful extension of the processor circuit is the RS232C/V24 interface. This section is connected to the processor's flag Φ output and sense B input, which are used as serial out- and input both in NIBL and in various other applications. For instance, this interface opens the possibility of connecting the unit direct to a terminal or teletype. The processor can itself take care of the necessary conversion from parallel to serial data format and vice versa - if the necessary software is available, that is. The saving in cost of hardware is well worth the additional processor-time required for this conversion.

The third and last section on the BASIC card is the Read-Only Memory. The complete NIBL-BASIC interpreter is supplied in a single so-called maxi-ROM. With its 32 Kbit (4096 bytes) memory capacity, this IC represented the absolute limit in Large Scale Integration (LSI) until quite recently, when a ROM with a 64 Kbit storage capacity was announced... It is to be expected that we

will see ever larger ROMs appearing for some time to come.

The inputs to the ROM represent a negligible load on the address bus, so there is no need to add buffer stages at this point. The ROM outputs, however, have a very low drive capability; for this reason, an output buffer is required.

The advantage of the system outlined above is that the processor and ROM sections are fully independent units. Although both are mounted on the same p.c. board, their only means of communication is via the general system bus - the same bus that is used for communication with any other part of the system. This means that it is possible, for instance, to fully utilise the processor's capabilities in a particular application where the ROM is not required.

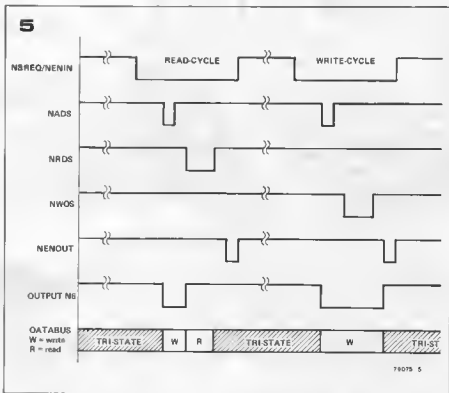
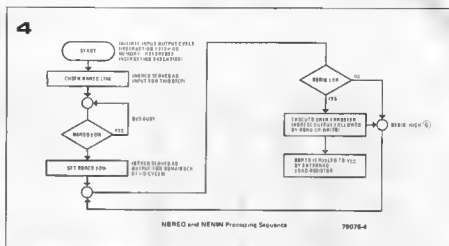
The circuits

The circuits of the processor section and the associated RS232C/V24 interface are given in figure 3.

Figure 3. The processor section with input/output interface. This section can also be used as fully buffered CPU card.

Figure 4. Flow diagram of the initial check procedure that precedes each read or write cycle.

Figure 5. Pulse diagram of the main control signals within the BASIC microcomputer.



The interface does two jobs. In the first place, the TTL logic level at the flag \emptyset output of the processor must be converted to RS232C/V24 level. This means that logic 1 must be at least +5V and not more than +15V; similarly, logic 0 must be some level between -5V and -15V. As in the Elekterminal, the logic levels chosen in this circuit are +5V for logic 1 and -12V for logic 0 - for the simple reason that these levels correspond to common supply voltages. The fact that they are asymmetrical with respect to 0V has no effect on the reliability of data transfer.

The flag \emptyset output of the processor drives transistor T1; in turn, this transistor switches a current source (consisting of T3 and a few resistors and diodes). The advantage of using a current source at the output is that it is short-circuit proof. Furthermore, it then becomes relatively easy to obtain a low output impedance, as required by the RS232C/V24 standard. Should a standard TTL level output be required for some appli-

cation, it is sufficient to add one extra diode (D4). Logic 0 will then correspond to -0.6V (and logic 1 remains +5V); the interface circuit is then a short-circuit proof TTL output buffer. The second thing the interface must do is limit the logic levels at the sense B input of the processor. This is easily accomplished by T2 and D3; R14 limits the input current to a comfortable level.

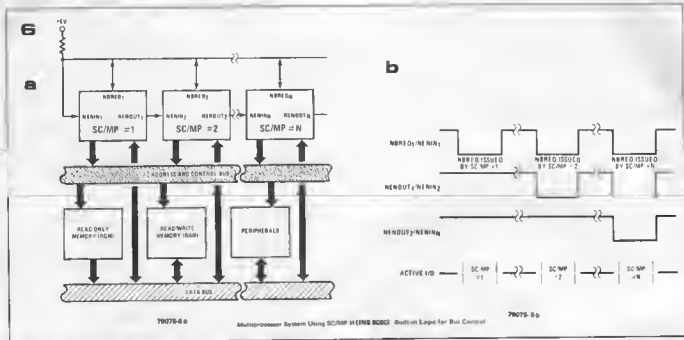
The basic principles of the processor section have already been explained. However, some further explanation of the circuit is called for - particularly where the Direct Memory Access and multiprocessing facilities are concerned. The CPU, or Central Processor Unit, (IC1) receives clock pulses from an internal oscillator, with an external crystal to determine the frequency. From this clock signal, the NRDS (Negative Read Data Strobe) and NWDS (Negative Write Data Strobe) are derived.

The address and data outputs of the CPU have a limited drive capability. For

this reason, the address bus is buffered by IC2 and IC3; similarly, IC4 and IC5 are included as databus buffer. These four ICs have an interesting feature: the input circuits incorporate PNP transistors in such a way that the input current is limited to 100 μ A.

A shift register (IC6) is used as a buffer memory for the four highest address bits (MSBs). Using the 74LS95 at this point has the advantage that the NADS (Negative Address Strobe) can be used, without need for an inverter, to read in the four MSBs to the register.

The NADS is also used to control the databus buffers, in conjunction with the NRDS and NENOUT signals (Negative Read Data Strobe and Negative Enable Output, respectively). This combination may seem rather strange to those of our readers who have previously studied the Elektor SC/MP system. One would expect that the NWDS (Negative Write Data Strobe) would also be involved in the control of the databus buffers. After all, the NWDS is supposed to control



the storing of data in memory. Rest assured: that is still the case, even with this system. The only difference is that the NWDS no longer determines the moment when the data is applied to the databus. The timing sequence is such that the data is already present at the memory inputs before the NWDS signal initiates the writing of that data into the memory. The advantage of this system is that it makes for a more reliable 'write' cycle.

Reading data out of the memory is done in the usual way: the databus buffers are controlled by the NRDS. When addressing memories and the like, a signal is used that is derived (as in the Elektor SC/MP system) by ANDing the NRDS and NWDS signals, in N1. These two signals are also brought out separately to the system bus via N2 (NWDS) and N4 (NRDS).

It should be noted at this point that both the 74(LS)08 and the 74(LS)09 can be used as output buffers; the 09 is only required in DMA or multiprocessor systems. The reason for this is that the 74(LS)09 has so-called open-collector outputs, so that several of these ICs can be connected in parallel (with one common set of pull-up resistors) without 'biting' each other. If only a simple system is contemplated, with one CPU and without DMA, the 74(LS)08 can be used instead; the pull-up resistors R1, R2, R3 and R5 can then be omitted.

There is a further reason for controlling the databus buffers by means of a combination of the NADS, NRDS and NENOUT signals — quite apart from the increase in speed and reliability when writing data into the memory. In systems where the SC/MP is used without output buffers, DMA and multiprocessing present few problems, since its tri-state outputs can easily be set in the 'floating' mode. However, in the buffered system described here, the output buffers are not controlled by the NWDS

signal; they could easily remain in the 'write' mode, forcing 'hard' logic levels onto the databus. This possibility is precluded by using the NENOUT signal to terminate the 'write' mode. In order to understand how this works, the 'read' and 'write' cycles in the SC/MP system must be explained in slightly greater detail.

Reading and Writing

As is often the case, the best place to start this explanation is at the beginning: logic 0 level at the NRST input (Negative ReSET). This situation is achieved by operating S1. The set/reset flip-flop (N7, N8) applies logic 0 to the NRST input of the SC/MP for as long as this key is held down, causing the processor to assume its initial (reset) state. All outputs, with the exception of the NENOUT (Negative Enable Output), are then in the floating (tri-state) mode. The pull-up resistors R4, R6 and R10 hold the NWDS, NRDS and NADS outputs at a defined logic level (logic 1), so that nothing untoward can occur...

When S1 is released, the SC/MP will check for a logic 0 level at the NBREQ and NENIN inputs (Negative Bus RE-Quest and Negative Enable Input, respectively). Figure 4 illustrates this procedure. In a basic single-processor system without DMA facility, R7 will always pull the NBREQ input high. As soon as the processor detects this logic 1 level, it will proceed to use the same connection as NBREQ output. Since the logic 1 level signifies that no other part of the system is using the bus at present (obviously, in a simple system without DMA this is always the case, since there is only the one CPU), the processor proceeds to stake its claim to the bus by making the NBREQ output logic 0. Having done this, it tests the logic level at the NENIN input. Since this input is connected to the NBREQ output (by

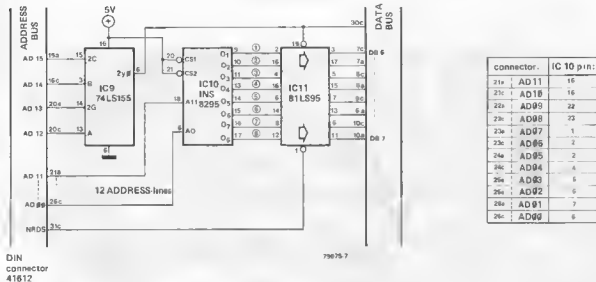
means of the link shown as a dotted line in figure 3) it will also be at logic 0 level. With both necessary conditions now fulfilled, the SC/MP will proceed to fetch its first instruction.

This first 'read' cycle is illustrated in figure 5. Shortly after the NBREQ output goes to logic 0, the NADS signal appears. The first register (IC6 in figure 3) takes this as its cue to store the four MSBs of the address; simultaneously flip-flop NS/N6 is set, switching the databus buffers into the write mode. However, when the NRDS signal appears it will reset this flip-flop and switch the databus buffers into the 'read' mode. The read cycle is terminated by a brief pulse on the NENOUT connection. In this case, the NENOUT pulse has no effect on the buffers — they had already been switched back to the floating state at the end of the NRDS pulse, as shown in figure 5.

The sequence of operations during the write cycle is similar, with one major difference: the output of N6 holds the databus buffers in the write mode for a much longer period. In fact, the NWDS signal falls well inside this period. The result is that the data to be stored are present at the memory input well before the NWDS signal appears, and remain there for a short time after this pulse is terminated. Finally, the NENOUT pulse causes the buffers to revert to the floating state.

The advantage of the system outlined above will become apparent from a closer look at the multiprocessor facilities that the SC/MP has to offer. Figure 6a gives a rough outline of a microcomputer system in which several SC/MPs are used. The first of these is connected in the same way as in the single-processor system described so far. For all the following SC/MPs, however, there is a minor modification to the circuit: the NENIN input of each is connected to the NENOUT of its predecessor in the

7



chain.

After the initial reset, the situation for the first processor is exactly as outlined above. All other processors, however, must wait for their turn: as long as one CPU is using the bus, all others must keep off. The principle is clear from figure 4: each time a CPU wants to 'get on the bus', it will first check the logic level on its NBREQ input. A logic 0 at this point signifies that one of the other SC/MPs is performing a read or write cycle at that moment, so that the bus is busy.

The interplay between the various CPUs is further determined by the NENIN and NENOUT signals. The rules of play are as follows. When a processor is using the system bus, its NENOUT is always at logic 1; if it is not on the bus, its NENOUT assumes the same logic level as that present at its NENIN. Bearing in mind that the NENIN must be at logic 0 before the actual read or write cycle can be initiated, the sequence of events is as follows.

Assume that a CPU somewhere in the middle of the chain wants to store some data in memory. Testing the NBREQ line, it discovers that this is at logic 0 and so it is forced to sit back and wait its turn. As soon as the NBREQ line goes high, the CPU quickly jumps in and pulls this line low again, staking its claim. This pulls the NENIN of the first SC/MP low and, assuming that this CPU is not interested in the bus, its NENOUT will follow - passing the logic 0 level on to number 2. The low NENOUT/NENIN level is passed down the chain in this way until it reaches the CPU that requested entry to the bus.

This unit takes this signal as a sign of approval, maintains its own NENOUT connection at a logic 1 level and proceeds to store the data.

It is, of course, conceivable that two CPUs jump in simultaneously when one other goes off the line - both pulling

Figure 6. A multiprocessor system contains several CPUs connected in a series chain as shown. The initial check procedure (illustrated in figure 4) ensures automatic 'time-sharing'; this is further illustrated in the pulse diagram given in figure 6b.

Figure 7. The (ROM) memory section of the BASIC microcomputer. The complete NIBL interpreter is contained in IC10.

the NBREQ line down to logic 0. No problem. The low level on the NENOUT/NENIN connections is passed down the chain until the first of the two CPUs is reached - and stops here! Only when that unit is finished with its read or write cycle will it produce a logic 0 level at its NENOUT (the NBREQ remains low because the second CPU is still holding it down), this signal then goes further down the chain until the second CPU is reached, and only then can it get onto the buses.

The same principles are involved in a Direct Memory Access (DMA) system: any other units (a terminal, for instance) that require direct access to the buses must include logic gating that provides the same relationships between 'NBREQ', 'NENIN' and 'NENOUT' signals. They can then be linked into the chain in exactly the same way.

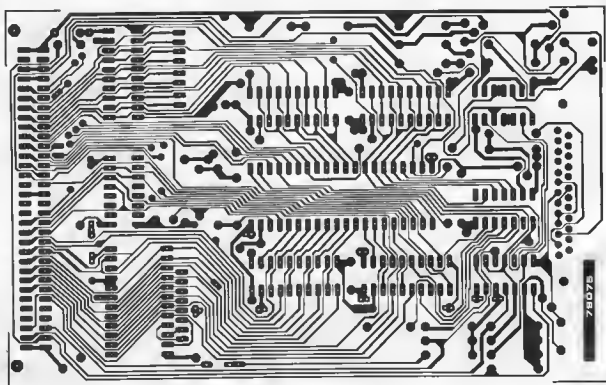
Memory

As stated earlier, the complete BASIC interpreter is stored in a single IC. This makes the memory circuit in the NIBL computer simplicity itself (figure 7).

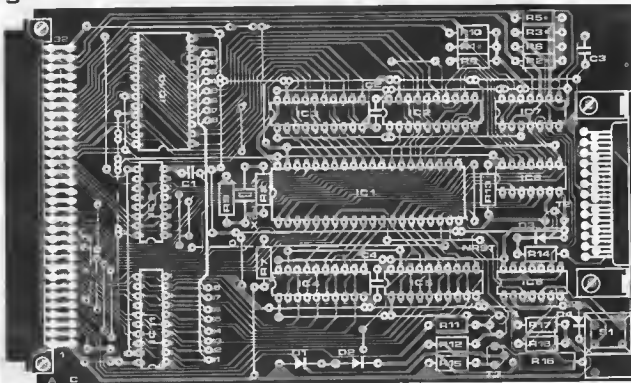
One integrated circuit, a 74LS155 (IC9), is used as address decoder. It detects the four MSBs of the address, and it is wired in such a way that the NIBL-ROM (IC10) is located on page 0 in the memory. The remaining twelve address lines go direct to the ROM; the outputs from the memory are buffered (IC11) and applied to the databus.

The output from the address decoder is also brought out to pin 30c of the edge connector. In the Elektor SC/MP system, this line is used for control of the databus buffer (EPS 9972). With this extra connection, the BASIC microcomputer is suitable for use as a replacement for the original CPU card in an existing Elektor SC/MP system with or without databus buffering.

8



9



| Resistors: | |
|----------------------|----------------------|
| R1 .. R3, R5 | = 2k2 |
| R4, R6, R7, R10, R11 | = 10k |
| R8 | = 100k |
| R9, R12 | = 1k |
| R13, R14 | = 4k7 |
| R15 | = 6ΩB |
| R16 | = 270Ω |
| Capacitors: | |
| C1 | = 27p |
| C2 ... C4 | = 100n |
| Semiconductors: | |
| T1, T2 | = 8C107B, 8C547B |
| T3 | = 8C177B, 8C567B |
| D1 ... D4 | = DUS |
| IC1 | = INS8060 (SC/MP II) |
| IC2, IC3, IC11 | = 81LS95 |
| IC4, IC5 | = 81LS97 |
| IC6 | = 74LS95 |
| IC7 | = 74LS08 |
| IC8 | = 74LS00 |
| IC9 | = 74LS155 |
| IC10 | = INS8295N |
| Sundries: | |
| 1 x 64-pin connector | DIN41612 (male) |
| 1 x 25-pin connector | 90° MIN D (female) |

Figure 8. Printed circuit board for the complete BASIC microcomputer (EPS 79075).

Figure 9. Component layout for the p.c. board. Note that some wire links are only required in certain applications.

NIBL

The NIBL-BASIC interpreter is a 4096 byte program for the SC/MP, that is used to 'translate' BASIC statements and commands to routines in machine language.

Use of BASIC as a programming language is explained in the BASIC course that is included as a series of supplements in the Elektor issues from March this year on. A brief summary of the commands and statements that are available when using NIBL is included in this article; some other details also need further clarification.

NIBL (National's Industrial BASIC Language) expects to find RAM storage area from address 1000H (on the 'H' stands for hexadecimal). The first 285 bytes of this memory are used by NIBL for storing data. All remaining memory from there on (i.e. from address 111EH) is available to the user.

Once the reset key has been operated, NIBL is ready to receive program lines. Single statements can be entered without a program line number, if required; in that case they will be carried out immediately (so-called 'direct' or 'immediate' mode). This can be particularly useful when testing a (section of) program. In the direct mode, variables can be given certain values so that the program can be started from a well-defined initial situation.

A program can be entered in two ways: from the keyboard of a terminal, or by means of a paper-tape reader or some similar device. In the latter case, the reader-relay should be controlled by the flag I output. However, relatively few people have access to a paper-tape reader and the associated 'hole-puncher', so a tape or cassette recorder will normally be used instead. For this, a cassette interface is required, as well as some additional 'software'.

The NIBL statements and commands are based on Tiny BASIC. However, NIBL contains several additional features. The most important of these are the DO ... UNTIL routine, which is derived from 'PASCAL', and the 'Indirect Operator'. The latter replaces the PEEK and POKE statements in other BASIC dialects: it can be used for direct addressing of the memory and I/O (Input/Output devices). Of lesser importance - although it can be useful - is the possibility of using so-called 'text variables'.

NIBL statements and commands

Program entry (program lines)

- a line without a line number is carried out immediately.
- a line with a line number is inserted in the program in the correct (numerical) position.
- line numbers from 0 to 32767 = $2^{15} - 1$ can be used.
- spaces are not permitted within 'Key words' (LET, IF, THEN, GOTO, GO-SUB, GO, TO, SUB, RETURN, IN-

PUT, PRINT, LIST, CLEAR and RUN).

- otherwise, spaces can be added in the program text as desired.
- SHIFT/O (or back-arrow on a teletype) deletes the letter that was typed in last.
- CONTROL/H (or backspace on a video terminal) has the same effect as SHIFT/O.
- CONTROL/U deletes the line that is being typed in at that moment, without affecting the data stored under that line number in memory.

Program control (commands)

- CLEAR returns all variables and 'stacks' to their initial state (usually zero).
- NEW erases page 1 in the memory.
- NEW n (where $2 \leq n \leq 7$) erases the corresponding page in memory.
- LIST initiates a print-out of the program from the first line or of the line number specified (e.g. LIST 200).
- RUN starts the program (starting at the first line).
- GOTO n (where $0 < n < 32767$) starts the program at the line number specified, without resetting the variables and stacks.

Variables, constants, operators

- 26 variables can be used: the letters A to Z.
- all operations ('expressions') are carried out using 16-bit 'two's complement' numbers.
- arithmetical operators: +, -, *, /.
- comparison symbols: <, >, =, <=, >=, <>.
- logic operators: AND, OR, NOT.
- decimal constants must remain within the range from -32767 to +32767.
- hexadecimal constants are recognised as such when preceded by the symbol #. Not more than four digits (16 bits) are permitted.
- program lines may contain more than one statement, provided the statements are separated by a colon (:).

Functions

- RND (a, b) generates a random number within the range from a to b.
- MOD (a, b) gives the remainder after the division a/b.
- STAT calls up the contents of the status register in the SC/MP.
- PAGE calls up the number of the page in memory that is currently in use.
- TOP calls up the upper boundary of the NIBL program, as a decimal address.

INPUT/OUTPUT statements

- INPUT X
 - INPUT X, Y, Z
 - PRINT "THIS IS NIBL"
 - PRINT "F = ", M * A
 - PRINT "SKIP", X, "PAGES";
- Note that the semicolon (;) suppresses the automatic CR/LF (Carriage Return/Line Feed) after a print statement.

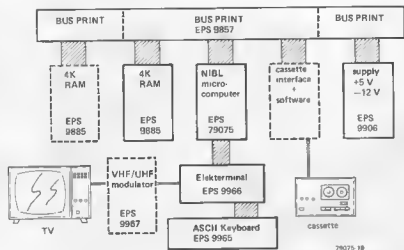


Figure 10. Block diagram of a complete BASIC microcomputer system with extension facilities, based on the main board described in this article.

Assignment statements

- LET X = 7
- E = 1 * R
- STAT = # 70
- PAGE = PAGE + 1
- LET @ A = 255
- @ (T + 36) = # FF
- B = @ (TOP + 5)

Control statements

- GO TO 15 or GOTO 15
- GOTO X + 5
- GO SUB 100 or GOSUB 100
- RETURN
- IF X + Y > # 1A GOTO 15
- IF A = B LET A = B - C
- FOR I = 10 TO 0 STEP -2
- NEXT I
- FOR K = 1 TO 5
- DO. X = X + 1: UNTIL (X = 10)
OR (@ X = 13)

Indirect operator

- the @ symbol can be used for immediate addressing of a location in memory; for instance: V = # 2000: LET @ V = 100 results in the decimal number 100 being stored at memory location 2000_H. Similarly, LET W = @ V gives the variable W the value stored in memory location V.

String handling (text facilities)

- \$A = "ONE LINE OF TEXT"
- PRINT \$T, \$(TOP + 72)
- INPUT \$(U + 20)
- U = \$(TOP + 2 * 36)

Sundries

- LINK (address): The program is continued in machine language, from the address indicated. The address must be given as a decimal number.
- REM offers the possibility of adding explanatory text (comments, reminders) to the program.
- END: this statement is used to con-

clude a program, and to add 'break points'.

Error indications

As soon as a program is started, error indications may appear as a result of incorrect or incomplete use of NIBL. The general error indication format is as follows:

... ERROR AT ...

The first four characters indicate the type of error; the final characters (up to five) give the line number. For example, incorrect use of a statement at line number 4500 would result in the print-out: STMT ERROR AT 4500

Error indications in NIBL all use 'words' of up to four letters. The following indications are possible:

- AREA The memory space available on the chosen page is exceeded.
- CHAR Redundant or incorrect characters in or following a statement.
- DIV0 Division by zero.
- END* No quotation marks after text to be printed.
- FOR FOR is not followed by NEXT.
- NEXT Subroutine possibilities are exceeded.
- NEXT NEXT used without FOR.
- NOGO The line number specified in a GOTO or GOSUB statement does not exist.
- RTRN RETURN was not preceded by GOSUB.
- SNTX Incorrect syntax.
- STMT Incorrect use of a statement.
- UNTIL UNTIL is used without DO.
- VALU Incorrect constant or number outside the range.

The p.c. board

The complete circuit can be mounted on the p.c. board shown in figure 8. The

board size corresponds to that used in the Elektor SC/MP system: it is Euro-card format, and the edge connector corresponds to the system bus. A second connector is included on the other end of the board; this is intended for connecting a teletype or videoterminal according to the RS232C/V24 standard. This 25-pin connector is variously referred to as a 'female modem connector' and as a 'D connector'.

Where possible, the component layout shown in figure 9 indicates which wire links should be included for a particular application. Reference to figure 3 should further clarify matters.

A complete microcomputer

The unit described here obviously requires a few additional circuits to be fully operational. A minimum system would consist of one bus board, a power supply board, one 4K RAM card and the BASIC computer card described in this article. The system can be extended by adding up to six memory cards.

An obvious choice for in- and output unit is the Elekterterminal. The complete Elektor BASIC microcomputer would then consist of the units shown in figure 10.

Lit.

1. SC/MP data sheet, pub. no. 420305227-001A
2. SC/MP instruction guide, pub. no. 4200110A.
3. SC/MP technical description, pub. no. 4200079A.
4. SC/MP microprocessor applications handbook, pub. no. 420305239-001A.
5. SC/MP programming and assembler manual, pub. no. 4200094B.
6. Elektor E31 ... E36 (November 1977 ... April 1978).

NIBL-E

A BASIC interpreter for the Elektor SC/MP system

A BASIC interpreter for the SC/MP has been available for some time. However, this can only be used in systems where page 0 is available for storing the interpreter program. In the Elektor SC/MP system, part of page 0 is used for the monitor program. Even so, an adapted version of the interpreter CAN be incorporated into the Elektor system — as described in this article.

(D. Hendriksen)

The BASIC interpreter for the SC/MP is known as NIBL. This is an abbreviation of National's Industrial BASIC Language.

This interpreter program occupies nearly 4K bytes, or one page in a SC/MP system. It would be asking too much to expect a complete BASIC interpreter in this area; for this reason, NIBL is derived from Tiny BASIC. Consequently, only whole numbers can be used in calculations, and the number range is limited: only numbers between -32767 and +32767 are permitted. Furthermore, 'scientific' calculations are outside the scope of NIBL; fortunately, they are not really essential.

Looking on the positive side, NIBL has some capabilities that are not included in Tiny BASIC. In fact, NIBL is more powerful in some ways than more sophisticated BASIC dialects. This is especially true of the IF... THEN... statement and the DO... UNTIL loop. NIBL is intended for self-contained SC/MP systems, where the interpreter can be started by operating the 'reset' key.

The programs can be stored in pages 1...7. As mentioned above, page 0 is normally occupied by the NIBL interpreter itself. Part of page 1 is used as 'scratch-pad memory' by the interpreter, so some RAM must be reserved in this area.

After starting the interpreter program (by means of the 'reset' key), NIBL will first check to see whether a program is present in page 2. If so, it will run this program immediately; if not, it will prepare page 1 to receive a program and wait until this is entered. If a different page is to be used, this can be specified by using the PAGE= (n) command, where n is 1...7.

Fitting NIBL into the Elektor SC/MP system

If NIBL is to be used in the Elektor system, some modifications are required. Page 0 is not available for the interpreter, since this area is used in part by 'Elbug'. Something's got to

move, and in this case it's the interpreter.

Fortunately, the SC/MP's CPU structure makes it a relatively easy matter to move a program. Normally, only instructions relating to pointer manipulations need changing. There are, of course, exceptions to this rule... and NIBL is one of them. It not only uses the three pointers: in the course of the program, some data-bits are also used to determine addresses. As a result of all this, the NIBL version described here contains some 300 modifications with respect to the original.

Placing Elbug on page 0 offers both advantages and disadvantages. The main disadvantage is that NIBL has to be moved; the main advantage is that the cassette routines in the monitor program can be used for storing programs on tape. In the Elektor version, there is no need for a paper-tape reader/puncher; in the original version of NIBL, some further modifications would be required to obtain the same easy cassette storage facility.

Modifications

It was decided to move the interpreter program to page 1. Admittedly, this costs one page of program memory — leaving six pages for the user. The possibility was considered of moving the interpreter out past the program memory — 'above' page 7 — but this would require a large number of additional modifications.

When the interpreter is moved, its 'scratch-pad memory' will also move up one page, to page 2. Therefore, RAM must be available at the top of this page. The interpreter program itself can be stored in EPROM. This is cheaper than using a complete 4K RAM card and, furthermore, the interpreter is then always available for immediate use. The RAM area at the top of page 2 must consist of at least 2K bytes. This is sufficient for a BASIC program of approximately 60 lines — more than enough for the first experimental programs.

Since the interpreter is on page 1,

```

1800 08 08 08 C4 20 36 C4 1C 32 C4 21 35 C4 20 31 C4
1818 FF C5 00 C9 01 C4 83 CA P6 C4 82 31 C4 38 35 89
1828 02 01 A9 02 C1 80 CA 8D 98 19 BA P6 C1 FF C9 00
1838 C9 01 C4 8D C9 FF P5 02 F4 10 EA 58 08 05 EA 88
1840 08 59 E8 C4 00 CA PA C4 P5 C4 50 CA FB C4 1C CA
1850 FA C4 00 CA EA 01 FD C4 80 EA CA 00 EA 01 C4 34 60
1862 9C F4 C4 58 CA FD C4 7A FA FF C4 6A CA FC C4 A6
1872 CA F9 C4 BA CA FE C2 FB 33 C2 FA 37 C7 01 01 C7
1880 01 33 CA FB 48 D4 1F DC 10 37 CA F4 48 D4 E8 EA
1892 20 98 2F EA A8 98 07 EA C8 98 E1 3F 98 D8 C2 F9
18A2 EA D6 9C C4 C4 0A 90 6F EA D6 33 CA EA C4 20 37
18B0 01 C2 FB CF 01 C2 FA 00 01 C2 EA 33 CA F9 48 37
18C0 90 BA CA E7 C5 01 EA 20 98 FA C5 FF C2 FA 37 CA
18D0 DC C2 FB 31 CA ED C7 01 81 BA E7 08 D4 F7 E5 01
18E2 9C 87 48 94 F1 98 95 90 80 C2 E7 01 C5 80 C2 ED
18F2 03 C2 DC 37 C9 C4 C4 20 37 C2 F9 33 C7 FF 01 C7
1900 FF 33 CA F9 40 37 98 B8 90 41 C2 FC 8A 7A 98 1C
1110 AA FC AA FC 33 C4 20 37 C2 F9 8A 35 CB FF 35
1120 31 CB FE 31 90 C1 C4 FF CB FF 98 BB C4 8A 90 1B
1130 C5 01 E4 20 98 FA C4 20 98 EA 47 9C 01 3F C4
1140 8A 90 08 C2 FC EA 6A 9C C4 C4 09 98 40 BA FC BA
1150 FC 33 C4 20 37 C3 01 94 06 C4 09 C4 P4 98 88 35
1160 C3 00 31 C4 01 C4 P4 90 F4 C2 F2 94 04 C4 08 98
1170 1C C4 01 CA P4 3F C4 1F 37 C4 C1 33 C5 01 EA 22
1180 98 D8 EA 2F 98 05 E4 00 3F 90 EB C4 07 90 35 C4
1190 20 37 AA FD AA FD 33 C4 0A CB FE C4 00 CB FF C4
11A0 05 CA E7 C4 FF CB 05 C3 FD 94 13 C4 20 CB 04 C4
11B0 08 03 FB FC CB FC C4 00 FB FD CB 98 9F C4 28
11C0 CB 04 90 98 57 AA FD AA FD 31 C4 20 35 AA E7
11D0 01 C1 81 DC 38 C9 88 C1 FD D9 FC 98 BA C4 1F CA
11E0 FA C4 33 CA FB 08 D6 C4 1F 37 C4 C1 33 C2 F5 9C
11F0 06 C1 84 3F C2 E7 01 C5 80 C1 00 3F C5 FF 94 FB
1200 C4 50 CA FD C2 F5 9C BA C4 20 3F 90 B5 C4 1F 37
1210 C4 C1 33 C4 8D 3F 08 BA 3F 90 A7 C4 85 CA EB C2
1220 EB CA C4 1F 37 C4 C1 33 C4 8D 3F C4 8A 3F C4
1230 1F 35 C4 3B 31 BA FE 98 05 C5 01 94 FC 90 F6 C5
1240 01 3F C1 FF 94 F9 C2 EA EA 08 98 00 C4 1F 35 C4
1250 3B 31 C5 01 3F C1 FF 94 F9 C2 F4 98 40 20 3F
1260 C4 1F C4 54 3F C4 20 37 AA FD AA FD 33 C2 F7
1270 CB 31 C2 FB CB FE C4 31 CA FB C4 1E CA FA 90 99
1280 C4 1E 98 9D C2 F4 98 22 C1 80 D4 80 9C 01 06 D4
1290 28 98 ED C1 FF EA 00 9C 08 05 01 C4 F7 05 02 CA
12A0 F8 C4 1C CA C4 86 CA FB F3 CA 00 CA P4 C4 50
12B0 CA FD C4 1C CA FB C4 1C CA FA C4 A6 CA P9 90 BE
12C0 AA F4 C2 E9 35 C2 E8 31 C4 6A CA 00 C4 8A CA FE
12D0 C4 7A CA FF 3F 90 EA 33 C5 01 CB FF C5 01 CB FE C5
12E0 28 37 AA FD AA FD 33 C5 01 CB FF C5 01 CB FE C5
12F0 01 C4 C1 P5 90 DE C4 00 CA F5 C4 12 37 C4 83
1300 33 3F 90 D1 98 D1 C4 1F 37 C4 C1 33 06 D4 28 98
1310 E6 C5 01 E4 00 98 05 E4 8D 3F 90 F9 C4 8D 3F C4
1320 BA 3F C2 C4 48 CA FB C4 1C CA FA 90 AC C4 20 37
1330 BA FD BA FD 33 02 C3 FE F3 00 CB FE C3 FF F3 01
1340 CB FF 90 BE C4 28 37 BA FD BA FD 33 03 C3 FE FB
1350 00 CB FE C3 FF FB 01 CB FF 90 A7 C4 28 37 C2 FD
1360 33 03 C4 00 FB FE CB FE C4 00 FB FF CB FF 90 D2
1370 90 92 C4 20 37 C2 FD 33 C3 FF E3 FD CA EA C3 FF
1380 94 00 03 C4 00 FB FE CB FE C4 00 FB FF CB FF C3
1390 FD 94 00 03 C4 00 FB FE CB FC C4 00 FB FD CB FD
13A0 C4 00 CB 00 CB 01 CB FC CB 03 C4 10 CA EB C3 FF
13B0 1F CB FF C3 FE 1F CB FE 06 94 11 02 C3 02 F3 FC
13C0 CB 02 C3 03 F3 FD CB 03 90 82 90 A4 02 C3 03 1F
13D0 CB 03 C3 02 1F CB 02 C3 01 1F CB 01 C3 00 1F CB
13E0 0A BA EB C9 C5 98 02 98 05 C2 EA 94 00 03 C4 00
13F0 FB 00 00 CB 00 C4 00 FB 01 CB 01 C3 00 CB FC C3 01

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1400 CB FD BA FD BA FD 90 DF C4 20 37 C2 FD 33 C3 FF
1410 DB FE 9C 04 C4 0D 90 B2 C3 FD E3 FF CA EA C3 FD
1420 94 11 C4 00 03 FE FB CB 03 C4 00 FB FD CB 02 90
1430 BA 90 BA C3 FD CB 02 C3 FC CB 03 C3 FF 94 00 C4
1440 00 03 FB FE CB FE C4 00 FB FF CB FF C4 00 CB 01
1450 CB 00 CA EB CB FD CB FC 02 C3 FC FC FC CB FC C3
1460 FD F3 FD FD FD 02 C3 03 F3 03 CB C3 CB C2 F3 02
1470 CB 02 C3 01 F3 01 CB 01 C3 00 F3 03 00 CB 03 C3
1480 01 FB FE CB 01 C3 00 FB CB FF 00 94 11 02 C3 E4
1490 F3 FE CB 01 C3 00 F3 1F CB 00 90 80 90 93 C3 FC
14A0 DC 01 CB FC CA EA EB EA 08 9E AC EA 94 00 C4 00
14B0 03 FB C2 CB C4 00 FB FD CB FD BA FD BA FD 90
14C0 DB C4 20 37 C2 FD 33 C7 FD 01 C3 01 CA 00 02 40
14D0 F4 01 01 C3 02 CA 88 33 CA FD C4 18 37 C4 75 33
14E0 3F C5 01 EA 20 98 FA C1 FF 03 FC 5B 94 05 03 FC
14F0 E6 94 12 C5 FF C2 FB 33 C2 FF C3 00 CA FA C3
1500 01 CA FB 90 D5 01 C1 00 03 FC 5B 94 05 03 FC E6
1510 94 E1 C4 20 37 AA FD 33 02 40 70 CB FF C4 02 02
1520 F2 FA CA FB C4 00 F2 FA CA FA 90 EA C4 20 37 AA
1530 FD 33 C3 FE 01 C2 00 CB FE 02 48 F4 01 81 C2 60
1540 CB FF 90 96 C4 01 90 12 C4 02 98 EB C4 03 90 BA
1550 C4 04 90 06 C4 05 98 02 C4 06 CA 00 CB C4 20 37 BA
1560 FD BA FD 33 03 C3 FE FB 00 CA EF C3 FF 01 CA
1570 EB E3 FF 01 C3 FF 03 E3 00 EA E2 EE CA C2 EE DA
1580 EF 98 02 C4 00 E4 00 01 BA EB 9C 85 40 98 2B 98
1590 B1 BA EB 9C 05 E4 00 E4 90 20 BA EB 9C 04 C2 EA
15A0 90 18 BA EB 9C 05 40 DA EA 90 0F BA EB 9C 07 40
15B0 DA EA EA 88 90 04 C2 EA EA 88 94 04 C1 91 90 02
15C0 C4 00 CB FE C4 00 CB FF C4 18 37 C4 F5 33 3F 90
15D0 BE C2 EF DA EE 98 02 98 B6 C5 01 E4 00 9C FA C4
15E0 12 37 C4 83 33 3F 90 A7 C4 10 98 06 C4 82 90 02
15F0 C4 03 CA EB C4 20 37 BA FD BA FD 33 BA EB 9C 0E
1600 C3 01 D3 FF CB FF C3 00 D3 FE CB FE 98 D8 BA EB
1610 9C 00 C3 01 DB FF CB FF C3 00 DB FE CB FE 90 C6
1620 C7 01 E4 FF CB FF C7 01 EA FF CB FF C3 CA FD 90
1630 B5 C2 F1 31 CA F1 C2 60 35 CA F0 3F C2 F4 98 01
1640 3F C4 03 CA EB C4 12 37 C4 1E 33 FF AA FD AA FD
1650 33 04 20 37 C4 00 CB FF CB FE CA EB C5 01 E4 28
1660 98 FA C5 FF C1 00 03 FC 3A 94 09 03 FC P6 94 13
1670 98 32 98 03 FC 00 84 94 2B 03 FC FA 94 02 90 24
1680 02 F4 0A C4 04 CA EA CA EB C3 FE 02 F3 FE CB
1690 FE C3 FF F3 FF CB FA EA 9C EP C3 FE 58 FB CB
16A0 C5 01 98 02 C2 EB 9C 87 C4 05 98 97 C5 01 E4 28
16B0 98 FA C5 FF 03 FC 3A 94 05 03 FC P6 94 21 C2 FB
16C0 33 C2 FA 37 C3 00 CA FA C3 01 CA FB 98 A4 C4 02
16D0 E2 F2 FB CA FD C4 00 F2 FA CA 90 95 98 CB 01
16E0 C4 20 37 AA FD AA FD 33 C4 00 CB FF 94 82 CB FE C5
16F0 01 C1 80 03 CA 94 06 03 FC P6 94 08 90 CF 01
1700 C3 FF CB 01 C3 FE CB 00 C4 82 CA EA 82 C3 FE F3
1710 FE CB C3 FF F3 FF CB FF D4 80 9C BA EA 9C
1720 EB 02 C3 FE F3 00 CB FE C3 FF F3 01 CB FF D4 88
1730 9C 1F 02 C3 FE F3 FE CB FE C3 FF F3 FF CB FF D4
1740 90 9C 0E 02 48 F3 FE CB FE C4 00 F3 FF CB FF 94
1750 9C 04 06 90 88 90 84 C4 20 35 C4 D6 31 C4 00 CA
1760 E7 F4 1F 37 C4 C1 33 C2 F4 98 08 C4 3F 3F C4 20
1770 3F 90 03 C4 3F C4 1F 37 C4 76 33 3F C4 C1 33
1780 40 98 F3 E4 8A 98 EF 48 E4 8D 98 58 40 E4 5F 98
1790 41 08 E4 80 98 36 40 E4 15 98 0F 40 E4 03 9C 1A
17A0 C4 5E 3F C4 43 3F C4 8E 98 A9 C4 5E 3F C4 55 3F
17B0 C4 00 3F C4 3F 90 9F 90 98 40 01 EA E7 EA
17C0 48 9C C4 0A 81 40 3F 90 12 98 07 C4 20 3F C4
17D0 08 3F C2 E7 98 BA EA E7 C5 FF 90 9A 40 01 C4
17E0 8A 3F C4 20 35 C4 D6 31 98 CE C4 20 37 C2 FD 33
17F0 C3 FF 35 01 C3 FE 31 CA EF C1 00 CB FE C4 00 CB

```

Elbug must be used to start the program. The normal hex-I/O start procedure is used; since the desired program is on page 1, the initial command is 'ru1000ru'.

Once started in this way, the first thing the interpreter does is look for a program on page 3 (not page 2; everything has been moved up one page!). If it finds a program there (stored in ROM), this will be run immediately. This first program can, if necessary, run over more than one page. However, as when programming in machine language, a

pointer change will then be required; when programming in NIBL, this is achieved by entering the instruction PAGE = PAGE + 1. The interpreter will 'read' this as an instruction to continue the program on the first line of the next page.

Obviously, this is a useful feature - not only when running an initial program that is stored in ROMs, but also when programs are stored in RAM. To achieve this latter capability, some further modifications in the original NIBL interpreter program proved necessary.

The problem is that the original NIBL version not only looks for a program in page 2; it also requires that this program is stored in ROM. If the program is stored in RAM, the interpreter refuses to run it! Not only that, it also blocks any programs stored on any of the other pages at the same time.

The reason for this 'mulishness' is that NIBL, on finding a program on page 2, proceeds to write an 'end-of-program' indication at the top of each page - or tries to, at least. This indication consists of 'Carriage Return' (0D), followed by


```

1800 FF C2 EF 31 40 35 90 B0 C4 20 37 C2 FD 33 C7 FE
1810 01 C7 FF CA EA C7 FF 33 CA FD C2 EA 37 40 CB 00
1820 90 CB 06 A6 C4 20 37 C2 FD 33 C3 01 CA F7 C3 00
1830 CA F8 C2 F1 33 C2 F8 37 C4 04 CA E7 C7 01 EA 0D
1840 90 84 AA E7 90 F6 C2 E7 EA 04 9C 02 CA E7 C2 07
1850 01 C2 F2 94 06 D4 7F CA F2 90 18 C5 83 40 02 P4
1860 FC 01 C5 01 E4 0D 98 8B 40 02 E4 FF 01 90 F3 90
1870 AF 90 AF 40 DA E7 98 F7 C4 7A CA F4 C6 6A FC
1880 C4 BA CA FE 40 98 60 94 10 C1 00 C9 80 C5 01 94
1890 F6 C1 00 94 F4 C9 80 90 4E C1 FE CA EA C4 FF C9
18A0 FE C4 50 C9 FF C5 01 94 CF C1 00 94 8F 35 CA EE
18B0 35 C1 CA EF 31 C2 02 78 C4 00 F2 EF E2 EE D4
18C0 F0 90 93 C4 00 01 C0 F0 F9 C9 80 C5 FF 94 FA C1 01
18D0 EA 50 98 04 C1 00 94 C2 EA C9 00 C4 00 C9 01
18E0 40 9C 04 C4 02 90 8A C2 E7 98 4A C2 F1 C1 C2 P8
18F0 35 C2 F3 33 C2 F2 37 C2 F7 CF 01 C2 P8 CF 01 C2
1900 E7 CF 01 C5 01 CF 01 E4 0D 9C F6 90 C4 C4 10 37
1910 CA 75 33 F7 90 CF BA BA FD 33 C2 20 37 C3 00
1920 CA EF C3 01 CA EE 90 E5 C2 FF 01 40 EA 7A 9C 04
1930 C4 8F 90 0D C2 EF EA EE 98 06 BA FF BA FF 90 CD
1940 40 33 C4 20 37 C3 FF 35 C3 FE 31 90 C0 C2 EF D4
1950 F7 07 90 89 90 BE C4 20 37 AA FD 33 C3 06 CB
1960 FE C4 00 CB FF 90 E2 C2 EE 37 C2 EF 33 C7 FF 3F
1970 C4 20 36 C4 1C 32 90 D4 C2 FF EA BA 9C 94 C4 8A
1980 90 D2 AA FF AA FF FF 33 C4 20 37 35 CB FF 35 C1 30
1990 FE 31 90 BE C2 E9 37 C2 E8 33 C3 00 94 02 90 87
19A0 C3 02 01 F7 80 90 F3 C7 02 AA FD AA FD 33 01 C4
19B0 20 37 CB FF 40 CB FE 90 D9 C5 01 EA 0D 9C FA 3F
19C0 C2 FD 33 C4 20 37 C3 03 CB FE C3 02 CB FF 90 C2
19D0 90 AE C4 00 CA EB C2 E5 01 C2 E4 CA EB 9C E2 E5 02
19E0 70 81 C2 EA 02 F2 E9 CA EA BA EB 90 F8 40 E2 F4
19F0 07 81 C2 ED 02 F4 07 1E CA EA 0A 96 98 03 4A CA
1A00 E5 C2 FD 33 C4 20 37 C4 01 CB 00 C4 00 CB 01 C3
1A10 FE CB 02 C2 FE CB 03 C3 CB BA C4 03 FD CB 05 C2
1A20 EA CB 02 C2 E5 EA FF D4 7F CB FF 87 06 33 C4 FD
1A30 90 9C 90 9C AA FD AA FD 33 C4 20 37 C4 00 CB FF
1A40 C4 01 CB FE 90 EA C2 FF E4 A6 9C 04 C4 0A 90 E2
1A50 EA A6 31 C1 C3 C4 20 35 CA F0 C2 FD 33 C4 20 37
1A60 C3 90 CD 01 C3 CF CD 01 C3 FD 01 C3 FE CD 01
1A70 C3 FF CD 01 C2 F1 CD 01 C2 F0 CD 01 35 C2 F1 31
1A80 CA FE C7 FC 33 CA FD 90 A7 C2 FE EA BA 9C 04 C4
1A90 0B 90 BB EA 8A 31 CA F1 C4 20 35 CA F0 C2 FD 33
1AA0 C4 20 37 C7 FF EF F9 98 06 C4 0C 98 A1 E1 F9 81
1AB0 C2 00 02 F1 FC CA 00 CB 00 C6 01 C2 00 F1 FD CA
1AC0 80 CB 01 C6 FF C1 FA CB 02 C1 FB CB 03 C1 FD 94
1AD0 10 C4 04 CA EB C7 01 EA FF CB FF BA 9C 90 F6 90
1AE0 02 C7 04 33 CA FD C2 F1 31 C2 P8 35 90 99 C2 EF
1AF0 90 88 C2 FE 02 F4 F9 CA FE 3F C2 FF 33 C4 20 37
1B00 C3 FF 35 C3 FE 31 90 EA 90 A1 C2 EE 35 C2 FE 31
1B10 C4 1F 37 C4 C1 33 C5 01 EA 07 98 D0 EA 0D 3F 06
1B20 D4 20 9C F2 90 C6 C2 EE 37 C2 EF 33 C5 01 CF 01
1B30 EA 0D 9C F8 90 B6 C2 EF 33 C2 EE 37 C5 01 EA 22
1B40 90 8E EA 2F 9C 04 C4 07 90 9E EA 0D CF 01 90 EC
1B50 C4 0D CB 00 0E DE C2 FD 33 C4 20 37 C7 FF 35 C7
1B60 FF 31 C7 FF 01 C7 FF 33 CA FD 40 37 C5 01 CF 01
1B70 EA 0D 98 C8 06 04 20 9C F3 98 B9 AA FD CA FD 33
1B80 C4 20 37 C2 F6 CB FE C4 00 CB FF 98 A7 C2 EF D4
1B90 06 98 04 C2 EF CA F6 37 C2 F6 EA 02 9C 09 C4 21
1BA0 CA EA C4 20 CA EB 3F EA 02 01 C4 04 CA EB C2 02
1BB0 70 81 BA EB 98 F4 CA EA C4 02 CA EB 3F C2 E9
1BC0 35 C2 E8 31 3F 35 01 40 35 40 1C 1C 1C CA F6
1BD0 3F C2 E9 35 C2 E8 31 C4 0D C9 FF C4 FF 09 C9
1BE0 01 3F C2 E9 35 C2 E8 31 C1 00 EA FF 94 12 03 C1
1BF0 01 FA EF C1 00 FA EE 94 07 C1 02 01 C5 80 90 E8

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1C00 31 CA F3 31 35 CA F2 35 C2 EF 01 01 9C 07 C2 EE
1C10 E1 00 9C 01 3F C2 F2 DC 00 CA F2 3F 12 0C 17 56
1C20 2C 25 8D 40 1E 16 AB 1C 35 1B 97 16 30 19 15 18
1C30 E1 18 23 4C 1E 2C 51 4C 49 53 D4 1B 97 16 AB 1C
1C40 47 19 15 10 E1 4C 49 1B BD 12 D8 8F 2F 13 05 4C
1C50 1C 2C 60 52 55 CE 11 2F 1B 97 1B 12 0F 12 83
1C60 2C 6D 43 4C 45 41 D2 11 2F 10 50 12 2F 2C 86 4E
1C70 45 07 16 AB 1C 78 4C 7A 1A 33 11 29 15 15 18 9C
1C80 1B 97 1B D0 12 C3 2C 8B 4C 54 D4 1E 8 1C 9A 2E
1C90 2F BD 8E 35 14 C0 11 2F 12 83 2C AA 08 8E AC 2E
1CA0 2F BD 8E 35 18 07 11 2F 12 83 2C BC 49 C6 8E 35
1CB0 2C 86 54 4E 45 CE 19 15 10 D0 4C 86 2C D1 55 4E
1CC0 54 49 CC 16 3B 8E 35 11 2F 19 15 17 27 1B C4 12
1CD0 63 2C DD 44 CF 16 38 11 2F 19 17 12 83 2D 00 47
1CE0 3C 2C EB 54 CF 8E 35 11 2F 4C P6 2E 53 55 C2
1CF0 8E 35 11 2F 11 09 1B 97 19 15 18 E1 11 68 12 83
1D00 2D 10 52 45 54 55 52 CE 11 2F 11 42 1C 4A 12 83
1D10 2D 2A 4E 45 58 D4 16 3B 14 08 1E 2F 11 2F 1A 88
1D20 8E 5F 19 15 1A ED 1B C4 12 83 2D 54 46 4F D2 16
1D30 3B 14 0A 1E 2F 2E 2F BD 8E 35 2E 2F 3F CE 8E 35
1D40 2D 4A 53 54 45 D0 8E 35 4D 4C 1A 33 11 2F 1A 45
1D50 14 0C 12 83 2D 67 53 54 41 D4 2E 2F BD 8E 35 19
1D60 15 19 4C 11 2F 12 83 2D 7E 50 41 47 C5 2E 2F BD
1D70 8E 35 11 2F 19 15 18 9C 1B 97 1B BD 12 83 2D 9E
1D80 4A 8E AC 2E 2F BD 2D 8F A2 19 15 18 35 4D 9A 2E
1D90 2F AA 8E AC 16 38 1B 55 16 30 11 2F 12 83 2D D1
1DA0 50 D2 2D A7 49 4E D4 2D AE A2 11 75 4D C1 2D BD
1DB0 A4 8E AC 16 38 19 15 1B 97 16 30 4D C1 8E 35 8F
1DC0 2F 2D C6 AC 40 A7 2D CB 88 4D 12 C0 1E 2F 12 12
1DD0 83 2E 09 49 4E 50 55 D4 16 3B 14 08 1E F6 16 30
1DE0 17 56 8E 35 14 08 16 38 2E 05 AC 14 00 1E 2F 16
1DF0 30 2E 2F AC 40 E2 2E 2F AA 8E AC 16 30 17 56 19
1E00 15 2E 15 16 30 11 2F 12 83 2E 12 45 4E C4 11 2F
1E10 12 7F 2E 26 4C 49 4E CB 8E 35 11 2P 16 30 19 15
1E20 19 66 16 30 12 83 2E 2F 52 45 4D 19 88 12 83 FD
1E30 1A 8F 2F 12 A9 8E 61 2E 3E BD 8E 61 15 43 2E 53
1E40 9C 2E 48 BD 8E 61 15 4F 2E 4F BE 8E 61 15 47 8E
1E50 61 15 40 2A 8E BE 2E 50 BD 8E 61 15 57 8E 61 15
1E60 53 2E 6E AD 8E 6D 13 5A 4E 6F 2E 6D AB 8E 6D 2E
1E70 78 AB 8E 6D 13 2C 4E 6E 2E 81 AD 8E 6D 13 43 4E
1E80 6F 2E 8B 4F D2 8E 8D 15 EB 4E 6F 10 8E 8E AC 2E
1E90 96 AA 8E AC 13 71 4E 8E AC 15 E7 4E 8F 14 07 4E
1EA0 8F 2E 8B 41 4E CA 8E AC 15 E7 4E 8F 14 07 1E B4
1EB0 15 2B 10 15 16 AB 1E BA 10 F5 2E C1 3 16 4B 10
1EC0 F5 2E CB A8 8E 35 2E A9 10 15 P5 2E D4 C0 8E AC
1ED0 17 89 10 P5 2E DF 4E 4D 4E 8E AC 15 F0 10 P5 2E
1EE0 E9 53 54 41 D4 19 55 10 F5 2E P4 54 4F D0 1B 97
1EF0 19 93 10 P5 2F 01 4D 4F 4C 8F 20 14 47 19 1B 10
1F00 P5 2F 16 52 4E C4 8F 20 19 D1 13 43 13 2C 14 07
1F10 19 8F 13 2C 10 P5 2E 50 41 47 C5 1B 7A 10 P5
1F20 2E 2F AB 8E 35 2E 2F AC 8E 35 2E 2F A9 10 P5 16
1F30 30 11 8E 14 07 11 C5 16 30 10 P5 20 45 52 52 4E
1F40 D2 41 52 45 C1 53 54 4D D4 43 48 41 D2 53 4E 54
1F50 D8 56 41 4C D5 45 4E 44 A2 4E 4F 47 CF 52 54 50
1F60 CE 4E 45 53 D4 4E 45 58 D4 46 4F D2 44 49 56 80
1F70 42 52 CB 55 4E 54 CC C4 08 CA EB 06 DC 00 87 06
1F80 D4 20 9C F7 C4 57 8F 04 06 D4 20 9C F2 06 D4 FF
1F90 D2 01 07 C4 7E 8F 08 06 D4 20 98 04 C4 01 90 04
1FA0 C4 00 9C 00 CA EA 1F 01 10 81 06 DC 01 E2 EA 07
1FAB BA 9C 9F 06 D4 FE 07 8F 8F 88 4D 7A 07 40 3F
1FC0 90 B5 01 C4 FF 8F 17 86 DC 01 07 C4 89 CA EB C4
1FD0 8A 8E 88 BA 98 10 4D D4 C1 CA E9 81 1C 01 06
1FE0 01 E2 E9 07 98 8E 8E D4 FE 07 3F 90 D4 00 00
1FF0 C4 19 37 C4 63 33 00 00 00 00 00 00 00 00 00

```

'FF'. If the program on page 2 was stored in ROM, no harm is done: the contents of the memory location at the top of the page cannot be altered, so the 'end-of-program' indication is not stored there. A jump to the next page for the continuation of the program is also possible, provided this continuation is also stored in ROM.

In the Elektor SC/MP system, however, programs will normally be stored in 4K RAM cards. The 'end-of-program' indication would then block every page. For this reason, NIBL-E is modified to

Table 1. Listing of the 4K NIBL-E interpreter.

Table 2. The interpreter can easily be adapted to virtually any transmission rate, by modifying the data in the nine addresses given here.

| Address | Baud rate | | | |
|---------|-----------|-----|-----|------|
| | 110 | 300 | 600 | 1200 |
| 1FB5 | 57 | 76 | A7 | 3D |
| 1FB7 | 04 | 01 | 00 | 00 |
| 1F94 | 7E | E5 | 45 | 76 |
| 1F96 | 0B | 02 | 01 | 00 |
| 1FB9 | 0B | 06 | 04 | 02 |
| 1FC4 | FF | 64 | 25 | 56 |
| 1FC5 | 17 | 06 | 03 | 01 |
| 1FD0 | 8A | F0 | 50 | 81 |
| 1FD2 | 0B | 02 | 01 | 00 |

ensure that this indication is only stored at the top of all pages under condition that no initial program is found on page 3. The only page that will still be blocked, initially, is page 2. This is no problem, though: pages 3...7 provide more than enough memory space for any initial program.

Having entered and tested BASIC programs, the cassette routine in Elbug can be used for storing them on tape. When retrieving them, one minor problem remains to be resolved: unless a program is stored on page 3, any programs entered on the other pages will immediately be blocked by the interpreter, as described above. One further modification in the interpreter and a slightly more extensive 'start' procedure are required to cure this.

The complete program

Although the main points have already been discussed, it is perhaps a good idea to give a brief survey of the complete system.

The starting point is a complete Elektor SC/MP system, including Elbug and the associated cassette interface. The NIBL-E interpreter is located on page 1 — it can be stored in either ROM or RAM. A listing of this program is given in table 1. Page 2 must contain at least 2K of RAM, as scratch-pad memory for the interpreter; a small program can also be stored here. Extending page 2 to 4K of RAM provides space for more extensive programs. Either ROM or RAM storage area can be included on the remaining pages (3...7), as required.

To be able to communicate with the interpreter (by means of a terminal, for instance), a small interface circuit must be included. This adapts the TTL logic levels in the SC/MP system to RS232C or V24, and vice versa; it also ensures correct polarity of the various signals. The in- and outputs from the interface can be hard-wired to the terminal, or a standard connector can be mounted on the p.c. board. The interface circuit and p.c.b. are described elsewhere in this issue.

A suitable terminal is the 'Elekterminal'; this can be connected to a normal TV set via the UHF/VHF modulator.

Transmission speed

In the original version, communication with the interpreter runs at a rate of 110 baud. The same is true of the NIBL-E version given in table 1. However, if it is used in conjunction with the Elekterminal, a much higher transmission rate is possible: up to 1200 baud.

Obviously, the software will have to be adapted if the transmission rate is changed. The memory locations that are affected by the transmission rate are listed in table 2; the data for the four most common transmission rates are

also included in this table. The values given are valid both for a SC/MP system with 1 MHz crystal and for a SC/MP II system with a 2 MHz crystal.

The NIBL-E interpreter opens the possibility of connecting a paper-tape reader to Sg. The reader-relay is controlled by the 'flag 1' output of the processor, via an output buffer. When developing NIBL-E, however, it was assumed that this facility would not be required, since the Elbug cassette routines will normally be used instead. However, it is a relatively simple matter to provide a 'paper-tape' input: the data in two addresses must be changed (1F7D becomes 02 and 1F8F becomes FD), and the reader is connected to the sense B input (via a parallel-to-series converter).

Storing a program on paper-tape is a simple matter: a LIST command provides simultaneous outputs to the terminal and to the puncher via flag 0. Normally speaking, the transmission speed for a puncher should not be higher than 300 baud.

Cassette routine

BASIC programs can be stored on tape and played back with the same ease as programs in machine language. The start address for the program on page 2 is 211F (hexadecimal); all other pages simply start at the top of the page, at address P0000 (where P is the page number).

The final address can be found, once the

program has been entered, by giving the command PRINT TOP (followed, as always, by Carriage Return). The computer will respond by giving the final address plus one, as a decimal number — in other words, it gives the first address that can be used for a new program. This decimal number (minus one) must be converted to hexadecimal. With both 'begin' and 'end' address known, the Elbug cassette routine can be used to store the program on tape. The jump back to Elbug can be achieved in two ways: either operating the NRST key or giving the command LINK 0.

The LINK command is used to call up a program that is stored in machine language; in this case, the Elbug program, starting at address 0000. The LINK command can be followed by an address in either decimal or hexadecimal code. If the hexadecimal code is used, the number must be preceded by the # symbol.

Having 'dumped' the program on tape, a jump back to NIBL-E is initiated by keying in 'ru1FF0ru'. By starting at this address, part of the interpreter's initial procedure is avoided — in particular, the section that might otherwise block all programs. The interpreter now prints a prompt (>), after which the current program can be developed further or a new page can be selected for a new program, using the command NEW (P) (where P is the page number). Note that the lowest page number possible is 2. If an attempt is made to select page 1, the interpreter will simply select page 2 instead.

To load a BASIC program from cassette, the routine is as follows. First, NIBL-E is started with the command ru1000ru. When the prompt symbol appears, the page that is to be loaded is selected: NEW (P). The next step is to jump back to Elbug: LINK 0. The program can now be loaded in the usual way, using the ca...up instruction; when loading is completed ('Elbug' appearing on the display), the jump back to NIBL-E can be executed (ru1FF0ru). As soon as the prompt symbol is printed, the program can be started by giving the RUN command.

Loading NIBL-E

It is well nigh impossible to load a 4K byte program from the keyboard without introducing errors somewhere along the line. For this reason, it is the intention to include the program on an ESS record in the near future.

Using NIBL-E

Only a few NIBL commands have been mentioned in the course of this article. A more extensive summary is given in the description of the BASIC micro-computer elsewhere in this issue; furthermore, the BASIC course explains the use of virtually all possible NIBL commands.

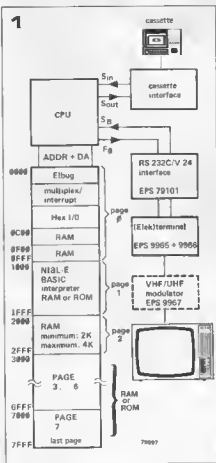


Figure 1. The complete system.

musical doorbell

(Lucas Witkam)



While on the subject of doorbells (see Random Tune Doorbell, elsewhere in this issue), an alternative gimmick is worth considering.

The circuit of this bell may at first sight appear similar, but there are basic differences between the two designs.

In the Random Tune doorbell circuit, a 'random' succession of tones with 'random' lengths is produced as long as the bell-push is held down. As soon as the button is released, the 'melody' stops.

With the circuit described here, a different effect is obtained. After even briefly pressing the bell-push, a short tune will be played. Holding the button down (or pressing it repeatedly in rapid succession) has two effects: a different melody is obtained, and it lasts longer. The circuit operates as follows.

By pressing pushbutton switch S1, the inputs of N1 and one of the inputs of N3 are taken low, with the result that pin 7 of IC2 (data input A) is taken high. IC2 is a four-bit static shift register, so that upon each successive clock pulse (provided by the clock generator,

N4), this logic '1' is transferred to successive outputs. The clock frequency is approximately 5 Hz. The number of '1's clocked through the shift register will be directly proportional to the length of time that S1 is held down.

Each time that one of the outputs of IC2 goes high, a current is supplied via the corresponding resistor to the base of the current controlled oscillator, T1. The pitch of the resultant tone is thus dependent upon the state of the various outputs of IC2. At each clock pulse, the '1's in the shift register move up one place, causing a change in pitch; if the pushbutton is depressed at that time, a new '1' will also be entered. One of the outputs (Q4B) is fed back via N2 and N3, so that the '1's in the register will keep going round the loop.

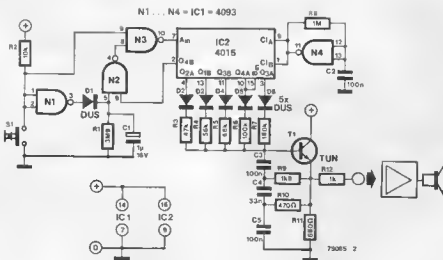
After the pushbutton is released, the circuit will keep running until C1 is discharged (through R1); if the button is pressed repeatedly, the capacitor will remain charged and so the bell will 'run' continuously. The only difference between pressing repeatedly and holding the button down is therefore that a

different succession of '1's will be entered, giving a different tune.

With this doorbell, it is necessary to add an output buffer amplifier. Alternatively, the complete CCO (T1, C3... C5 and R9... R12) can be replaced by either the complete output section of the Random Tune doorbell (from P2 on) or by the output section of the Simple Sound Effects generator (from R9 on).

The supply requirements are not critical (5...15 V, 10 mA); the supply circuit given for the Random Tune doorbell is quite suitable.

1



MARKET

8 and 10 bit converters

Two new 8-bit converters, the ZN427 successive approximation A-D converter and the ZN428 latching D-A converter, are available from Ferranti Electronics Limited. The ZN427 is microprocessor compatible and contains multiplying D-A for ratiometric applications, successive approximation logic with tri-state outputs for data bussing, a 2.5 V precision reference and a comparator. For basic operation, the device requires a minimum of external components, only two resistors and a capacitor.

The ZN428 is also microprocessor compatible and contains multiplying D-A with direct voltage output, latches, and a 2.5 V precision reference. The resolution accuracy is 8 bits ± 0.5 LSB linearity at 25°C whilst the settling time is typically 0.5 microseconds. Both devices are available in moulded or ceramic encapsulations.

A range of 10-bit converters, the ZN432 series successive approximation A-D converter and the ZN433 series tracking A-D converter, has also been announced by Ferranti. The ZN432 is a bipolar monolithic device using ± 5 V TTL/CMOS compatible power supplies and containing 10-bit current switching multiplying D-A using a matrix of diffused resistors and requiring no trimming, successive approximation logic with serial or parallel outputs, and a fast comparator with a good overload recovery. It is claimed that a conversion time of 20 microseconds is guaranteed. The input range can be varied as desired by the selection of an external resistor network.

The ZN433 series IC has many features of the ZN432 together with a window comparator and a 1 μ s conversion time for continu-

ous update making practicable a single channel approach on data acquisition systems. Both the ZN432 and the ZN433 series are presented in 28 pin D.I.L. ceramic packages.

*Ferranti Electronics Limited,
Fields New Road,
Chadderton, Oldham, OL9 8NP.*

Logical analysis test kit

A logical analysis kit (model LTC-1) to meet most design, test, production line, educational and trouble-shooting requirements, has been introduced by Continental Specialties Corporation (UK) Limited. The kit is housed in a portable case and includes a logic probe, digital pulser and logic monitor together with full manuals, application guides, accessory probe tips, adapters and leads. The logic probe offers a 0.1 M Ω input impedance and can detect pulses as narrow as 50 nanoseconds. Separate switch-selectable TTL/DTL and CMOS/HTL thresholds program the dual threshold window comparator to drive the high and low LED indicators. A built-in pulse stretcher drives the third LED and the pulse-memory switch will latch the pulse LED on at the leading edge (positive or negative going) of a single shot low repetition-rate pulse and hold it on until the switch is reset.

The digital pulser provides either single pulses or 100 Hz pulse trains with a push of its button. A pulse indicator LED confirms operation and a TTL/CMOS mode switch selects the proper levels. The logic monitor clips onto any standard 14 or 16 pin D.I.L. IC and

the state of each pin is indicated by LEDs on the top of the monitor.

Continental Specialties Corporation (UK) Limited, Shire Hill Industrial Estate, Saffron Walden, Essex, U.K.

(1158 M)

Single board computer

A powerful microcomputer (the iSBC 86/12 from Intel) has been announced by GIC Semiconductors Limited. The iSBC 86/12 uses the 5 MHz 8086 16-bit CPU, has up to 48 K bytes of memory, dedicated parallel I/O and a serial communications interface all on the same board. It plugs into the standard Intel Multibus and can be expanded by using any of the wide range of expansion cards available. These expansion boards include RAMs up to 64 K bytes, ROMs up to 64 K bytes, battery powered RAM boards, PROM programmer boards, mini and standard disc controllers, hard disc controllers, 3M cartridge controllers, cassette controllers, video graphic boards, and a range of analogue I/O boards, keyboard/CRT controller boards, relay output boards, isolated input boards, combination I/O boards, communications controllers etc. The 8086 CPU is designed to support high-level languages and has a comprehensive instruction set which includes multiply and divide in binary, BCD or ASCII. On-board memory includes 32 K bytes of dual-port read/write memory and sockets for up to 16 K bytes of read only memory. The dual-port feature allows the read/write memory to be accessed by both the 8086 CPU and any other bus master which shares the system.

The memory can be expanded up to 1 Mbyte while the programmable parallel I/O on the boards extends to 24 lines which can be configured as the application demands. Sockets are available on the board to accommodate standard line drivers and receivers.

*GIC Semiconductors Limited,
East Lane, Wembley,
Middlesex, HA9 7PP, U.K.*

(1169 M)

Hand-held DMM

A new high performance hand-held digital multimeter (DMM) has recently been announced by Data Precision Corporation and is available from Farnell International Instruments Limited. Designated the model number 935, it

was intended primarily for field use and is a full function 3 $\frac{1}{2}$ digit DMM with a basic accuracy of 0.5%. It has a total of 29 measurement ranges, 8 for current (AC or DC), 10 for voltage (AC or DC) and 11 for resistance including both high and low resistance excitation.

The push-button switches which select all ranges and functions can be operated with one hand leaving the other completely free for probe use. The high-contrast 0.5" high liquid-crystal display includes polarity sign, decimal points and a low battery voltage warning indicator.



Calibration is guaranteed for one year and the unit has full protection from overvoltage, overcurrent and high voltage transients. One thousand volts can be applied to any DC voltage range and 700 V r.m.s. to any AC range. All DC ranges can withstand greater than 5 kV pulses of 1 microsecond duration. All resistance ranges will tolerate 500 V r.m.s. or DC without damage or loss of accuracy. Current ranges are fuse protected against inadvertent inputs greater than 2 A. A standard 9 V alkaline battery (PP9 or equivalent) will power the 935 for over 200 hours continuous use. An optional AC mains adaptor is available and other accessories extend measurement capability to 1000 A, 40 kV, r.f. at 700 MHz or temperature from 60 to +150°C. The 935 is housed in an unbreakable 'Noryl' case and has been designed with the emphasis on field use. Data Precision claim that it can be dropped from bench height without damage or loss of calibration! Its small size, (3 $\frac{1}{2}$ " x 6 $\frac{1}{2}$ " x 1 $\frac{1}{2}$ ") and light weight (9 $\frac{1}{2}$ ounces including battery) makes it a 'carry anyh'ere' personal multimeter.

*Farnell International Instruments Ltd,
Sandheck Wat, Wetherby,
West Yorkshire, LS22 4DH, U.K.*

(1163 M)



MARKET

60 Volt VMOS power FETs

Two new VMOS power FETs have been introduced by Siliconix Ltd. of Swansea. The first of these devices is the VN64GA which has a continuous current rating of 12.5 Amps; applications include use in motor control, high efficiency switching power supplies, switching amplifiers and linear power amplifiers. Packaged in a TO-3 can, the VN64GA features turn-off and turn-on times of 45 ns, an on-resistance of less than 0.4 ohms and a maximum power dissipation of 80 Watts.

The second device is the high speed VN10K which features turn-on and turn-off speeds of typically 5 ns and load currents of up to ½ Amp continuous and 1 Amp pulsed. The VN10K is housed, complete with heatsink for maximum power handling (1 Watt at 25°C), in the latest TO-237 (TO-92-plus) package and can be used in applications such as high speed line drivers, TTL and CMOS to high current interlaces, transducer and relay switching and LED digit strobe drivers.

VMOS devices require no secondary breakdown or thermal runaway protection while giving improved reliability. Other advantages include an input drive current of less than 100 nA and high gain and fan-out from standard CMOS logic.

Siliconix Ltd., Morrison,
Swansea, SA6 6NE, U.K.

(1161 M)

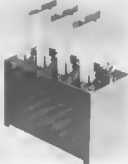
'Soft touch' push button switches

A versatile, multi-pushbutton switch matrix, featuring a very low operating force and the option of having illuminated keys, has been introduced to the U.K. by Impeptron Limited. Produced by Petreck Switches in West Germany, the Series 324 is designed primarily for radio, TV and HiFi applications such as channel or function selection, wavechange, etc.

The switch is available in three standard sizes, having pushbutton matrices of 4 x 2, 6 x 2, or 8 x 2. Each size may be ganged with others to provide multi-pushbutton arrays having 8, 12, 16, 24 or 32 keys. Each pushbutton has a very light action, and requires only the lightest touch to operate fully. This 'soft touch' feature will be of particular interest to designers of light or portable equipment, where operation of a stiff pushbutton selector switch can cause rocking or tipping.

The normal action is of maintained contact, and a latching release

mechanism ensures that previously operated keys are released at the instant that further keys are pressed. In addition, each matrix can be fitted with a 'muting' switch, which isolates audio circuits while the selector is being operated. This prevents the annoying loudspeaker noise which is often heard during wavechange switching on TV sets and Hi-Fi equipment.



By inverting miniature lamps into the base of each group of push-buttons, the keys may be illuminated. This is done by 'collecting' light using small plastic prisms, and passing it along the acrylic arms which form the pushbutton supports. In this way, individual keys may be illuminated without the need for separate lamps for each key. Eight and twelve pushbutton arrays require 2 lamps, while a sixteen pushbutton array requires 3 lamps.

Maximum power handling is 15 W, with a maximum switching voltage of 30 V DC.

All three basic types in the 324 Series are designed for PCB mounting, and have a regular matrix of contact pins protruding from the back plane.

Impeptron Ltd.,
Impeptron House,
23-31 King Street,
London W3 9LH.

(1160 M)

Display consoles

A range of easy access display consoles with the option of either a satin black aluminium display panel or red, green or neutral grey, translucent filter windows for illuminated displays, are now available from Boss Industrial Mouldings Limited. The contoured sides of this BIM7500 series of

Bimconsoles are of 12.7 mm (0.5") thick, solid oiled walnut, contrasting with the textured sand finished exterior panels. They are available in 9 sizes offering the combination of 4 keyboard panel widths and overall dimensions ranging from 250 x 260 x 112 mm (10" x 10.3" x 4.4") high to 500 x 431 x 200 mm (20" x 17" x 7.9") high with the larger sizes having a fully hinged upper section. The exterior panels of all models are quickly detachable on the removal of 2 or 3 concealed screws.

Also available are small desk console to accommodate full and half-size I/O cards. The BIM8005 and BIM8007 Bimconsoles have removable ABS bottom panels which incorporate stand-off bosses for ease of board mounting. Both sizes are of a three piece construction with the 1 mm thick grey aluminium top panel sitting flush with the upper face of the



main ABS body which also incorporates vertical guide slots for holding 1.5 mm (0.06") thick printed circuit boards. Screws running into integral brass bushes within the main body are used for attaching both the top and bottom panels the latter also being supplied in grey and thereby toning with the blue, black, grey or orange main body colours. Both of these units can be cleanly drilled and punched, have excellent insulation properties and will withstand temperatures up to 85°C (185°F).

Boss Industrial Mouldings Ltd.,
Higgs Industrial Estate,
2 Herne Hill Road,
London, SE24 0AU, England.

(1165 M)

Temperature controlled soldering irons

A range of low voltage soldering irons which are thermally self-limiting at approximately 325°C, 370°C or 410°C and which can be used with many existing solder stations are available from Tele-Production Tools Limited. Known as the Telpio TL range, these nominal 16-20 Watt irons are available for 12, 24 or 48 Volt



operation and are supplied with a detachable high-purity iron-clad soldering bit which can be inter-changed with any of twelve other bits of various shapes and sizes. The iron coating on these bits minimises the migration of copper molecules from soldering tips thereby increasing bit life and eliminating the time required to redress copper bits. The soldering irons in the TL range feature a fast heat recovery cycle, are light, well-balanced and are manufactured in compliance with CEE11 and BS3456 regulations.

Tele-Production Tools Ltd.,
Simon House,
Electric Avenue, Westcliff-on-Sea,
Essex, SS0 9NW.

(1162 M)

Fibre-optic lighting system

A compact and portable fibre-optic lighting system for industrial and medical applications which provides complete electrical isolation, variable intensity of cold white light and elimination of overhead glare and shadows has been developed by Valtec Corporation. Known as the series 300, the unit comes complete with a lensing system and 150 Watt light source and is suitable for applications such as microscopic assembly work or examination.



The inspection light is available in a variety of lengths, diameters and fibre-optic bundle combinations to suit requirements. The fibre-optic bundle is inserted into a combination flexible and stayput surgical grade interlocking steel (or silicone if desired) goose-neck, with the lensing system and light source at each end.

Valtec Corporation,
West Boylston, MA 01583, U.K.

(1164 M)

MARKET

Universal voltage tester

A universal voltage tester has been designed by Verospeed which will detect voltages between 4.5 V and 380 V without switching.



Indication of DC voltage polarity is given by the illumination of a light emitting diode against positive or negative symbols whilst AC voltages are indicated by the alternate flashing of the LEDs. The probe is well suited for many applications in the telecommunications, automotive, R and D and servicing industries. The tester is fully VDE approved and requires up to 1.5 milliamps to operate with response time of 3 milliseconds.

Verospeed,
Barton Park Industrial Estate,
Eastleigh,
Hampshire, SO5 5RR, England.

(1124 M)

couples a proven display with a microprocessor-based controller to provide an easy-to-read display with very low power requirements and easy interfacing has recently been introduced by Hewlett-Packard. Incorporated into the microprocessor controller are pre-programmed routines to accept, decode and display standard ASCII data. In addition, the 5.0 volt operation, standard low power schottky TTL compatible inputs and four separate display formatting modes, allow easy interface to keyboard or microprocessor based systems.

The low voltage, compact size, and solid state features are ideal for applications in word processing equipment, desktop calculators, and automatic banking terminals. The HDSP-24XX series provides optional upper and lower case character fonts, or user-programmed custom character sets. Single line 16, 24, 32 or 40 character display lengths are available.

Hewlett-Packard Ltd.,
King Street Lane,
Winkers, Wokingham,
Berkshire, RG11 5AR, England.

(1125 M)

Microwave transistors

Two new microwave transistors, offering high linear power, gain and power-added efficiency, are announced by Hewlett-Packard. Both NPN bipolar transistors, the HXTR-5103 and the HXTR-5104, offer low thermal resistance through the use of a BeO heat conductor in a metal/ceramic package. They also feature Ta2N ballasted resistors for additional ruggedness, and both have

dielectric scratch protection over their active areas.

HXTR-5103 has a guaranteed 1 dB compressed gain of 11 dB at 2 GHz, with associated P₁ dB linear output power of 23 dBm typical at 2 GHz. With excellent uniformity and reliability, this linear power microwave transistor has typical power-added efficiency of 34 percent. HXTR-5104 provides typical linear output power of 29 dBm at 2 GHz and is useful in amplifier applications ranging up to 4 GHz,

ment of a new cost-cutting range of high quality instruments. BPL herald the meters as the most competitively priced range offering high accuracy and performance coupled with an extensive series of options. The products will meet the requirements of virtually all users of DPMs.

This new range of digital products is intended to supplement BPL's wide range of moving coil meters. Designed for use in all types of professional instrumentation and measuring equipment, meters can also be supplied to customers' special requirements. Production quantity prices for standard LED models are under £20 and for LCD models, under £30, with immediate delivery availability. Both LED (3½ and 4½ digit) and LCD models are built into low profile housings less than one inch (25 mm) high and are also available in stackable castings. The LED instruments are TTL supply compatible and high-contrast LCD versions are built around the latest CMOS/LSI technology with low power consumption suitable for battery/portable operation.

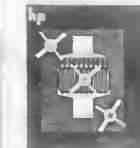
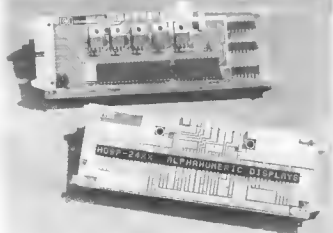
Standard facilities include display blanking/dimming, auto zero, sample and hold, overload indication, programmable decimals, display testing and a differential input facility. The meters can be scaled to read in engineering units and autoranging models for both AC and DC are available. Other features offered are non-standard ranges, suppressed zero and BCD outputs. Full stocks of standard Rcal-BPL DPMs together with technical back-up are available both from BPL's factory and head office in Radlett and their German office in Neu-Isenburg. BPL's leading European agents will also be able to supply from stock.

British Physical Laboratories,
Watling Street, Radlett,
Hertfordshire, WD7 7HJ,
England.

(1180 M)

Alphanumeric display modules

A stand-alone dot matrix alphanumeric display system that



Associated P₁ dB gain is 9 dB typical at 2 GHz, and power-added efficiency of 35 percent.

Hewlett-Packard Ltd.,
King Street Lane,
Winkers, Wokingham,
Berkshire RG11 5AR, England.

(1126 M)

Digital panel meter

British Physical Laboratories has entered the digital panel meter field with the recent announce-

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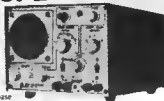
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Input Impedance — 1 Meg 40 pF in shunt
Input Voltage Max — 600V P-P
Horizontal Axis (X)
Deflection Sensitivity — 0—400mV/division (Bandwidth between 3dB points) — 1Hz — 250KHz
Gain control — Continuous when time-base in EXT position
Input Impedance — 1 Meg
Input Voltage Max — 600V P-P

TIME BASE

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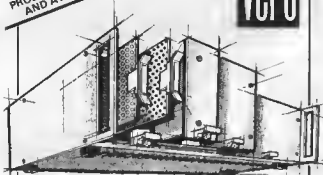
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elektor '79

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