

elektor

up-to-date electronics for lab and leisure

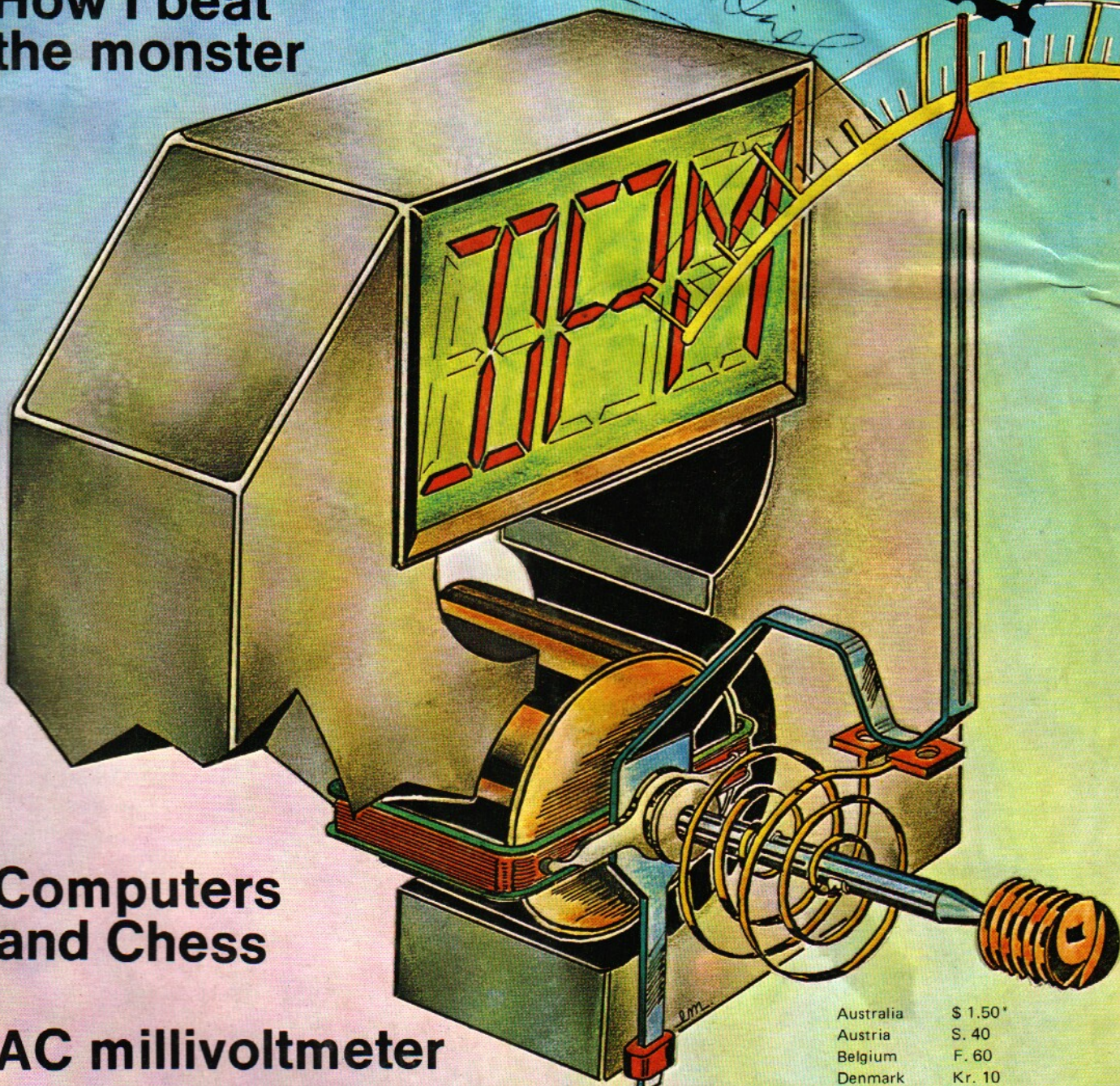
45
January 1979

U.K. 55p.
U.S.A. | Can. \$1.75

Marshalls 1979 product
range catalogue
- 48 pages -
bigger than ever
- worth 40p -
Free inside this issue.

Universal digital meter

How I beat the monster



Computers and Chess

AC millivoltmeter

Australia	\$ 1.50*
Austria	S. 40
Belgium	F. 60
Denmark	Kr. 10
France	F. 8
Germany	DM. 4.20
Netherlands	DFL. 3.50
New Zealand	\$ 1.50
Norway	Kr. 10
Sweden	Kr. 14
Switzerland	F. 4.40

*recommended

elektor 45 decoder

Volume 5

Number 1

Elektor Publishers Ltd., Elektor House,
10 Longport, Canterbury CT1 1PE, Kent, U.K.
Tel.: Canterbury (0227) 54430. Telex: 965504.
Office hours: 8.30 - 12.45 and 13.30 - 16.45.

- Bank: 1. Midland Bank Ltd., Canterbury, A/C no. 11014587
Sorting code 40-16-11, Giro no. 3154524.
2. U.S.A. only: Bank of America, c/o World Way
Postal Center, P.O. Box 80689, Los Angeles,
CA 90080, A/C no. 12350-04207.
3. Canada only: The Royal Bank of Canada,
c/o Lockbox 1969, Postal Station A, Toronto,
Ontario, M5W 1W9, A/C no. 160-269-7.

Please make all cheques payable to Elektor Publishers Ltd. at the above address.

Elektor is published monthly.
Number 51/52 (July/August) is a double issue.

SUBSCRIPTIONS: Mrs. S. Barber

Subscription 1979, January to December incl.:

U.K.	U.S.A./Can.		other countries	
	surface mail	airmail	surface mail	airmail
£ 8.50	\$ 21.00	\$ 31.00	£ 8.50	£ 14.00

Subscriptions normally run to December incl. Subscriptions from

February issue:

U.K.	U.S.A./Can.		other countries	
	surface mail	airmail	surface mail	airmail
£ 7.75	\$ 19.00	\$ 28.00	£ 7.75	£ 13.00

Back issues are available at original cover price.

Change of address: Please allow at least six weeks for change of address. Include your old address, enclosing, if possible, an address label from a recent issue.

ASSISTANT MANAGER: R.G. Knapp

ADVERTISING MANAGER: N.M. Willis

National advertising rates for the English-language edition of Elektor and international rates for advertising in the Dutch, French and German issues are available on request.

EDITOR

W. van der Horst

U.K. EDITORIAL STAFF

I. Meiklejohn

TECHNICAL EDITORIAL STAFF

J. Barendrecht
G.H.K. Dam
P. Holmes
E. Krempelsauer
G. Nachbar

A. Nachtmann
J. Oudelaar
A.C. Pauptit
K.S.M. Walraven
P. de Winter

Technical telephone query service, Mondays only, 13.30 - 16.45.

For written queries, letters should be addressed to dept. TQ.

Please enclose a stamped, addressed envelope or a self-addressed envelope plus an IRC.

ART EDITOR: F. v. Rooij

Letters should be addressed to the department concerned:

TQ = Technical Queries	ADM = Advertisements
ED = Editorial (articles submitted for publications etc.)	EPS = Elektor printed circuit board service
SUB = Subscriptions	

The circuits published are for domestic use only. The submission of designs or articles to Elektor implies permission to the publishers to alter and translate the text and design, and to use the contents in other Elektor publications and activities. The publishers cannot guarantee to return any material submitted to them. All drawings, photographs, printed circuit boards and articles published in Elektor are copyright and may not be reproduced or imitated in whole or part without prior written permission of the publishers.

Patent protection may exist in respect of circuits, devices, components etc. described in this magazine.

The publishers do not accept responsibility for failing to identify such patent or other protection.

Dutch edition: Elektor B.V., Postbus 75, 6190 AB Beek (L), the Netherlands.

German edition: Elektor Verlag GmbH, 5133 Gangelt, W-Germany

French edition: Elektor Sarl, Le Douliou, 59940 Estaires, France.

Distribution in U.K.:

Seymour Press Ltd., 334 Brixton Road, London SW9 7AG.

Distribution in CANADA: Fordon and Gotch (Can.) Ltd., 55 York Street, Toronto, Ontario M5J 1S4.

Copyright © 1978 Elektor publishers Ltd. — Canterbury.

Printed in the UK.

What is a TUN?
What is 10 n?
What is the EPS service?
What is the TQ service?
What is a missing link?

Semiconductor types

Very often, a large number of equivalent semiconductors exist with different type numbers. For this reason, 'abbreviated' type numbers are used in Elektor wherever possible:

- '741' stand for μ A741, LM741, MC641, MIC741, RM741, SN72741, etc.
- 'TUP' or 'TUN' (Transistor, Universal, PNP or NPN respectively) stand for any low frequency silicon transistor that meets the following specifications:

UCEO, max	20V
IC, max	100 mA
hfe, min	100
Ptot, max	100 mW
fT, min	100 MHz

Some 'TUN's are: BC107, BC108 and BC109 families; 2N3856A, 2N3859, 2N3860, 2N3904, 2N3947, 2N4124. Some 'TUP's are: BC177 and BC178 families; BC179 family with the possible exception of BC159 and BC179; 2N2412, 2N3251, 2N3906, 2N4126, 2N4291.

- 'DUS' or 'DUG' (Diode Universal, Silicon or Germanium respectively) stands for any diode that meets the following specifications:

	DUS	DUG
UR, max	25V	20V
IF, max	100mA	35mA
IR, max	1 μ A	100 μ A
Ptot, max	250mW	250mW
CD, max	5pF	10pF

Some 'DUS's are: BA127, BA217, BA218, BA221, BA222, BA317, BA318, BAX13, BAY61, 1N914, 1N4148.

Some 'DUG's are: OA85, OA91, OA95, AA116.

- 'BC107B', 'BC237B', 'BC547B' all refer to the same 'family' of almost identical better-quality silicon transistors. In general, any other member of the same family can be used instead.

BC107 (-8, -9) families:

BC107 (-8, -9), BC147 (-8, -9), BC207 (-8, -9), BC237 (-8, -9), BC317 (-8, -9), BC347 (-8, -9), BC547 (-8, -9), BC171 (-2, -3), BC182 (-3, -4), BC382 (-3, -4), BC437 (-8, -9), BC414

BC177 (-8, -9) families:

BC177 (-8, -9), BC157 (-8, -9), BC204 (-5, -6), BC307 (-8, -9), BC320 (-1, -2), BC350 (-1, -2), BC557 (-8, -9), BC251 (-2, -3), BC212 (-3, -4), BC512 (-3, -4), BC261 (-2, -3), BC416.

Resistor and capacitor values

When giving component values, decimal points and large numbers

of zeros are avoided wherever possible. The decimal point is usually replaced by one of the following abbreviations:

p (pico-)	= 10 ⁻¹²
n (nano-)	= 10 ⁻⁹
μ (micro-)	= 10 ⁻⁶
m (milli-)	= 10 ⁻³
k (kilo-)	= 10 ³
M (mega-)	= 10 ⁶
G (giga-)	= 10 ⁹

A few examples:

Resistance value 2k7: 2700 Ω .
Resistance value 470: 470 Ω .
Capacitance value 4p7: 4.7 pF, or 0.000 000 000 004 7 F...
Capacitance value 10n: this is the international way of writing 10,000 pF or .01 μ F, since 1 n is 10⁻⁹ farads or 1000 pF.
Resistors are $\frac{1}{4}$ Watt 5% carbon types, unless otherwise specified.
The DC working voltage of capacitors (other than electrolytics) is normally assumed to be at least 60 V. As a rule of thumb, a safe value is usually approximately twice the DC supply voltage.

Test voltages

The DC test voltages shown are measured with a 20 k Ω /V instrument, unless otherwise specified.

U, not V

The international letter symbol 'U' for voltage is often used instead of the ambiguous 'V'. 'V' is normally reserved for 'volts'. For instance: $U_b = 10$ V, not $V_b = 10$ V.

Mains voltages

No mains (power line) voltages are listed in Elektor circuits. It is assumed that our readers know what voltage is standard in their part of the world!
Readers in countries that use 60 Hz should note that Elektor circuits are designed for 50 Hz operation. This will not normally be a problem; however, in cases where the mains frequency is used for synchronisation some modification may be required.

Technical services to readers

• **EPS service.** Many Elektor articles include a lay-out for a printed circuit board. Some — but not all — of these boards are available ready-etched and predrilled. The 'EPS print service list' in the current issue always gives a complete list of available boards.

• **Technical queries.** Members of the technical staff are available to answer technical queries (relating to articles published in Elektor) by telephone on Mondays from 14.00 to 16.30. Letters with technical queries should be addressed to: Dept. TQ. Please enclose a stamped, self addressed envelope; readers outside U.K. please enclose an IRC instead of stamps.

• **Missing link.** Any important modifications to, additions to, improvements on or corrections in Elektor circuits are generally listed under the heading 'Missing Link' at the earliest opportunity.



The American Institute of High Fidelity (IHf) recently published a new standard, dealing with 'Methods of Measurement for Audio Amplifiers'. When it comes to buying audio equipment, it would be a great help if manufacturers started 'Measuring by the book'.

p. 1-02



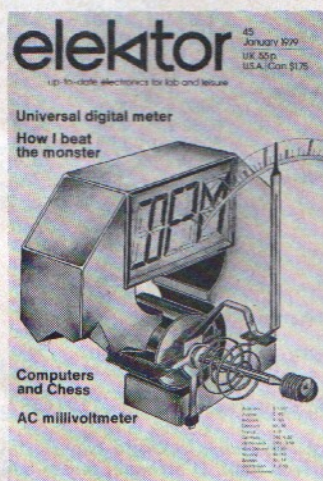
A reliable nicad charger should prove a useful item to owners of portable radios, flash guns and the like: the prices of nicad cells have dropped to the point where it has become a viable proposition to use them in almost any type of battery-powered equipment.

p. 1-08



How will a chess-playing computer fare against a strong human player? Mr. Levy describes how the reigning world champion computer lost... 'How I beat the monster' should prove of interest! A companion article takes a look at the background of Computers and chess.

p. 1-34



Digital displays are replacing conventional pointer instruments in many applications. Rapidly falling prices now seem to be hastening the final demise of the pointer instrument: a digital panel meter is now actually cheaper than its analog counterpart.

contents

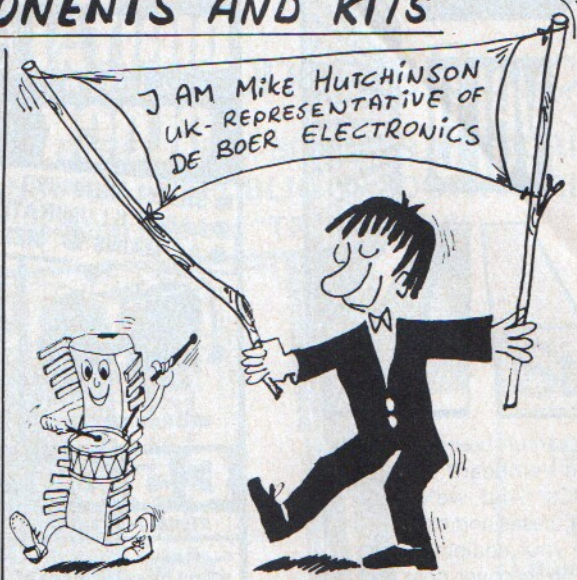
selektor	1-01
measuring by the book	1-02
IHF toneburst generator	1-06
For certain audio measurements, the new IHf standard specifies a particular toneburst signal.	
reliable nicad charger	1-08
improved LED VU/PPM (J.M. Heuss)	1-12
In April 1977 (Elektor 24) a design was published for an audio output level meter. With the aid of an add-on circuit it is possible to improve the resolution of the meter at the lower end of its scale.	
oscillographics on board	1-13
The oscillographics circuit published in September 1978 has proved to be a highly popular design, and several readers have asked for a printed circuit board.	
AC millivoltmeter and signal squirt	1-16
The lowest AC range on most multimeters is usually several volts (f.s.d.) and it presents a relatively low load impedance to the circuit under test. A 'pre-amplifier for multimeters' can solve this problem.	
DC polarity protection	1-19
sixteen logic levels on a scope (R. Rastetter) ...	1-20
When trouble shooting digital circuits it is often useful to be able to examine the logic level of a number of signals simultaneously.	
class tells	1-22
This article takes a look at a recent commercial power amplifier design which combines the inherently low distortion of Class-A output stages with the high efficiency of a Class-B configuration.	
ejektor	1-25
Electronically variable resistance.	
FM-stereo generator	1-26
Using relatively straightforward means it is possible to construct a simple yet extremely useful FM stereo generator, which can be employed to check the operation of stereo decoders and FM receivers.	
passive oscilloscope probe	1-30
The 10:1 probe described here can be constructed from standard parts.	
aplikator	1-32
Programmable sound generator.	
computers and chess	1-34
How the monster thinks.	
chess challenger 10 plays like a human	1-39
how I beat the monster (David Levy)	1-40
universal digital meter	1-43
Digital replacement for pointer instruments.	
automatic emergency lighting unit	1-48
market	UK-15
advertiser's index	UK-26

DE BOER ELECTRONICS

LOTS OF COMPONENTS AND KITS

ELEKTOR KITS

LM300	£ 1.30	LM377	£ 2.21	TA9910	£ 1.73
LM301	£ 2.88	LM380	£ 1.19	TA91001	£ 3.65
LM301P	£ 1.25	LM381	£ 1.79	TA91004	£ 4.22
LM302	£ 1.74	LM382	£ 1.79	TA91005	£ 4.83
LM302P	£ 1.41	LM383	£ 1.59	TA91008	£ 2.37
LM303	£ 1.27	LM387	£ 0.95	TA91012	£ 3.74
LM303P	£ 1.21	LM391	£ 1.31	MC1303P	£ 2.99
LM304	£ 1.41	LM393A	£ 2.21	MC1310P	£ 2.05
LM304P	£ 1.25	LM394	£ 1.92	MC1312P	£ 2.31
LM305	£ 1.44	LM395	£ 1.72	MC1314P	£ 2.31
LM305P	£ 1.21	LM396	£ 1.96	MC1315P	£ 2.28
LM307	£ 2.75	LM397	£ 3.30	MC1330P	£ 1.19
LM308	£ 2.75	LM398	£ 2.12	LM1458	£ 0.43
LM309	£ 1.75	LM399	£ 0.44	LM1458B	£ 1.03
LM310	£ 0.84	LM350	£ 2.41	LM1458T	£ 1.10
LM310A	£ 0.87	NE551	£ 0.29	ML1468G	£ 4.09
LM310B	£ 1.00	NE556	£ 1.10	TM20202	£ 1.85
LM312	£ 1.08	NE560	£ 2.30	TM20202	£ 3.67
LM312P	£ 1.02	NE560C	£ 2.38	GAJ28	£ 1.20
LM313	£ 1.02	LM597C	£ 2.80	GA308	£ 1.05
LM316	£ 2.13	LM597D	£ 2.80	GA309	£ 1.05
LM317	£ 2.07	LM597E	£ 2.80	GA309A	£ 1.05
LM318	£ 1.91	LM597F	£ 2.80	GA309B	£ 1.05
LM319	£ 1.91	LM597G	£ 2.80	GA309C	£ 1.05
LM319P	£ 1.74	LM597H	£ 2.80	GA309D	£ 1.05
LM320	£ 2.09	LM597I	£ 2.80	GA309E	£ 1.05
LM320P	£ 1.99	LM597J	£ 2.80	GA309F	£ 1.05
LM321	£ 2.20	LM597K	£ 2.80	GA309G	£ 1.05
LM321P	£ 1.82	LM597L	£ 2.80	GA309H	£ 1.05
LM322	£ 1.99	LM597M	£ 2.80	GA309I	£ 1.05
LM323	£ 2.20	LM597N	£ 2.80	GA309J	£ 1.05
LM323P	£ 1.82	LM597O	£ 2.80	GA309K	£ 1.05
LM324	£ 1.99	LM597P	£ 2.80	GA309L	£ 1.05
LM325	£ 2.20	LM597Q	£ 2.80	GA309M	£ 1.05
LM325P	£ 1.82	LM597R	£ 2.80	GA309N	£ 1.05
LM326	£ 1.99	LM597S	£ 2.80	GA309P	£ 1.05
LM327	£ 2.20	LM597T	£ 2.80	GA309Q	£ 1.05
LM327P	£ 1.82	LM597U	£ 2.80	GA309R	£ 1.05
LM328	£ 1.99	LM597V	£ 2.80	GA309S	£ 1.05
LM329	£ 2.20	LM597W	£ 2.80	GA309T	£ 1.05
LM329P	£ 1.82	LM597X	£ 2.80	GA309U	£ 1.05
LM330	£ 1.99	LM597Y	£ 2.80	GA309V	£ 1.05
LM330P	£ 1.82	LM597Z	£ 2.80	GA309W	£ 1.05
LM331	£ 1.99	LM598	£ 2.80	GA309X	£ 1.05
LM331P	£ 1.82	LM598A	£ 2.80	GA309Y	£ 1.05
LM332	£ 1.99	LM598B	£ 2.80	GA309Z	£ 1.05
LM332P	£ 1.82	LM598C	£ 2.80	GA309AA	£ 1.05
LM333	£ 1.99	LM598D	£ 2.80	GA309AB	£ 1.05
LM333P	£ 1.82	LM598E	£ 2.80	GA309AC	£ 1.05
LM334	£ 1.99	LM598F	£ 2.80	GA309AD	£ 1.05
LM334P	£ 1.82	LM598G	£ 2.80	GA309AE	£ 1.05
LM335	£ 1.99	LM598H	£ 2.80	GA309AF	£ 1.05
LM335P	£ 1.82	LM598I	£ 2.80	GA309AG	£ 1.05
LM336	£ 1.99	LM598J	£ 2.80	GA309AH	£ 1.05
LM336P	£ 1.82	LM598K	£ 2.80	GA309AI	£ 1.05
LM337	£ 1.99	LM598L	£ 2.80	GA309AJ	£ 1.05
LM337P	£ 1.82	LM598M	£ 2.80	GA309AK	£ 1.05
LM338	£ 1.99	LM598N	£ 2.80	GA309AL	£ 1.05
LM338P	£ 1.82	LM598O	£ 2.80	GA309AM	£ 1.05
LM339	£ 1.99	LM598P	£ 2.80	GA309AN	£ 1.05
LM339P	£ 1.82	LM598Q	£ 2.80	GA309AO	£ 1.05
LM340	£ 1.99	LM598R	£ 2.80	GA309AP	£ 1.05
LM340P	£ 1.82	LM598S	£ 2.80	GA309AQ	£ 1.05
LM341	£ 1.99	LM598T	£ 2.80	GA309AR	£ 1.05
LM341P	£ 1.82	LM598U	£ 2.80	GA309AS	£ 1.05
LM342	£ 1.99	LM598V	£ 2.80	GA309AT	£ 1.05
LM342P	£ 1.82	LM598W	£ 2.80	GA309AU	£ 1.05
LM343	£ 1.99	LM598X	£ 2.80	GA309AV	£ 1.05
LM343P	£ 1.82	LM598Y	£ 2.80	GA309AW	£ 1.05
LM344	£ 1.99	LM598Z	£ 2.80	GA309AX	£ 1.05
LM344P	£ 1.82	LM599	£ 2.80	GA309AY	£ 1.05
LM345	£ 1.99	LM599A	£ 2.80	GA309AZ	£ 1.05
LM345P	£ 1.82	LM599B	£ 2.80	GA309BA	£ 1.05
LM346	£ 1.99	LM599C	£ 2.80	GA309BB	£ 1.05
LM346P	£ 1.82	LM599D	£ 2.80	GA309BC	£ 1.05
LM347	£ 1.99	LM599E	£ 2.80	GA309BD	£ 1.05
LM347P	£ 1.82	LM599F	£ 2.80	GA309BE	£ 1.05
LM348	£ 1.99	LM599G	£ 2.80	GA309BF	£ 1.05
LM348P	£ 1.82	LM599H	£ 2.80	GA309BG	£ 1.05
LM349	£ 1.99	LM599I	£ 2.80	GA309BH	£ 1.05
LM349P	£ 1.82	LM599J	£ 2.80	GA309BI	£ 1.05
LM350	£ 1.99	LM599K	£ 2.80	GA309BJ	£ 1.05
LM350P	£ 1.82	LM599L	£ 2.80	GA309BK	£ 1.05
LM351	£ 1.99	LM599M	£ 2.80	GA309BL	£ 1.05
LM351P	£ 1.82	LM599N	£ 2.80	GA309BM	£ 1.05
LM352	£ 1.99	LM599O	£ 2.80	GA309BN	£ 1.05
LM352P	£ 1.82	LM599P	£ 2.80	GA309BO	£ 1.05
LM353	£ 1.99	LM599Q	£ 2.80	GA309BP	£ 1.05
LM353P	£ 1.82	LM599R	£ 2.80	GA309BQ	£ 1.05
LM354	£ 1.99	LM599S	£ 2.80	GA309BR	£ 1.05
LM354P	£ 1.82	LM599T	£ 2.80	GA309BS	£ 1.05
LM355	£ 1.99	LM599U	£ 2.80	GA309BT	£ 1.05
LM355P	£ 1.82	LM599V	£ 2.80	GA309BU	£ 1.05
LM356	£ 1.99	LM599W	£ 2.80	GA309BV	£ 1.05
LM356P	£ 1.82	LM599X	£ 2.80	GA309BW	£ 1.05
LM357	£ 1.99	LM599Y	£ 2.80	GA309BX	£ 1.05
LM357P	£ 1.82	LM599Z	£ 2.80	GA309BY	£ 1.05
LM358	£ 1.99	LM600	£ 2.80	GA309BZ	£ 1.05
LM358P	£ 1.82	LM600A	£ 2.80	GA309CA	£ 1.05
LM359	£ 1.99	LM600B	£ 2.80	GA309CB	£ 1.05
LM359P	£ 1.82	LM600C	£ 2.80	GA309CC	£ 1.05
LM360	£ 1.99	LM600D	£ 2.80	GA309CD	£ 1.05
LM360P	£ 1.82	LM600E	£ 2.80	GA309CE	£ 1.05
LM361	£ 1.99	LM600F	£ 2.80	GA309CF	£ 1.05
LM361P	£ 1.82	LM600G	£ 2.80	GA309CG	£ 1.05
LM362	£ 1.99	LM600H	£ 2.80	GA309CH	£ 1.05
LM362P	£ 1.82	LM600I	£ 2.80	GA309CI	£ 1.05
LM363	£ 1.99	LM600J	£ 2.80	GA309CJ	£ 1.05
LM363P	£ 1.82	LM600K	£ 2.80	GA309CK	£ 1.05
LM364	£ 1.99	LM600L	£ 2.80	GA309CL	£ 1.05
LM364P	£ 1.82	LM600M	£ 2.80	GA309CM	£ 1.05
LM365	£ 1.99	LM600N	£ 2.80	GA309CN	£ 1.05
LM365P	£ 1.82	LM600O	£ 2.80	GA309CO	£ 1.05
LM366	£ 1.99	LM600P	£ 2.80	GA309CP	£ 1.05
LM366P	£ 1.82	LM600Q	£ 2.80	GA309CQ	£ 1.05
LM367	£ 1.99	LM600R	£ 2.80	GA309CR	£ 1.05
LM367P	£ 1.82	LM600S	£ 2.80	GA309CS	£ 1.05
LM368	£ 1.99	LM600T	£ 2.80	GA309CT	£ 1.05
LM368P	£ 1.82	LM600U	£ 2.80	GA309CU	£ 1.05
LM369	£ 1.99	LM600V	£ 2.80	GA309CV	£ 1.05
LM369P	£ 1.82	LM600W	£ 2.80	GA309CW	£ 1.05
LM370	£ 1.99	LM600X	£ 2.80	GA309CX	£ 1.05
LM370P	£ 1.82	LM600Y	£ 2.80	GA309CY	£ 1.05
LM371	£ 1.99	LM600Z	£ 2.80	GA309CZ	£ 1.05
LM371P	£ 1.82	LM601	£ 2.80	GA309DA	£ 1.05
LM372	£ 1.99	LM601A	£ 2.80	GA309DB	£ 1.05
LM372P	£ 1.82	LM601B	£ 2.80	GA309DC	£ 1.05



YOU CAN REACH ME BY PHONE FROM MONDAY TILL FRIDAY 13:00 PM TO 18:00 PM SATURDAY 10:00 AM TO 13:00 PM AT HILLINGTON (04856)553-OR BY LETTER TO: MIKE HUTCHINSON, 2 LYNN ROAD, GRIMSTON, KINGS LYNN, NORFOLK PE321AD. CHEQUE AND POSTAL ORDER ONLY TO THE NAME OF DE BOER ELECTRONICS. ALL PRICES ARE VAT-INCLUDED ADD 50P FOR POST AND PACKAGE

- ¼ Gigahertz counter CPL (9887) £ 104.50
- A. Time base control (9887-1) £ 48.90
- B. Low frequency input amp (9887-3) £ 6.65
- C. Counter and display (9887-2) £ 65.90
- D. High frequency input amp (9887-4) £ 15.30
- Automatic mono/stereo switch (9923) £ 6.30
- T.V. sound modulator (9925) £ 6.30
- Mini counter (9927) £ 27.70
- Mini short wave receiver (9920) £ 9.05
- Digital reverberation main board (9913-1) £ 67.25
- Digitale reverberation extension board (9913-2) £ 69.55
- Percolator switch (9902) £ 8.40
- Colour modulator (9873) £ 14.90
- Moving coil preamp (9911) £ 19.50
- Elektormat (with heatinks) (9874) £ 20.—
- Colour T.V. games board (9892) £ 24.45

- Infra red light gate transmitter (9862-1) £ 3.30
- Infra red light gate receiver (9862-2) £ 9.85
- Development timer (9840) £ 18.50
- Elekter equaliser (9832) £ 23.—
- UAA 180 LED meter (9817 1+2) £ 12.10
- Simple function generator (9453) £ 27.75
- Signal injector (9765) £ 6.—
- Sensitive lightmeter (9886) £ 12.55
- M.W. reflex receiver (9880) £ 7.55
- Heating controller (9877) £ 28.50
- Analogue freq. meter (9869) £ 10.15
- Elekter m.v. preamp (9866) £ 5.10
- UHF T.V. modulator (9864) £ 3.70
- Magnetiser (9827) £ 4.50
- Sensor for electrometer (9826-2) £ 5.80
- Electrometer (9826-1) £ 5.80
- Video bio feedback generator (9825-1) £ 12.35
- Video bio alpha amplifier (9825-2) £ 12.35
- Ioniser (9823) £ 11.40
- Infra red transmitter (9822) £ 23.05
- Log darkroom timer (9797) £ 16.05
- F.M. mains intercom (9359) £ 37.80
- 3½ Digit DVM (77109) £ 23.50
- 4 Watt car radio amp (77101) £ 5.25
- T.V. games with AT-3-8500 (77084) £ 13.75
- Guitar preamp (77020) £ 6.05
- Precision time base (9448) £ 15.85
- Power supply for prec. time base (9448-1) £ 5.60

- SOME OTHER KITS:**
- PRECONSONANT £6.25
 - LUMINANT £20.50
 - CONSONANT £42.50
 - TOUCH DIMMER £7.45
 - POWER FLASHER £3.85
 - ELECTRONIC GONG £3.65
 - BICYCLE SPEEDMETER £3.40
 - GLOWPLUG REGULATOR £7.50
- ASK MIKE FOR THE NEW ELEKTOR KITS!

- MICROPROCESSOR SC/MP. KIT**
- RAM I/O (9846-1) £ 32.35
 - SC/MP board (9846-2) £ 26.75
 - CPU card (9851)* £ 90.50
 - BUS board (9857) £ 3.—
 - Memory card (9863)* £ 57.50
 - HEX I/O (9893)* £ 67.25
 - 4-k RAM (9885)* £ 122.05
 - Power supply (9906)* £ 23.05
 - Cass. interface (9905)* £ 16.05
 - 3 Elbug programmed EPROMs* £ 68.85
 - Cpl. system (consists of kits with *) £ 349.—

- NEW KITS**
- ELEKTERMINAL £ 69.00
 - VIDEOSCOPE (9969-2) £ 5.85
 - " (9969-3) £ 5.40
 - " (9969-1) £ 37.00

PAYMENT: CHEQUE AND POSTAL ORDER ONLY TO THE NAME OF DE BOER ELECTRONICS. ALL OUR PRICES ARE VAT-INCLUDED! ADD 50P FOR P&P.

de boer elektronika
 Kleine Berg 39-41 Eindhoven.
 Nederland, tel. 040-448229.

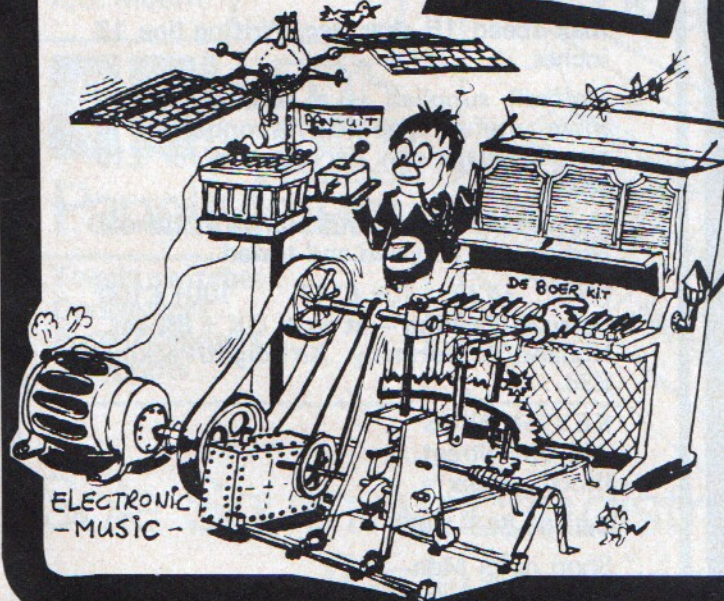
FORMANT

SYNTHESIZER

- Interface (9721-1) £ 18.15
- Interface receiver (9721-2) £ 3.85
- Power supply (9721-3) £ 37.—
- VCO module (9721-4) £ 2.25
- Keyboard divider (9721-4) £ 52.35
- VCO modul (9723-1) £ 21.40
- VCF (9724-1) £ 14.45
- ADSR (9725-1) £ 19.30
- Dual VCA (9726-1) £ 18.15
- LFO (9727-1) £ 11.15
- Noise (9728-1) £ 13.75
- COM (9727-1) £ 13.85
- Front panels cpl (11 items) £ 60.—
- 3 okt. Keyboard with K.A contacts £ 365.—
- Cpl. set with keyboard, all necessary moduls (thus inkl. 3 x VCO and 2 x ADSR), and front panels

ELEKTOR PIANO

ELECTRONIC PIANO. COMPLETE KIT WITH ALL PCB'S, KEYBOARD AND CONTACTS K.A., X-TAL ETC. £ 259.00



SELEKTOR

Unique colour enlarger

Philips recently introduced a unique, electronic system for making photographic colour enlargements from either negatives or slides.

Designated the Electronic Tri-one Colour System (ETC), the system comprises a universal enlarger equipped with a built-in colour light source which is electronically controlled via a separate control unit at the baseboard. Use is made of the principle that by mixing the three primary colours, red, blue and green, any colour can be reproduced.

In order to create natural colours it is no longer necessary to use single or moving filters in the darkroom when printing colour pictures.

It is now possible to create light in any desired colour by using three special lamps and fixed filters with narrow band colour channels closely related to the colour sensitivity of photographic paper. The required colour balance is made by adjusting three knobs at the

control unit. Using this principle offers the advantage that the photographic paper has to be exposed only once with an integral timer, hence the name of the system: 'Tri-one' (triple colours with one exposure time).

Technical details Enlarger PCS 130

- Universal enlarger house for standard enlarger lamp and colour light source
- 110 to 6x7 format. Maximum enlargement on baseboard 40 x 50
- Universal negative carrier with sliding masks and glass mounts for all negatives up to 6 x 7 and glassless 35 mm film metal mask as standard
- Filter drawer
- Rigid column with easy twist-lock grip movement
- Enlarger unit rotates through 180° for wall projection and column is reversible for floor projection
- Full movement of lens boards and enlarger housing for distortion control with edge to edge focus

- Double (right and left) focus knob
- Aided by effortless counterbalance system
- Universal condensers

Light source PCS 150

- No moving parts — no filter adjusting, no heat instability
- Precise control of colour and light output
- Colour balance at various aperture/exposure combinations
- Light source with three separate cool beam halogen lamps
- Precise, narrow spectral bands for maximum colour saturation
- No stray light — no accidental casts
- Low operating voltage — safety
- No UV and virtually no infra-red — shorter analyser times
- Grade control for black and white

Control unit PCS 150

- Colour channels supported by visual 'logic' colour wedges — calibrated in densities
- Integral timer (5 - 40 secs.)
- On/off switches for each channel/monochromatic prints
- Simple three-position switch for max. white light, controlled light and stand-by
- Well illuminated scales — switched off in stand-by position
- Softly illuminated start exposure knob
- Lighting level and colour density easily controlled
- Colour balance obtainable for various exposure time/aperture combinations.

*Philips gloeilampenfabrieken
Eindhoven
The Netherlands.*



High Fidelity 79

The High Fidelity 79 Spring audio exhibition, now established as a major international high fidelity exhibition, will take place at the Cunard International Hotel in London between 24th and 29th April. The exhibition will, as in previous years, provide an excellent international showcase for high fidelity products from all over the world. The Exhibition Organisers anticipate that once again there will be a large number of visitors to the exhibition from Europe, and in addition look forward to receiving applications for exhibition space from European companies interested in displaying their products in the large and buoyant British market. Such companies should contact Don Quillen or Barry Horne, Emberworth Limited, London House, Exford Road, Stokenchurch, Buckinghamshire HP14 3SX.

measuring by the book

Measurement standard for audio amplifiers

When it comes to buying audio equipment, the specifications given in advertisements and manufacturer's literature may prove to be woefully misleading. Often, consumers misunderstand the technical 'jargon'; furthermore, manufacturers tend to stress those figures that make their product 'look good' and only include other specifications in small print — if at all. Confusion becomes complete when all sorts of new inventions are included in an otherwise technical specification list. Take, for instance, 'Instantaneous peak music power, one channel driven' . . . Ugh.

The American Institute of High Fidelity (IHF) recently published a new standard, dealing with 'Methods of Measurement for Audio Amplifiers'. Some of the most important points are dealt with in this article.

Numbers are an important feature in our society. All sorts of 'things' are expressed in figures. Provided the 'thing' in question can be measured objectively and provided some kind of reference scale is available, there is no real problem. Distances are measured in kilometres or miles; value is expressed in pounds or dollars (a gradually changing scale, that); earthquakes are measured according to the Richter scale.

Trying to express 'quality' in this way is rather more difficult. Quality usually refers to a subjective evaluation of the sum total of all the good and bad points associated with some item. The problems here are, first of all, to identify all the characteristics involved; secondly, to find a way of measuring them; finally, to 'weight' them accurately — i.e. to determine how important each one is when it comes to 'calculating' the overall 'quality'.

When it comes to evaluating hi-fi audio equipment, no such overall 'quality measurement' exists. The customer who is interested in buying quality is forced to make do with lists of technical specifications, provided by several different manufacturers — each trying to sell his own product. The potential buyer must now decide:

- 1) Do the specification lists contain all relevant information required for evaluating the equipment — without padding and/or omissions?
- 2) Insofar as the figures in the specification lists are the result of some measurement, how relevant and accurately defined are the measurement procedures?

The second question refers to the fact that some manufacturers seem to devote more time to finding loop-holes in the existing standards than to designing good equipment in the first place. The result has been 'data-sheet inflation', with even well-meaning manufacturers being forced to join in.

The first question is even more fundamental: is it possible to define a series of measurements that covers all 'quality' aspects and, if so, does the specification list contain the complete set of figures (without any irrelevant 'frills')?

The answer, regrettably, is no. The final

quality decision is made by the human ear and, as yet, no set of measurements has been found from which a 'figure of merit' can be derived that agrees with the ear's decision in all cases. Obviously, this is a rather unsatisfactory situation. At present, researchers are concentrating on three main problems: what performance aspects are we forgetting to measure?; what is the relative importance of those aspects that we do measure?; is everybody measuring the same aspects in the same way?

It is the last question, in particular, that is the subject of this article. The new IHF measurement standard specifies what performance aspects are to be measured and how to measure them. It doesn't attempt to give minimum specifications, as in the (in-)famous DIN 45.500 norm. An amplifier can (and should) be 'measured according to the IHF-A-202 standard' but to say that it 'meets the IHF standard' is nonsense.

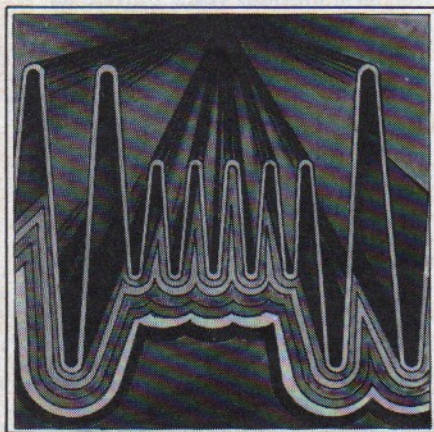
IHF-A-202 1978

In the twelve years that have elapsed since the last IHF Amplifier Standard (IHF-A-201, 1966) was presented, many changes have occurred in amplifier design. The new 'Standard Methods of Measurement for Audio Amplifiers' are based on current theory and practice. It is unlikely that they should prove to be the final word: future developments will probably necessitate a further revision in ten years time. Meanwhile, however, the new Standard should make amplifier specification sheets more meaningful than ever before.

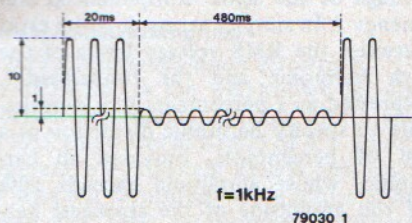
The Table lists all specifications that are to be measured — 28 in all. A clear distinction is made between 'primary ratings' and 'secondary disclosures'. To rate amplifiers according to IHF standards, all primary ratings must be listed. In addition, the secondary disclosures may be listed *provided that they are based upon measurements made in accordance with this standard.*

In this article, the standards will be dealt with in three sections:

1. Power, Watts and Watt-nots;
2. Distortion;
3. Odds and ends.



1



IHF standard toneburst

Table

Primary ratings, that must be listed:

For Power Amplifiers

1. Continuous Average Power Output
2. Dynamic Headroom
3. Frequency Response
4. Sensitivity
5. A-weighted Signal-To-Noise Ratio

For Preamplifiers

1. Frequency Response
2. Maximum Voltage Output
3. Total Harmonic Distortion
4. Sensitivity
5. A-weighted Signal-To-Noise Ratio
6. Maximum Input Signal
7. Input Impedance

For Integrated Amplifiers

1. Continuous Average Power Output
2. Dynamic Headroom
3. Frequency Response
4. Sensitivity
5. A-weighted Signal-To-Noise Ratio
6. Maximum Input Signal
7. Input Impedance

Secondary Disclosures that may be given, as applicable:

1. Clipping Headroom
2. Output Impedance
3. Wideband Damping Factor
4. Low-Frequency Damping Factor
5. CCIR/ARM Signal-To-Noise Ratio
6. Tone-control Response
7. Filter Cutoff Frequency
8. Filter Slope
9. Crosstalk
10. A-weighted Crosstalk
11. CCIR/ARM Crosstalk
12. SMPTE Intermodulation Distortion
13. IHF Intermodulation Distortion
14. Transient-Overload Recovery Time
15. Slew Factor
16. Reactive Load
17. Capacitive Load
18. Separation
19. Difference of Frequency Response
20. Gain-Tracking Error
21. Tone-control Tracking Error

Watt's in a norm

The output power rating of an amplifier is still one of the first things that a prospective buyer looks for. Manufacturers know this . . . Stringent rules are required, both as to measurement method and description of the result.

In future, output power specifications can be given either in Watts or in 'dBW', where 0 dBW is equivalent to a reference output power of 1 Watt into the reference load resistance. The dBW is a logarithmic power-rating scale: it refers to the number of dB by which the output power exceeds 1 Watt.

equivalent to 10 dBW; 100 watts becomes 20 dBW; 250 mW is -6 dBW. Use of the dBW may come as a disappointment to those who favour large numbers ('200 watts' sounds better than '23 dBW'), but it is a far more realistic specification.

Continuous Average Power Output

The continuous average power output* of an amplifier is the power that is delivered into the rated load when the amplifier is driven by a sine-wave via a line input. The corresponding rating of the amplifier should be valid over the full rated bandwidth at the rated maximum total harmonic distortion. No 'small print' on the lines of '1 kHz, 10% THD'.

The power rating is obtained by measuring the RMS value of the output voltage and calculating the corresponding power from this. If a power amplifier is rated for more than one load impedance, then the Continuous Average Power Output must be rated separately for each load impedance. Further 'rules of play' are as follows:

- all channels should be operating under identical conditions; in other words, for a stereo amplifier *both* channels are fully driven when determining the output power rating.
- the rated load impedance(s), rated bandwidth (e.g. 20 Hz . . . 20 kHz) and rated total harmonic distortion must be specified as part of the output power rating.
- prior to this measurement, the amplifier must be run for one hour at one-third of the specified continuous average power output. (Warming-up with a vengeance! That should please the manufacturers of cooling fans).
- for the measurement itself, the sine-wave must be applied for a period of not less than five minutes.
- the rated total harmonic distortion percentage must be valid for all output powers from -6 dBW (250 mW) up to full drive, over the full rated bandwidth. This means that amplifiers with low distortion at full drive but with nasty cross-over distortion at lower levels (these are more important in practice) are doomed to fall flat on their faces.

Dynamic Headroom

A favourite 'specification' in modern advertising is 'Music Power'. More watts than 'continuous power' and ideally suited to poetic licence. Music power is supposed to refer to the number of watts an amplifier can deliver for short periods. The question is: how short . . .

The original idea was quite reasonable. An amplifier with a simple, unregulated supply is capable of delivering a lot of power for a short period - that is, until the supply voltage collapses. Music consists of short peaks at high level, with an average power that is approximately 17 dB lower (on average program material). Therefore, an amplifier with a continuous power rating of 20 W and a 'music power' rating of 100 W may well sound just as good, just as 'clean' and just as loud as an amplifier with continuous and 'music power' ratings both equal to 100 W. Regrettably, there was no standard measurement procedure to determine the 'music power' rating.

The new IHF standard retains the idea, but does away with the confusion. Instead of specifying 'music power' in watts, it introduces a 'dynamic headroom rating' in dB. More importantly, it specifies the measuring method:

- a toneburst signal is used, with a period time of 500 ms; a 4% duty-cycle; a frequency of 1 kHz; a 20 dB level difference. In other words, the 1 kHz signal is at standard level for 480 cycles; it is then boosted by +20 dB for 20 cycles; then back to reference level for 480 cycles, and so on. The level jumps must occur in the zero crossing of the 1 kHz signal. (A simple circuit to produce this signal is described elsewhere in this issue).
- the amplifier is loaded with the rated load impedance(s) and driven by this test signal, applied to the line input.
- the output of the amplifier is observed on an oscilloscope, and the input level is adjusted to the maximum value that just does not cause clipping of the peaks of the signal during the +20 dB bursts.
- the output voltage during the +20 dB bursts is determined, and the corresponding output power is calculated; the ratio between this value and the Continuous Average Power rating, expressed in dB, is quoted as the 'dynamic headroom'.

To take an example. Say that the rated Continuous Average Power Output is 40 W (= +16 dBW); the power output corresponding to an undistorted toneburst is 50 W (= +17 dBW); the dynamic headroom is a staggering 1 dB. The 20 ms 'high level' period of the toneburst is more than adequate: the peaks in music and speech rarely last for more than 10 to 15 ms. Furthermore, it is rare indeed for such peaks to occur at half-second intervals.

Clipping Headroom

Well. We must allow the advertising boys some 'headroom'. Let us refresh

* Continuous power is sometimes listed as 'RMS power'. Wrong.

our memories: 'continuous average power output' must be valid over the full bandwidth and at the rated harmonic distortion level. It will often be possible to obtain a higher output level at 1 kHz — certainly if the level is specified as the 'clipping point' of the amplifier, i.e. the point at which clipping is just not visible on an oscilloscope. 'Clipping Headroom', according to the IHF standard has the saving grace that it is to be rated in dB.

An example. The continuous power output rating of an amplifier is 40 W (+16 dBW), but at 1 kHz it is possible to obtain a 'clean-looking' sinewave trace on an oscilloscope at 45 W (+16.5 dBW). The clipping headroom may be specified as 0.5 dB — if any advertising copy-writer feels so inclined.

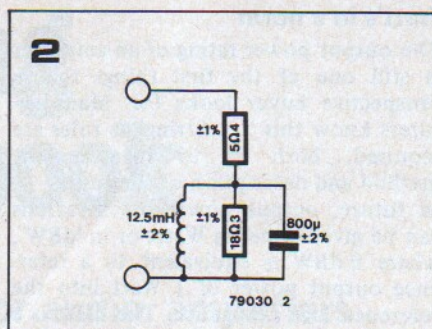
If no frequency is specified, the measurement should be performed at 1 kHz. Other frequencies may be used, provided they are specified. It is also permissible to perform the measurement over a band of frequencies. Note, however, that once one value is given the clipping headroom must be specified for all rated load impedances.

Reactive load

Now *that* is something new in amplifier specifications. It is common knowledge that many amplifiers meet all their 'official' specifications when working into a resistive load, but start to do horrible things when loaded by a loudspeaker. 'Horrible things' in the sense that any attempt to operate at full power into a loudspeaker ('when the deci-bell tolls') causes the built-in protection circuits to operate briefly — but audibly! This effect is especially noticeable at frequencies close to the resonant frequency of the loudspeaker.

A possible solution to the problem would be to use a reference loudspeaker instead of a load resistor and measure the distortion as a function of frequency under full-drive conditions. However, there is one minor problem. Where do you obtain a 'reference loudspeaker' that will withstand full-blast continuous (sinewave!) power without departing for those PA systems in the skies where all good loudspeakers go? It is a common misconception that, say, a 40 W loudspeaker will actually withstand 40 watts of continuous power over its full frequency range. No sir! It is designed to handle the music or speech signal output from a 40 W amplifier. And that is, most definitely, something else.

A different solution is required. What about using a load network that has similar characteristics (for low frequencies in particular) to a loudspeaker? A suitable circuit is shown in figure 2. Basically this network (specified in the IHF standards) 'looks' like a loudspeaker, as far as the amplifier is concerned. It is a damped parallel resonant circuit with a series resistor; the resonance frequency is 50.3 Hz. The

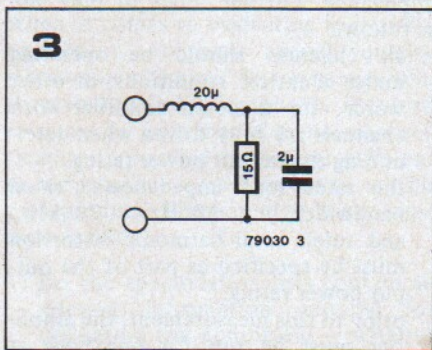


maximum phase shift is $\pm 39^\circ$, at 40 Hz and 63 Hz respectively.

The measurement procedure is as follows. A 40 Hz sinewave is applied, and the output level is determined that corresponds to a THD of 1%. This test is repeated at 63 Hz. The lower of the two levels is used to derive a power rating. The ratio between this power rating and the continuous average power rating, expressed in dB, is the 'reactive power rating'. At best, this rating will probably be 0 dB; normally, it will be negative.

Capacitive load

Oops! Sorry, the IHF boys forgot that one. A pity, though: electrostatic loudspeakers are quite common in modern installations. A similar test to the one described above, using a network that has similar characteristics (for high frequencies in particular) to an electrostatic loudspeaker, will produce highly interesting results in many cases. Gentlemen of the IHF, may we offer you a wicked little network? See figure 3.



Distortion

Another favourite specification. The less there is, the better — or so one would assume. The question is: how are low distortion figures obtained? By good design, or...

Let us see what the IHF standard specifies.

Harmonic distortion

The best known, oldest, and most easily measured type of distortion. As specified in the past, however, the figures quoted have little bearing on audible 'quality'. With the advent of the 'spectrum analyser', it is possible to give a more useful specification — based on a more realistic measurement procedure. First of all, let us quote a few new (or revised) definitions:

The *percentage of Xth harmonic distortion* of a sinewave of frequency f is numerically equal to 100 times the ratio of the RMS voltage of the signal component at frequency Xf , to the RMS voltage of the signal component at frequency f . In simpler terms, it is the ratio between the RMS voltage levels of the X th harmonic and the fundamental, expressed as a percentage. It is permissible to specify harmonic distortion as a list of percentages, provided all harmonics whose amplitude exceeds 10% of the amplitude of the strongest harmonic are included in the list.

The *percentage of total harmonic distortion (THD)* of a sinewave of frequency f is (take a deep breath!) 'numerically equal to 100 times the ratio of the square root of the sum of the squares of the RMS voltages of each of the individual harmonic components, to the RMS voltage of the fundamental'. A formula looks simpler:

$$\%THD = 100 \times \frac{\sqrt{X_2^2 + X_3^2 + X_4^2 + \dots}}{\sqrt{X_1^2}}$$

As before, all harmonics with an amplitude above 10% of the strongest harmonic are to be included.

A variation on this theme is the *percentage of weighted total harmonic distortion (WTHD)*. Basically, the same formula is used, with one difference: the X^2 -factors are each multiplied by a weighting factor that is intended to express the subjective nuisance value of that particular harmonic. However, the weighting factors are not specified by the IHF and so a WTHD rating can only be evaluated if the manufacturer specifies his weighting system.

The three harmonic distortion ratings listed so far are all based on measurements performed with an (expensive) spectrum analyser. A traditional (and relatively inexpensive) distortion meter may still be used, provided the results obtained are specified as *the percentage of total harmonic distortion plus noise (THD + N)*. Which is exactly what it is.

Of the four harmonic distortion ratings described above, at least one must be included in the specification of a power amplifier; as stated earlier, this specification is an integral part of the 'continuous average power output' rating.

For preamplifiers, the total harmonic distortion rating is defined as the greatest value of total harmonic distortion measured at the output terminals at any frequency within the rated bandwidth. (!). The measurement must be performed for each input, under the following conditions:

- input signal level (line inputs): 2.0 V (= +6 dBV);
- output level also 2.0 V;
- input signal level for dynamic pickup inputs: 20 mV at 1 kHz, the level being adjusted with frequency according to the inverse of the normalized equalisation;

— input signal level for moving-coil inputs: 2 mV at 1 kHz, again adjusted to follow the equalisation curve. All in all, a quite realistic measurement procedure.

Intermodulation distortion

SMPTE intermodulation distortion

(*SMPTE-IM*) is the well-known IM distortion measurement, using 60 Hz and 7 kHz sinewaves at a ratio of 4:1. In our opinion a completely useless test, since it does not furnish any more information than the THD measurement. Without wasting time, let us move on to

IHF intermodulation distortion

(*IHF-IM*). Two sinewaves, f_1 and f_2 , of equal amplitude and with a constant frequency difference (1 kHz) are applied to the input. The percentage of IHF-IM distortion components are plotted as a function of the 'centre frequency' $\frac{1}{2}(f_1 + f_2)$. Five plots are specified, corresponding to output levels of -12 dB, -9 dB, -6 dB, -3 dB and 0 dB with respect to the reference output level. A complete set of five plots should be given for all rated load impedances (power amplifier section) and for all inputs (preamplifier section; disc inputs driven via an inverse frequency correction network). Never again need advertising copy-writers rack their brains to find a sufficient number of illustrations!

It is also permissible to specify IHF-IM in figures. In that case, the highest percentage found is specified for each load impedance and for each input.

What exactly is the IHF-IM distortion percentage?

Only the second- through fifth-order intermodulation components are measured, defined as follows:

second-order: $f_1 \pm f_2$

third-order: $2f_1 \pm f_2$ and $f_1 \pm 2f_2$

fourth-order: $2f_1 \pm 2f_2$

fifth-order: $3f_1 \pm 2f_2$ and $2f_1 \pm 3f_2$

Of these 12 components, only those whose frequency is less than 20 kHz and whose amplitude exceeds 10% of the amplitude of the strongest intermodulation component are included in the final calculation. The RMS value of these components is calculated, and divided by the RMS value of the complex input signal ($f_1 + f_2$). The result, expressed as a percentage, is the IHF-IM distortion rating.

Transient intermodulation distortion

(*TIM*) receives honourable mention in the IHF Standard: it is 'a form of dynamic intermodulation distortion that may be associated with feedback amplifiers that use internal lag-compensation, and is caused by the non-linear operation (slew-limiting) of one or more of the gain stages within the feedback loop, under conditions that include a rapid change in input voltage'. However, the Standard does not specify a measurement procedure; it merely informs us that 'several methods have been proposed in the literature. Any of these may be used, provided that the method

be stated with the results of measurement'.

How well an amplifier can handle rapid changes in the input voltage is, however, to be measured:

The *slew factor* is defined as the ratio of the highest frequency that can be applied to the input of an amplifier, at a level that produces rated output at 1 kHz, and be reproduced at the output with acceptable linearity, to 20 kHz.

The measurement procedure is as follows:

The gain control is set to give maximum gain (power amplifier) or to give +12 dB overall gain (preamplifier). A 1 kHz sinewave is applied to the input (each input is to be measured in turn) and the level is increased until the rated continuous average output power level (or voltage output level, for a preamplifier) is obtained.

The frequency is now increased until the total harmonic distortion of the output signal is 1%. The frequency at which this occurs, divided by 20 kHz, is the slew factor. In other words, if the 1% level is reached at 10 kHz the slew factor is 0.5; on the other hand, if 1% THD is only found for frequencies above 20 kHz the slew factor is 1.0.

As with all distortion tests, the measurement must be repeated for all inputs and all rated load impedances; dynamic or moving-coil cartridge inputs should be preceded by a network having the inverse frequency response characteristic.

Miscellaneous odds and ends

A great many 'other' standard measurements are described. Too many for this article. We will confine ourselves to the most interesting 'ratings'.

The *sensitivity* rating of an amplifier refers to the RMS input voltage required to obtain a certain output level. To be more precise: the reference output level, i.e. 1 W for a loudspeaker output and 0.5 V for a preamplifier output. The measurement is carried out at 1 kHz, for all inputs, and with the gain control at maximum. If (preset) gain controls are provided for each input, the sensitivity must be measured and specified in the two extreme settings of this control: first the maximum sensitivity, then the minimum.

The *maximum input signal* rating refers to the maximum signal level, in volts, that the input amplifier can handle without clipping. Note that this applies to all stages preceding the main gain control: the gain is progressively reduced to avoid clipping. It is quite easy to distinguish input- and output clipping, when using an oscilloscope: in the former case, adjusting the main gain control alters the output level but any 'flat tops' remain visible; if clipping is occurring in the output stage, the only effect of the gain control is to alter the

width of the tops — the level remains constant.

The measurement must be repeated at a number of frequencies within the rated bandwidth of the amplifier, and the minimum value thus obtained taken as the maximum input signal rating. As usual, a frequency response correction network is used when measuring disc preamp inputs.

We have one minor bone to pick here. All measurements relating to disc preamps that have been discussed so far are realistic. This one, in our opinion, is not — quite. As we have pointed out several times in the past, the signal handling capabilities of a disc preamp should be considered in the light of theoretically possible input signal levels: i.e. the maximum signal level that can be recorded, as a function of frequency. To cut a long story short, at frequencies above approximately 3 kHz the maximum input signal level rating as measured according to the IHF standard procedure may decrease at 6 dB/oct without affecting the performance. Forcing manufacturers to specify the minimum value obtained within the full rated bandwidth (up to, say, 20 kHz) may lead to unfairly biased comparisons.

The *maximum voltage output* rating of a preamplifier is the minimum sinewave output level in RMS volts (or dBV) that can be delivered over the rated bandwidth at 1% THD. All inputs should be measured, and the gain control should be set to give +12 dB overall gain. A fairly straightforward definition, with one interesting twist: the output of the preamplifier must be loaded by a 10 k resistor in parallel with a 1 nF capacitor ('Standard reference load' for a preamplifier).

Signal-to-noise-ratio (S/N)

A riddle: A 100 W power amplifier specification lists 'S/N = 80 dB'. The S/N ratio of a forty-watter is given as 70 dB. Which one is noisier? Any offers? The boy with the right answer can keep the manufacturers, with our compliments.

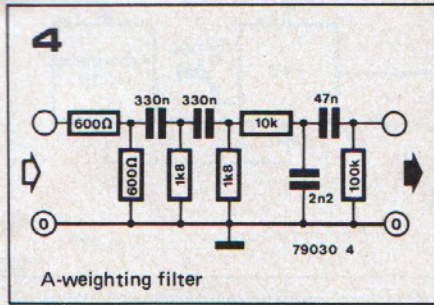
You come across the craziest things. What about this one: an amplifier with a S/N ratio of *minus* 60 dB! The bulk of the circuit must consist of a broadband noise generator.

Signal-to-noise ratio specifications are useless unless the relevant signal level is known. It must either be included in the specification given, or else the measurement must be performed in accordance with a standard that specifies a certain level. The IHF standard takes the latter approach: the signal-to-noise ratio must be specified at the output reference level (0.5 V for preamplifiers, 1 W for power amplifiers).

The noise output is measured with the aid of a 'weighting filter'. The frequency characteristic of this filter allows for the fact that some noise frequency bands are more annoying than others. The

IHF Standard therefore specifies the

A-Weighted-signal-to-noise ratio (S/N). This is the ratio of the output reference level to the A-weighted output noise level, in dB. The measurement is performed on all inputs, with the gain

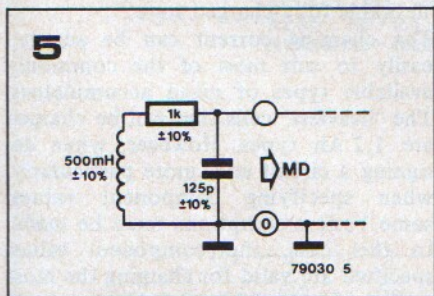


control set according to standard test conditions (e.g. 0 dB overall gain for a line input). The input under test must be terminated with a specified impedance: a 1k resistor for line inputs; a 100 Ω resistor for moving-coil inputs; the network shown in figure 5 for dynamic disc inputs. No nonsense: no short-circuited inputs. The terminations specified are reasonable approximations of the type of input load that will normally be found in practice, and so the measurement results are likely to be more realistic than in the past. A great idea.

The standard does include a warning: care should be taken that the termination networks do not act as pickup links for electrostatic or electromagnetic fields. Not to worry: any unwanted pickup of this type would produce poorer figures - and no manufacturer will make *that* mistake.

A similar measurement can be performed using the CCIR weighting network. In this case, the result is listed as the 'CCIR/ARM signal-to-noise ratio'.

Last but not least, the *Transient overload recovery time* of an amplifier refers to the time required for an amplifier to recover from a 10 dB overload of 20 ms duration, occurring at a repetition rate of once every 0.5 seconds.



The tone-burst signal shown in figure 1 is applied to the relevant input. The gain control is set so that a reference-level input will produce an output level 10 dB below the continuous average power rating (or voltage output rating, as the case may be). The output signal is monitored on an oscilloscope; in particular, that portion of the cycle that occurs immediately following the return

of the input signal to reference level. The number of sinewaves that are still visibly distorted is determined; this figure, expressed in milliseconds, is the recovery time.

In conclusion

It will probably take a while for the new Standard to penetrate into advertising copy. Since it originates in the USA, it is to be expected that American (and Japanese) manufacturers will be the first to use it.

What about Europe? Embarrassed silence. The Common Market and European Unity notwithstanding,

European manufacturers and standards institutes still haven't succeeded in coming up with a similar up-dated-standard. They're working on it, give them their due, but there's a distinct lag compared to the situation in the States. Come on boys, hurry it up! DIN 45.500 is dead. It's high time it was buried.

Lit.:

The official IHF Standard document IHF-A-202 can be obtained from: The Institute of High Fidelity, Inc. 489 Fifth avenue, New York N.Y. 10017, USA. Price: \$ 7.50.

Decibels made easy

The decibel (dB) is the tenth part of a 'Bel', but for some reason decibels are the only 'unit' ever used. Who ever heard of centibels or millibels? The dB is used to specify voltage, current and power ratios (to name a few) - on the lines of: how much larger is this voltage with respect to that one. The number of dBs is defined as 10 or 20 times the logarithm of the ratio in question; '10 times' for power ratios and '20 times' for voltage or current ratios.

Why? In particular, why use logarithms, and why use a different multiplication factor for power ratios? To start with the first point: the ratios that we are interested in can be very large, easily going up to 100,000:1. Furthermore, in most cases where dBs are used, 'significant' changes in level are those where a signal is multiplied by a certain factor. For instance, the *perceived* increase in a power level from, say, 10 W to 20 W (x 2) is the same as the *perceived* increase from 100 W to 200 W! In both cases the power is doubled, and that is what counts. Expressed in dB, both ratios are equivalent to a 3 dB increase. Use of the dB also solves the first point: power ratios from 100,000:1 to 1:100,000 correspond to a dB scale from +50 dB to -50 dB (for power ratios). In spite of this 'scale compression' a (significant) ratio of 2:1 is still clearly expressed as +3 dB.

The second point, the difference in multiplication ratios, is easy to explain. Power (in Watts) corresponds to voltage *squared* divided by resistance. Therefore, if a voltage increases from, say, 1 V to 3 V (x 3), the corresponding power will increase from, say, 1 W to 9 W (x 9). However, the effect is the same: these are just two different ways of expressing the same level change. When using dBs it is effects that interest us, and so it is preferable to use the same dB-value to express both ratios; in other words, if the power ratio is given in

dB, it is useful to give the voltage ratio *squared*. Since dBs are logarithmic, this is equivalent to multiplying the logarithm of the ratio by 2: if 'power-dBs' are 10x the log of the ratio, voltage (and current, etc.) dBs must be 20 x the log of the ratio.

So much for theory. In practice, dBs now lead a life of their own. Although it is quite possible to calculate logarithms of ratios, there is usually no need. Bearing in mind that *adding* dBs is equivalent to *multiplying* the ratio, only a few dB values need to be memorised in order to 'calculate' virtually any ratio with a sufficient degree of accuracy. Here we go:

number of dBs	power ratio	voltage ratio
0	1:1	1:1
+3	2:1	$\sqrt{2}:1$ ($\approx 1.4:1$)
+6	4:1	2:1
+10	10:1	$\sqrt{10}:1$ ($\approx 3:1$)
+20	100:1	10:1

To give a few examples:

A voltage ratio is specified as 32 dB. $32 = 20 + 6 + 6$, so the ratio is $10 \times 2 \times 2 = 40$.

Voltage ratio 34 dB:

$34 = 20 + 20 - 6$, so the ratio is $10 \times 10 \times \frac{1}{2} = 50$. Note that the minus sign simply implies that the ratio works 'in the opposite direction': +6 dB = 2:1 (= x2), so -6 dB = 1:2 (= x $\frac{1}{2}$).

Voltage ratio 33 dB. Now what? Using a 'rule of thumb': 1 dB is approximately equal to 10% for voltages (20% for power ratios), so $33 = 32 + 1$ (or $34 - 1$) and the ratio is $40 + 10\% \approx 44$ (or 45).

The output power of an amplifier is 60 W. How many dBW? In other words, what is the power ratio in dB between 60 W and reference level (1 W)? One approach: 60 W is 'just over' 50 W; $50 = 100 \div 2$, so 50 W is $20 - 3 = 17$ dBW. 60 W must be a bit more... How much more? $1 \text{ dB} \approx 20\%$ - perfect! So 60 W must be 18 dBW. A spot-on accurate calculation would give the following result: $17.78151250 \dots$ '18' is near enough.

reliable nicad charger

Nickel-Cadmium accumulators, or nicad cells for short, are becoming ever more popular. As prices drop and the number of available types increases, it has become a viable proposition to use them in almost any type of battery-powered equipment. For this reason it is reasonable to assume that many owners of portable radios, cassette decks, electronic flash guns, pocket calculators and the like — not to mention remote-control enthusiasts — are on the look-out for a really good nicad charger. It shouldn't be expensive (otherwise it's still cheaper to use conventional batteries), but it must automatically provide the correct charging current and time: on the one hand, overcharging must be impossible; on the other hand, the cells must be fully charged.

Anyone who has had previous experience with charging nicad cells will probably have discovered what features are desirable for a nicad charger. For that matter, even without the benefit of past experience — good or bad — the basic requirements are fairly obvious. A good charger should be reliable, and under no circumstances should it damage the nicad cells. Regrettably, not all commercially available chargers fulfil these requirements.

The charger described in this article was designed to meet the following specifications:

- it should be suitable for practically all commercially available types of nicad cells;
- the charging current should be held constant, at 1/10 of the capacity of the accumulator in Ah; however, it should also be possible to select a higher current for so-called sintered cells, since these may be charged at 1/3 of their capacity;
- a timer should be incorporated in the charger, to ensure the correct charging time;
- to preclude the possibility of damaging the nicad cells, they should first be discharged to a well-defined level before starting the charging cycle. In this way, the danger of drastically overcharging near-full batteries is virtually eliminated;
- preferably, the changeover from discharge cycle to charging cycle should be carried out automatically;
- after completing the charging cycle, it should be permissible to leave the cells connected to the charger (for months, even). Furthermore, under these conditions they should be trickle-charged to keep them fully-charged at all times.

This list of requirements was presented to one of our designers, with the request to come up with a cheap and reliable circuit, suitable for home construction — an important point, if it is to be published in a magazine! — that would do the job properly. After the usual head-scratching, breadboarding (more of a bird's nest, actually), testing and evaluating, a circuit evolved. The underlying principles are best clarified with the aid of a block diagram.

Block diagram

Figure 1, the functional block diagram of the nicad charger, illustrates the basic principles of the final design. Compared with most conventional chargers, this block diagram may seem frighteningly complicated. In practice, it is not nearly as bad as it seems, since several of the 'blocks' actually consist of quite simple units. For instance, the block marked 'trickle-charge' merely represents one resistor.

To start at the beginning:

When the start pushbutton is operated, a flip-flop (FF1) initiates the discharge cycle for the nicad cell(s). This is indicated by a red LED. When the voltage across the cell (or cells) drops below a preset level, a comparator (IC1) resets the flip-flop FF1. As a result, the discharge cycle is terminated and a second flip-flop (FF2) is triggered. The charge cycle is now automatically initiated; a green LED lights to reassure any passing nicad owners . . .

When FF2 changes state, a timer is triggered. This unit is included to fulfil one of the main requirements stated earlier: the charging cycle must be terminated automatically after a certain time has elapsed. At the end of the preselected time, FF2 is reset by the timer. The main charger (T1) is cut off, but the trickle-charger remains operative, maintaining the cells in the highly desirable fully-charged state.

The charging current can be adapted easily to suit most of the commonly available types of nicad accumulators. The 'heaviest' cells that can be charged are 1,2 Ah types. However, when designing a circuit and, more particularly, when specifying component values, some basic assumptions must be made. In this case, the component values specified are valid for charging the most commonly available 0.5 Ah types of nicad cell. These cells are charged at 1/10 of their Ah rating — 50 mA — for the specified period of 14 hours. When charging sintered-cells — as stated earlier, these cells can withstand charging at up to 1/3 of their Ah rating — the charging current can be 'upped' to 150 mA; at the same time, the charging time is reduced to 3½ hours. Wide-awake readers may have noticed that both these

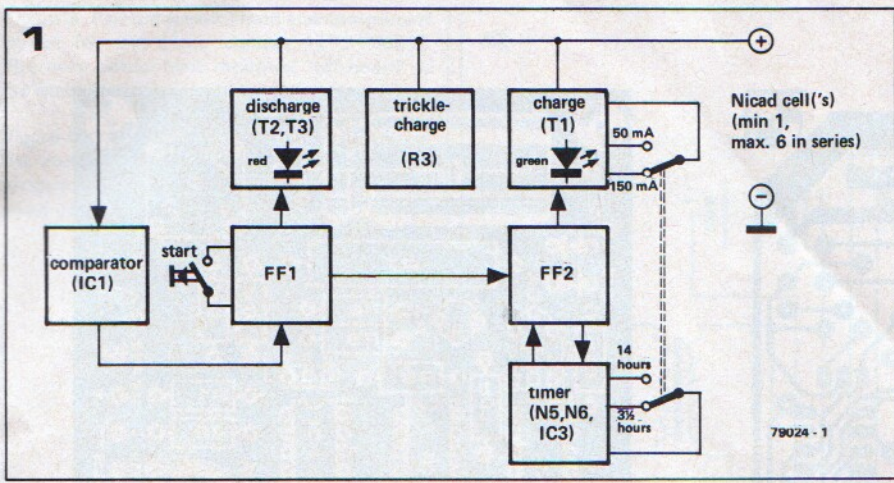
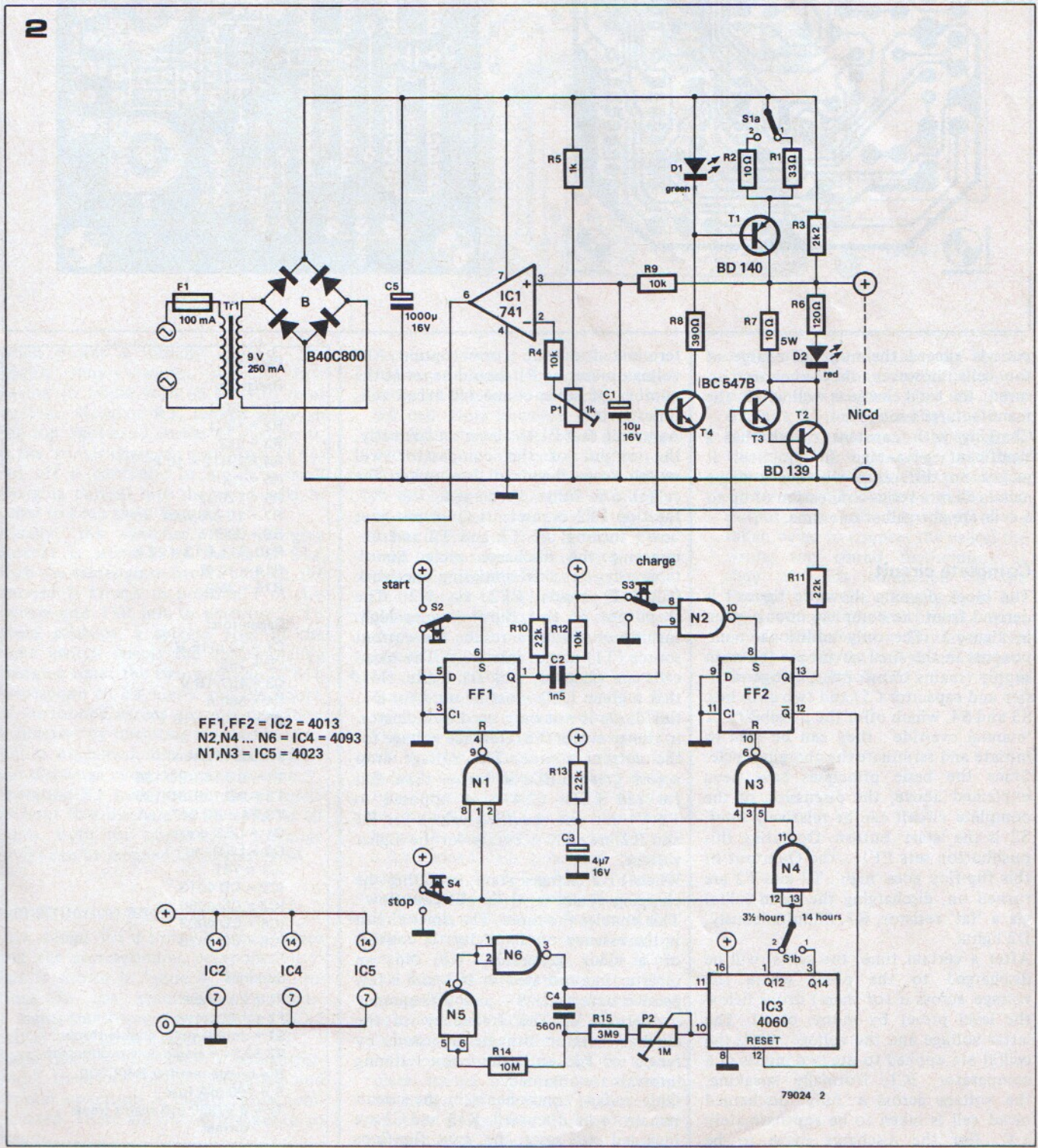
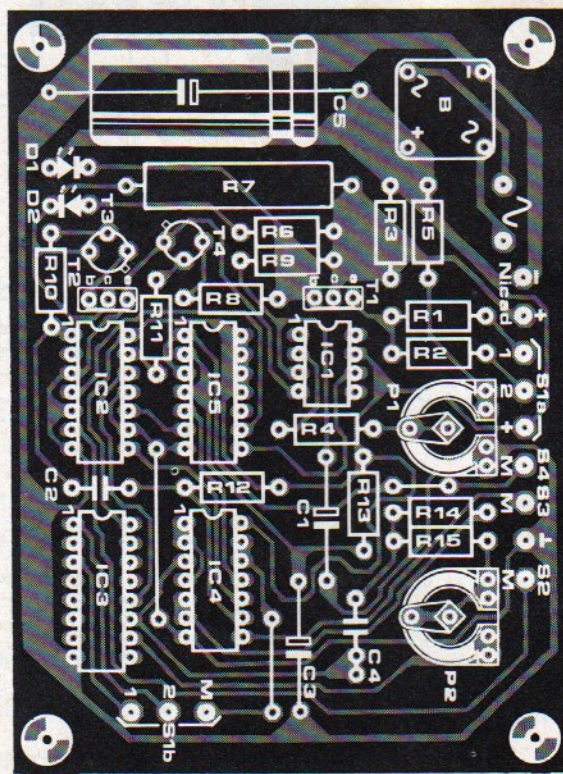
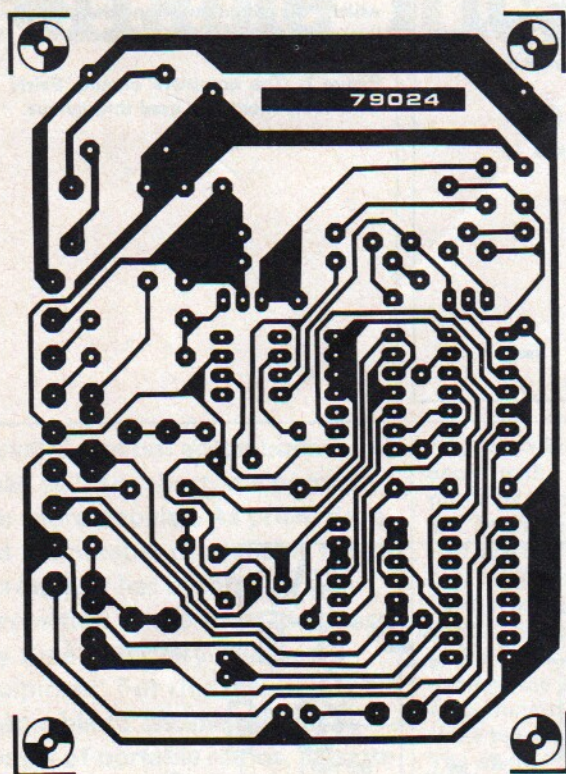


Figure 1. Block diagram of the automatic charger for nicad accumulators. The cell (or cells) is first discharged to a preset level, after which the fixed-duration charging cycle is initiated.

Figure 2. The complete circuit. Fairly standard components are used throughout.



3



periods exceed the nominal charge of the cells; however, they may rest assured: the total charge is well within the manufacturer's tolerance.

Charging with constant *current* has a significant advantage in practice: it makes no difference whether a single nicad cell or a series-connection of up to 6 cells are charged at one time.

Complete circuit

The block diagram shown in figure 1 is derived from the complete circuit given in figure 2. The only additional components in the final circuit are the main supply (mains transformer, bridge rectifier and capacitor C5) and two switches, S3 and S4, which offer the possibility of 'manual override': they can be used to initiate and terminate the charging cycle. Since the basic principles have been explained above, the discussion of the complete circuit can be relatively brief. S2 is the 'start' button. Operating this pushbutton sets FF1 — the Q-output of this flip-flop goes 'high'. T3 and T2 are turned on, discharging the nicad cell(s) via a 'fat' resistor, R7. Simultaneously, D2 lights.

After a certain time, the cell(s) will be discharged to the point where the voltage across it (or them) drops below the level preset by means of P1. The latter voltage and the voltage across the cell(s) are applied to the two inputs of a comparator, IC1. Normally speaking, the voltage across a 'fully' discharged nicad cell is taken to be approximately 1 V. For the discharge cycle to be

terminated at the correct point, the voltage preset by P1 should be set at the number of series-connected nicad cells times 1 volt.

Assuming that P1 has been set correctly, the output of the comparator will switch from 'high' to 'low' when the cell(s) are fully discharged. Via N1, flip-flop FF1 is reset; its Q output goes 'low', turning off T3 and T2 and terminating the discharge cycle. Simultaneously, a differentiating network (C2/R12) resets FF2 via N2. The Q output of this flip-flop goes high, turning on T4; as a result, the current source (T1) comes into play. The nicad cells are charged, and D1 lights. Note that a green LED *must* be used for D1: this diode is not only used as indicator, it also provides the reference voltage for the current source. The voltage drop across green LEDs is higher than that for red LEDs (2.4 V as opposed to 1.6 V) and the specified values for R1 and R2 are only accurate for the higher voltage.

When FF2 changes state, initiating the charging cycle, its Q output goes 'low'. This enables the timer. The timer circuit is the essence of simplicity: it consists of a clock generator — N5, N6, an inverter incorporated in IC3 and a few passive components — and a frequency divider (IC3). The frequency of the clock generator can be adjusted, by means of P2, until the correct timing intervals are obtained.

Only a few components in the circuit remain to be discussed. R13 and C3 are included to reset the two flip-flops

Parts list

Resistors:

R1 = 33 Ω
 R2 = 10 Ω
 R3 = 2k2
 R4, R9, R12 = 10 k
 R5 = 1 k
 R6 = 120 Ω
 R7 = 10 μ /5 watt
 R8 = 390 Ω
 R10, R11, R13 = 22 k
 R14 = 10 M
 R15 = 3M9

Capacitors:

C1 = 10 μ /16 V
 C2 = 1n5
 C3 = 4 μ /7/16 V
 C4 = 560 n
 C5 = 1000 μ /16 V

Semiconductors:

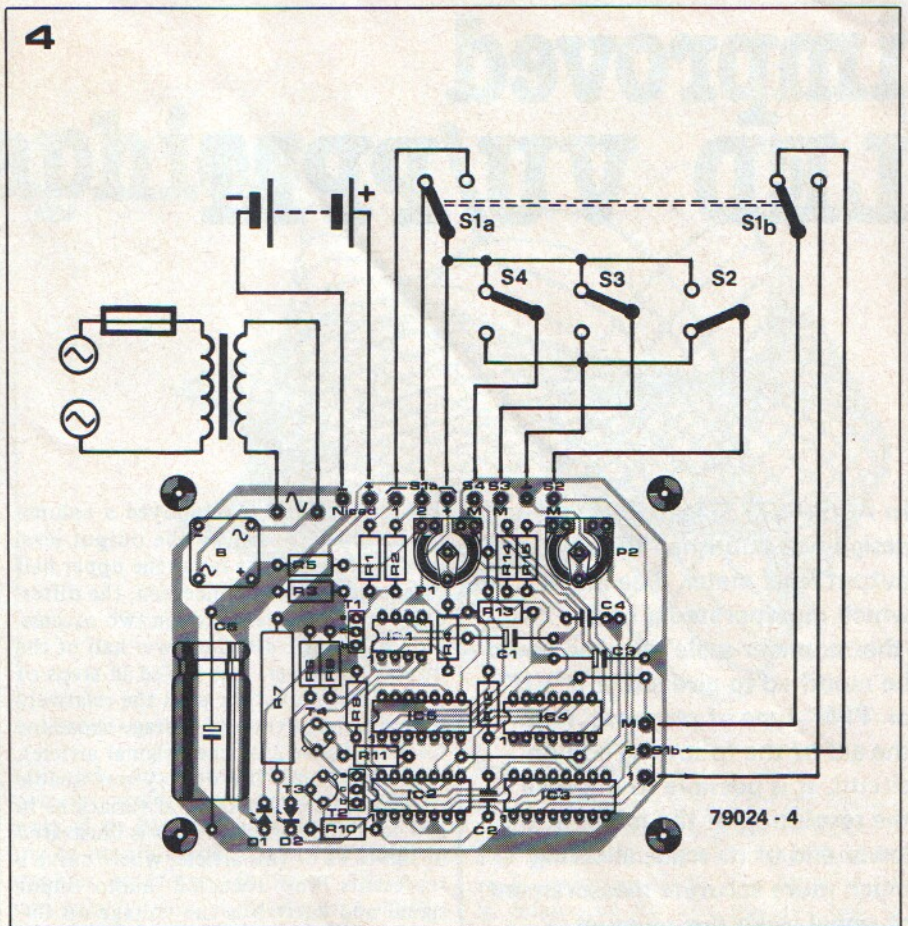
T1 = BD 140/BD 136
 T2 = BD 139/BD 135
 T3, T4 = BC 547
 D1 = LED green
 D2 = LED red
 IC1 = 741
 IC2 = CD 4013
 IC3 = CD 4060
 IC4 = CD 4093
 IC5 = CD 4023

Sundries:

P1 = 1 k preset
 P2 = 1 M preset
 S1 = double-pole, double throw
 S2, S3, S4 = single-pole pushbutton
 B = bridge rectifier B40C800
 F = 100 mA fuse
 Tr = 9 V/250 mA mains transformer

Figure 3. Printed circuit board and component layout for the nicad charger (EPS 79024). The only component mounted 'off-board' is the mains transformer.

Figure 4. This wiring diagram clearly illustrates the connections from the p.c. board to the various switches, the transformer and the nicad cell(s).



when power is initially applied – the circuit simply works, without first having to fiddle with all sorts of reset buttons. Resistor R3, tucked away in the top right-hand corner of the circuit, is the 'trickle-charger': even after T1 has cut off it continues to supply a small charging current into the nicad cells, in order to keep them 'topped up'.

Finally, the switches. The charging current is selected by means of S1a; with the values given for R1 and R2, the current is 50 mA in position 1 of this switch and 150 mA in position 2. To avoid mishaps, a second pole of the same switch selects the corresponding charging time: the two positions of S1b correspond to 14 hours and 3½ hours, as mentioned earlier. Normal operation is initiated by operating the start button, S2; as explained, this actually initiates the discharge cycle. If one is in a hurry, operating S3 initiates the charge cycle without first discharging the cells. At all times, both the charge and discharge cycles can be stopped by operating S4.

Construction and operation

The design for a printed circuit board and the corresponding component layout is shown in figure 4. The connections to the external components – mains transformer, switches and nicad cell(s) – are given in figure 5.

Basic construction is fairly straightforward, therefore; initial calibration and normal operation is hardly more complicated. There are only a few points to watch:

- As stated, from 1 to 6 cells (connected in series) can be charged at a time, provided P1 is set correctly: 1 volt per cell. Note however, that D2 will not light during the initial discharge cycle if only one cell is connected. Furthermore, if more than one cell is to be charged they should all initially be discharged to approximately the same degree; if they have all been used in the same item of equipment, this will normally be the case. In case of doubt, it is advisable to first discharge each cell (or set of cells from the same unit) individually until the green LED just lights.
- If other charging currents are required, the values of R1 and/or R2 must be modified accordingly. The charging current (in amps) is equal to 1.6 V (the voltage drop across D1 minus the voltage drop across the base-emitter junction of T1) divided by the value of R1 or R2. If the unit is to be used for rapid charging of 1.2Ah nicad cells (charging current approximately 360 mA), T1 should be provided with a cooling fin.
- If desired, accurate calibration of the timer circuit can be carried out by means of P2. However, there is no real harm in merely setting it in the mid-position... Perfectionists may consider this rather less than satisfactory, whereas they may also be rather reluctant to sit out the complete timing cycle of 3½ or even 14 hours. No problem: there is yet another alternative. Monitor the Q4 output of IC3 (pin 7) with a multi-

meter and operate the start button (no nicad cells connected). If this output swings positive after 45...50 seconds, P2 is set correctly.

- One final – important – point: since this circuit first discharges and then charges the cell(s), no protection diodes could be incorporated at the output. Care should therefore be taken never to connect the cell(s) the wrong way round; furthermore, if they are left connected to the charger after the charging cycle has been completed, the charger must remain switched on. Otherwise the cell(s) would be 'trickle-discharged' through R3, R5 and P1!

improved LED VU/PPM

In April 1977 (Elektor 24) a design was published for an audio output level meter. The meter, which incorporated a LED 'thermometer-scale' display, could be modified to give either a 'VU' or 'PPM' type of response. With the aid of the following add-on circuit, it is possible to improve the resolution of the meter at the lower end of its scale, allowing much more accurate measurement of signal levels during quiet passages of music and speech.

J.M. Heuss

The original meter employed a column of 20 LEDs to display the output level of each channel. As far as the upper half of the display was concerned, the difference in signal level between two successive LEDs was 1 dB; the lower half of the display, however, was scaled in steps of 5 dB. In conjunction with the relatively long discharge time of storage capacitor C4 (see figure 2 of the original article), this meant that the display was unable to register small and rapid variations in low level input signals. This is illustrated in figure 1a of this article, where curve a represents the rectified audio input signal and curve b is the voltage on C4, i.e. the voltage which is actually displayed on the LEDs.

However, if one arranges that, as soon as the voltage on C4 drops below a preset reference voltage U_{ref} the capacitor's decay time constant is reduced, the voltage across this capacitor will track rapid variations in the rectified input voltage much more closely. This process is illustrated in figure 1b, and in fact

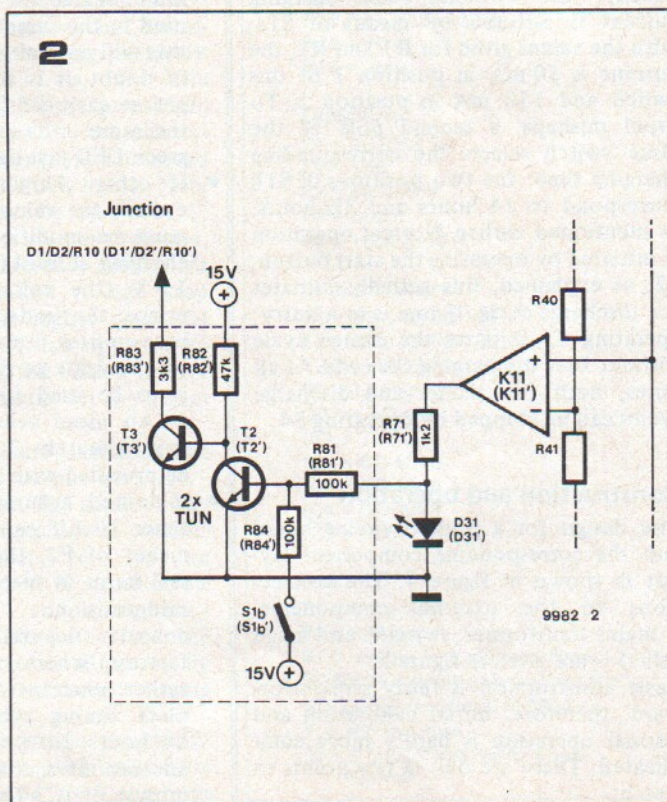
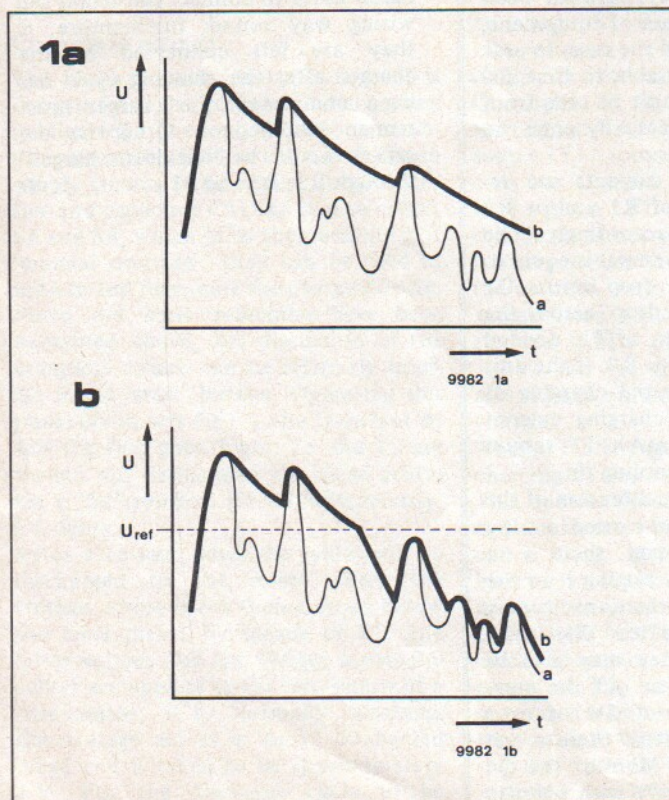
represents the basic function of the circuit described here.

The additional components required to improve the meter's response are shown within the dotted lines in the circuit diagram of figure 2. This diagram is for one channel only and should of course be duplicated for stereo applications. Comparator K11 (K11'), the potential divider resistors and LED are as shown in figure 5 of the original article.

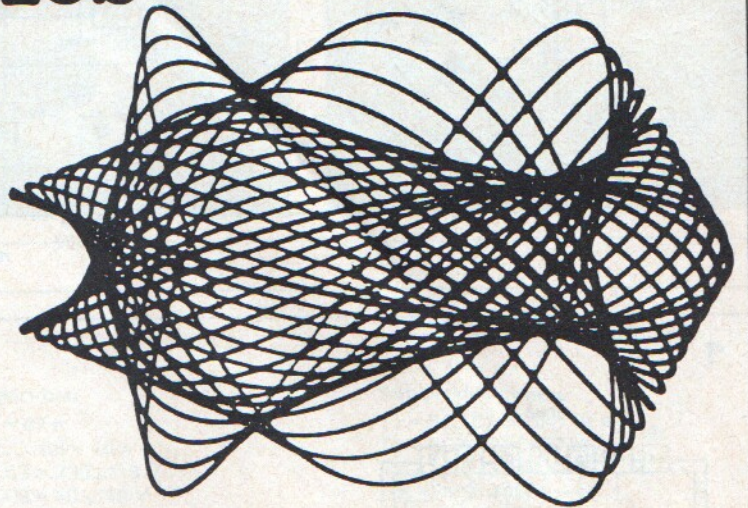
The actual operation of the circuit is straightforward. When the voltage on C4 (which is applied to the non-inverting input of K11) falls below U_{ref} , LED D31 is extinguished and transistor T2 is turned off. T3 is then turned hard on and R83 appears in parallel with C4. This reduces the discharge time constant of C4, with the result that, at low input levels, the voltage across this capacitor follows fluctuations in the rectified audio signal much more accurately.

If the 'peak memory' switch S1 is included, it should be fitted with a second pole, S1b (for stereo applications two extra poles will obviously be required).

It is worth pointing out that the frequency response and the 'ballistics' (attack-decay times) of the meter can be improved by replacing the 741 op-amps with more modern and faster devices. For example, if less than unity gain is required, an LF356 can be used for IC1. If a gain greater than 5 is desired, then an LF357 is also suitable (see original article regarding the choice of values for R2 and R3). As far as IC2, IC3 and IC4 are concerned, an LF356 will prove eminently suitable. If an LF356 is also used for IC5, then the offset adjustment can be dropped (i.e. potentiometer P2 omitted).



oscillographics on board



The Oscillographics circuit published in September 1978 has proved to be a highly popular design, and several readers have asked for a printed circuit board. For the benefit of those who have not seen the original article, the basic principles of the circuit are repeated here in brief.

Although an oscilloscope is an extremely useful instrument, it spends most of its life 'displaying' a horizontal line or even a blank screen. The Oscillographics generator, shown in figure 1, can remedy this: it produces a multitude of fascinating and attractive geometrical patterns on the screen of the scope. The patterns are actually so-called 'Lissajous' figures: two resonant circuits (IC2/IC3 and IC5/IC6) are triggered at regular intervals by a multivibrator (IC1), producing two damped sinusoidal outputs. These are fed to the X- and Y-inputs of the scope, producing an intriguing display.

Both the frequency and the decay rate of each sinusoidal output are independently variable (by means of P1/P3 and P2/P4, respectively), so that a virtually infinite number of different patterns can be obtained. An 'intensity' output is provided (Z or \bar{Z} , depending on the type of scope), which can be used to blank the spot on the screen during triggering of the resonant filters.

It is also possible to modulate either (or both) oscillator signal(s) by an external signal applied to the M_x and M_y inputs, so that the patterns are continuously changing. Various types of (low frequency) modulation signal can be used: squarewave, triangle, ramp, etc., with varying amplitude and frequency. The only constraint upon the modulation signals is that they should not contain a DC component (in other words, they should be AC coupled), since otherwise there is the possibility that part of the pattern will be off the screen. The maximum amplitude of the modulation signal is $15 V_{pp}$. If desired, the values of R13 and R20 (and/or R14 and R21) can be altered if the effect of the modulation signal is more or less noticeable than was intended.

Power supply

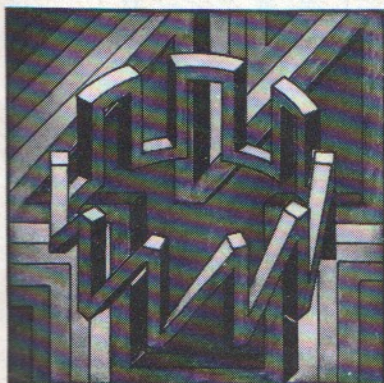
A suitable supply circuit for the Oscillographics generator is given in figure 2. The positive supply rail is stabilised by an IC regulator (IC9). The negative rail is referenced to the positive rail by means of an opamp (IC10) and a transistor (T2). This is an interesting little circuit, which can prove useful in many other applications: the voltage on the negative rail is maintained at such a level that the voltage at the R24/R25 junction is 0 V. Since R24 is equal to R25, the negative output voltage must be equal and opposite to the positive output voltage. In other words, if the positive voltage is varied, the negative voltage will vary in step — providing a variable *symmetrical* output voltage. However, in this application a fixed $\pm 5 V$ supply is required.

The printed circuit board

Although it is the *raison d'être* for this article, the p.c. board (figure 3) requires little comment. It accommodates the Oscillographics generator and the power supply, with the exception of the mains transformer.

Both Z and \bar{Z} modulation outputs are provided. These are, of course, only useful if a modulation input is provided on the oscilloscope. Depending on the type of scope, one or other of these outputs will give the desired result.

If the picture is not completely flicker-free (again, this depends on the characteristics of the scope), then the value of C1 can be reduced.



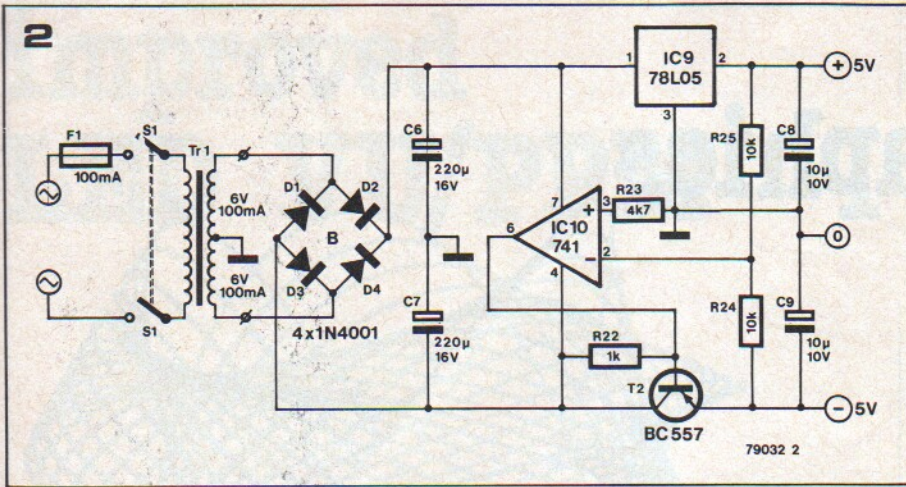
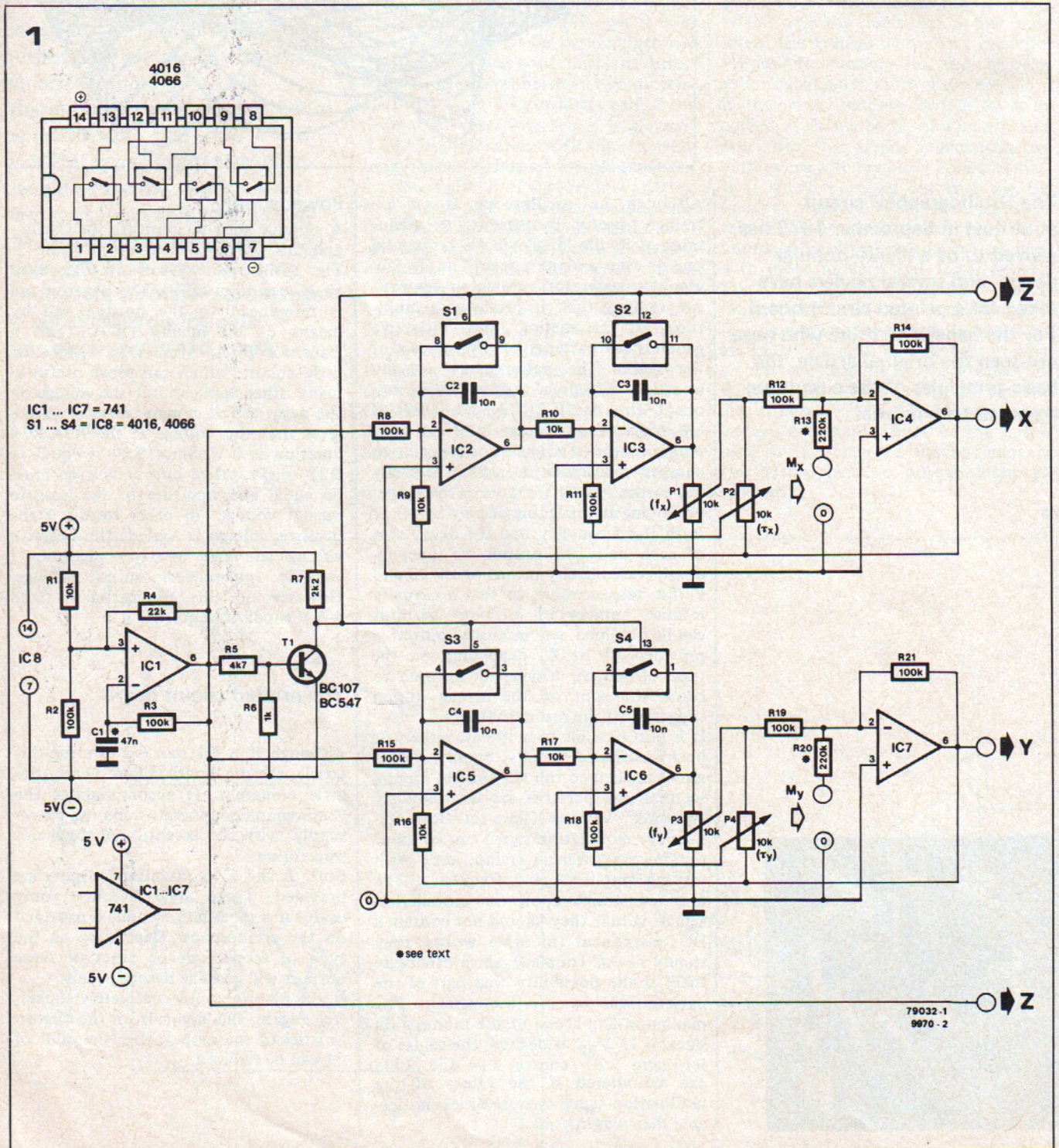


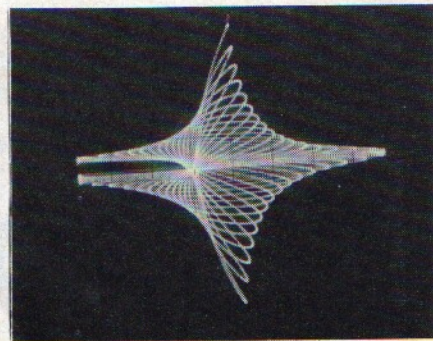
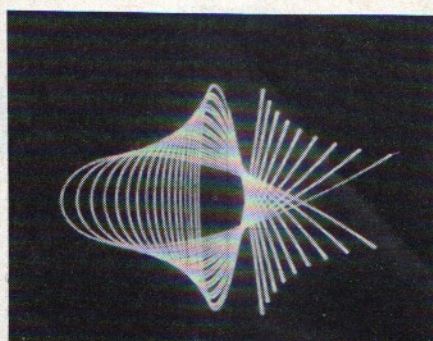
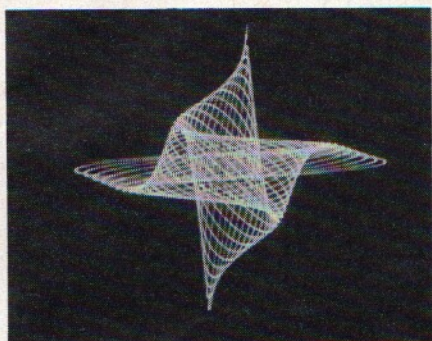
Figure 1. Circuit diagram of the Oscillographics generator.

Figure 2. A symmetrical stabilised power supply is also incorporated on the p.c. board.

Figure 3. The printed circuit board for the Oscillographics generator (EPS 9970).



* see text



Parts list

Resistors:

R1,R9,R10,R16,R17,R24,
R25 = 10 k
R2,R3,R8,R11,R12,R14,R15,
R18,R19,R21 = 100 k
R4 = 22 k
R5,R23 = 4k7
R6,R22 = 1 k
R7 = 2k2
R13,R20 = 220 k
P1 . . . P4 = 10 k lin.

Capacitors:

C1 = 47 n
C2 . . . C5 = 10 n
C6,C7 = 220 μ /16 V
C8,C9 = 10 μ /10 V

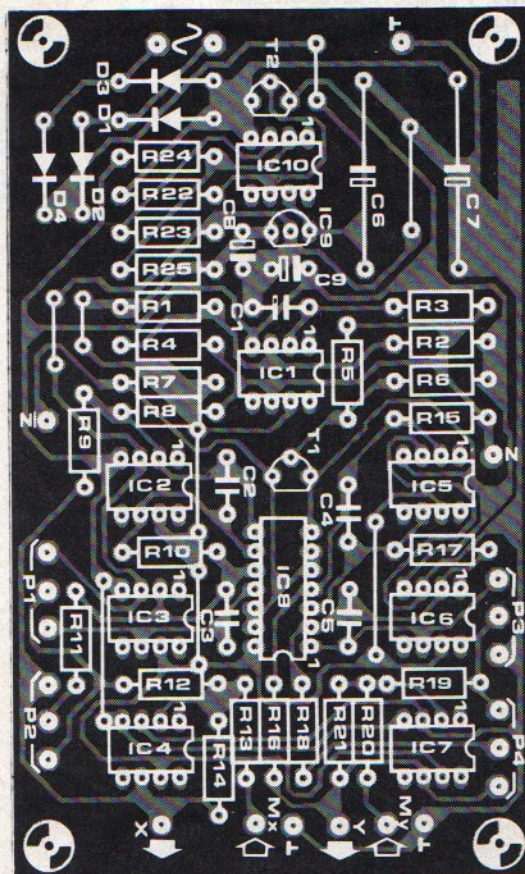
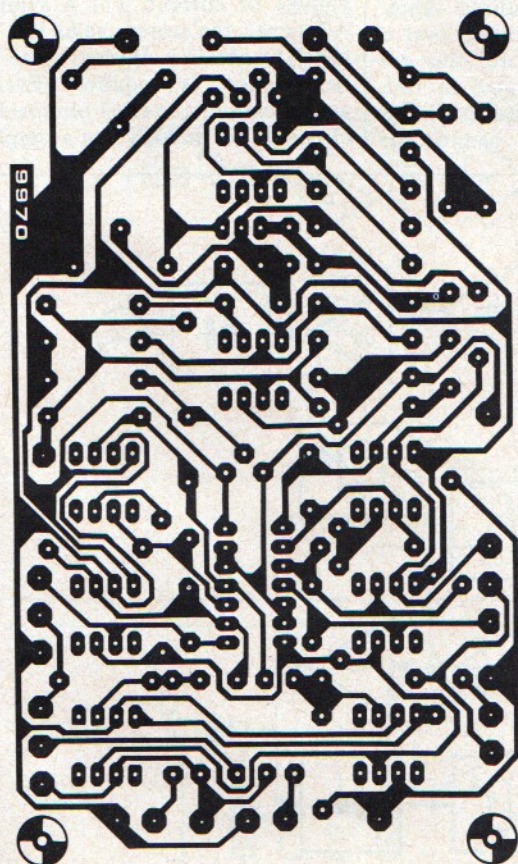
Sundries:

Tr1 = 2 x 6 V/100 mA mains
transformer
S1 = double-pole mains switch
F1 = 100 mA fuse

Semiconductors:

T1 = BC 107,BC 547 or equ.
T2 = BC 177,BC557 or equ.
IC1 . . . IC7,IC10 = 741
IC8 = 4016,4066
IC9 = 78L05A(C)Z
D1 . . . D4 = 1N4001

3



AC millivoltmeter and signal squirt

It is often useful to be able to measure low-level audio signals. However, the lowest AC range on most multimeters is usually several volts (f.s.d.) and — to make matters worse — it presents a relatively low load impedance to the circuit under test. A 'preamplifier for multimeters' can solve this problem.

Since a suitable preamp should have a high input impedance and a sufficiently large bandwidth, it seems logical to use FET-input opamps. Furthermore, since a single IC contains four of these opamps it is a relatively simple matter to include a 'signal squirt' on the same board.

The circuit described here is quite useful in its own right. The output is not only suitable for driving a multimeter — a normal panel meter can be used instead. It is also possible to use it in conjunction with the 'Universal Digital Meter' described elsewhere in this issue. Furthermore, the current consumption is so low that a 9 V battery supply can be used, thereby retaining the flexibility and portability of the multimeter.

When measuring very small AC voltages, it is important to ensure that the measuring instrument does not present an excessive load to the circuit being tested. This requirement can be fulfilled quite easily by using FET-input opamps. A further requirement is that the frequency of the signal being measured has no effect on the measured value. This is only possible, of course, over a limited bandwidth; therefore, this requirement can best be stated in two parts: the frequency response should be 'flat' within the specified bandwidth,

and the bandwidth should be as large as possible. Based on these primary requirements, and bearing various secondary requirements in mind (price, reliability, availability of components), it was decided to use the Texas Instruments IC type TL084 — a quad FET-input opamp.

The upper section of figure 1 is the block diagram of the AC millivoltmeter. An input capacitor blocks any unwanted DC voltages, after which the remaining AC signal can be amplified to a reasonable level. So far so good, but amplifying the signal is not enough. A normal panel meter, or a multimeter switched to its most sensitive DC voltage or current range, tends to display the average value of the applied voltage or current. For a symmetrical AC signal, the average value is 0 V. . . In order to obtain a display, some kind of rectification is required. Even after amplification, the level obtained in this circuit is not so high that a simple diode

1

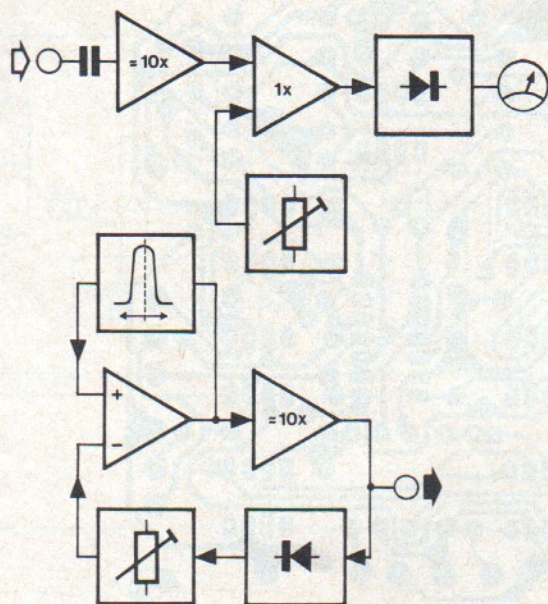
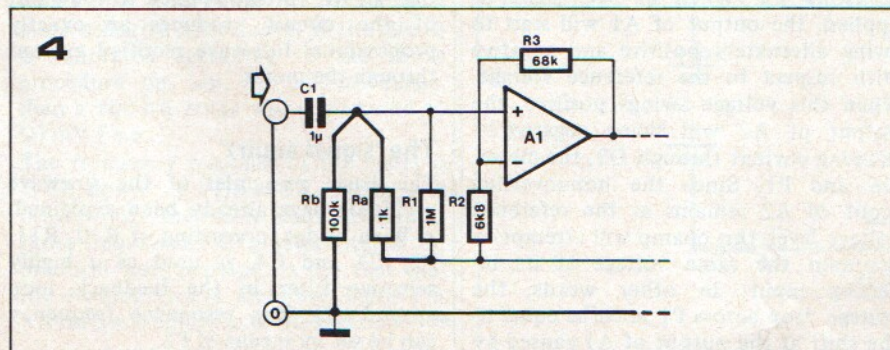
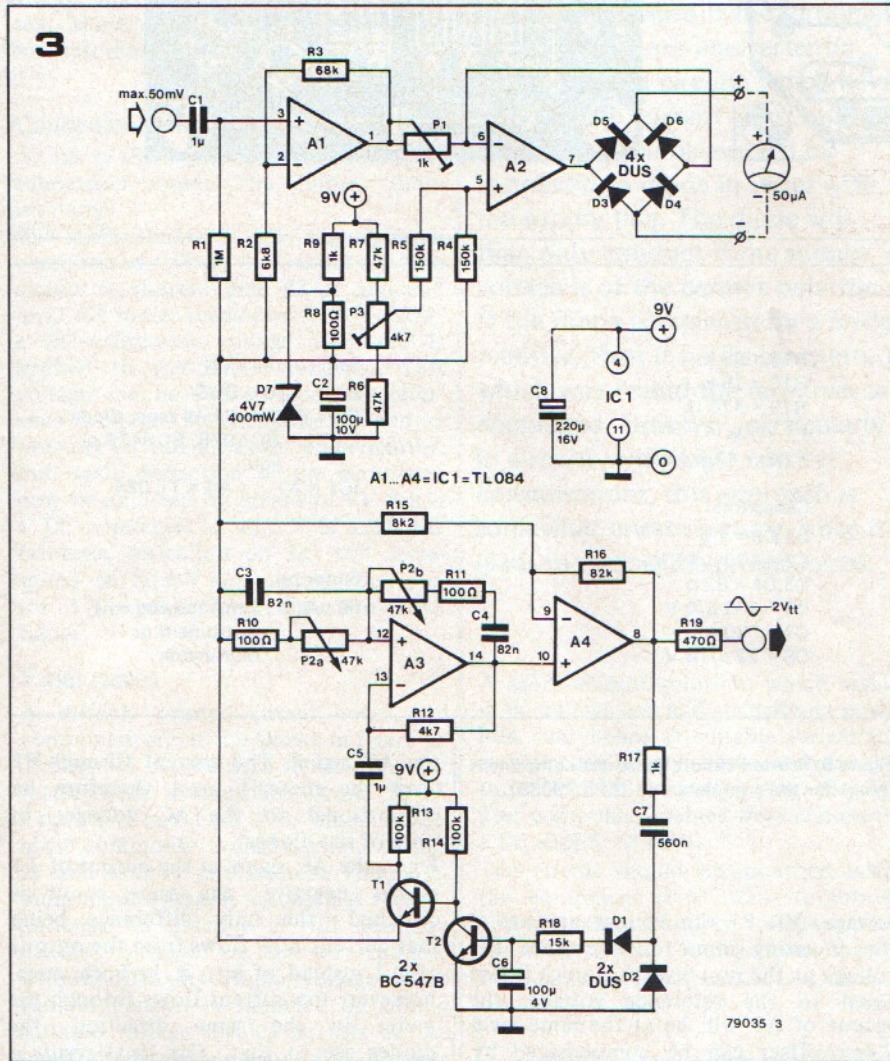
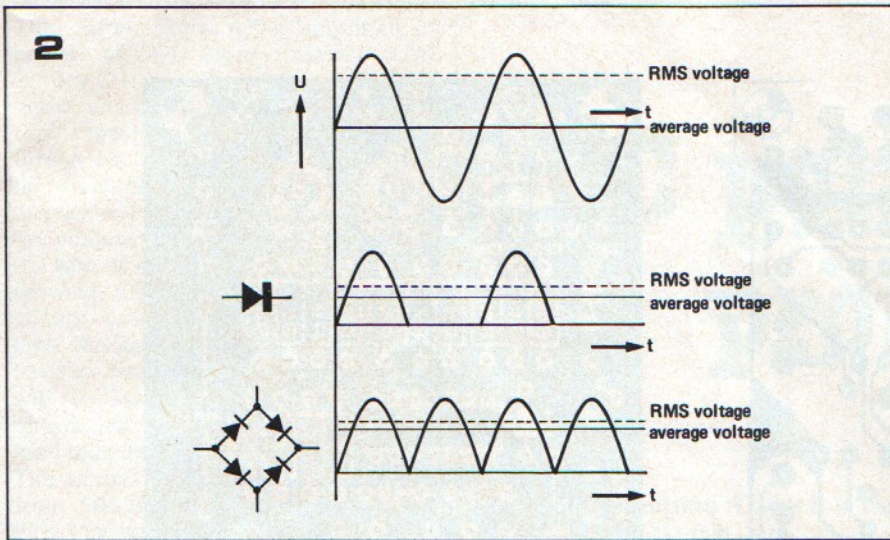


Figure 1. Block diagram of the millivoltmeter (upper section) and of the signal squirt (lower section).

Figure 2. The average value of a full-wave rectified sine wave is higher than that of a half-wave rectified signal. Furthermore, for the full-wave rectified sine wave, the RMS value is 1.11 x the average value.

Figure 3. Complete circuit diagram. As in the block diagram, the upper section is the millivoltmeter and the lower section is the signal squirt.

Figure 4. For calibration purposes, the R1/C1 junction must be offset by 45 mV (DC). This can be achieved by temporarily adding Ra and Rb, as shown.



in series with the meter will suffice – the forward voltage drop across the diode would swamp the signal. Since there are plenty of opamps available in the same IC, the solution is to incorporate the diode(s) and the meter in the feedback loop around an opamp – the forward voltage drop across the diode is then compensated for automatically.

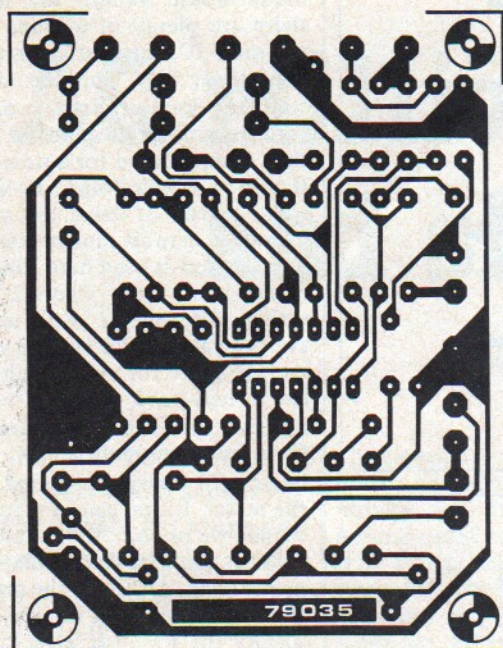
If a job's worth doing, it's worth doing well: instead of using half-wave rectification, as in most multimeters, full-wave rectification is used here. One advantage is apparent from figure 2. As stated earlier, the meter will measure the average value of an applied voltage. The average value for an AC voltage is zero; for a half-wave rectified voltage it is positive, so it can be measured; however, for a full-wave rectified AC voltage it is larger still – giving a higher reading on the meter. Extra 'gain' for free!

While we're on the subject of AC voltages, a further point is worth mentioning. Although the meter displays the average value, it is more common to specify the RMS (or 'effective') value of an AC signal. This is done to keep electronics simple. . . For DC, power (P) in Watts is equal to the voltage, squared, divided by resistance. For the same formula to be valid for AC, the RMS value of the AC voltage must be used. The abbreviation 'RMS' stands for 'Root Mean Square', which is exactly what it is: the root out of the sum of the average values (mean) of the squares of the momentary voltages. This may sound quite complicated, but for the moment the only important thing to know is that the RMS value of a sine wave is equal to 0.707 x the peak value. The meter will display the average value, and for a sine wave this is 0.636 x the peak value. The ratio between RMS and average values is therefore 1.11, and when calibrating the meter the scale will have to be offset by this factor. This is no problem, as will be seen.

So far, only two opamps have been used; however, the IC contains four. It seems a good idea to use the remaining two for a simple signal squirt – another item of test equipment that can prove quite useful to the home constructor.

The lower section of the block diagram (figure 1) refers to this 'signal squirt'. It is little more than a conventional 'Wien bridge' oscillator. The Wien bridge proper is shown as a selective filter in the feedback loop around one opamp. Provided the total loop gain is greater than unity (no problem with opamps), the circuit will oscillate. The sinusoidal output is amplified by the last remaining opamp, to provide a 2 V_{pp} sine wave at the output. In order to obtain a 'clean' sine wave, the loop gain around the first opamp should be almost exactly unity. To avoid critical calibration procedures, this adjustment is performed automatically: the output signal is rectified and fed back to a suitable control point.

5



Parts list:

Resistors:

R1 = 1 M
 R2 = 6k8
 R3 = 68 k
 R4 = 150 k
 R5 = 150 k
 R6, R7 = 47 k
 R8, R10, R11 = 100 Ω
 R9, R17 = 1 k
 R12 = 4k7
 R13 = 100 k
 R14 = 100 k
 R15 = 8k2

R16 = 82 k
 R18 = 15 k
 R19 = 470 Ω
 P1 = 1 k
 P2ab = 47 k (stereo)

Capacitors:

C1, C5 = 1 μ
 C2 = 100 μ /10 V
 C3, C4 = 82 n
 C6 = 100 μ /4 V
 C7 = 560 n
 C8 = 22 μ /16 V

Semiconductors:

D1 ... D6 = DUS
 D7 = 4V7/400 mW zener diode
 T1, T2 = BC 107B, BC 547B or
 equ.
 IC1 = A1 ... A4 = TL 084

Sundries:

50 μ A ... 1 mA moving coil
 instrument or
 multimeter

AC millivoltmeter circuit

The complete circuit is shown in figure 3; the upper half is the AC millivoltmeter. A reference voltage is derived from the 9 V battery by means of R8, D7, R9 and C2. This voltage is applied, via R1 and R2, to both inputs of the first opamp, A1. R1 determines the input impedance (approx. 1 M). The gain of A1 is determined by the ratio of R3 to R2 — or, to be more precise, by the ratio (R3 + R2): R2 — in this case, a gain of x11 is obtained.

The output from A1 is fed to A2 via a preset potentiometer (P1); the latter can be used for full-scale calibration. The non-inverting input of A2 is connected to the reference voltage across C2 and a further (small) offset compensation is introduced via R6, R7 and P3.

Four diodes, D3 ... D6, provide full-wave rectification. This part of the circuit operates as follows. Under quiescent conditions (i.e. without any signal applied to the input) the output of A1 will be equal to the reference

Figure 5. Printed circuit board and component layout for the complete unit (EPS 79035).

voltage. Via P1 this voltage appears at the inverting input of A2; since the voltage at the non-inverting input is also equal to the reference voltage, the output of A2 will be at the same level — any offset can be compensated by adjusting P3. When an AC signal is applied, the output of A1 will start to swing alternately positive and negative with respect to the reference voltage. When this voltage swings positive, the output of A2 will swing negative — drawing current through D3, the meter, D6 and P1. Since the non-inverting input of A2 remains at the reference voltage level, this opamp will attempt to maintain the same voltage at its inverting input; in other words, the voltage drop across P1 must be equal to the shift at the output of A1 caused by

the AC signal. The current through P1 (and the meter!) must therefore be proportional to the AC voltage — in spite of the diodes!

When the AC signal at the output of A1 swings negative, the same result is obtained — the only difference being that current now flows from the output of A2 instead of into it. In both cases, however, the current flows through the meter in the same direction — the diodes see to that. The final result is that an AC voltage applied to the input of the circuit produces an exactly proportional full-wave rectified current through the meter.

The 'signal squirt'

The basic principles of the sinewave oscillator have already been explained. A Wien bridge, consisting of R10, R11, P2, C3 and C4, is used as a highly selective filter in the feedback loop around A3. The resonance frequency can be set by means of P2.

The output from A3 is amplified by means of A4 (approximately $\times 11$). Diodes D1 and D2 rectify the output signal, charging C2; as the voltage across this capacitor rises, T2 is gradually turned on. This, in turn, causes T1 to be turned off; effectively, its 'resistance' increases. Since the 'resistance' of T1 (in conjunction with R12) determines the gain of A3, this causes the gain to be reduced. Effectively, then, if the output voltage tends to rise above a certain level the gain is reduced; if the output tries to drop below that level the gain will be increased. There is only one option left for the circuit: the output level must remain constant. And it does. The output frequency can be adjusted from 500 Hz to 25 kHz (by means of P2). The output level is approximately 2 V_{pp}, and protection against inadvertent short circuits is provided by the simplest means possible: a resistor, R19.

Calibration procedure

As far as the signal squirt is concerned, calibration couldn't be simpler: there isn't any.

The millivoltmeter is only slightly more complicated. First, the input to the circuit is shorted and P3 is adjusted until the meter reads exactly 0 V. Now, a DC calibration voltage of 45 mV is applied to the R1/C1 junction. This voltage can be derived from the reference voltage by temporarily adding resistors Ra and Rb as shown in figure 4. Full scale deflection of the meter can now be adjusted by means of P1. Since a DC reference of 45 mV is used, the full-scale deflection on AC will correspond to 50 mV - remember that factor 1.11 between average and RMS values!

Final notes

A suitable printed circuit board and component layout are shown in figure 5. The circuit can be used to drive any DC meter with a sensitivity from 50 μ A f.s.d. to 1 mA f.s.d. - in other words, most commonly available panel meters as well as most multimeters. The maximum input voltage is specified as 50 mV, although in practice it will normally handle voltages of up to 100 mV without difficulty. Higher voltage ranges can, of course, be included by adding suitable voltage divider circuits at the input. On the other hand, a multimeter offers the possibility of obtaining a more sensitive instrument: if the circuit is calibrated according to the above procedure on, say, the 500 μ A range, then a 100 μ A range will correspond to 10 mV f.s.d.

The frequency response of the meter is '3 dB down' at 1 Hz and 125 kHz - in other words, the meter reads 30% low at those frequencies. Of greater interest for practical use, perhaps, is the fact that the reading (for a sine wave input!) is within 5% from 3 Hz to 40 kHz. ■

DC polarity protection

Electronic equipment which is fed from an external DC voltage can easily be damaged if the terminals of the supply are inadvertently transposed. In circuits which have only a small current consumption this danger can be averted by connecting a diode in series with the supply line. The diode will then only conduct if the supply voltage is of the correct polarity. If the diode is replaced by a bridge rectifier, then it no longer matters which way round the terminals are connected. However, particularly in circuits with larger current consumptions, this approach is somewhat unsatisfactory, since it leads to noticeable power losses.

A more elegant solution, which results in no voltage loss and virtually no power loss, and hence is suitable for circuits carrying relatively large currents, is shown in the accompanying diagram. The component values were chosen for a DC supply of 12 V.

The circuit should be mounted inside the equipment it is meant to protect and the external supply voltage connected to terminals 1 and 2. Assuming the

polarity of the supply is correct, once the on/off switch, S1, is closed, the relay, Re, will pull in, causing two things to happen. The normally closed contact, re1, will open, reducing the relay current through R1. Since the drop-out current is less than the pull-in current, assuming R1 is the correct value, relay Re will remain energised. This little trick reduces the dissipation in the protection circuit.

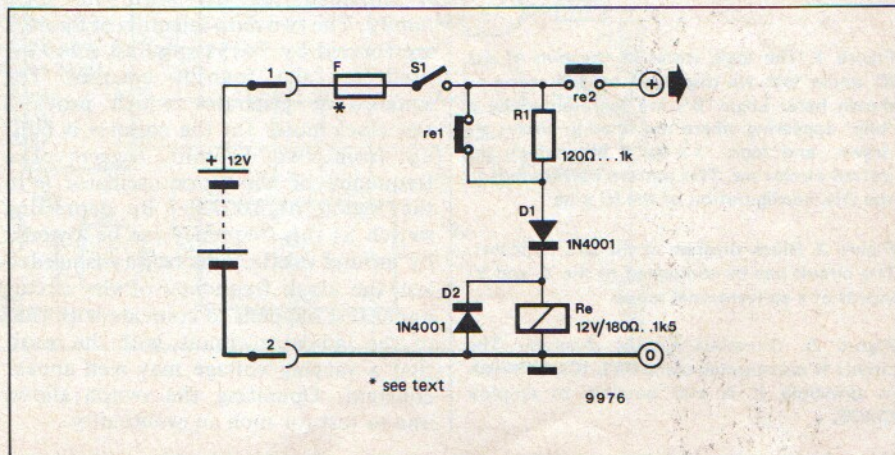
Secondly, the normally open contact, re2, will close, thereby applying power to the rest of the equipment.

However, if the terminals of the supply are transposed, diode D1 will be reverse-biased, preventing the relay from being pulled in. Diode D2 suppresses any inductive voltages produced when the relay coil is de-energised.

If there is a fuse in the supply line of the equipment, then it is recommended that this be inserted between the supply and the protection circuit, so that it will blow should a fault occur in the latter. The current consumption of the protection circuit is so small compared with that of the equipment it guards that there is no need to alter the rating of the fuse.

The values of the components in the circuit can of course be modified to suit other supply voltages. One should bear in mind that the pull-in voltage of the relay, Re, should be the same as the supply voltage.

The value of R1 will depend to a certain extent on the type of relay used, and is best determined experimentally. ■



sixteen logic levels on a scope

R. Rastetter

When troubleshooting digital circuits it is often useful to be able to examine the logic level of a number of signals simultaneously. For example, one might wish to look at the logic state of all the pins of a dual-inline IC. To this end there are a number of commercially available test clips, which, via rows of LEDs, indicate which pins are at logic '1'. If one has access to an oscilloscope, a similar result can be obtained with the aid of the circuit described here.

The DIL-indicator is used in conjunction with a 16-pin test clip, which is attached to the IC being examined. From the sixteen input signals provided by the test clip the circuit generates two new signals, namely the X- and Y- input signals for the scope. Figure 1 illustrates how the logic levels are displayed on the scope screen: i.e. in the same pattern as the pins of the IC. The 'high' logic levels are displayed slightly higher on the screen than the 'low' logic states, both being represented by a white 'blip'. The block diagram of the DIL-indicator circuit is shown in figure 2. With the aid of the two data-selectors the sixteen logic signals on the test clip are scanned one at a time. Open inputs, for instance when testing 14-pin ICs, are represented as being at logic '1'. Both data selectors are clocked by a four-bit binary counter, which in turn is controlled by a separate clock generator. The counter also clocks a digital-analogue converter, the output of which provides a staircase waveform with 8 'steps'. The staircase voltage forms the X-input of the scope and determines the horizontal position of each spot on the screen. The vertical position of the spots are controlled by the least significant bit of the counter and by the logic state of the signal selected by the data-selector, i.e. the Y-input of the scope is obtained by summing these last two signals.

The complete circuit diagram of the DIL-indicator is given in figure 3. The circuit is constructed using TTL ICs and is intended for use with this logic family. The two data-selectors of figure 2 are formed by 74151's, whilst a 7493 is used for the four-bit counter. The squarewave generator which provides the clock pulse for the counter is built up from two Schmitt triggers. The frequency of the clock oscillator is in the region of 70 kHz. By depressing switch S1 this frequency can be lowered by around 3 kHz. This facility is needed lest the clock frequency of the circuit under test happens to coincide with that of the indicator circuit, with the result that a varying voltage may well appear constant. Operating the switch allows one to test for such an eventuality.

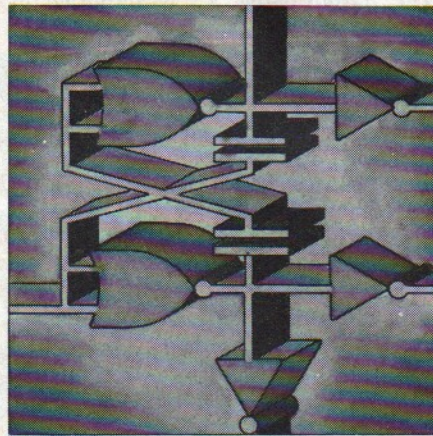
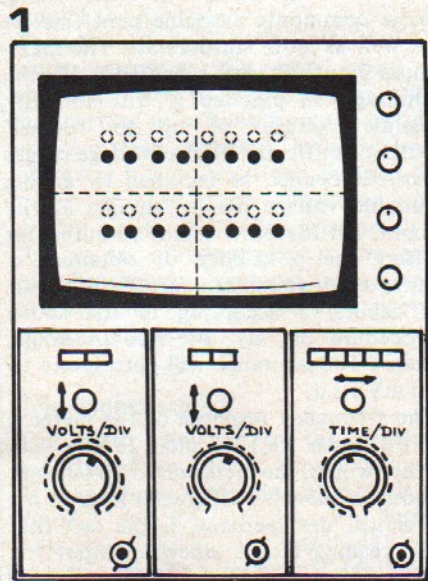


Figure 1. The logic states at the pins of the IC under test are displayed on the scope as shown here. Logic '0's are represented by a 'blip' appearing where the filled-in circles are drawn, and logic '1's by a blip where the dotted circles are. This pattern corresponds to the DIL-configuration of the IC pins.

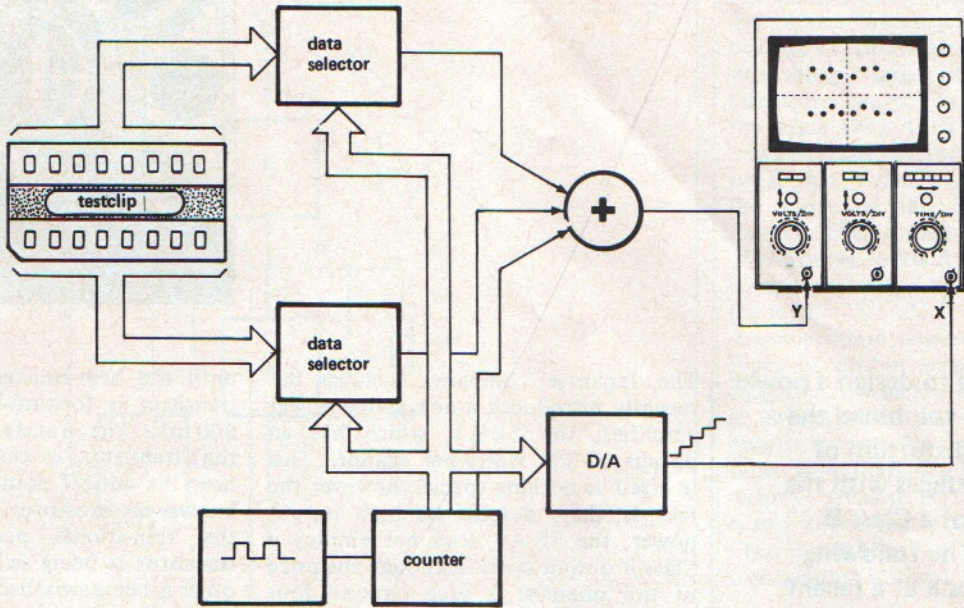
Figure 2. Block diagram of the DIL-indicator. The circuit can be connected to the X- and Y- inputs of a conventional scope.

Figure 3. Complete circuit diagram. The circuit is constructed using TTL ICs, although in principle it is also possible to employ CMOS.

The summing circuit of the block diagram consists of nothing more than three resistors (R7, R8, R9), whilst the digital-analogue converter is scarcely more complicated; it consists of three NAND gates (N1...N3) connected as inverters and resistors R1...R6. The identical circuit can also be built using CMOS ICs, in the event that it is to be used to test CMOS circuits operating off a voltage supply other than the 5 V used here. Although it is possible to do so in principle, it is not recommended that the indicator be built with the CMOS ICs and then used to test TTL circuits. (Problems may occur with correct timing and triggering). The 5 V supply (stabilised) should be capable of providing at least 125 mA.

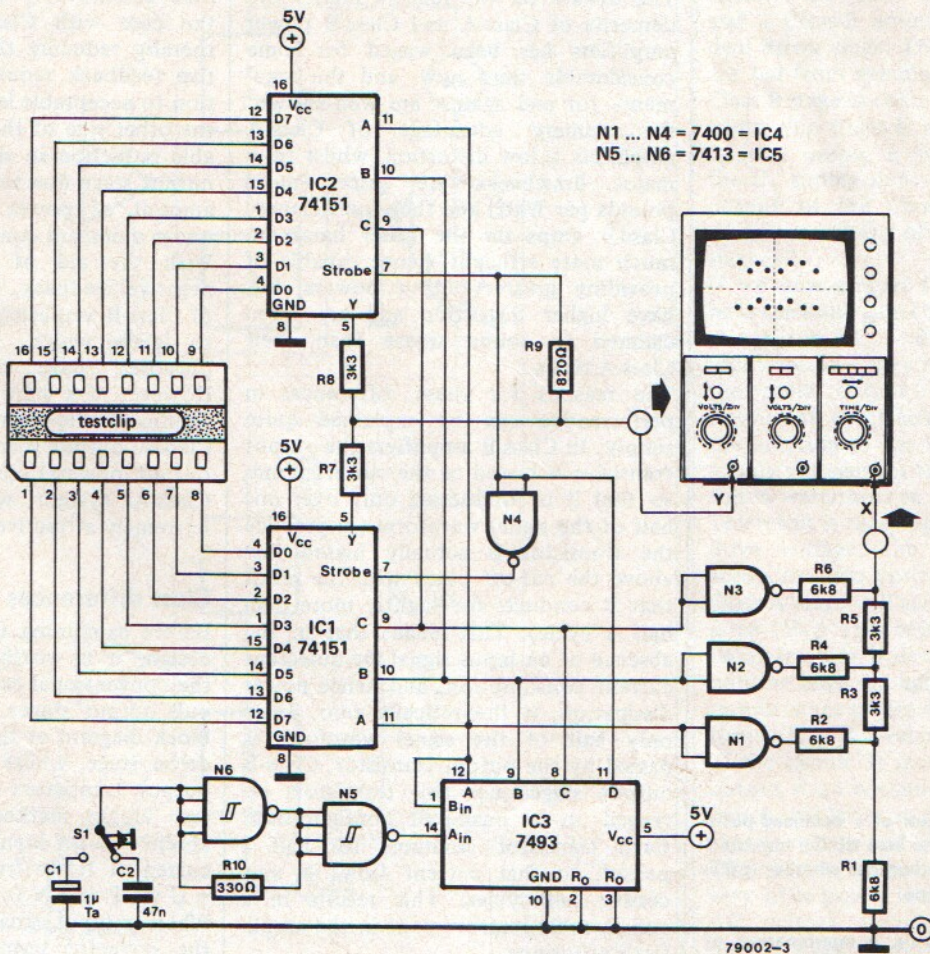


2



79002 2

3



79002-3

class tells

It would be nice to design a power amplifier which combined the inherently low distortion of Class-A output stages with the high efficiency of a Class-B configuration. The following article takes a look at a recent commercial design which appears to offer the best of these two worlds.

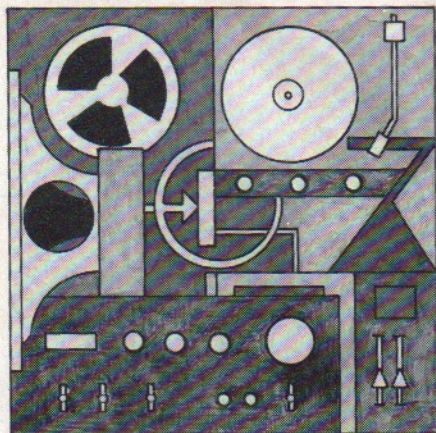
The Japanese company Technics has recently introduced a new stereo power amplifier, the SE-A1, which has an output of 350 Watts per channel. This in itself is nothing special, however the fact is that, despite its high output power, the SE-A1 does not employ a Class-B output stage. Although the price of the amplifier is such (around four thousand dollars) that it is beyond the means of most hi-fi enthusiasts, the operating principle of this new hybrid will doubtless be of interest to many readers.

Class-A v. Class-B

The debate on the relative merits and demerits of Class-A and Class-B power amplifiers has been waged for some considerable time now, and the arguments for and against are well-known: the primary advantage of Class-A amplifiers is low distortion, whilst their major drawbacks are price (more pounds per Watt) and their inefficiency. Class-B amps on the other hand are much more efficient, hence capable of providing greater output powers, but have higher distortion and are often claimed to sound worse than their Class-A rivals.

The reasons for these differences in performance can be explained quite simply. In Class-B amplifiers the output transistor is biased to the cut-off point, so that it is conducting only over one half of the signal waveform (in practice the transistor is actually biased just above the cut-off point with the result that it conducts for slightly more than half a cycle). This means that in the absence of an input signal the quiescent current consumption, and hence power dissipation, is theoretically zero. Since only half of the signal waveform is passed by the output transistor, Class-B output stages use two transistors arranged in a push-pull configuration. Each transistor conducts for half a period, so that current flows in successive half-cycles. This results in a considerable improvement in the amplifier's efficiency.

Unfortunately, however, since the transistors are biased to the cut-off point, it means that they cannot conduct fully



until the base-emitter junction of the transistor is forward-biased by at least 600 mV. The transfer characteristic of the transistor is therefore non-linear near the cut-off point, causing what is known as 'crossover distortion' during the transitional periods when one transistor is being switched off and the other is being switched on. Furthermore, since this distortion is relatively constant for any input signal level, the relative distortion of the output stage deteriorates at lower signal levels.

In a Class-A output stage, on the other hand, the transistors are biased to conduct over the entire cycle of the input waveform. The output stage is thus considerably more linear than is the case with Class-B configurations, thereby reducing the amount of negative feedback required to keep distortion to acceptable levels. Unfortunately, the other side of the coin is a considerable reduction in the efficiency of the output stage due to the fact that a large amount of power is dissipated even under quiescent conditions.

With the aid of judiciously applied negative feedback, the distortion levels of Class-B amplifiers have been reduced to levels which, to all intents and purposes, have no audible effect. However, if it were possible to virtually eliminate the inherent problems of Class-A output stages (inefficiency, low output powers), then such a modified Class-A system would represent an extremely attractive proposition.

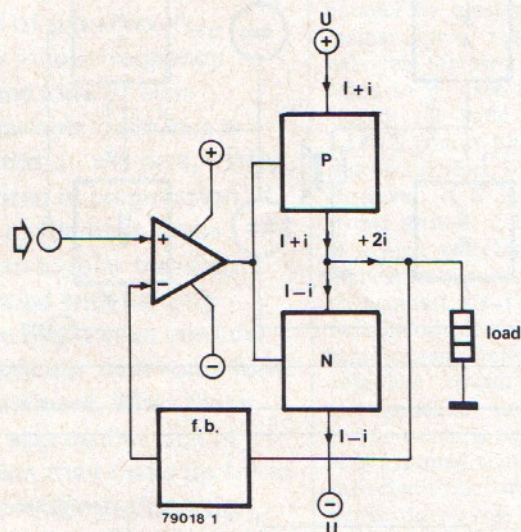
Class differences

Before examining the modified Class-A design, it is worth briefly considering the conventional configuration of push-pull output stages. The triangle in the block diagram of figure 1 represents the driver stage, whilst the complementary output transistors are depicted as the two blocks marked P and N. In the absence of an input signal, a quiescent current I flows from the positive rail + U via P and N to the negative rail - U. When an input signal is applied, however, the collector current of one of the transistors will rise by a value i , whilst the collector current of the other transistor will fall by a corresponding

Figure 1. Block diagram of a balanced push-pull output stage. The size of the current I (with respect to i) determines whether it is a Class-A or a Class-B type.

Figure 2. By employing a combination of Class-A and Class-B output stages it is possible to obtain both the low dissipation of the latter and the excellent signal-handling characteristics (low distortion) of the former.

1



amount. The difference between the two collector currents flows through the load. Thus the greater i is, the greater the voltage developed across the load.

The size of the quiescent current, I , determines which class the amplifier belongs to. In a class-A output stage I is sufficiently large that both output transistors are conducting regardless of the value of i . In a Class-B amplifier, however, the quiescent current is so small that, when a signal is applied to the bases of the output transistors, thereby driving them in antiphase, one of the transistors will soon be turned off, leaving the other to feed current into the load.

A compromise between the above two types of output stage is the Class-AB amplifier in which the quiescent current is chosen such that, below a certain output power the output stage functions as a Class-A amplifier, (i.e. both output transistors are conducting), whilst above that point it operates as a Class-B amplifier (i.e. the output transistors conduct in turn).

Class A + B

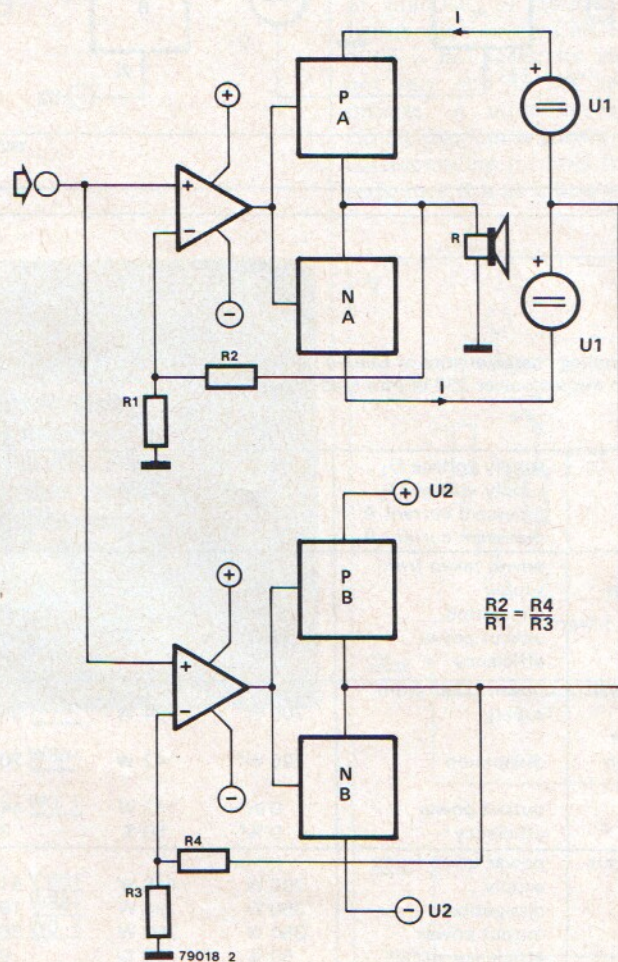
To the above three types of amplifier a fourth can now be added: the Class A + B, of which the Technics SE-A1 is an example. The block diagram of this new amplifier is shown in figure 2.

As can be seen, two amplifiers per channel are used: a Class-A amplifier and a Class-B amplifier, each with its own driver stage. The two output stages are fed from symmetrical supplies: The Class-B stage is connected to + and $-U_2$, whilst the Class-A stage is fed by the floating supply $\pm U_1$. The junction of the U_1 supply lines is connected to the output of the Class-B amplifier. The quiescent current of the Class-A output stage is I .

If we now arrange that both amplifiers have the same gain (by choosing suitable values for $R_1 \dots R_4$), then for equal input voltages they must obviously have the same output voltage. Since the output of the Class-B stage feeds into the junction of the U_1 supply rails, the supply voltages for the Class-A stage will follow variations in the output voltage. The result is that, regardless of the input drive voltage, the voltage developed across the two output transistors of the Class-A stage will always be (almost) the same (U_1). This being the case, U_1 can be as small as is desired, in fact it need only be large enough to ensure that the output stage is still functioning satisfactorily. This low value of U_1 is the secret of the circuit. It means that the Class-A output stage consumes very little power (since the latter is the product of total supply voltage and quiescent current).

The Class-A output stage itself delivers very little power into the load, since the AC voltage across each half of the output stage is almost zero. Under the influence of the drive voltage, the current through the Class-A output transistors may vary as much as it likes

2



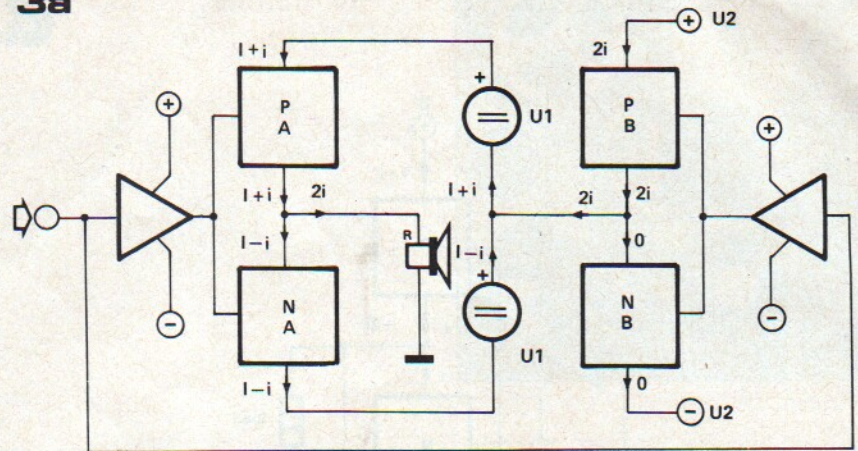
(and does in fact do so), but the stage itself cannot be used to deliver output power into the loudspeaker. Any power developed is dissipated as heat; however thanks to the low supply voltage, this is limited to safe levels. Thus the task of actually supplying the Watts is left to the Class-B stage, which as we have seen, is inherently more efficient than Class-A output stages.

As is apparent from figure 3 (figure 3a shows the case for a positive-going signal, figure 3b for a negative-going signal), the output current of the Class-B stage is fed to the load via the supply lines $\pm U_1$ and the Class-A output transistors. The current I is always sufficiently large to ensure that, regardless of the size of the AC signal current from the Class-B stage, the Class-A output transistors are never cut-off or saturated.

Since the Classe-B amplifier has virtually no quiescent current, it is inevitably subject to crossover distortion. Does this then mean that the Class A + B amp must also be afflicted with this problem? Fortunately the answer is no. Although, in the absence of quiescent current, the Class-B output does indeed produce crossover distortion, the latter never actually has any effect upon the final output. Quite apart from the fact that the local negative feedback (round R3/R4 in figure 2) reduces the distortion to very low levels anyway, the sole effect of the Class-B induced crossover distortion is to cause a small difference in the output voltages of the two (Class-A and Class-B) stages — i.e. a small AC voltage is produced across the Class-A stage. The current source/drain characteristic of the Class-A output stage is easily good enough to ensure that this has a negligible effect upon the output signal.

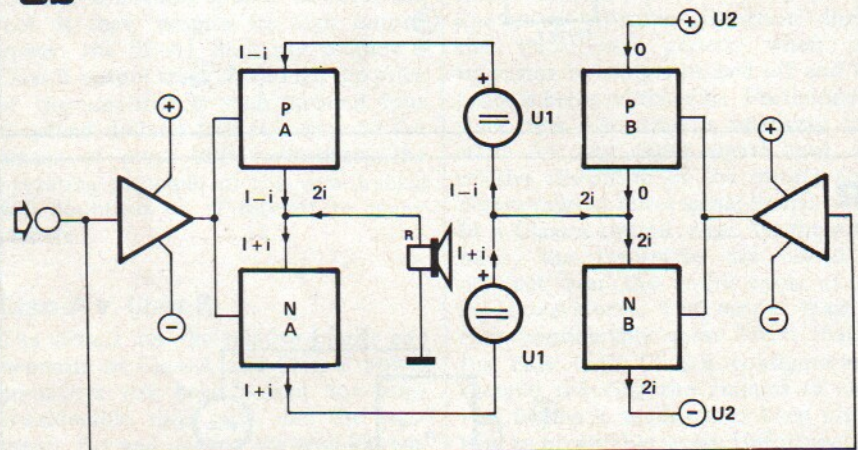
The result of employing both a Class-A and Class-B output stage in the above-described fashion is to obtain the high efficiency (disregarding the relatively small constant dissipation in the Class-A stage) and output power of the latter with the low distortion and excellent linearity of the former. The accompanying table lists and compares the power handling characteristics of Class-A, Class-B and Class A + B amplifiers for (an admittedly unrealistic) output power of 350 W into 4 Ω . The distinctive performance of the A + B amp is expressed not so much in the figures for efficiency, but rather for maximum dissipation, which of course also has a decisive influence on the size of the amplifier and weight of the heat sink. In conclusion it can be said that the Class-A + B principle represents an interesting approach and one which need not always cost four thousand dollars to implement!

3a



79018 3a

3b



79018 3b

Table

Power handling characteristics of Class-A, Class-B and Class A + B amplifiers. Maximum output power 350 W into load resistance of 4 Ω .

		A	B	A + B
	supply voltage U_1	53 V	—	5 V
	supply voltage U_2	—	53 V	53 V
	quiescent current A	6.6 A	—	6.6 A
	quiescent current B	—	0 A	0 A
quiescent conditions	power taken from supply	700 W	0 W	66 W
	dissipation	700 W	0 W	66 W
	output power	0 W	0 W	0 W
	efficiency	0 %	—	0 %
output level at which maximum dissipation occurs	power taken from supply	700 W*	284 W	$\xrightarrow{+66W}$ 350 W
	dissipation	700 W*	142 W	$\xrightarrow{+66W}$ 208 W
	output power	0 W*	142 W	$\xrightarrow{+0W}$ 142 W
	efficiency	0 %*	50 %	31 %
max. output level	power taken from supply	700 W	446 W	$\xrightarrow{+66W}$ 512 W
	dissipation	350 W	96 W	$\xrightarrow{+66W}$ 162 W
	output power	350 W	350 W	$\xrightarrow{+0W}$ 350 W
	efficiency	50 %	78 %	68 %

* Maximum dissipation occurs under quiescent conditions

Figure 3. Current flow in the output stages of figure two for a positive and negative-going drive signal (figures 3a and 3b, respectively).

EJEKTOR

electronically variable resistance

For control of signal levels, particularly in low-frequency circuits, some kind of electronically variable resistance is often required. In the past, LDRs have been used in conjunction with LEDs or filament lamps; FETs or even bipolar transistors have been tried with varying success; one might even consider using a thermistor with some form of heating element. What these and similar approaches lack in sophistication they make up for in associated problems: distortion, noise, non-linearity, etc. Not to mention the difficulties involved in ensuring reasonable tracking between several units. However, the alternative proposed here seems quite promising.

Figure 1 shows a resistor, R1; a second resistor, R2, can be connected in parallel by closing a switch, S. If S remains open, the total resistance R between the two ends of the circuit is equal to R1 (see figure 2b); if S is kept closed, the total resistance is equal to R1//R2 (figure 2b). Not exactly world-shattering news, so far.

However, if S is replaced by an electronic switch; if this switch is operated at a high switching rate (well over the highest frequency the circuit is expected to handle); if the duty-cycle of the switch-control signal is proportional to some external control signal - then the complete circuit will operate as an electronically variable resistor! Why? Let us examine figure 3.

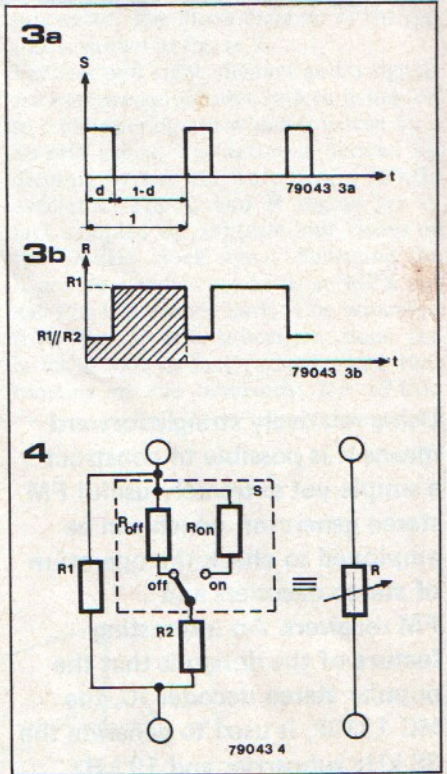
It is assumed that the control signal for the electronic switch is a squarewave with duty-cycle d (figure 3a). The effective total resistance will then vary as shown in figure 3b; for relatively steady-state signals, this is equivalent to the 'average' resistance of the shaded area in figure 3b;

$$R = \frac{\text{shaded area}}{\text{period time}}, \text{ i.e.}$$

$$R = d.R1//R2 + (1-d).R1$$

In practice, of course, an electronic switch such as the CMOS type 4016 or 4066 is not ideal: its 'on' resistance is not zero and its 'off' resistance is not infinite. A more accurate equivalent circuit diagram is shown in figure 4; the corresponding formula for the 'average' resistance R is as follows:

$$R = d.R1/(R2+R_{on}) + (1-d).R1/(R2+R_{off})$$



The average resistance value varies linearly with the duty-cycle, d; if linear voltage-control is required, the only 'missing link' is a linear voltage-to-duty-cycle converter. This particular conversion was dealt with quite recently, in the article 'PWM audio amplifiers' (Elektor December 1978).

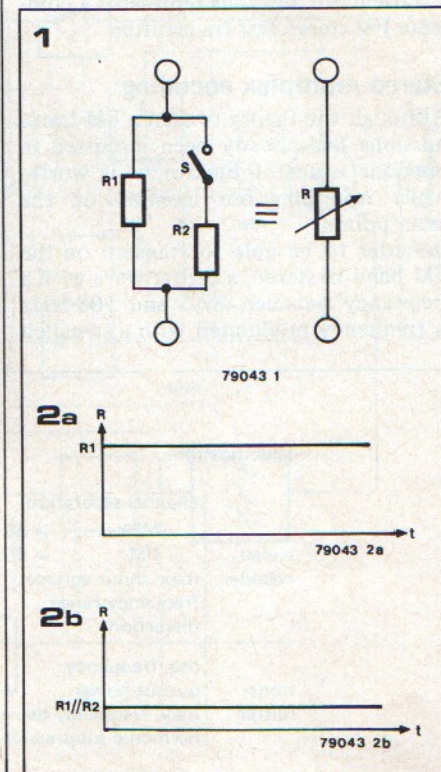
If accurate tracking of several variable resistors is required, a single voltage-to-duty-cycle converter is used to drive them all. For up to 4 resistors, tolerances in Ron and Roff can be quite small, since 4 electronic switches are contained on the same chip. For R1 and R2, 5% tolerance types will usually prove quite satisfactory - although precision types or even accurately adjusted presets can be used if required.

Depending on the circuit in which the variable resistor is to be used, it may prove necessary to include a low-pass filter before and/or after it - as with any other sampling circuit.

The principle outlined above may well prove useful in a wide field of applications:

- amplitude control in RC oscillators;
- voltage-controlled oscillators;
- voltage-controlled filters;
- voltage-controlled attenuators;
- vibrato circuits in electronic organs;
- compander circuits;
- and so on;
- and so forth.

an invitation to investigate, improve on and implement imperfect but interesting ideas



FM-stereo generator

Using relatively straightforward means it is possible to construct a simple yet extremely useful FM stereo generator, which can be employed to check the operation of stereo decoders and FM receivers. An interesting feature of the design is that the popular stereo decoder IC, the MC 1310P, is used to generate the 38 kHz subcarrier and 19 kHz pilot tone.

For even the simplest of checks or the most approximate alignment of a stereo decoder or FM receiver, some sort of test transmitter providing a stereo multiplex-encoded FM signal is virtually indispensable. Although the stereo multiplex encoder which was described in the article of that name and published in *Elektor* 25, May 1977 proved — to judge from the reactions of readers — to perform quite adequately, the fact that it did not include an FM test generator meant that it could not be used to test the entire FM receiver, but only the stereo decoder. Furthermore, it also failed to provide the lowpass filtering necessary if the multiplex stereo output of the encoder is to be modulated onto an FM carrier.

For these reasons it was decided to produce the design presented here, which features thorough filtering of the encoder output signal, requires virtually no alignment, has excellent channel separation and very low distortion. More importantly, the circuit also includes an FM oscillator and thus represents a complete FM stereo test transmitter.

Stereo multiplex encoding

Although the theory of stereo FM transmissions has already been discussed in previous issues of *Elektor*, it is worthwhile refreshing our memory on the main points.

In order to be able to transmit on the FM band in stereo, a carrier wave with a frequency between 87.5 and 108 MHz is frequency modulated with a so-called

stereo-multiplexed (MPX) signal. The spectrum of this MPX signal is shown in figure 1, and as can be seen, it consists of three basic signals:

- a sum signal (L + R)
- a difference signal (L - R) which is modulated onto a 38 kHz subcarrier
- a 19 kHz pilot tone

The sum signal (L + R) is obtained by adding together the left and right channel audio signals. The bandwidth of these signals stretches from approx 15 Hz to 30 kHz. Mono FM receivers receive only this sum signal, since the other signals shown in figure 1 lie outside their passband.

The stereo information is added to the transmitted signal by amplitude modulating the difference between the left and right channel signals onto a 38 kHz subcarrier. The L - R information is thus contained in two sidebands, namely 23 ... 39.97 kHz and 38.03 ... 53 kHz. The 38 kHz subcarrier is not in fact broadcast; in order to improve the efficiency of the transmitter, it is suppressed, and regenerated at the receiver by means of the low level 19 kHz pilot tone to which it is phase-locked. The rise in the frequency response of the audio signal above approx. 3 kHz is the result of pre-emphasis at the transmitter. This has the effect of boosting the higher frequencies and helping to improve the signal-to-noise ratio. A de-emphasis network in the receiver with the inverse characteristic ensures that the overall frequency response of the system is flat.

Specifications.

stereo encoder	channel separation:	
	MPX:	≥ 50 dB (1 kHz); 40 dB (10 kHz)
	FM:	≥ 40 dB (1 kHz); 30 dB (10 kHz)
	max. input voltage:	100 mV RMS
	frequency range:	30 Hz - 15 kHz
	distortion:	< 0.1% (1 kHz)
trans- mitter	osc. frequency:	88 ... 108 MHz (variable)
	output power:	-6 ... 0 dB
	max. frequency deviation:	approx. 1 MHz
	harmonic suppression:	> 50 dB for all harmonics

Design

As one might expect, there are several possible ways of generating an MPX signal such as that shown in figure 1. The L + R signal and pre-emphasis are simple enough to realise, however the modulated L - R signal presents slightly more of a problem. In addition, there is the separate question of suppressing the 38 kHz subcarrier and all signal components with a frequency greater than 53 kHz.

In many stereo encoders (including that published in May '77) the L - R signal is obtained simply by inverting the R signal and then summing it with the L signal, before modulating the result onto the 38 kHz subcarrier. The circuit

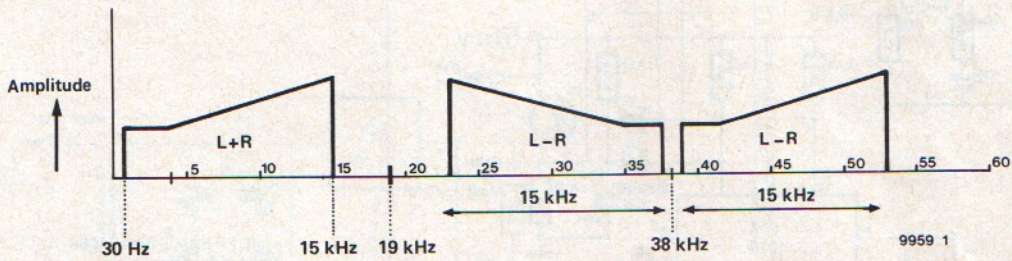
Figure 1. Frequency spectrum of a multiplex encoded stereo signal.

Figure 2. Block diagram of the complete stereo generator.

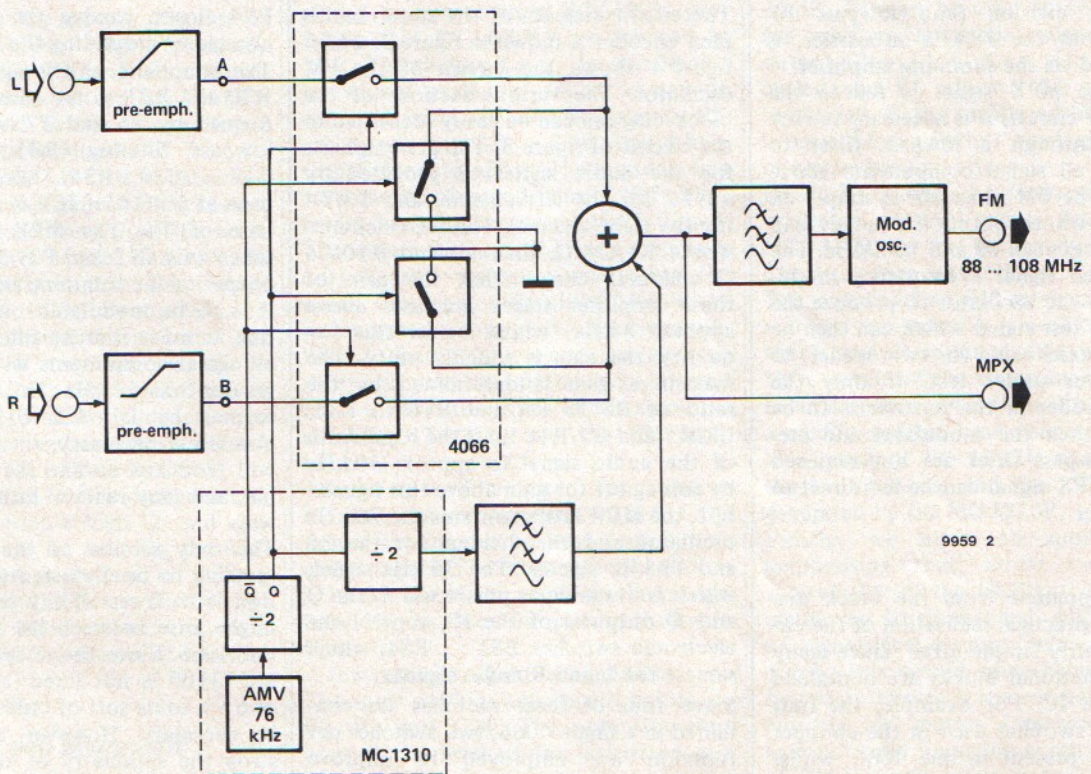
described here, however, operates on a different principle, which is both simpler and ensures better suppression of the subcarrier. The block diagram of the circuit is shown in figure 2.

The left and right channel audio signals are first pre-emphasised before being fed to a chopper circuit which is driven by a 38 kHz signal. The latter is derived by dividing by two the output of a 76 kHz oscillator. The L and R signals are in fact sampled by *opposite* half cycles of the 38 kHz clock signal. Summing the L and R samples produces an MPX signal which does not have to be separated from the 38 kHz subcarrier, since the latter is not in fact present - all that remains are the sidebands. The 19 kHz

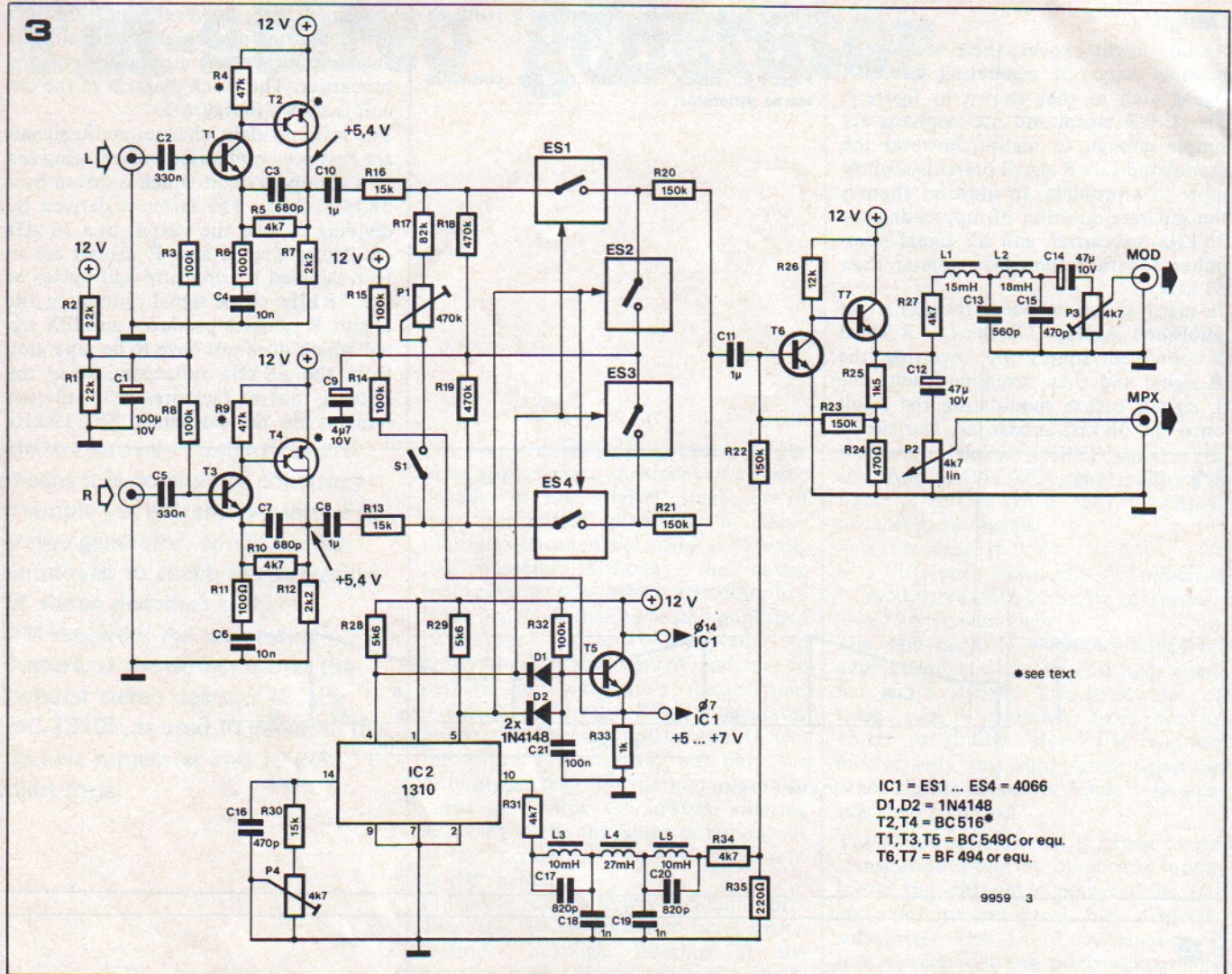
1



2



9959 2



pilot tone, which is similarly derived by frequency division (and lowpass filtering) from the 38 kHz subcarrier, is introduced via the summing amplifier. Before the MPX signal is fed to the modulator circuit, it is necessary to first feed it through a lowpass filter to eliminate all signal components above 53 kHz. The FM generator is simply an oscillator whose output frequency can be varied between 88 and 108 MHz. The MPX stereo signal is frequency modulated onto the oscillator so that the FM stereo test signal which can then be fed via coaxial cable (or twin feeder) to the receiver under test. If only the stereo decoder in the receiver is to be checked, then the modulator and preceding lowpass filter are not required and the MPX signal can be fed direct to the decoder.

Circuit

As was apparent from the block diagram, the practical realisation of the circuit is a fairly simple affair, since many of the functional blocks are contained in a single IC. For example, the four electronic switches used in the chopper circuit are present in one 4066, whilst the 76 kHz oscillator and the divide-by-two stages for the 38 kHz and 19 kHz signals are available in the shape of the well-known stereo decoder IC,

MC 1310P.

The circuit diagram of the stereo multiplex encoder is shown in figure 3, whilst figure 4 shows the circuit of the FM oscillator. The various sections of the block diagram can be easily identified in the circuit of figure 3. The pre-emphasis for the audio signals is provided by T1/T2 for the left channel and T3/T4 for the right channel. The feedback networks R5/C4 (L channel) and R10/C6 (R channel) ensure that the gain of these amplifier stages increases above approx. 3 kHz, whilst below this frequency the gain is roughly unity. The maximum gain is determined by the ratio of R5 to R6 and R10 to R11; C3/R5 and C7/R10 limit the bandwidth of the audio signal to approx. 30 kHz by rolling off the gain above this figure. IC2, the MC 1310P, contains the 76 kHz oscillator and the dividers for the 38 and 19 kHz signals. The 38 kHz signal, which is available at pins 4 and 5 (the Q and \bar{Q} outputs) of the IC, control the electronic switches ES1 ... ES4, which sample the L and R audio signals.

Since four of these switches are contained in a single 4066, two switches per function are employed to improve switching efficiency: when ES1 is closed, thereby letting the left channel signal through, ES3 is also closed, so that the right channel signal is simultane-

ously shorted to earth; similarly, when ES4 closes, passing the R signal, ES2 also closes grounding the L signal.

The sampled L and R signals are fed via R20 and R21 to the summing amplifier formed by T6 and T7. After extensive lowpass filtering (R31, L3, L4, L5, C17 ... C20, R34), the 19 kHz pilot tone at pin 10 of IC2 is also fed to the base of T6. The MPX signal can be taken (via C12 and P2) direct from the output of the summing stage, however if it is to be modulated onto an FM carrier, it must first be filtered to remove all signal components with a frequency greater than 53 kHz. This filter, which is formed by L1, L2, C13 and C15, is absolutely necessary, since FM receivers will tend not to like the unfiltered signal, and may react in rather an alarming way.

The only section of the circuit which remains to be discussed is T5. Its function is to forestall any problems which might arise between the MC 1310P and the 4066. Since the output level of the MC 1310P is not fixed (it can be e.g. 4 or 6 V), some sort of buffer stage should be necessary. However, this would destroy the symmetry of the circuit, and for this reason T5 was included to provide the supply voltage for the 4066, using the output voltage of the MC 1310P as a reference.

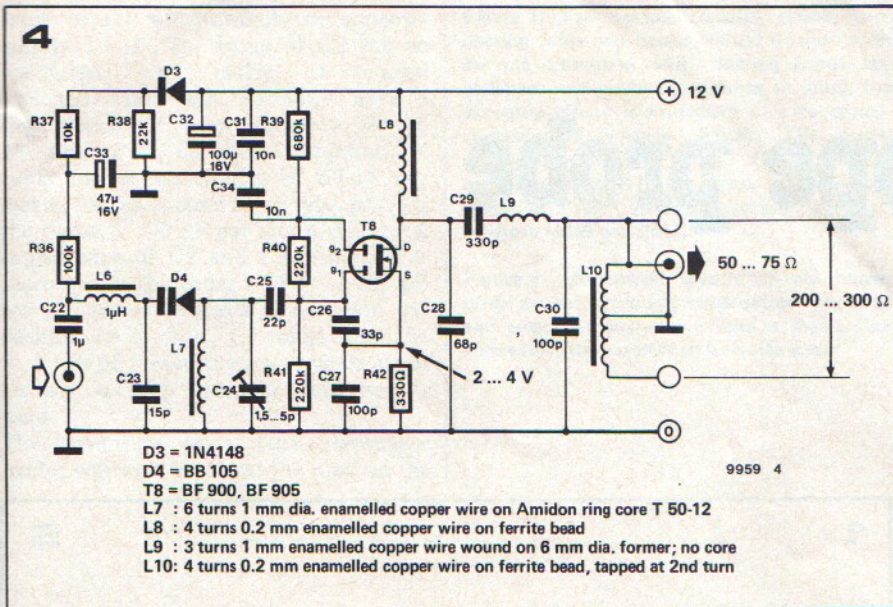
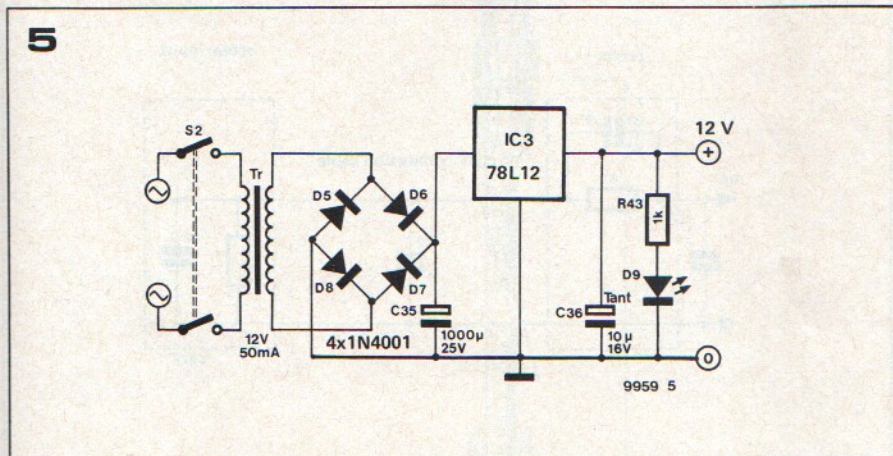


Figure 3. Circuit diagram of the multiplex encoder. The 38 and 19 kHz signals are derived from the stereo decoder IC, the MC 1310P.

Figure 4. The FM generator basically consists of an extremely stable oscillator in the shape of a single dual-gate MOSFET, the output of which can be frequency modulated.

Figure 5. A simple but perfectly adequate power supply circuit. R43 and the LED, D9, are included to provide visible on/off indication.



FM test generator

Figure 4 shows the circuit diagram of the oscillator which, when frequency modulated by the MPX signal, will provide an FM stereo-encoded signal which can be fed direct to the antenna input of the receiver to be tested.

Despite the fact that it is constructed using only one dual-gate MOSFET, even under varying load conditions the oscillator is extremely stable, and exhibits very little temperature drift. The output filter (C28, C29, C30, L9) ensures good suppression of harmonics and also has the advantage of requiring no adjustment. The ferrite bead transformer at the output (L10) allows connection to the receiver to be made either via coaxial cable (50 or 75 Ω) or twin feeder.

A ring core is used for the oscillator coil (L7), which means a high Q, and also has the advantage of reducing the likelihood of either producing, or picking up r.f. radiation. The oscillator frequency can be tuned between approx. 88 and 108 MHz by means of trimmer C24.

Construction and alignment

Most of the components should prove to be fairly readily obtainable. Problems may be encountered, however, with the Darlington transistors, T2 and T4. If

that is the case, then they can be replaced by conventional BC 559C's, providing that R4 and R9 are reduced to 22 k. The chokes, L1 . . . L6 should also be widely available, whilst as can be gathered from the details given in figure 4, winding L7 . . . L10 should be a straightforward affair. The Amidon ring core can be obtained from T.M.P. Electronic Supplies, Leeswood, Mold, Clwyd. The circuit as a whole is not especially critical, and assuming one takes the usual care, no difficulties should be encountered during its construction. Wiring should of course be kept as short as possible, particularly around ES1 . . . ES4, the input of the summing amplifier (T6/T7), and the FM oscillator.

Thanks to the low current consumption of the circuit (approx. 40 mA), the power supply can be kept both simple and compact. The most obvious solution is to use one of the many common regulator ICs, as does the circuit shown in figure 5.

A few remarks regarding alignment: The most obvious adjustment points are P2, P3 and C24. The potentiometers control the level of the unfiltered and filtered MPX signal respectively, whilst the trimmer varies the frequency of the FM oscillator.

Preset P1 influences the channel separ-

ation. Although this is always at least 40 dB, P1 can be used to compensate for negative crosstalk caused by the output filter L1/L2/C13. S1 should be closed and P1 adjusted for maximum separation. If the unfiltered MPX signal is used, S1 can be left open and P1 will of course have no effect.

Preset P4 allows the frequency of the oscillator in the stereo decoder IC, MC 1310P, to be accurately adjusted. The procedure is as follows:

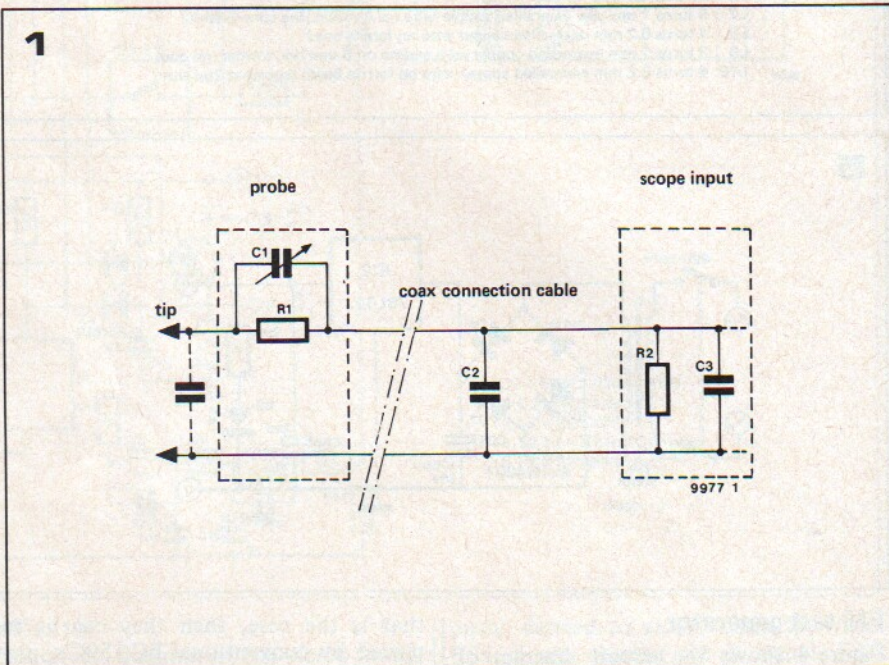
The output of an FM receiver tuned to a stereo transmission is used to provide the L and R input signals, whilst the MPX output of the stereo encoder is fed to an amplifier. P4 is then adjusted until a clearly audible beat note is produced as a result of the 19 kHz pilot tone in the L + R signal and the 19 kHz tone generated by the MC 1310P.

Finally, we make no apologies for emphasising that, *under no circumstances* should the oscillator output be connected to an antenna. Although the r.f. signal level does not exceed roughly 1 mW, this would nonetheless be sufficient to ensure a transmitter range of approx. 100 metres. One would therefore not only incur the wrath of owners of FM receivers living in the immediate vicinity, but more importantly one would be breaking the law!

passive oscilloscope probe

Many users of oscilloscopes fail to get the best from their instrument simply through not using a proper input probe. It is not an uncommon sight to see 'scopes being used with ordinary unscreened test leads, or with large lengths of screened cable hung on the input terminals. The unscreened leads may, of course, pick up all kinds of interference signals, whereas a long screened lead greatly increases the effective input capacitance of the oscilloscope — thus attenuating high-frequency signals from high source impedances.

The latter problem can be overcome by using a passive oscilloscope probe. The 10:1 probe described here can be constructed from standard parts.



If an oscilloscope is to present a true 'picture' of an electric signal, the connection between the signal source (i.e. the circuit being tested) and the 'scope must fulfil a few basic requirements. In the first place, excessive loading of the signal source must be avoided, since otherwise the amplitude and/or the waveshape of the signal may be modified. Secondly, having ensured that the signal is not modified at the source, it is also important to preserve the waveshape as accurately as possible when it is passed through the connection to the 'scope.

To sum it up briefly: if a signal in a circuit is to be displayed on a 'scope, it is important to ensure that both waveshape and amplitude remain unaltered in the circuit and that the waveshape remains undistorted throughout the connection to the 'scope. It is not so important to preserve the amplitude of the signal, provided the ratio between input and output signal level is known. In order to reliably fulfil these requirements, probe, connecting cable and 'scope must be considered as a whole. Generally speaking, however, commercially available probes are suitable for use with commercially available 'scopes

— even if they are made by different manufacturers — since the input impedance of oscilloscopes is fairly well standardised. Commercial probes do have one disadvantage for amateur use: they are fairly expensive. . .

The passive 10:1 probe described here is relatively cheap to build, and its performance is quite acceptable for amateur use. Depending on the care taken in the construction, reliable results can be obtained up to at least 500 kHz.

The circuit of the probe is shown in figure 1. The input impedance of the 'scope will normally be equivalent to a 1 M resistor (R2) in parallel with a 30 pF capacitor (C3). The impedance of the connecting cable can be represented by a further capacitor (C2). By adding R1 and C1 in the probe, a divide-by-10 frequency compensated attenuator can be obtained. Since R2 is 1 M, the 10:1 attenuation ratio implies that R1 must be 9 M. This value can be obtained by series-connection of a 6M8 and a 2M2 resistor.

In order to obtain a flat frequency response, the capacitive voltage divider (C1, C2 and C3) should have the same 10:1 division ratio. As stated earlier, the

value of C3 will normally be approximately 30 pF. The value of C2 can be estimated: one metre of coaxial screened cable will normally have a capacitance of approximately 50 to 150 pF. For instance, 'uniradio 70' cable has a capacitance of 67 pF per metre; for 50 Ω coax cable type RG58U the figure is 100 pF per metre. The total capacitance of C2 and C3 in parallel is therefore in the order of 80...180 pF for a 1 metre test lead. To obtain the desired 10:1 ratio, C1 must then be 9...20 pF; since the exact value is not known, a 20 p trimmer capacitor is used.

The advantage of a 10:1 attenuator probe will now be clear: the load on the

Figure 1. For optimal results, probe, connecting cable and 'scope should be dealt with as one complete unit. Bearing input impedances and cable capacitance in mind, the complete circuit is equivalent to a frequency-compensated voltage divider. The probe proper consists only of C1 (20 p trimmer capacitor) and R1, the latter actually representing the series-connection of two resistors (6M8 and 2M2).

Figure 2. Mechanical layout of the home-made probe. Although constructed from odds and ends like piano wire and a mains flex connector, the results can be quite good.

circuit under test is drastically reduced. The input resistance has been increased from 1 M (R2) to 10 M (R1 + R2); the input capacitance has been similarly decreased. The latter is perhaps less obvious, but to give an example let us assume that C3 (the 'scope input capacitance) is 30 pF; that C2 (the cable capacitance) is 100 p; and that the capacitance of the probe tip is 5 p. If C1 and R1 are omitted, the total capacitance loading the circuit under test is then 135 pF. However, the correct value for C1 under these conditions is $\frac{130}{9} \approx 14.5$ pF; series-connection with C2 and C3 effectively reduces this to approximately 13 pF. The load capacitance at the probe tip is therefore reduced to approximately 13 + 5 = 18 p!

Construction

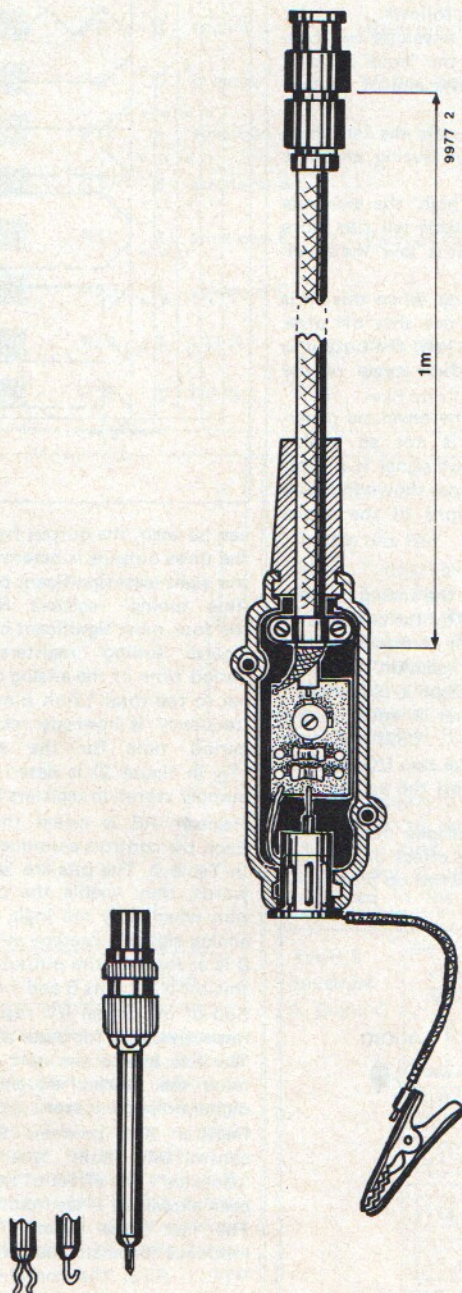
The probe circuit can be housed in a standard mains flex connector. This is ideal as it has a hole at each end, space for the components and cable clamps. To make room, the internal dividers which normally separate the cable terminals can be broken out using a pair of pliers. The components can be mounted on a piece of Veroboard, and placed inside a screen bent from a piece of copper foil, with a single hole in it and the side of the connector to adjust C1. The coax lead is connected at one end and fixed firmly under the cable clamp. The input connection to the probe is made by means of a coaxial socket into which the probe tip plugs. This means that probe tips can easily be changed if damaged or if a different type of tip is required.

Probe tips can be made by removing about 5 cm (2") of the inner insulation from a piece of low-loss UHF coaxial cable. In other words, the outer insulation, the screening braid and the core are all removed, leaving the inner insulation. This is then sleeved with a piece of brass tube (available from model shops) and a piece of piano wire is inserted down the centre. Instead of piano wire, any other type of stiff wire that is a good conductor and sufficiently resistant to oxidation can be used (e.g. beryllium-copper), the idea being to obtain a reliable and sturdy tip.

The complete assembly is then mounted in a coaxial plug, the piano wire being soldered to the centre pin and the brass tube being gripped by the cable grip. Finally, the end of the probe tip is sealed with epoxy glue to prevent the ingress of dirt and moisture, and the brass tube is covered with silicone rubber, heat-shrink sleeving, or some other suitable insulation. Figure 2 gives an impression of the completed probe.

To set up the probe a good, clean squarewave with a fast risetime is fed into it and C1 is adjusted until there is no rounding off nor peaking of the squarewave's leading and trailing edges. ■

2



APPLIKATOR

Programmable sound generator

A few months ago, a new 'Complex Sound Generator' introduced by Texas Instruments was discussed under the heading 'Applikator' (Elektor, September 1978). That IC could be used to produce a wide variety of 'complex sounds': from trains and planes to gun-shots and space war. The desired sound effect was 'programmed' by means of wire links and resistor and capacitor values.

A distant relative of that IC is a new chip introduced by General Instrument Microelectronics (GIM): the AY-3-8910. This IC is a programmable sound generator: it can emit a broad range of complex sounds under microprocessor control. Although primarily intended for use in conjunction with General Instrument's own PIC 1600-series microprocessor system, it will also interface easily with several other 8-bit or 16-bit microprocessors (e.g. Texas Instruments TMS 1000 and Intel 8000-series). Sounds ranging from musical notes for musical instruments and complex sound-effects for electronic games and broadcasting to jarring warning signals for security applications and ultrasonic signals for remote control etc. are all easily generated. GIM are so impressed with the performance and versatility of the Programmable Sound Generator (or PSG for short) that they are offering automatic demonstrations over the telephone to all callers. To hear a demonstration of the device simply call the special number in London: 01 - 439 7052.

As illustrated in figure 1, the sound generator is linked directly to the microprocessor chip — in this particular example, GIM's own CP 1600 is shown. The link between the two chips consists of an 8-bit data/address bus (DA0...DA7), three Bus Control Signals (BC1, BC2, BD1R) and the reference clock signal Φ 1. Communication between the controller and the AY-3-8910 is based on the concept of memory mapped I/O. To a microprocessor such as the CP1600, the sound generator chip looks like a block of memory, organized as 16 consecutive memory locations. The base address of this block of memory is determined by the chip select lines (CS0...CS2).

In addition to the links to the microprocessor, the AY-3-8910 is provided with two 8-bit parallel bidirectional data ports that are TTL compatible. Each of these ports corresponds to a chip that can be used either as input or as output.

Although these digital in- or outputs will be useful in many applications, the main purpose of this chip is to provide an analog (sound)

output. In fact, the IC has three of these outputs, each of which can be individually programmed to produce any desired frequency and/or noise signal. The possibilities for programming the desired envelope are rather more limited: the AY-3-8910 contains only one envelope generator, common to all three analog outputs. Partly for this reason, the three outputs will normally be summed as shown in figure 1 to obtain one total (complex) sound.

The envelope generator can be programmed to give either a 'one-shot' or a continuously varying envelope. The various possibilities are illustrated in figure 2. As can be seen, the envelope shape is determined by four bits, labelled (rather loosely, as will become apparent) 'hold', 'alternate', 'attack' and 'continue'. The dotted lines in several of the envelope plots indicate 'channel off' — no output signal, in other words.

The effect of these four control bits can be described approximately as follows:

Hold: if this bit is 0 the envelope can continue to change freely; if the 'hold' bit is 1, the envelope is fixed at the end of its first period.

Alternate: the amplitude of the envelope signal increases and decays during alternate periods.

Attack: when this bit is 'high' the envelope will 'attack', i.e. its amplitude will rise more or less rapidly; when the bit is 'low' the envelope will decay.

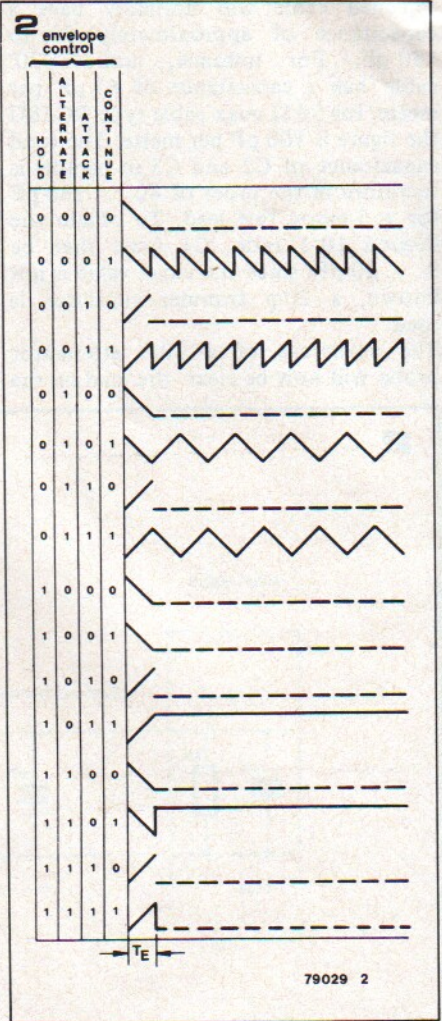
Continue: generally speaking, when this bit is 1, the analog output will not shut off after one cycle; when the bit is low, the output is only present during the first cycle of the envelope.

It should be noted that the envelope generator in the AY-3-8910 is not an analog circuit: its (internal) output signal is a 4-bit digital code. The wave shapes shown in figure 2 are analog approximations of the actual staircase output.

Programming for sound

The final output signals at the analog outputs A, B and C are determined by the contents of 14 registers in the IC. Each of these registers corresponds to a 'memory location' (as far as the controlling microprocessor is concerned); the address of each register is equal to the base address (set by CS0...CS2) displaced by the register number. The two I/O registers have no direct influence on the analog outputs.

The function of the various registers is illustrated in Table 1: the effect of the contents of each register is summed up briefly. As



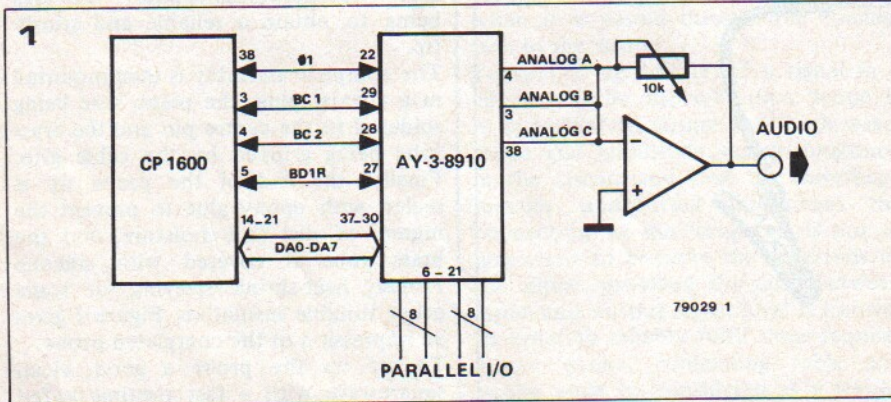
79029 2

can be seen, the output frequency for each of the three outputs is determined by twelve bits; the eight least significant bits are stored in the 'fine tuning' registers R0...R2, whereas the four most significant bits are stored in the 'coarse tuning' registers R4...R6. The period time of the analog output is proportional to the total 12-bit binary number, i.e. the frequency is inversely related. Similarly, the period time for the envelope generator (T_E in figure 2) is determined by the 16-bit number stored in registers R3 and R7.

Register R8 is called the 'enable' register. Each bit controls a unique function, as shown in Table 2. The bits are 'active low', in other words, they enable the corresponding function when they are logic 0. For instance, an analog signal is present at output A when bit 0 is at logic 0; the output is turned off when this bit is '1'. Bits 6 and 7 determine the function of the digital I/O registers (R4 and R15, respectively); 0 for input and 1 for output. The five bits in the next register, R9, determine the clock frequency of the internal digital noise generator.

Register R10 contains the four envelope-control bits, 'hold', 'alternate', 'attack', and 'continue'. The effect of these bits has already been explained — see figure 2.

The last three registers that can directly influence the analog output signals are R11...R13. The contents of these registers control the envelopes, as shown in Table 3.



79029 1

APPLIKATOR

Table 1.

organization	register	bits	function	description
	R0	8	f0	Fine tunes frequency on channel A. 8 bits are proportional to period.
	R1	8	f1	Similar to f0 but channel B.
	R2	8	f2	Similar to f0 but channel C.
	R3	8	fE	Fine tunes envelope period.
	R4	4	P0	Coarse tunes channel A (high four bits).
	R5	4	P1	Coarse tunes channel B (high four bits).
	R6	4	P2	Coarse tunes channel C (high four bits).
	R7	8	PE	Coarse tunes the envelope period.
	R8	8	enable	Each bit controls a unique function (active low): see table 2.
	R9	5	N clock	Varies the frequency of the clock for the noise generator.
	R10	4	envelope control	Each bit controls a function in the envelope generator: see figure 2.
	R11	6	envelope A	Each of these registers controls its respective envelope as shown in table 3.
	R12	6	envelope B	
	R13	6	envelope C	
	R14	8	I/O A	With the control bits of R10 set for the output mode, data can be written to these ports from the CPU, and latched. With the control bits set for input, data can be read into the CPU. Each port is independently programmable.
	R15	8	I/O B	

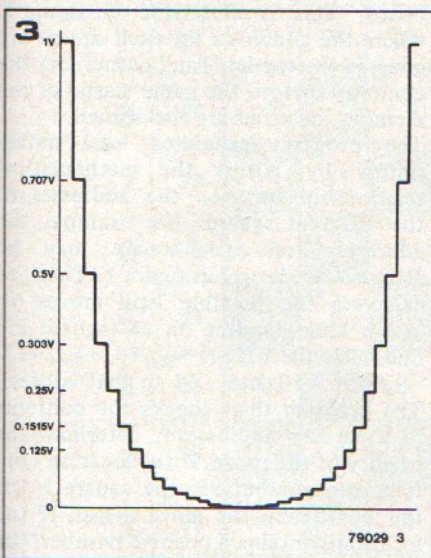


Table 2.

Enable bits R8

- Bit 0: Tone on channel A.
 - Bit 1: Tone on channel B.
 - Bit 2: Tone on channel C.
 - Bit 3: Noise on channel A.
 - Bit 4: Noise on channel B.
 - Bit 5: Noise on channel C.
 - Bit 6: Register R14 (I/O A)
 - Bit 7: Register R15 (I/O B)
- } 'active low'
} 0 for input,
} 1 for output

signal is actually a 4-bit binary number. For this number to determine the output signal level, some kind of digital-to-analog conversion is useful. A suitable D/A converter is incorporated in the IC; since human hearing

works logarithmically, as far as perception of sound level is concerned, logarithmic D/A conversion is used for the envelope level. The result is shown in figure 3: as the binary number changes from 15 through 0 and back up to 15 the envelope signal is varied in such a way that the audible level appears to vary smoothly over a 45dB range. Finally, the Bus Control Signals — generated by the controlling microprocessor — are decoded within the AY-3-8910 to control all bus operations: writing into and reading out of the internal registers.

Litt:
General Instrument Microelectronics: Preliminary Information on the AY-3-8910 Programmable Sound Generator.

Table 3
Envelope A, B and C

six bits in R11 ... R13	amplitude		remarks
	determined by envelope generator	constant	
00 - - - -	*		envelope x1
01 - - - -	*		envelope x½
10 - - - -	*		envelope x¼
11 D3 D2 D1 D0		*	amplitude determined by bits D3 ... D0

Of the six bits stored in each of these registers, the first two are used as control bits. If these are both at logic '1', the output amplitude (of the corresponding output) is constant: it is proportional to the 4-bit binary number stored in the remainder of the register. If either or both of the control bits is at logic 0, the level of the corresponding analog output is determined by the output of the envelope generator — multiplied by a constant factor (x1, x½ or x¼).

As mentioned earlier, the resultant 'envelope'

computers and chess

How the monster thinks



The game of chess has long been regarded as a symbol of man's intellectual prowess. Until recently, the prospect of a chess-playing computer defeating a master-strength human opponent seemed remote. A few months ago, however, in a much publicised match an International Chess Master, David Levy, actually lost a game to a program from North America. The story of the match is recounted by Mr. Levy himself elsewhere in this issue. The following article takes a look at the background to computers and chess: how they play, their weaknesses and strong points, and speculates on the chances of Karpov being the last flesh-and-blood World chess champion!

Thirty years ago, with the electronic computer still in its infancy and illustrating above all else the First Law of Thermodynamics ('Work is Heat'), the game of chess attracted the interest of a number of researchers in the field of artificial intelligence. The first person to actually propose how a computer might be programmed to play chess was the English Mathematician Claude Shannon. In 1949 he presented a paper entitled 'Programming a computer for playing chess', which was significant, both for the fact that it was the first paper expressly on this subject, and more importantly since many of Shannon's ideas are still employed in the strongest chess-playing programs of today. Shannon's interest in chess programming stemmed from his belief that the game represented an ideal test of machine intelligence. Chess is clearly defined in terms of legal operations (moves of the pieces) and ultimate goal (checkmate), whilst being neither so simple as to be trivial nor too complex to be unsusceptible to analysis.

Board, pieces and moves

Shannon suggested that the machine represent the chess board by assigning a location in computer memory to each square of the board. Each piece is then designated as a numerical value: +1 for a white pawn, +2 for a white knight, +3 for a white bishop etc; -1 for a black pawn, -2 for a black knight, and so on. These numbers are stored in the memory location which represents the square occupied by the corresponding piece. An empty square is represented by storing a zero in the appropriate

location. A number of more recent programs also adopt this method, with the exception that a 10 x 12 board is used instead of 8 x 8, and that a unique number (such as 99) is stored in all the off-board locations, thereby allowing the program to detect the edge of the board. This is illustrated in figure 1, where the addresses for each square are given in the top left-hand corner and the contents (before the game starts) of the memory locations are also shown.

The program generates legal moves simply by noting the mathematical relationship between the addresses of the different squares. For example, the addresses for each square may be assigned as shown in figure 1. Then, to calculate the possible legal moves of, say, a king standing on e1 (square 25) one adds the offsets +1, +9, +10, +11, -1, -9, -10 and -11 to that address. The program then checks the contents of these new addresses to determine the legality of the move. If the location contains the number 99, the square is off the board and the move illegal. If the location contains a positive number, the square is already occupied by a white piece. If the contents of the location are negative, on the other hand, the king can legally move to that square capturing an enemy piece (always assuming that the piece is not defended). Finally, a location containing a zero also represents a legal move assuming that the corresponding square is not attacked by an enemy piece.

Calculating the legal moves for a sliding piece such as a bishop, is only slightly more complicated. With a white bishop situated on square XY (e.g. 54, where X = 5 and Y = 4), the program examines

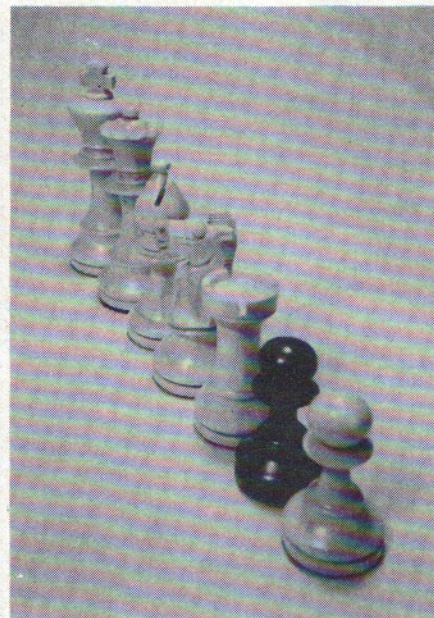
address $[X + 1, Y + 1]$ (i.e. 65), checks to see whether the contents of that location are zero, and if so proceeds to examine address $[X + 2, Y + 2]$ and so on (if $[X + 1, Y + 1]$ turns out to contain a negative number, then the bishop can move to that square, capturing a piece, but obviously can move no further along that diagonal). The machine repeats the above procedure for $[X - 1, Y - 1]$, $[X - 2, Y - 2]$ etc, then does the same for $[X - 1, Y + 1]$, $[X - 2, Y + 2]$ etc., and finally for $[X + 1, Y - 1]$, $[X + 2, Y - 2]$ etc. In this way the program can generate legal moves along all four diagonals of the bishop.

Similar operations can be performed to determine the legal moves of all the pieces, although one must bear in mind that certain moves have to be checked for the existence of pins (is the piece pinned against the king, for instance) and the procedure is complicated when considering castling and capturing *en passant*.

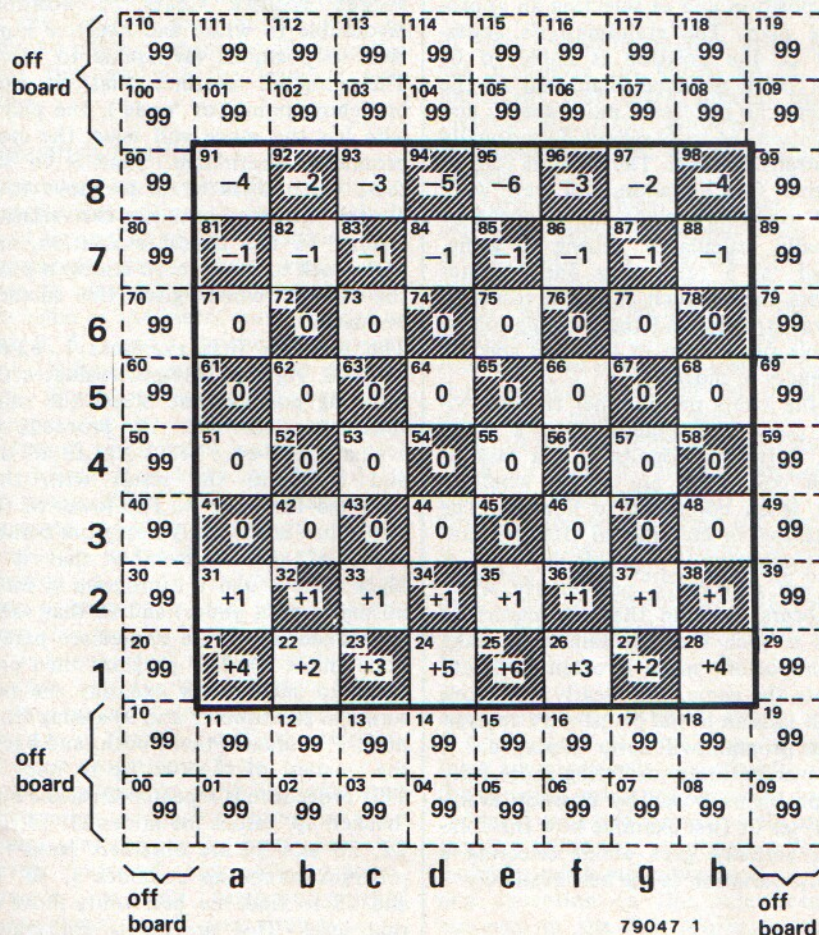
A more 'logical' approach

The above approach is still adopted by many modern programs, although an

Figure 1. The computer can represent the chess board by assigning a location in memory to each of the squares on the board.



1



79047 1

alternative method which is particularly suited for use with large computers has subsequently been developed. This utilises the fact that certain large computers operate with 64-bit words. If one bit is assigned to each square, only 12 64-bit words suffice to represent the position of all the pieces on the board. For example, one word will provide information on the position of all white pawns on the board by setting a bit to '1' for each pawn that resides on the corresponding square. If a square is empty the bit remains unset ('0'). A second word will represent the position of all the black pawns, a third the position of both white knights, and so on.

In addition to the position of pieces, these 'bit maps' or 'bit boards' as they are called can be used to represent other information. For example, one 64-bit word might represent all the squares attacked by white's pieces, another all squares which are a knight's move away from the black king, and so on.

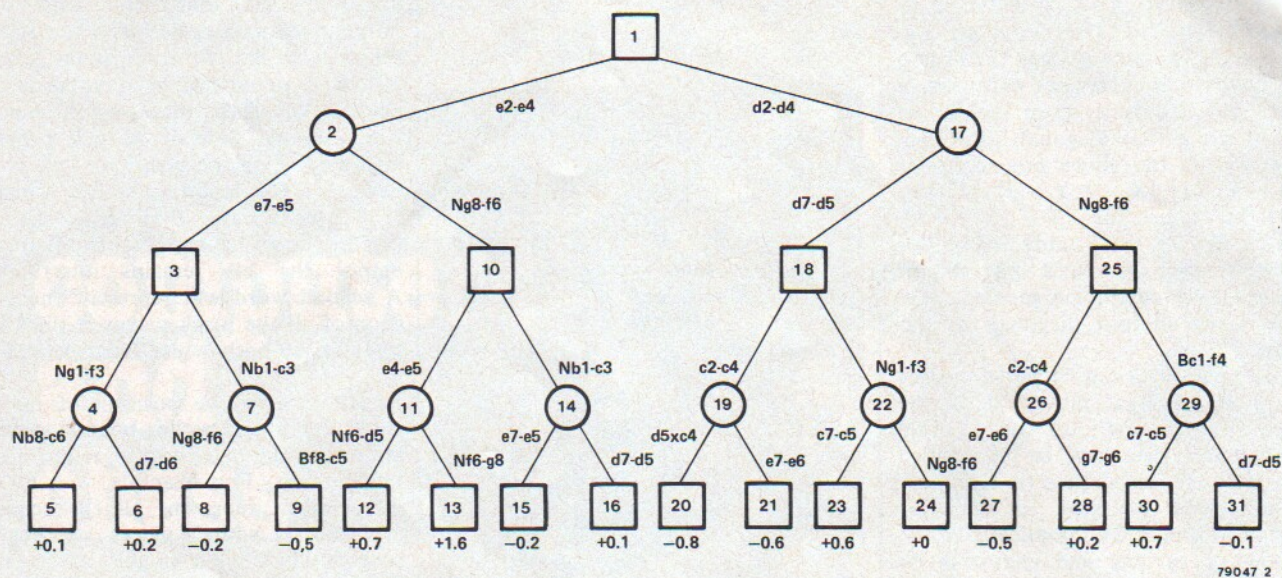
The real advantage of this alternative approach can be seen if one considers the instruction set of a modern computer, containing as it does a number of 'Boolean Logic' operations. These can be used to combine considerable amounts of information stored in bit maps. For example, assume that we wish to know whether white has a knight's move that will fork black's king and queen. One simply fetches two bit maps of potential knight's moves from the black king and queen respectively, and a bit map of knight moves from their present squares. Since the square may not be occupied by a white piece, a map of all white pieces is inverted and then ANDed with the first three maps. If the result is non-zero, then a forking square exists. Finally, this map is ANDed with a map representing all squares attacked by black pieces to determine whether the forking square is defended. It can be seen that the above operation takes very few program steps.

Looking for good moves

Having enabled the program to generate legal moves, there comes the problem of selecting the good from the bad. This is where the difficulties start to accumulate. The most obvious approach is to have the program examine all legal moves by white, followed by all legal replies by black, all legal counter-replies, and so on to a fixed depth.

This procedure, which Shannon called the 'type-A strategy' does however suffer from a number of serious drawbacks. The number of legal moves in each position is on average around 38. This means that a 2-ply analysis of all legal moves (i.e., one move each side; ply = 1/2 move) would produce $38^2 = 1444$ terminal positions to be evaluated. An analysis only 4-ply deep would yield 2,085,136 terminal positions, and a mere 6-ply look-ahead would involve evaluating some

2



3,010,936,389 positions! Because of this 'exponential explosion' as it is called, an exhaustive look-ahead of this type rapidly becomes unmanageable.

A second disadvantage of a fixed-depth exhaustive look-ahead is that the machine may well terminate its search in the middle of a series of exchanges — with the result that its evaluation of the position will be hopelessly wrong. It may, for instance, be deceived into thinking it is a piece ahead, when in actual fact it is about to lose a piece back — or even worse. A fascinating example of this type of 'computer blindness' will be given later — in the game COKO v. GENIE.

Shannon was well aware of the inherent problems of a type-A strategy, and therefore proposed an alternative model which he called type-B strategy. The latter is characterised by the notion of 'quietest' positions, i.e. the program is encouraged to continue its search until all forcing variations are exhausted and the position for evaluation is 'static'. More importantly, a B-type strategy will not attempt to generate all legal moves in a given position, but rather will select a small number of 'plausible' moves for subsequent analysis. This approach obviously requires that the program have some criteria by which it can select the more promising moves from those which are plainly irrelevant, i.e. that the program have a 'plausible-move generator'.

The interesting feature of the type-B strategy is that it attempts to simulate the approach of the most efficient chess model we know of, namely the human. Contrary to uninformed opinion, the chess master does not analyse dozens of moves deep and investigate hundreds of different variations before selecting a move. Quite the reverse is true. Research carried out by a Dutch psychologist,

de Groot, revealed that, in a fairly typical middlegame position, Grandmasters tended to look at only three or four different possible moves, and that the maximum depth to which they calculated was not much more than 7-ply! However, the grandmaster is adept at perceiving the critical features of a position and at selecting an appropriate plan. The grandmaster's assessment of the position is liable to be much more nuanced than that of the amateur; he has 'seen' more deeply and recognised the truly salient, functionally important features. The story is told of the great Czech grandmaster Reti, who, when asked how many moves ahead he normally calculated during a game, replied 'as a rule, only one'. Grandmasters think much more in terms of general strategy and the formulation of suitable plans than in terms of specific sequences of moves.

For the chess programmer this knowledge comes as something of a blow, since pattern recognition is a task at which computers are as yet woefully inept when compared to humans. The difficulties in creating an effective position evaluator and plausible-move generator are enormous, particularly when one bears in mind that the nature of chess is such that the failure to make one important move is often sufficient to lose the game, and clearly any move which fails an initial plausibility analysis by the program will never be played.

However before considering more fully the problems posed by position evaluation, let us first examine how the computer actually goes about selecting a specific variation as the best available.

Growing trees

Shannon suggested that the program adopt the 'minimax' procedure first

proposed by Morgenstern and von Neumann in their work on game theory. Basically, the program grows a 'tree' of variations. An example of a simplified game tree is given in figure 2, which starts from the initial position with white to move and assumes that some form of static evaluation function awards positive values to positions favourable to white and negative numbers to positions favourable to black. The program assumes that, at each branching point (or 'node'), the player who has the move will select the most promising alternative. That is to say that, when it is white to move (odd nodes), the program selects the variation leading to the largest evaluation, and with black to move (even nodes) it picks the branch which gives the smallest evaluation.

The program first examines 1. e2-e4, e7-e5 2. Ng1-f3, Nb8-c6, evaluates the resulting position and stores the value thus obtained. Next it proceeds to evaluate 1. e2-e4, e7-e5 2. Ng1-f3, d7-d6, and compares the result with that obtained for node 5. The lower of the two values is obviously best *from black's point of view* (remember that it is black's move and the program is minimising at even nodes) and so that value is 'backed up' to its immediate parent node (node 4). The program then proceeds to successively examine the two terminal positions (8 and 9) arising from node 7, evaluates them both, and backs the smallest of the two up to node 7. This procedure is repeated until the best 'backed-up' values for nodes 11, 14, 19, 22, 26 and 29 are obtained. Next the program maximises at nodes 3, 10, 18 and 25 to find the best white move at that level. This process is continued, 'minimaxing' back up the tree, until the best move for the current position is determined.

Figure 2. A simplified game tree.



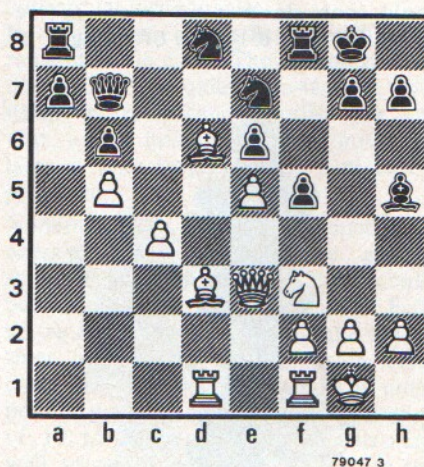
Although this procedure seems 'logical', a full-width search to the depth shown here (4-ply) would produce, on average, some two million terminal positions for evaluation. Fortunately, subsequent research showed that techniques can be employed which result in a substantial pruning of the game tree. A more fundamental problem, however, is presented by the 'bottom line' of the tree: in order to select good moves, the program must first evaluate the terminal positions.

Evaluating positions

Shannon's paper provided a simple example of an evaluation function which could be applied to static positions. Not surprisingly, the greatest weight was given to material balance and the relative value of the pieces were assessed as 200, 9, 5, 3 and 1 for the king, queen, rook, bishop/knight and pawn respectively. Positional evaluation was then incorporated by penalising doubled, backward or isolated pawns ($= -\frac{1}{2}$) and rewarding mobility by adding 1/10 for every legal move. Shannon also suggested additional features which should be included in the evaluation function, such as control of centre, open or semi-open files, passed pawns, pawn structure around the king, and so on. It is important that one arrive at an accurate weighting of the various factors in the evaluation function, and this is in fact one of the most difficult problems the chess programmer faces.

Early programs in particular exhibited an alarming tendency to bring out their queens very early in the game, since this greatly increased their mobility score. However, as any beginner quickly learns, this is usually poor strategy... The problem of writing an efficient evaluation function is compounded by the fact that the importance of certain

positional features changes during the course of the game. Furthermore, a particularly thorny problem is the difficulty in assessing whether a 'terminal' position is truly 'quiescent', or whether it in fact occurs, say, half way through a series of exchanges. As mentioned, most programs attempt to resolve the latter problem by performing an additional search for all checks and captures until these are exhausted. However, this approach is at best a makeshift solution, since it fails to deal with purely positional manoeuvres which a strong human player would examine as part of his evaluation of the position. In the position in figure 3, for example, the most significant feature is the 'hole'



in Black's position at c6 to which White can manoeuvre his knight on f3. It is important that Black prevent this by playing Bh5 x f3. However, this is extremely difficult for a program to perceive.

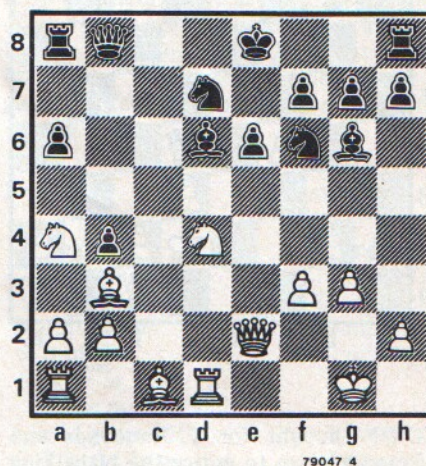
A further problem associated with evaluation functions is that many programs contain an 'opening book' (i.e. lists of standard opening variations) which has been included by the programmers to ensure a reasonable position from the opening. However, due to the unsophistication of the program's evaluation function, when the book runs out and the program has to start to think for itself, it naturally assesses the position quite differently from the Grandmaster whose game (or analysis) it is following. It therefore spends the next few moves re-arranging its pieces until they correspond with the evaluation function's idea of where they should be!

Computers are greedy

A typical fault of most programs is that they are excessively materialistic (even the Russian programs succumb to this capitalist evil) and are extremely loth to sacrifice a pawn or even a piece for less tangible, positional advantages. A startling exception to this rule occurred however in the first World Computer Chess Championships held in Stockholm in 1974.

Favourite to win was a North American

program called Chess 4.0, written by three former students of Northwestern University: Larry Atkin, Keith Gorlen and David Slate. In the second round Chess 4.0, which hitherto had been undefeated by another program reached the following position (as black) against another North American entry, CHAOS:



Black is a pawn ahead, having greedily consumed white's king pawn, however he is behind in development, and in particular is not yet castled. White seizes the opportunity to make a decisive piece sacrifice. What is surprising about this offer is that it must have been based on a purely positional evaluation of the resulting position, since the program could not possibly have seen sufficiently far ahead to ascertain that he would eventually more than recoup his investment

16. Nd4 x e6! ...

This move has been praised as 'the finest ever played by a computer'

f7 x e6
17. Qe2 x e6 + Bd6-e7
18. Rd1-e1 Qb8-d8
19. Bc1-f4 ...

The threat is Bf4-c7

19. ... Ke8-f8
20. Ra1-d1 Ra8-a7
21. Rd1-c1 Nf6-g8
22. Rcl-d1 a6-a5

Black has no good moves, white has a stranglehold on the position

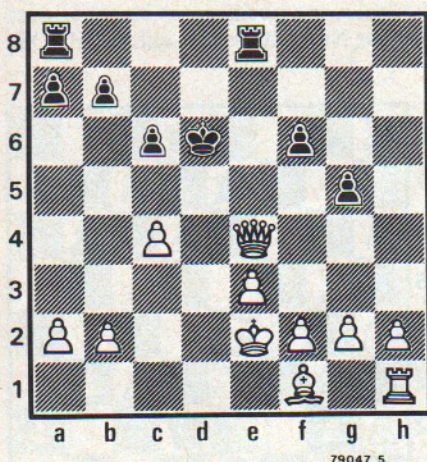
23. Bf4-d6 Be7 x d6
24. Qe6 x d6 + Ng8-e7
25. Na4-c5 Bg6-f5
26. g3-g4 Qd8-e8
27. Bb3-a4 b4-b3
28. g4 x f5

And white eventually won, although it took another 47 moves to do so.

Horizon effect v. snow-blindness

Selecting a suitable search depth also creates a number of problems when evaluating positions deep in the game tree. A particularly harrowing example of the fate that can befall a program when faced with a choice of equally promising continuations occurred in a -now notorious - game between two programs called COKO and GENIE

which was played during the second ACM tournament in 1971. After the first 27 moves the following position was reached with COKO (white) to play:



COKO thought for 120 seconds and offered a pawn to entice the black king out into the centre:

28. *c4-c5 + Kd6 x c5 ?*

Too greedy! COKO, having seen ahead the next 8½ moves, played:

29. *Qe4-d4 +*

And announced mate in 8!

29. . . . *Kc5-b5*

30. *Ke2-d1 + Kb5-a5*

31. *b2-b4 + Ka5-a4*

32. *Qd4-c3 Re8-d8 +*

33. *Kd1-c2 Rd8-d2 +*

34. *Kc2 x d2 Ra8-d8 +*

35. *Kd2-c2 Rd8-d2 +*

Black's last four moves are a classic example of a typical computer weakness which is called 'the horizon effect'. Since the program's evaluation function scores the mate, i.e. the loss of its king as being very much worse than anything else that can happen to it, it indulges in a rather disarming piece of self-deception; it attempts to postpone the evil hour by sacrificing whatever comes to hand and so push the mate beyond the horizon of its look-ahead! Two rooks down is better than mate it thinks, however it doesn't 'realise' that it cannot prevent mate anyway.

The horizon effect is an extremely difficult problem inherent in all programs, particularly those with a short look-ahead. Any combination or manoeuvre which is longer than the look-ahead will be misperceived by the computer. However, just for once, maybe the program knew what it was doing, for there then followed:

36. *Qc3 x d2 Ka4-a3*

Still after the pawns!

37. *Qd2-c3 + Ka3 x a2*

White now has a choice of two mates in one (*Bf1-c4, Qc3-b2*) and a large number of mates in 2, 3, 4 etc. Unfortunately, COKO seemed unable to distinguish between the value of so many promising lines, and it made a random choice between the mating continuations:

38. *Kc2-c1*

Black, not having much else to do played:

38. . . . *f6-f5*

39. *Kc1-c2 f5-f4*

40. *Kc2-c1 g5-g4*

41. *Kc1-c2 f4-f3*

42. *Kc2-c1 f3 x g2*

43. *Kc1-c2*

One can imagine the anguish of COKO's programmers

43. . . . *g2 x h1 = Q*

This is now COKO's last chance, does he take it?

44. *Kc2-c1*

Alas no. GENIE now played:

44. . . . *Qh1 x f1 +*

whereupon white's game started to fall apart. COKO's unfortunate masters could soon stand it no longer and resigned for their disgraced offspring.



Pruning the game tree

As was mentioned, a full-width search strategy to a depth of even a few ply rapidly generates an enormous number of terminal positions. However, in 1958, three researchers at the Carnegie Institute of technology, Alan Newell, John Shaw and Herbert Simon, published a paper which demonstrated that the number of positions which it was necessary to evaluate could be drastically reduced with the aid of a relatively simple algorithm. To understand how this is done let us look at the simple game tree of figure 2. If we propose a crude evaluation function of material balance, mobility (+0.1 for each legal move), centre control (+0.2 for each centre square, i.e. e4, d4, e5, d5, attacked) and king safety (defined as the number of moves required to castle: subtract 0.5 per move), we obtain the values shown.

To select its move the program first examines terminal positions 5 and 6, then backs up the smaller value to node 4 (+0.1), as explained earlier. The two positions descended from node 7 could then be evaluated, and the best

backed-up value for it obtained (-0.5). However, since the program will maximise node 3 (white to move), we know that the best backed-up value for it will never be less than +0.1, since the program would always select the branch leading to node 4. Thus, having found the value for node 8 (-0.2), the program can deduce that it is pointless to generate and evaluate node 9: the evaluation for node 8 is already smaller than that backed up to node 4. The same argument can be applied throughout the game tree, resulting in a substantial pruning in the number of nodes requiring evaluation.

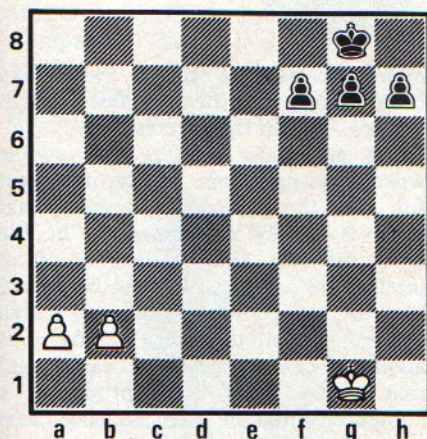
To obtain the full benefit of this procedure, it is important that the program examine the best moves first. Many moves fail to an immediate and obvious reply — the loss of one's queen for example. Clearly if the queen capture is generated and evaluated first, then it substantially reduces the number of nodes for subsequent evaluation. Modern programs all contain a number of 'heuristics' (rules of thumb) which provide the computer with information on the type of move it should examine first. One common heuristic involves the program storing refutation or 'killer' moves which were effective for positions earlier in the tree and testing to see whether they still work. Unfortunately, one effect of the capture heuristic is to make programs avid exchangers of pieces. Many programs dissipate an advantage by allowing the opponent to free a cramped game by trading off pieces. (See game 1 of Levy v. Chess 4.7.)

A number of additional techniques for speeding up the tree search have also been developed in recent years, and the full-width search has become a feasible proposition. However the fact remains that, with a type-A strategy, the program is searching blindly on a trial-and-error basis, generating and evaluating an enormous number of largely irrelevant positions. The computer is unable to formulate any sort of plan or, for that matter, recognise the plan of its opponent. It is at the mercy of the necessarily over-generalised positional factors of its evaluation function, and its vision is limited to a fixed-depth look-ahead. For this reason early programs in particular were atrocious at playing the endgame, often being unable to win such elementary positions as king and queen or rook against king. Unfortunately their human opponents were often unaware of this fact and resigned prematurely!

How (not) to play the endgame

Most evaluation functions are oriented towards opening- and middle-game features (such as development, control of centre, etc.), whereas the endgame demands the ability to perceive a winning process. Often the winning plan will take twenty or thirty moves to execute, effectively ruling out the possi-

bility of the program stumbling across it in a full-width search. To the human this presents no problem because it simply becomes a question of implementing an idea, manoeuvring a piece to a key square, etc. The computer however does not have ideas, so it just sits there churning through tens of thousands of positions which all look pretty much the same to it anyway. A commonly cited example of the problems presented by the inability of programs to apprehend the salient features of a position, combined with a necessarily limited look-ahead, is shown in figure 6.



79047 6

Any beginner faced with this elementary position would instantly recognise that the black king is too far away to prevent the white rook's pawn from queening. Unfortunately, if the program has a look-ahead of less than 9-ply it will fail to appreciate this fact, and assessing the position on the merits of material inequality, will decide that black has the advantage! Even with a 9-ply search it calculates the following variation: 1. a2-a4, h7-h5 2. a4-a5 h5-h4 3. a5-a6, h4-h3 4. a6-a7, h3-h2 + 5. Kg1 x h2. Black, by sacrificing the h-pawn has succeeded in pushing the pawn promotion over the program's horizon. However white will nevertheless select this line because it wins a pawn! The inability of the program to form a respectable plan is painfully embarrassing.

It seems likely that an alternative approach will have to be adopted for the endgame, and indeed promising work has been done in Russia on writing programs for specific types of endgame. David Levy lost a less well-publicised bet of a case of Scotch that the programmers of KAISSA would be unable to write a program which played the ending of king, rook and pawn against king and rook correctly for both sides before the end of 1975.

What of the future?

Despite the inherent problems of a Shannon type-A strategy, there is no doubt that programs employing this technique have been making progress over recent years, whereas the diffi-

culties involved in the development of a reliable plausible-move generator have remained largely intractable. In particular, Chess 4.7, the primary exponent of the type-A strategy, is gradually acquiring a rating near to that of an Expert of the US Chess Federation grading list, and more spectacularly has beaten an International Master under tournament conditions (as well as beating a Grandmaster in a blitz game) — see David Levy's article in this issue.

However these advances are to a certain extent due to progress in hardware — faster, more powerful computers — and more efficient programming techniques which increase the look-ahead of the program to a point where brute force exhaustive analysis is disguising its conceptual inadequacies.

In the endgame in particular much work remains to be done. The computer is at its weakest in quiet non-tactical positions where it cannot utilise the fact that, unlike humans, it never miscalculates a line, forgets about a piece *en prise* etc.

Nonetheless it cannot be denied that chess-playing computers are getting stronger and the best of them could defeat most average club-players. Estimates as to how long it will take before they play World Championship level chess are extremely difficult. The most popular guess is somewhere in the region of 10 to 20 years, although this may well prove to be wildly inaccurate (in 1958 Simon predicted that there would be a computer program as World Champion within 10 years).



Literature:

Bell, Alex G., 'The machine plays chess' Pergamon Press 1978.

Frey, Peter, 'Chess skill in man and machine'.

Springer Verlag, New York 1977.

Levy, David, 'Chess and computers' Batsford chess books, 1976.

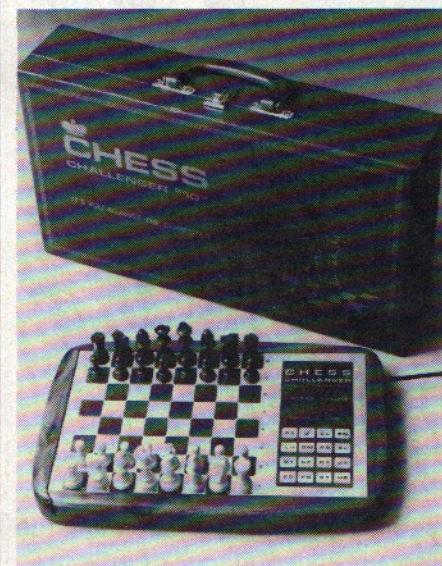
Shannon, Claude, 'Programming a computer for playing chess'.

Philosophical magazine, vol 41, pp 256-275, March 1950.

chess challenger 10 plays like a human

The introduction of Chess Challenger 10 is an excellent 'state of the art' example of the space-age technology and almost human capabilities that can now be built into these computerised board games. It features no less than 10 levels of play:

Level	Average Response Time
1. Beginner	5 seconds
2. Intermediate	15 seconds
3. Experienced	35 seconds
4. Advanced	1:20 minutes
5. Superior	2:20 minutes
6. Mate in Two (two move puzzles and end games)	1 hour
7. Postal Chess	24 hours
8. Expert	11 minutes
9. Excellent	6 minutes
10. Tournament Practice	3 minutes



The levels are interchangeable at any time and during any move of a game and the player can select offense (light pieces) or defense (dark pieces) at the touch of a key.

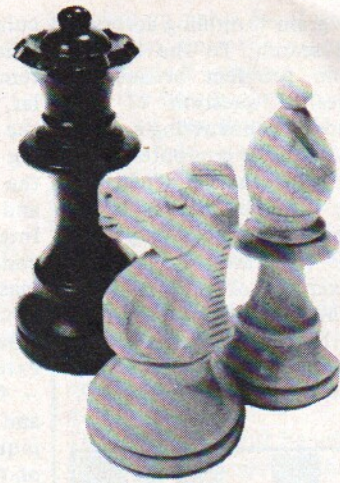
A new feature of Chess Challenger 10 is its ability to play and follow a patterned classic book opening, e.g. Sicilian, French, Ruy Lopez, Queen Gambit Declined and so on.

Computer technology is growing so fast that the microprocessor 'brain' in Chess Challenger 10 can now analyse up to 3,024,000 board positions before making its move — a logic capability equal to the instinctive ability of even very experienced players.

An override key permits the player to make multiple moves before the computer responds and also permits the addition or subtraction of any piece to either side. Ideal for cheating!

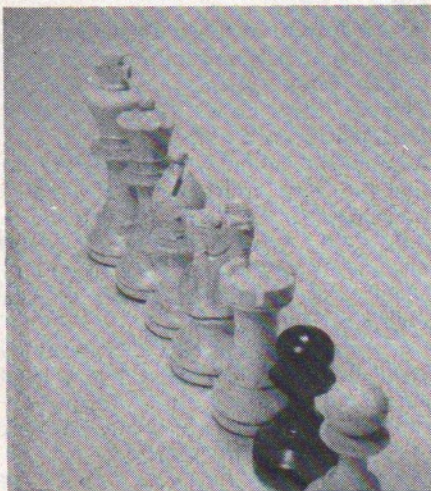
Chess Challenger 10 sells for £ 200.

how I beat the monster



Until quite recently, computer chess was regarded by even mediocre chess players as little more than a joke — 'Computers are such stupid things'! However, recent computer chess tournaments have demonstrated that the best programs are becoming quite good. Even so, a lingering doubt remains: one computer may be able to convincingly wipe up another, but how will it fare when confronted with a human player? Recently, Mr. Levy — an international chess master — was challenged by the reigning world champion computer. His description of the historical background and of the contest itself should prove of interest! Perhaps it should be noted, however, that Mr. Levy had an 'unfair advantage' in this contest: as an ex-computer programmer he has a fairly good idea of how his opponent 'thinks' . . .

David Levy



One evening during August 1968 I was playing chess at a cocktail party in Edinburgh. My opponent was John McCarthy, Professor of Artificial Intelligence at Stanford University, California, and one of the world's leading experts in his field. At that time I was the reigning Scottish Chess Champion.

I won the game against McCarthy who then remarked that although he was not strong enough for me there would be, within ten years, a computer program which could win a match against me. I was amazed by his suggestion because in the preceding two decades there had been very little progress made on computer chess, and the strongest programs were very, very much weaker than I was. We began to debate the point and when I realised that he was completely serious I suggested that we test our opinions with a £ 500 bet. Our host for the evening, Professor Donald Michie of the Department of Machine Intelligence and Perception at Edinburgh University, joined in our conversation and agreed to share the bet with McCarthy, each of them wagering £ 250 against me.

During the next few years the bet grew in size. Two more academicians joined the consortium, Seymour Papert from M.I.T. and Ed Kozdrowicki from the University of California at Davis. Donald Michie also increased his original stake to £ 500 and added a further £ 500 wager that if I did lose the original bet it would be to a program written by him or under his guidance. The total staked in the original bet was therefore £ 1,250.

One of the beneficial effects of this bet was that it created publicity and encouraged programmers to work on computer chess. During the decade following August 1968 computer chess became so popular that a number of tournaments were arranged in which all the competitors were chess programs. There is an annual competition in the U.S.A. and there have been two World Championships and one European Championship. Computer chess is growing in popularity at an amazing rate, and recently there was a tournament in London for chess programs running on

microprocessors (a similar event had been held in California a few months earlier). Why all this interest?

There are many reasons why people write chess programs. Firstly, it is great fun. But the principal purpose is that chess is widely considered to be the most difficult and challenging of all intellectual games and it can be argued that to play good chess requires a high degree of intelligence. Taking this argument one step further it can be said that if we succeed in producing a computer program that can play chess as well as a Grandmaster or even a World Champion, it will also be possible to write programs that will perform other intellectually difficult tasks in long range planning. Indeed, when a group of Artificial Intelligence biggies sat down some years ago to formulate a list of the aims of their science, one of their targets was a program that could win the World Chess Championship.

With the increased interest in computer chess there was a steady though undramatic increase in the strength of the best programs. Until late in 1976 computer chess was regarded by the chess playing community as little more than a joke, but suddenly everything changed. The leading American program, CHESS 4.6, won the class-B section at the Paul Masson chess tournament in Saratoga, California. This was the first time that a computer program had ever won an event intended for humans and it caused considerable consternation amongst some of the competitors, even though the programmers had announced in advance that they would forsake any prize money. The following February the same program won the Minnesota Open Championship. In March it demonstrated that it was at least as strong as I am at blitz chess, a form of the game in which each player must make all of his (or its) moves at great speed. I had never expected, when I made the bet in 1968, that computer programs would have made so much progress so quickly. In fact, I thought it unlikely that there would be a program strong enough to challenge me to a match, and I expected to win the bet by forfeit.

In April 1977 I was formally challenged

to play a match against CHESSE 4.6. It was to be a two game match, though if I won the first game the match would be over since in order to lose the bet I would have to lose the match by at least 1½ points to ½. Play took place under perfect conditions at Carnegie Mellon University in Pittsburgh, one of the leading centres for Artificial Intelligence. I won the first and only game of the match fairly convincingly, though at one time the program did have the advantage against me.

In December 1977 I was asked to play again, this time against KAISSE, written at the Institute for Control Science in Moscow. KAISSE had been World Computer Champion from 1974 to 1977 but I found it to be slightly weaker than CHESSE 4.6 and managed to win without much trouble.



By then the interest in my bet was really hotting up. It had only eight months to run and it soon became known that David Slate, one of the programmers of Northwestern University's CHESSE 4.6, was going over to part time work so that he could devote six man months to his program, in an attempt to produce my downfall. His partner, Larry Atkin, was working on a robot arm which would move the program's pieces and punch the button on the chess clock.

Shortly before the August deadline I was challenged to play a two game match at M.I.T. against an updated version of the program named MacHack VI, which was the world's strongest program at the time I first made the bet. MacHack was written by Richard Greenblatt and was running on some special purpose chess hardware, which enabled it to analyze 150,000 positions per second. Although this special analyzer could detect certain tactical traps, the program exhibited no more strategic understanding than CHESSE 4.6. I won the first game of the encounter and then played the second game, just for fun, and won that as well.

The end of August approached. I went from Boston to Toronto where I was about to face my final challenge. The hoped for version CHESSE 5.0 had not been completed in time, so my opponent was CHESSE 4.7, an upgraded 4.6. The program was running on a CDC Cyber 176 computer, the world's fastest commercially available machine.

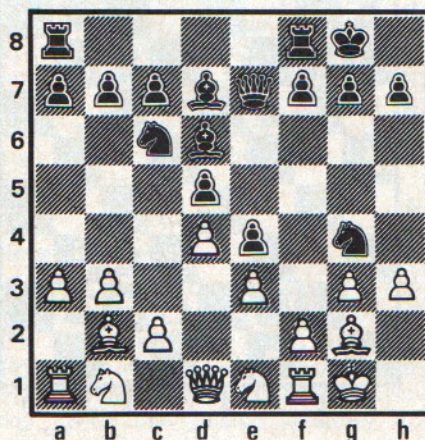
We played at the Canadian National Exhibition, a gigantic fair which takes place in Toronto at the same time each year. I was seated in an almost sound-proofed glass booth, wearing a dinner jacket. I played on a special chess board which had been designed and built by CDC consultant David Cahlander. This board could detect the movement of my pieces by means of magnetic sensitive switches beneath each square - the lead weights in the pieces had been replaced by magnets. Another feature of this board was a small red light on each square. When the program had decided on its move it would illuminate the lights on the 'from' square and the 'to' square, as well as those on the intervening squares.

The match was to be a six game encounter. Under the terms of the bet I would win if I scored 3 points or more. The program needed 3½ to beat me. In the very first game I suffered an extremely unpleasant shock after only twelve moves:

White: Levy

Black: CHESSE 4.7

- | | |
|-------------|--------|
| 1. g2-g3 | d7-d5 |
| 2. Bf1-g2 | e7-e5 |
| 3. d2-d3 | Ng8-f6 |
| 4. Ng1-f3 | Nb8-c6 |
| 5. 0-0 | Bc8-d7 |
| 6. b2-b3 | Bf8-c5 |
| 7. Bc1-b2 | Qd8-e7 |
| 8. a2-a3 | e5-e4 |
| 9. Nf3-e1 | 0-0 |
| 10. d3-d4 | Bc5-d6 |
| 11. e2-e3 | Nf6-g4 |
| 12. h2-h3?? | |



I took several minutes over this move, but no sooner had I made it on the board than the program, which thinks in its opponents' time, replied with ...

12. ... Ng4xe3!!

I had considered this move to be hopeless, because I had not seen the follow-up.

13. f2xe3 Qe7-g5!

And suddenly I realized that my position was in shreds. Black's queen threatens the pawns on e3 and g3, and once the queen gets to g3 Black will be able to capture the h3 pawn with its bishop. In short, White is helpless. But 'nil desperandum'.

14. g3-g4!

The best practical try.

14. ... Qg5xe3+

15. Rf1-f2!

I played this move because programs know that they should exchange material when they are ahead, so after ...

15. ... Bd6-g3

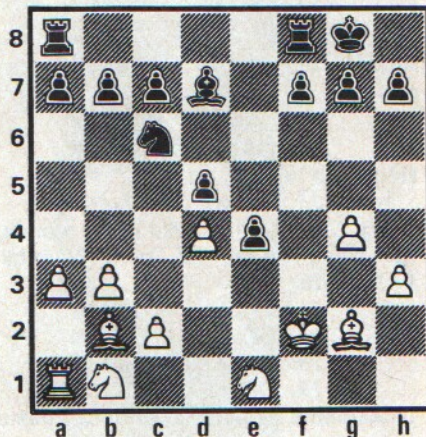
16. Qd1-e2

... instead of taking the exchange (16... Bg3xf2+) and then keeping the queens on so as to launch an attack against my king, the program played ...

16. ... Qe3xf2+

17. Qe2xf2 Bg3xf2+

18. Kglxf2



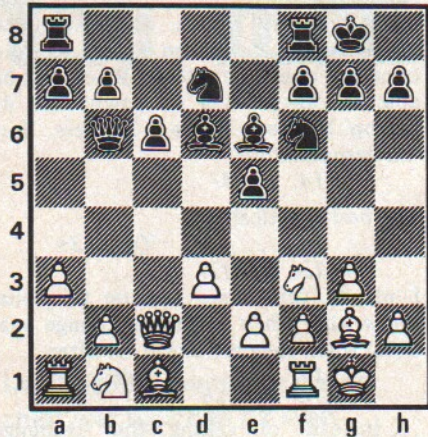
79037 - 2

and despite my material deficit I was able to draw the ending through a combination of resourcefulness (on my part) and ineptitude (by my opponent).

This was the first time that a computer program had ever drawn with an International Chess Master under strict tournament conditions. The final result of the match was a win for me by 3½ - 1½. Out of the next four games I scored three wins and one loss. I am unable to give all the games here, for reasons of space, so I shall invite the reader to examine only the most interesting game of the match. At first I shall keep you in the dark as to which of us was White and which of us won the game. Please acquire pen and a small piece of paper before you play through this game, so that you can perform a little experiment.

- | | |
|-----------|--------|
| 1. c2-c4 | Ng8-f6 |
| 2. a2-a3 | c7-c6 |
| 3. d2-d3 | d7-d5 |
| 4. Qd1-c2 | d5xc4 |
| 5. Qc2xc4 | e7-e5 |
| 6. Ng1-f3 | Bf8-d6 |

- 7. g2-g3 Bc8-e6
- 8. Qc4-c2 Nb8-d7
- 9. Bf1-g2 0-0
- 10. 0-0 Qd8-b6



79037 - 3

Now, write down who you think was White: Man or machine?

- 11. Nb1-d2

Preventing 11...Be6-b3.

- 11. ... Qb6-c5
- 12. Qc2-b1 h7-h6

Preventing 13 Nf3-g5 followed by Nd2-e4 and Bc1-e3, with an active position.

- 13. b2-b4 Qc5-b5
- 14. Qb1-c2 Nd7-b6

Hoping to jump in on a4.

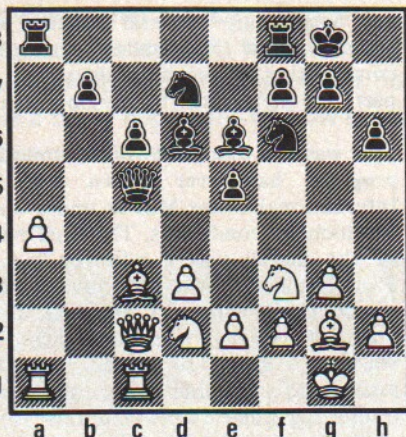
- 15. Bc1-b2 a7-a5

If 15...Nb6-a4 16 Nd2-c4!, winning the pawn on e5 (if 16...Na4xb2? 17 Nc4xd6).

- 16. a3-a4 Qb5-a6
- 17. b4xa5 Qa6xa5
- 18. Bb2-c3 Qa5-c5
- 19. Rf1-c1

Threatening 20 Bc3xe5, winning a pawn.

- 19. ... Nb6-d7



79037 - 4

Defending e5. Now, write down once again who you think is White.

- 20. a4-a5 Qc5-a7
- 21. Qc2-b2 Nf6-g4
- 22. Nd2-e4 Bd6-c7
- 23. h2-h3

Now, if the knight on g4 retreats to f6, White can simply capture the pawn on e5.

- 23. ... f7-f5

The white knight on e4 cannot move because of the threat of 24...Qa7xf2+, and so the following sequence is forced.

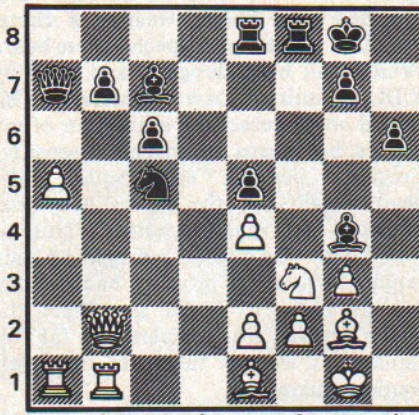
- 24. h3xg4 f5xe4
- 25. d3xe4 Be6xg4
- 26. Bc3-e1 Nd7-c5

Attacking the e4 pawn.

- 27. Rc1-b1

White is happy with 27...Nc5xe4 28 Qb2xb7.

- 27. ... Ra8-e8



79037 - 5

The pawn on e5 was attacked twice. Now who do you think was White?

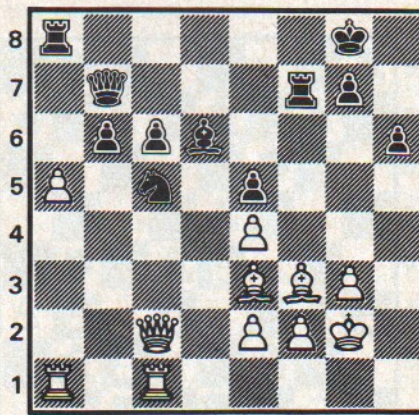
- 28. Be1-d2 Rf8-f7
- 29. Bd2-e3 Bc7-d6
- 30. Qb2-c2 Bg4xf3
- 31. Bg2xf3

Threatening 32 Bf3-h5.

- 31. ... Re8-a8
- 32. Rb1-c1 b7-b6

White has considerable pressure on the Q-side but if 33 a5xb6 Qa7xa1! 34 Rc1xa1 Ra8xa1+ 35 Kgl-g2 Ral-a5, and it is not clear how White makes progress.

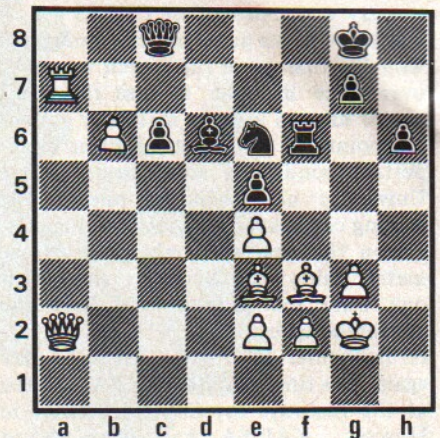
- 33. Kgl-g2 Qa7-b7



79037 - 6

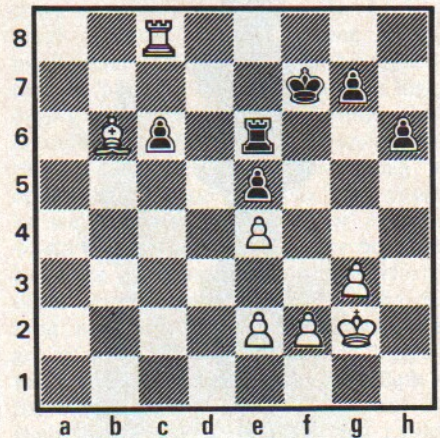
Write down who you think is White.

- 34. a5xb6 Ra8xa1
- 35. Rc1xa1 Nc5-e6
- 36. Ral-a7 Qb7-c8
- 37. Qc2-a2 Rf7-f6



79037 - 7

- 38. Ra7-a8 Bd6-b8
- 39. Bf3-g4 Kg8-f7
- 40. Qa2-a7+! Bb8xa7
- 41. Ra8xc8 Ba7xb6
- 42. Bg4xe6+ Rf6xe6
- 43. Be3xb6 Resigns



79037 - 8

For the last time, who was White? Now turn the page.



I was White. Many of you probably guessed, at least once during the game, that the program was white. The point of this experiment is that the program plays chess so well that it is almost impossible to tell for certain who is White and who is Black, and the program must therefore be considered to have some sense to be intelligent. The English mathematician Alan Turing devised a test for machine intelligence and our experiment here is a kind of Turing test for chess programs. One might argue that CHES 4.7 is definitely intelligent because it could take 1 1/2 points off me in a five game match, but since the program 'thinks' by examining hundreds of thousands of positions every time it makes a move (15...a7-a5 required in 906,758 positions) its method of play can hardly be called intelligent in the human sense.

universal digital meter

digital replacement for pointer instruments

In all fields of electronic measuring, the conventional pointer instrument is becoming outmoded. In many applications the inaccurate, mechanically delicate and short-lived electro-mechanical panel meter is being replaced by a robust and clearly legible digital display. Until recently, conventional meters were cheaper; however, things are changing. The delicate mechanical system is becoming more expensive (even when 'Made in Hong Kong'), whereas its digital counterpart is becoming cheaper - 'Made in Singapore'? Goodbye magnet - hello LED!

It is perhaps an exaggeration to assume that our old and trustworthy friend, the mechanical pointer instrument, is soon to disappear completely. It still has some advantages over present-day digital displays. In some applications, especially where absolute accuracy is not so important - as is often the case! - the analog pointer instrument is still preferable. Calibration procedures involving accurate recognition of peaks or dips in a voltage level (or any other level, for that matter) can be carried out with greater ease with a swinging pointer than with a rapidly changing numerical display. The same is true when it comes to detecting sudden (and sometimes unexpected) fluctuations in levels - a pointer jumping over a scale, or even wrapping itself round the pin, is decidedly more noticeable than a digital display changing from 153 to 999.

However, digital meters have their advantages. The reading is clear and precise; the scale is usually clearly indicated; the unit is less sensitive to mechanical shock (see figure 1). Furthermore, the illuminated digits can be clearly read in most lighting conditions. When it comes to accuracy, a digital display can easily beat its analog rival. At best, on a pointer instrument with a full-scale calibration of 1000 units a reading of, say, 615 can be obtained: three digits. On a digital instrument, such as the 1/4 GHz frequency counter (Elektor, June 1978), it is possible to obtain a reliable reading in six digits (e.g. 10.7234 MHz) where only the last digit is doubtful.

How they work

If digital instruments are so much better, why aren't they used more often? The reason is simple: they are more difficult to design. For an analog (pointer) instrument, some kind of conversion from one analog quantity to another is required (from current, say, to position of a pointer on a scale). In many applications, this conversion is relatively straightforward. Digital instruments, on the other hand, require a more complicated conversion: the analog quantity must be converted into a digital value ('digitalised', to coin a

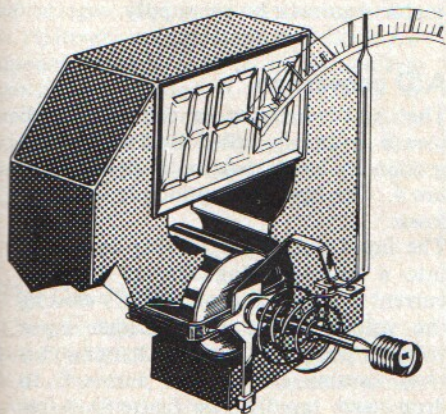
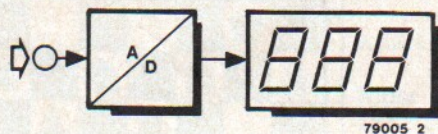
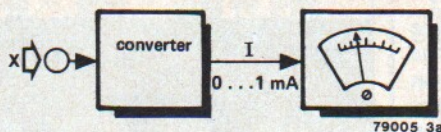


Figure 1. An analog measuring instrument (figure 1a) is not as easy to read as a digital instrument (figure 1b).

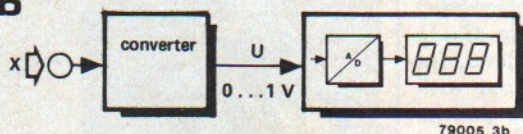
2



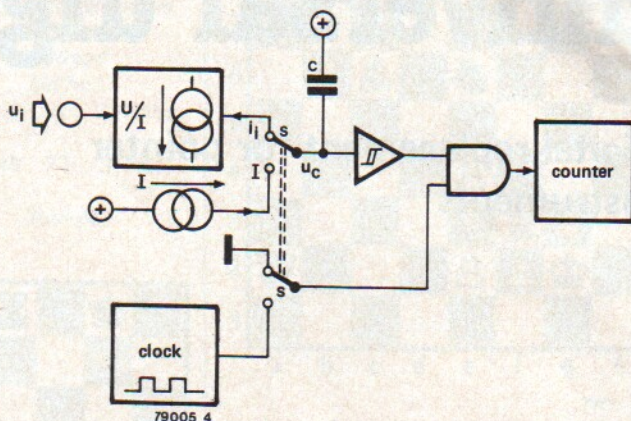
3a



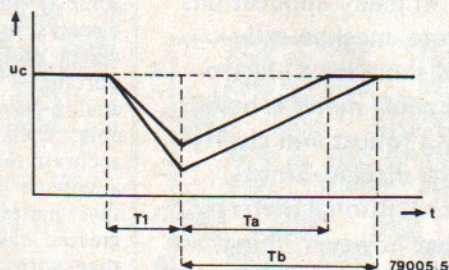
3b



4



5



horrible word). The unit which performs this conversion is aptly named: 'Analog-to-Digital converter', or A/D converter for short.

This A/D converter is an essential part of most digital meters — the only exception being meters that measure digital quantities. A chain is never stronger than its weakest link, and the performance of a digital meter is usually determined by the A/D converter. As more and more 'digits' are desired, the demands placed on this component become increasingly severe: accuracy, linearity, range, stability and resolution — all to within a ten-thousandth of one percent for a six-digit display!

The high demands placed on an A/D converter are providing some of the best brains in the electronics industry with a full-time job — witness the proliferation, in recent years, of new conversion principles, new designs, new hybrid and integrated circuits.

Circuits for A/D converters tend to be complicated. Any attempt to build them using discrete components soon gets out of hand. Integrated circuits are the obvious answer, and the number of suitable ICs presently available is staggering — with more being introduced almost every day. As IC technology progressed to medium and even large scale integration (MSI and LSI), it became tempting to go one step further: complete digital measuring instruments on a single chip became available. Rapidly falling prices — a welcome by-product of advances in semiconductor technology — now seem to be hastening

the final demise of the pointer instrument: a digital meter is now actually cheaper than its analog counterpart.

A universal digital meter

Many analog measuring instruments work on the principle that the quantity to be measured (voltage, resistance, capacitance, magnetic field strength, sound level, wind speed and so on) is first converted into an electric current; this current is then displayed on a milliammeter. In a sense, then, a milliammeter is a universal analog meter: once the quantity to be measured has been converted into a current, the pointer instrument takes care of the actual measurement and display.

It would be useful to have a universal meter with a digital display: a universal digital meter. Such an instrument would be capable of measuring some basic analog quantity (such as current or voltage) and displaying the result in digital form. Any other analog quantity can then be measured in the usual way, using suitable converters in conjunction with the universal digital meter.

This idea is illustrated in figure 3. The traditional system is shown in figure 3a: a 'universal analog meter' preceded by a suitable converter. The input quantity, be it ohm, candle, apostilb or pascal-second (yes, they all exist), is converted into a current and displayed on the pointer instrument. Figure 3b represents the alternative: again, the analog input quantity is first converted (into voltage,

say) and then displayed — this time on a 'universal digital meter'.

The second section in figure 3b is the main subject of this article. Recently, several ICs have been introduced that perform almost all the functions required for a universal digital meter. Furthermore, they are so cheap that the complete unit can be built for practically the same price as a conventional pointer instrument.

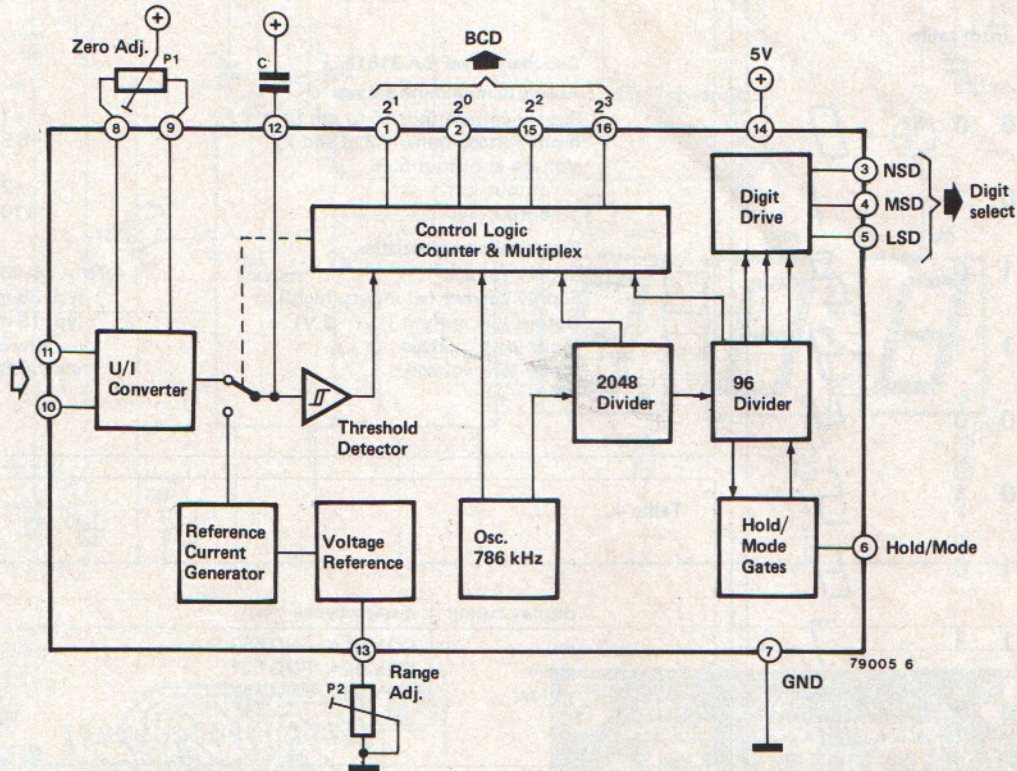
One of these ICs is the RCA type CA 3162E. This integrated circuit accepts an analog (voltage) input and delivers an equivalent three-digit output in multiplexed BCD code. The IC is intended to work in conjunction with a BCD to seven-segment decoder/driver, the CA 3161E. Only a few more components are required for a universal digital meter that will out-perform even a good pointer instrument. The only disadvantage, in comparison with a pointer instrument, is that the digital meter requires a power supply.

A/D conversion

The A/D converter in the CA 3162E uses a principle called dual-slope integration. A block diagram is given in figure 4. The operating principle is as follows:

The input voltage, u_i , is first converted into a corresponding current (i_i). This current charges a capacitor C , causing the voltage u_c to drop. Larger input voltages produce a greater charging current, causing the voltage across C to drop more rapidly (see figure 5). After

6



a certain fixed time, T_1 , the switch is operated. The capacitor is now discharged by a fixed current, I ; the discharge time is therefore proportional to the initial voltage drop across the capacitor. Again, this can be seen in figure 5: two input voltages, u_a and u_b (where u_b is the larger of the two) have caused initial voltage drops; the resultant discharge times, T_a and T_b , are proportional to these voltage drops. To sum it up: i_i is proportional to u_i ; $u_{c, \text{minimum}}$ is proportional to i_i ; the discharge time is proportional to $u_{c, \text{minimum}}$. . . in other words, the discharge time must be proportional to the input voltage! During the discharge period, the output from a 'clock generator' is counted; at the end of the period, the total count must therefore correspond to the input voltage level. Which is what A/D conversion is all about.

Dual-slope integration has a number of advantages. The value of the capacitor is relatively unimportant; the clock frequency doesn't need to be particularly constant, provided it is also used to define the initial charging time (T_1); the measurement itself is integrating, so that noise and the like tend to be averaged out.

The CA 3162E

The simplified internal block diagram of the CA 3162E is given in figure 6. The U/I converter, reference current generator, threshold detector and 786 kHz

Table 1.

A/D converter CA 3162E

Absolute maximum ratings

Supply voltage (pin 14 to pin 7)	+ 7 V
Input voltage (pins 10 and 11 to 7)	± 15 V

Electrical characteristics (+ $U_b = 5$ V; P1 centered; P2 set to 2k4)

Supply voltage	4.5 . . . 5.5 V
Supply current	max. 17 mA
Input impedance	typ. 100 M Ω
Input bias current	typ. -80 nA
Unadjusted zero offset	± 12 mV
Unadjusted gain (display for $U_{in} = 900$ mV)	846 . . . 954 mV
Linearity	± 1 count
Accuracy	0.1% ± 1 count
Common-mode input voltage range	± 200 mV
BCD sink current (pins 1, 2, 15, 16)	min. 0.4 mA
Digit select sink current (pins 3, 4, 5)	min. 1.6 mA
Zero temperature coefficient	typ. 10 μ V/°C
Gain temperature coefficient ($U_{in} = 900$ mV)	typ. 0.005%/°C

Figure 2. An essential part of a digital meter is the A/D converter. This is the most difficult part to design . . .

Figure 3. Many measuring instruments consist basically of a 'quantity'-to-current converter followed by a milliammeter (figure 3a). The same principle can be used for digital measuring, provided a 'universal digital meter' is available (figure 3b).

Figure 4. Simplified circuit diagram of the 'dual-slope' A/D converter.

Figure 5. During each conversion cycle, the voltage u_c in figure 4 first drops at a rate determined by the input voltage level; it then rises at a fixed rate. Since T_1 is constant, the rise time (T_a or T_b) must be proportional to the input voltage.

Figure 6. Functional block diagram of the CA 3162E.

oscillator will be recognised from figure 4; the gating, counter and switch from figure 4 are all contained in the 'control logic, counter and multiplex' block in figure 6. The counter actually consists of three BCD counters, one for each digit; the outputs appear at the BCD output in turn (multiplex operation). Simultaneously, the corresponding 'digit enable' output goes low. The abbreviations MSD, NSD and LSD stand for, respectively: Most Significant Digit, Next Significant Digit and Least Significant Digit - from left to right in the three-digit number.

The various timing intervals are derived from the 786 kHz oscillator. Division by 2048 provides the multiplex frequency: 384 Hz. Further division by 96 gives the conversion frequency, 4 Hz; in other words, four measurements per second.

Table 2.

CA 3161E truth table

0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	-
1 0 1 1	E
1 1 0 0	H
1 1 0 1	L
1 1 1 0	P
1 1 1 1	

Table 3.

Decoder/driver CA 3161E

Absolute maximum ratings

Supply voltage (pin 16 to pin 8)	+7 V
Input voltage (pins 1, 2, 6 and 7)	+5.5 V
Voltage at output pins:	
output 'off'	+7 V
output 'on'	+10 V

Electrical characteristics

Supply voltage	4.75 . . . 5.25 V
Supply current (all inputs 'high')	typ. 35 mA
Output low current ($U_O = 2 V$)	typ. 15 mA
Input 'high' voltage	min. 2 V
Input 'low' voltage	max. 0.8 V

Table 4.

display colour	display types
red	CQY 91A, FND 557
green	CQY 92A, FND 537
yellow	CQY 93A, FND 547

Table 5.

f.s.d.	R7	+ R7 (dotted)	R8	division ratio
1 V	wire link	+ wire link	wire link	1.00
10 V	820 k	+ 82 k	100 k	10.02
100 V	820 k	+ 160 k	10 k	99.00
100 V	1 M	+ wire link	10 k	101.00
100 V	560 k	+ 120 k	6k8	101.00
100 V	470 k	+ 82 k	5k6	99.57
100 V	560 k	+ 3M3	39 k	99.97
1 A	wire link	+ wire link	1 Ω	—
100 mA	wire link	+ wire link	10 Ω	—
10 mA	wire link	+ wire link	100 Ω	—
2 mA*	wire link	+ wire link	470 Ω	—

* When used in conjunction with the AC millivoltmeter.

This low conversion rate is only obtained with pin 6 floating or connected to supply common; connecting this pin to half-supply (2.5 V) stops the conversion, but the display continues ('hold' mode); with pin 6 connected to positive supply, the conversion rate becomes 96 Hz.

The permissible input voltage range is -99 mV to +999 mV. In conjunction with the companion decoder/driver, underranging is indicated by a '----' display and overranging by 'EEE'. Negative voltages are indicated with a minus sign, e.g. '-55'.

The most important specifications of the CA 3162E are listed in table 1.

The CA 3161E

The CA 3161E is a BCD to seven-segment decoder/driver, ideally suited

to operate in conjunction with the CA 3162E. The inputs are TTL compatible, and the segment outputs are buffered. The output buffers operate as current sinks, so the seven-segment LED displays can be connected direct to the IC, without any need for current-limiting resistors.

The IC is pin-compatible with well-known BCD to seven-segment decoders, such as the 7447 and 74247. A BCD input produces the digits from 0 to 9, as is to be expected; the remaining binary numbers in a 4-bit code also provide useful displays, as illustrated in table 2. The main electrical characteristics are given in table 3.

The circuit

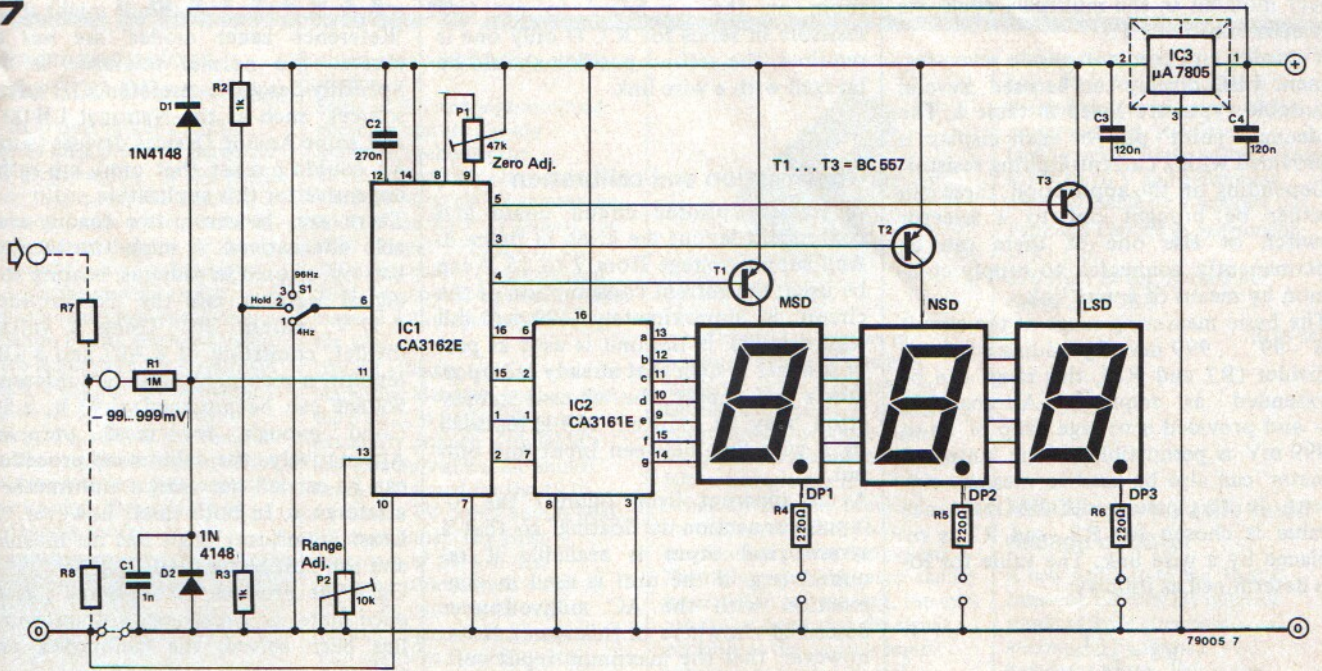
The complete circuit is given in figure 7. As can be seen, the two ICs and three

displays together form most of the circuit.

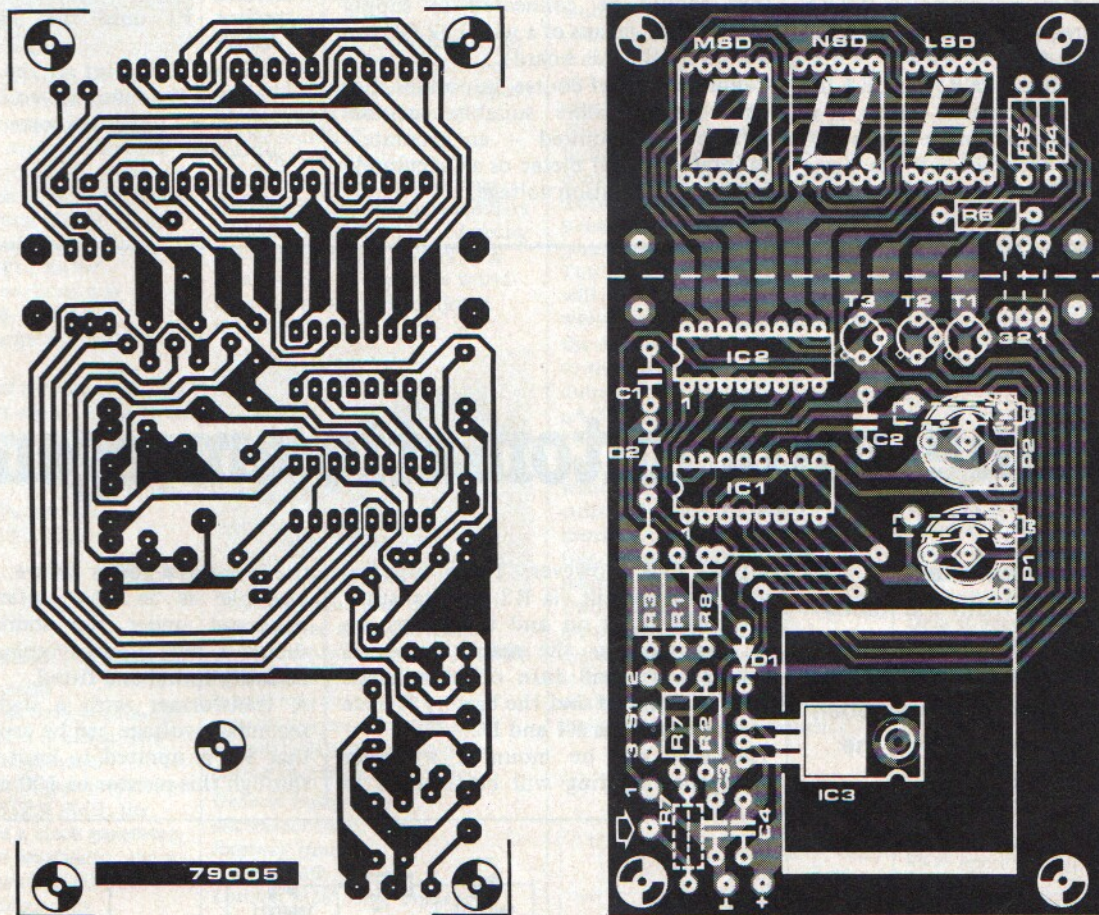
The analog input is applied, via R1, to the A/D converter IC. Two diodes, D1 and D2, provide input protection; C1 helps to keep the input 'clean' — the IC is designed to cope with a DC input! Three operating modes can be selected by means of S1: conversion rate 4 Hz (position 1); hold (position 2); conversion rate 96 Hz (position 3). C2 is the timing capacitor (C in figure 6); the two calibration potentiometers will be discussed later.

The BCD outputs from IC1 are connected to the corresponding inputs of IC2: the BCD to seven-segment decoder/driver. The outputs of the latter IC are connected direct to the corresponding segments of the three displays. The three digit-select outputs from IC1 are

7



8



Parts list.

Resistors:

- R1 = 1 M
- R2, R3 = 1 k
- R4 ... R6 = 220 Ω
- R7, R8 = see table 5
- P1 = 47 k
- P2 = 10 k

Capacitors:

- C1 = 1 n
- C2 = 270 n
- C3, C4 = 120 n

Sundries:

- cooling clip for IC3
- S1 = single-pole three-way

Semiconductors:

- T1 ... T3 = BC 177, BC 557 or equ.
- D1, D2 = 1N4148
- IC1 = CA 3162E
- IC2 = CA 3161E
- IC3 = μA 7805
- DP1 ... DP3 = see table 4

Figure 7. Complete circuit diagram of the universal digital meter.

Figure 8. Printed circuit board and component layout for the complete unit (EPS 79005).

used to enable the displays at the correct moment in the multiplex cycle, via transistors T1 . . . T3.

Virtually any common-anode seven-segment LED display can be used. Several suitable types are listed in table 4. The 'decimal point' pin for each display is provided with a current-limiting resistor. Depending on the application, these can either be brought out to a selector switch or else one of them can be permanently connected to supply common by means of a wire link.

The basic measuring range of the circuit is $-99 \dots 999$ mV. By adding a voltage divider (R7 and R8), this range can be extended as required. Alternatively — and provided a voltage drop of up to 999 mV is permissible! — the 'universal meter' can also be used to measure current. In this case a suitable resistance value is chosen for R8, and R7 is replaced by a wire link. The value for R8 is determined as follows:

$$R8 = \frac{1}{I_{f.s.d.}}$$

where $I_{f.s.d.}$ is the desired full-scale current reading. For instance, if a $50 \mu\text{A}$ instrument is required, the correct value for R8 would be 20 k.

Table 5 gives values for R7 and R8 for several voltage and current ranges. It is advisable to use precision resistors (1% tolerance): the accuracy of the basic unit is $0.1\% \pm 1$ mV and the linearity

is typically within 0.1 mV! There is room on the p.c. board to use two resistors in series for R7. If only one is required, the second position should be bridged with a wire link.

Construction and calibration

A suitable printed circuit board and component layout are given in figure 8. Any supply voltage from 7 to 15 V can be used; the current consumption of the circuit is approximately 200 mA (all segments lit). If the unit is used as part of a larger system that already incorporates a 5 V supply, the 'on-card stabilisation' may be omitted: IC3 is replaced by a wire link between input and output.

As is apparent from figure 7 the '0' input connection is floating, so that a symmetrical input is available if required (e.g. if the unit is used in conjunction with the AC millivoltmeter described elsewhere in this issue). Note, however, that the maximum input voltage range may not be exceeded! For most applications, the '0' input connection should be connected to supply common by means of a wire link (shown dotted on the p.c. board).

Calibration is, of course, important. For best results, some suitably accurate reference is required — an accurately calibrated digital meter or an accurately specified calibration voltage.

Finding a suitable reference voltage source is not as easy as one might think. 'Reference zener diodes' are *not* accurate: the normal tolerance is 5%. Specially-designed reference voltage sources, such as the National LH 0070 and some Analog Devices devices (sorry, we couldn't resist that one), are rather expensive for this application.

There are, however, two readily-available alternatives. A miniature mercury battery, as used in cameras, hearing aids, digital watches and the like produces 1.37 V, within 3%. Using a voltage divider, consisting of a 4k7 and a 10 k resistor, a reasonably accurate reference voltage can be obtained: 0.93 V, $\pm 5\%$. Good enough for most purposes. Alternatively, the calibration procedure can be carried out using a multimeter as a reference. In both cases, however, the Least Significant Digit has no meaning and can best be omitted.

Once the problem of obtaining a reference meter or a reference voltage source has been solved, the calibration procedure is easy:

- short the input to ground (a wire link across R8);
- adjust P1 until the displays read '000';
- remove the short at the input, and connect the reference voltage source;
- adjust P2 until the correct display is obtained.

lighting unit automatic emergency

This unit charges a nickel-cadmium battery from the mains to provide a standby power supply for emergency lighting in the event of a mains failure. When the mains supply drops out, the lighting is switched on automatically.

The circuit of the unit is extremely simple. Tr1, D1 and C1 provide a half-wave rectified and smoothed DC supply of approx. 6 V, which is used to continuously charge the Ni-Cad battery at about 100 mA via R1 and D2. A 2 Ah Ni-Cad can safely be charged at this rate.

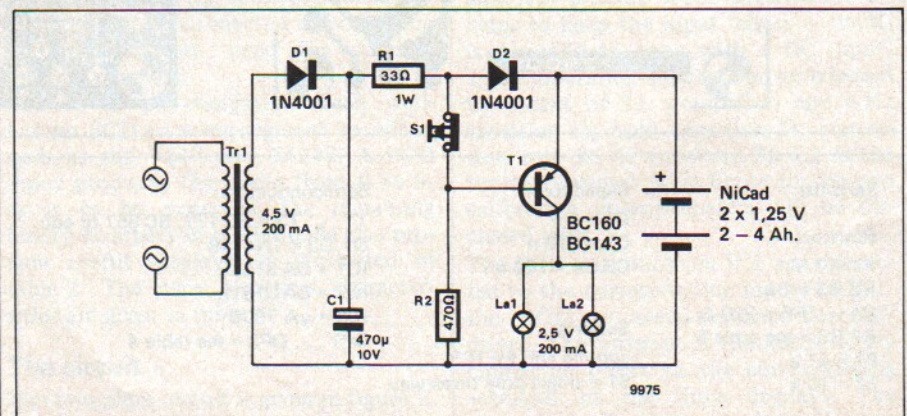
The voltage drop across D2 reverse-biases the base-emitter junction of T1, so that this transistor is turned off and the lamps are not lit. When the mains

supply fails, however, T1 is supplied with base current via R2; the transistor therefore turns on and the lamps are lit. As soon as the mains supply is restored, T1 will turn off, the lamps are extinguished and the battery is once more charged via R1 and D2.

The unit can be mounted wherever emergency lighting will be required in

the event of a power failure. An obvious example is in that infamous dark cupboard under the stairs, so that, should a fuse blow, a replacement can be easily found and fitted.

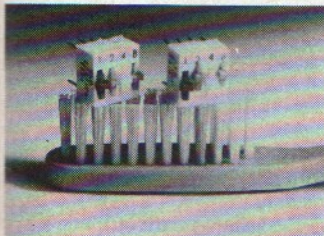
A transformer with a slightly higher secondary voltage can be used, provided that R1 is uprated to limit the current through this resistor to 100 mA.



MARKET

Number and colour coded BCD DIL switches

Erg BCD dual in-line switches offer an ideal means of hardware BCD programming. Of low profile (body height only 7.9 mm maximum) each switch status is clearly seen at a glance by the position of colour coded arrow heads on the moving switch elements that stand out against the white bodies. Each individual switch is numbered in a standard 1, 2, 4, 8 coding. The switches may be set up with the aid of a small probe, such as the blade of a small screwdriver and, since the switching members have a positive detent action, they cannot be accidentally moved.



Capable of switching 1 μ V to 100 V, 1 μ A to 1 A up to 10 VA, Erg BCD dual in-line switches have an initial contact resistance of only 8 m Ω (typical). A contact resistance repeatability of ± 1 m Ω (measured at only 10 mV/10 mA over 100 operations) is usual. Tested to BS2011 Ea for vibration, the switches will operate reliably over a temperature range of -55°C to $+100^{\circ}\text{C}$.

Free samples of the Erg BCD dual in-line switches are available on request.

*Erg Industrial Corporation Limited,
Luton Road, Dunstable,
Bedfordshire LU5 4LJ*

(978 M)

sound generation and on-screen scoring.

Some of the cartridge-mounted microcircuits are already available, including the 8610 'Supersport' (20 games), the 8765 'Motorcycle' (8 games) the 8603 'Road Race' (3 games), the 8607 'Target' (12 games), the 8606 'Wipeout' (24 games) and 8605 'Warfare' (10 games) - with more to follow before the end of the year.

David Letheren, GIM's Consumer Marketing Manager, believes that the SYSTEM 8601 will prove extremely popular with OEM's and amateurs alike, the launch being well timed for the 1978 Christmas TV games buying peak. He comments: 'The chief advantage of the low cost programmable system is that it offers the consumer a large number of game combinations with cartridge flexibility at a console price of approximately one-half that of the programmables currently in the marketplace.

We also intend to consolidate our market lead by adding between four and six additional cartridges to the system over the next twelve months.'

In 1976 GIM introduced the AY-3-8500, which has become the dedicated video game industry standard. Since then the company has dominated the market by a combination of aggressive worldwide marketing and continual innovation.



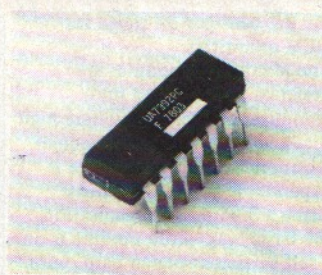
The development of the 8601 system came after extensive consumer preference studies. With several of the major games manufacturers already introducing models using this system GIM's marketing plans appear to have been justified.

*General Instrument Microelectronics Ltd.,
Regency House,
1-4 Warwick Street,
London W1R 5WB, England*

(979 M)

DC motor speed control

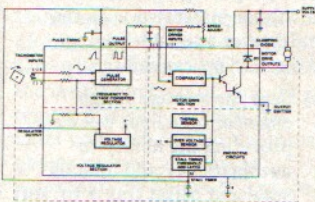
Fairchild's proprietary $\mu\text{A} 7392$ 14-pin DIP DC motor speed control circuit is designed to provide precision, closed-loop,



speed control of motors in systems where a tachometer reference signal is available as an indication of speed. It is ideal for design situations where current requirements are either less than 300 mA or greater than 2 A (when drive can be provided through an external power transistor or power darlington). The tachometer frequency can be generated in any manner, the only constraint being that the signal available at the device's input terminals exceeds 100 mV p-p. Possible types of tachogenerator that can be used include; a multiple pole motor winding, an optical pick-up from the motor's shaft or an optical or magnetic pick-up from a tape recorder capstan or record turntable.

The $\mu\text{A} 7392$, on receipt of the tachogenerator signal, first converts it into a pulse with a defined width and amplitude, the pulse is then integrated to generate a sawtooth waveform. This sawtooth is then compared with a DC reference and a pulse width modulated signal generated the duty cycle of which is related to the error signal. Average output current available from the $\mu\text{A} 7392$ is up to 300 mA.

The motor inductance provides adequate smoothing so ensuring what is, essentially, a direct current through the motor, provided the tachometer frequency is a sufficiently large multiple of the motor speed. Two distinct design advantages are offered by the $\mu\text{A} 7392$ system. Firstly, speed regulation is independent of the amplitude of the tachometer signal - it depends only on the frequency.



Secondly, at higher battery voltages the system is more efficient than the equivalent DC control system. This results in extended life for battery powered equipment. Specific design features include precision performance (frequency-to-voltage conversion

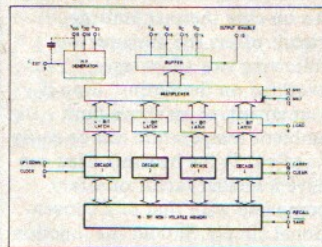
stability is typically 0.1% for V+ from 10 V to 16 V); on-chip thermal shutdown, over-voltage protection and 'stalltimer' facility; wide supply voltage range 6.3 V to 16 V and a clamping diode available on a separate pin.

*Fairchild Camera & Instrument (UK) Ltd.,
230 High Street, Potters Bar,
Herts, EN6 5BU*

(976 M)

MNOS non-volatile quad decade counter

A new addition to the 'Novol' (non-volatile MNOS) range of standard logic circuits is announced by Plessey Semiconductors. This is the MN9105 which comprises a 4-decade BCD up/down counter with the output of each decade addressed from two input pins and available on a common 4-bit data highway.



In parallel with an MOS counter is a 16-bit MNOS memory into which the contents of the counter can be written by applying a SAVE signal to the circuit. When this data has been written into the memory it is retained even in the absence of applied power, and then it can subsequently be recalled from the memory to preset the counter.

Data storage in the absence of applied power is guaranteed for at least one year at temperatures up to 70°C , and the guaranteed number of write operations is 10^6 . The device has a count frequency range from DC to 250 kHz.

A major feature of the MN9105 is that it requires only normal MOS operating supplies of +5 volts and -12 volts. All inputs and outputs are TTL/CMOS compatible.

The MN9105 has a wide range of applications, for example as replacements for electro-mechanical batch counters in vending machines, or time elapse indicators.

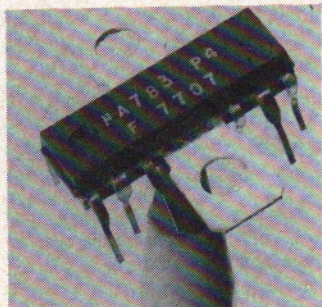
*Plessey Semiconductors,
Cheney Manor,
Swindon, Wiltshire, SN2 2QW*

(985 M)

MARKET

9 Watt audio amplifier

A proprietary Fairchild design the μ A 783 audio power amplifier is designed for high voltage (24 V) applications driving 8 and 16 ohm loads. Encapsulated in the standard 12-pin package two heatsink configurations are available. Designed for use as a low frequency class B power amplifier it can provide 9 W into an 8 ohm load (typically).



The μ A 783 is able to operate from a wide supply voltage range, with a maximum of 30 V. A high output current (repetitive) capability of 2.5 A is also exhibited by the device.

An on-chip thermal limiting circuit offers the designer the following two advantages; 1) an overload on the output, even if permanent, or an above-limit ambient temperature can be easily handled, 2) the heatsink used can have a smaller factor of safety compared with that of a conventional circuit. Should the junction temperature rise too high, power output, power dissipation and the supply current decrease so protecting the device.

Typical applications for the μ A 783 include tv audio circuits, inexpensive radio receivers etc. A design point worth noting is that by operating audio amplifiers at higher voltages simplifies power supply filtering problems.

Fairchild Camera & Instrument (UK) Ltd,
230 High Street, Potters Bar,
Herts EN6 5BU

(925 M)

High speed 128 k word core memory

Dataproducts (Dublin) Limited announce the availability of a new 128 k, 18 bit word core memory module. To be known as Maxi-store, the new memory module has been designed to combine high speed access time with mass storage — a 325 nanosecond access time and 750 nanoseconds cycle time. Cost per bit with Maxi-store is in

the 0.2 cent per bit range for OEM quantities.

The Maxi-store modules are designed for mini and midi computer applications where high speed large storage is a principal requirement. The Maxi-store is expandable to 1024 k words. Using a 3 wire, 3D organisation, the basic Maxi-store module is on a self sufficient planar card, with the address, data registers timing and control logic. The module operates in the read/restore, clear/write and read/modify/write modes. It requires only two voltages: +5 volts DC and +15 volts DC.

Up to 4 Maxi-store modules can be housed in a 10½" (26.7 cm) high by 19" (48.3 cm) wide by 24" (61 cm) deep rack mountable chassis. The chassis also contains a power supply and an extra slot for either a self-test card or a custom interface card. A memory protect circuit provides data saving upon loss of power. Optional chassis wiring permits 36 bit double word configurations or daisy-chaining two chassis for expansion to 1024 k by 18 bit capacity.

The Maxi-store may be purchased as a complete system or as an individual module.

Dataproducts (Dublin) Limited,
Telephone (01) 31166

Dataproducts International Inc.,
Tel: Reading (0734) 58723 - 6

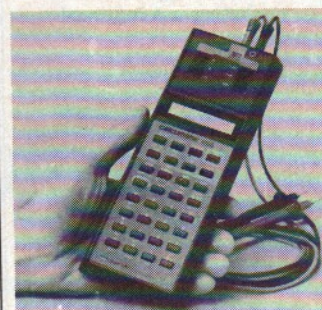
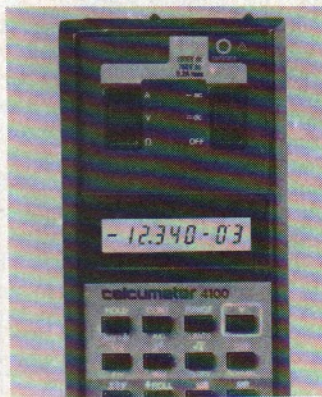
(931 M)

Handheld 3-1/2 digit DMM controlled by CMOS microcomputer

The first handheld 3-1/2 digit multimeter to be fully controlled by a CMOS microcomputer chip has been introduced for less than \$400 by Electro Scientific Industries of Portland, Oregon. Called the Calcumeter 4100, it is essentially a high performance calculator integrated with the multimeter to enable some extraordinary capabilities:

- 1) Save the average design engineer hours per week by providing the ability to automatically and directly scale and offset ($mx + b$); sort with high-low limits; average noise away; measure dB volts directly; display in percent deviation; troubleshoot by sound.
- 2) Measure and HOLD one million times on a single 9 V battery.
- 3) Control and datalog remotely with an accessory printer.

- 4) Perform math conversions with 11 special keys.
- 5) Store measurements and/or calculations in five different memory locations.
- 6) Operate with autoranging, autozeroing and autopolarity.
- 7) Select from three different display formats: Scientific notation, engineering notation (exponents in multiples of three) or any fixed decimal up to 7. The multimeter operates in six ranges as follows: 10 microvolts sensitivity through 1000 volts DC, 750 AC; 10 microamps sensitivity up to 200 milliamps (extended to 20 amps with accessory shunt); 0.1 ohms resolution through 20 mega-ohms. Basic accuracy is 0.25% DC V.



Available since September, the standard product comes with test leads (with fingerguard probes and recessed connectors), direct prod for probing with instrument in hand, two alligator clips that screw on to the end of the probes, a complete Owner's Handbook consisting of more than 100 pages, shortform manual which snaps into a plastic storage case (the latter serves as a benchtop cradle), and a spare fuse.

Micrometrics, Inc., of Portland, Oregon;
Suntek Business Park,
9450 S.W. Barnes Rd., Portland,
Oregon 97225

(989 M)

8-bit bi-directional bus-buffer

A new 8-bit TRI-STATE™ bus transceiver from National Semiconductor provides bi-directional drive for bus-oriented microprocessor systems. Offered in a single 20-pin DIP, the INS8208B device is manufactured by low power Schottky technology.

The INS8208B is part of National's expanding Series 8000 family of microprocessor peripheral digital I/O, peripheral control, communications and memory support products. All products are compatible with National's Universal Microbus™ concept as well as all other bus-oriented microprocessor systems.

The chip has 48 milliamperes drive capability on the B-port (Bus-transceiver) and 16 mA drive capability on the A-port; an additional PNP transistor input on both ports allows reduced input loading.

Typical short-circuit output current is 38 mA for the A-port and 50 mA for the B-port. For 300 pf load, the A to B-port propagation delay is 18 nanoseconds for logical '0', and 16 nanoseconds for logical '1' transition.

Each receiver section requires a minimum of 2 volts at only 0.1 micro-amperes (typical) for a logical '1' signal; logical '0' requires 70 μ A. The INS8208B has lower supply requirements than most other available bus transceivers. The power supply requirement will not exceed 130 mA.

For simplified system interconnections, the INS8208B



transmitter and receivers, connected as reversed pairs in parallel, are applied to two sets of eight I/O ports. Only two control signals are required — a transmit/receive signal to enable the transceivers and a chip disable signal which places both sets of ports in a TRI-STATE condition.

National Semiconductor GmbH,
Industriestraße 10,
D-8080 Fürstfeldbruck,
West Germany

(977 M)

MARKET

Pocket terminal

The GR Electronics Pocket Terminal is the most practical low cost, hand-held communications unit yet developed, with a wide range of input/output facilities and multiple signalling options.



Its total portability and rugged packaging will make it an essential item of equipment for technicians, programmers and operators — in fact anyone with a need to communicate with computer systems or stand-alone processors.

Features

- * 16-segment 'starburst' LED display providing instantly legible 64-character ASCII alphanumeric and symbols
- * All 128 ASCII codes generated from positive action keyboard
- * 30-character memory displayable in eight-character blocks
- * Single 5 V supply required at 350 mA, typical
- * 110 or 300 baud transmission rates, internally selectable
- * Full duplex operation, with interface for 20 mA loop or V24/RS232 levels
- * Parity codes and stop bits settable to suit your transmission standard
- * Internal 'bleeper' reacts to 'BEL' code; unit also responds to cursor controls, 'display clear' and 'new line' codes

Applications

As well as its use in conventional small-scale I/O operations, the Pocket Terminal opens up a new range of applications made possible by its portability, low cost, convenience and flexibility.

- In situ fault diagnosis on processor-based systems
- Clear, unambiguous mobile communications
- On-site reprogramming of operating parameters
- Commissioning of digital systems
- Interactive debug, information

retrieval, status monitoring, etc.

- Bench testing
- Educational and home computing

Description

The unit is a hand-held terminal with a 40-key positive tactile response keyboard comprising two single-function and 38 dual-function keys. These give internal control and allow transmission of all 128 ASCII codes, with a maximum rate repeat facility. Audible response to an external signal is also provided by an internal 'bleeper'.

The display is of the 16-segment 'starburst' type, with capacity for eight characters in line. Alphanumeric and symbols are conventionally formed, and the full 64-character upper case ASCII set may be generated. As characters are received via the data link they are stored in the unit's memory, which may be visualised as a 32 character line. The display acts as an eight character 'window' onto the 'memory line'. Far left and far right positions in the line are reserved for display of the internal control status, i.e. 'shift', 'control', 'repeat', leaving 30 positions for data received.

The display window may be stepped left or right in blocks of four characters along the line, or in a single move to the 'left home' or 'right home' limits. Location of the display window in the line is indicated on the display.

The terminal allows two modes of operation. In the first, each character received is entered in the memory at a position determined by a cursor which may be controlled remotely by received codes. This allows data to be entered in any required format, as well as permitting data already in the memory to be edited.

In the second mode the cursor is static and information is input at the right hand end of the memory line, 'shuffling' existing data in the line one step left as each character is received. If the line is filled in the first mode, the terminal will automatically enter the second mode.

A removable panel on the rear of the unit gives access to a switch set allowing the following options to be selected:

1. Single or dual stop bits
2. Control code response enable/disable
3. Parity bit EVEN/ODD/SET/RESET
4. 300/110 baud transmission rate

GR Electronics Ltd.,
Fairoak House, Church Road,
Newport, Gwent NPT 7EJ

(983 M)

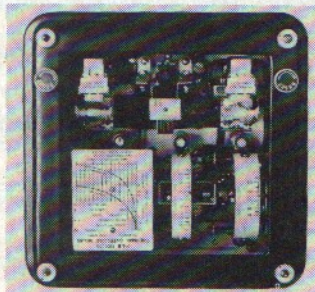
Motor protection relay

A range of temperature-sensitive motor-protection relays which have a rapid response-time with negligible overshoot, has been announced by P & B Engineering Co. Ltd., of Crawley, Sussex, England. Called the Model MW Golds' Relays, they protect industrial multi-phase motors against damage from overloads or failure of a phase in the mains supply.

The relays also provide a continuous indication of the percentage of full-load current at which the motor is operating. Additional relays which give protection against earth-leakage and short-circuit damage can be fitted.

The new thermal relays are between 25% and 50% less expensive than solid-state electronic motor-protection devices and are extremely reliable. Fast operation is achieved through the use of a special contact-mechanism which is actuated by three bi-metallic coil assemblies heated directly by current derived from transformers in the motor's supply.

The coil assemblies have a heating curve similar to that of most industrial motors. Each assembly comprises two bi-metallic coils, one mechanically-linked to a contact of the contact mechanism, the other providing temperature-compensation. The coil of the centre phase is linked to the 'H'-shaped centre frame which carries the outer pairs of two sets of contacts. The centre contact of each set is linked to one of the other two phases.



Under normal operating conditions, all three coils deflect through the same angle, so that the centre contacts of each set remain mid-way between the outer contacts. Should the three phases become unbalanced — through the failure of a phase, for example — the bi-metallic coil of the affected phase slowly reverts to its zero position (i.e. goes cold). At the same time the increased currents through the other two phases deflect their coils further, so that in a matter of seconds, the contact of the affected phase touches that of the adjacent phase and completes the

trip circuit. Tripping also occurs when the currents in the outer and centre phases differ by approximately 12% of the full load value.

The MW relays have a power consumption of only 2VA per phase at full-load. Their contact mechanism can be set to trip at any percentage of full-load current between 80% and 125%. Accuracy of setting is $\pm 3\%$; repeatability at a given trip-setting is better than $\pm 1.0\%$. Contact assemblies can be fitted with auxiliary contacts for actuating alarm systems and other switching functions.

The relays are housed in dust-proof cases and can also be supplied in withdrawable cases for ease of inspection and maintenance.

P & B Engineering Co. Ltd. is looking for agents and distributors in France, Italy and Germany for its range of products which, in addition to thermal motor protection devices, includes maximum-demand load indicators as well as portable earthing equipment for earthing electricity sub-stations and overhead-lines up to 400 kV during maintenance.

P & B ENGINEERING CO. LTD.
29/31 Kelvin Way,
Crawley,
West Sussex RH10 2PT,
England.

(1026 M)

Diode for fiber optics

The new infrared transmitter diode FV 21 IR from Siemens with flat epoxy encapsulation of the light-emitting GaAs chip has been designed specially for optical-fiber cables. The glass fiber ends can be attached directly, the wavelength of the IR beam is 880 nm. The chip is mounted on a TO46 base plate, the cathode being metallically connected to the housing.



The diode provides an optical power of 1 to 2 mW at a 100-mA drive. The housing has a diameter of 5.4 mm and a height of 1.3 mm.

Siemens AG, Zentralstelle für
Information
Postfach 103
D-8000 München 1
Federal Republic of Germany

(1037 M)

TTL	★	74109	25p
7400	10p	74120	80p
7402	10p	74121	25p
7404	10p	74122	25p
7404A	12p	74123	40p
7405	12p	74126	30p
7406	25p	74127	40p
7407	25p	74128	40p
7408	12p	74130	120p
7409	12p	74131	90p
7410	12p	74132	90p
7411	12p	74133	90p
7412	15p	74134	90p
7413	15p	74135	90p
7414	45p	74136	100p
7415	45p	74137	100p
7416	12p	74138	100p
7417	25p	74139	100p
7418	25p	74140	270p
7419	25p	74141	270p
7420	25p	74142	270p
7421	25p	74143	270p
7422	10p	74144	100p
7423	10p	74145	100p
7424	10p	74146	100p
7425	20p	74147	90p
7426	22p	74151	45p
7427	22p	74152	45p
7428	25p	74154	70p
7429	25p	74155	45p
7430	12p	74156	45p
7431	20p	74157	45p
7432	20p	74158	45p
7433	20p	74159	45p
7434	20p	74160	55p
7435	20p	74161	55p
7436	20p	74162	55p
7437	20p	74163	55p
7438	20p	74164	55p
7439	20p	74165	55p
7440	20p	74166	75p
7441	50p	74167	100p
7442	50p	74170	100p
7443	50p	74171	100p
7444	50p	74172	100p
7445	50p	74173	100p
7446	50p	74174	100p
7447	50p	74175	100p
7448	50p	74176	100p
7449	50p	74177	100p
7450	12p	74178	100p
7451	12p	74179	100p
7452	12p	74180	90p
7453	12p	74181	90p
7454	12p	74182	90p
7455	12p	74183	120p
7456	12p	74184	120p
7457	25p	74185	120p
7458	25p	74186	320p
7459	25p	74187	320p
7460	25p	74188	320p
7461	25p	74189	320p
7462	75p	74190	320p
7463	75p	74191	320p
7464	75p	74192	320p
7465	75p	74193	320p
7466	75p	74194	320p
7467	75p	74195	320p
7468	75p	74196	320p
7469	75p	74197	320p
7470	75p	74198	320p
7471	75p	74199	320p
7472	75p	74200	320p
7473	75p	74201	320p
7474	75p	74202	320p
7475	75p	74203	320p
7476	75p	74204	320p
7477	75p	74205	320p
7478	75p	74206	320p
7479	75p	74207	320p
7480	75p	74208	320p
7481	75p	74209	320p
7482	75p	74210	320p
7483	75p	74211	320p
7484	75p	74212	320p
7485	75p	74213	320p
7486	75p	74214	320p
7487	75p	74215	320p
7488	75p	74216	320p
7489	75p	74217	320p
7490	75p	74218	320p
7491	75p	74219	320p
7492	75p	74220	320p
7493	75p	74221	320p
7494	75p	74222	320p
7495	75p	74223	320p
7496	75p	74224	320p
7497	75p	74225	320p
7498	75p	74226	320p
7499	75p	74227	320p
7500	75p	74228	320p

CMOS			
4000	12p	4040	60p
4001	12p	4041	60p
4002	12p	4042	60p
4003	12p	4043	60p
4004	12p	4044	60p
4005	12p	4045	60p
4006	12p	4046	60p
4007	12p	4047	60p
4008	12p	4048	60p
4009	12p	4049	60p
4010	12p	4050	60p
4011	12p	4051	60p
4012	12p	4052	60p
4013	12p	4053	60p
4014	12p	4054	60p
4015	12p	4055	60p
4016	12p	4056	60p
4017	12p	4057	60p
4018	12p	4058	60p
4019	12p	4059	60p
4020	12p	4060	60p
4021	12p	4061	60p
4022	12p	4062	60p
4023	12p	4063	60p
4024	12p	4064	60p
4025	12p	4065	60p
4026	12p	4066	60p
4027	12p	4067	60p
4028	12p	4068	60p
4029	12p	4069	60p
4030	12p	4070	60p
4031	12p	4071	60p
4032	12p	4072	60p
4033	12p	4073	60p
4034	12p	4074	60p
4035	12p	4075	60p
4036	12p	4076	60p
4037	12p	4077	60p
4038	12p	4078	60p
4039	12p	4079	60p
4040	12p	4080	60p
4041	12p	4081	60p
4042	12p	4082	60p
4043	12p	4083	60p
4044	12p	4084	60p
4045	12p	4085	60p
4046	12p	4086	60p
4047	12p	4087	60p
4048	12p	4088	60p
4049	12p	4089	60p
4050	12p	4090	60p
4051	12p	4091	60p
4052	12p	4092	60p
4053	12p	4093	60p
4054	12p	4094	60p
4055	12p	4095	60p
4056	12p	4096	60p
4057	12p	4097	60p
4058	12p	4098	60p
4059	12p	4099	60p
4060	12p	4100	60p

CLEARANCE OFFERS			
Assorted Japanese I/F Transformers			
100 for \$1.25	100 for \$1.25	100 for \$1.25	100 for \$1.25
Assorted Ceramic Capacitors (No resistors)			
100 for \$1.25	100 for \$1.25	100 for \$1.25	100 for \$1.25
Hook-up Wire in solid black			
100 Yards for \$1.25	100 Yards for \$1.25	100 Yards for \$1.25	100 Yards for \$1.25
Assorted Transformers			
BC147	BC148	BC149	BC150
BC148	BC149	BC150	BC151
BC149	BC150	BC151	BC152
BC150	BC151	BC152	BC153
BC151	BC152	BC153	BC154
BC152	BC153	BC154	BC155
BC153	BC154	BC155	BC156
BC154	BC155	BC156	BC157
BC155	BC156	BC157	BC158
BC156	BC157	BC158	BC159
BC157	BC158	BC159	BC160
BC158	BC159	BC160	BC161
BC159	BC160	BC161	BC162
BC160	BC161	BC162	BC163
BC161	BC162	BC163	BC164
BC162	BC163	BC164	BC165
BC163	BC164	BC165	BC166
BC164	BC165	BC166	BC167
BC165	BC166	BC167	BC168
BC166	BC167	BC168	BC169
BC167	BC168	BC169	BC170
BC168	BC169	BC170	BC171
BC169	BC170	BC171	BC172
BC170	BC171	BC172	BC173
BC171	BC172	BC173	BC174
BC172	BC173	BC174	BC175
BC173	BC174	BC175	BC176
BC174	BC175	BC176	BC177
BC175	BC176	BC177	BC178
BC176	BC177	BC178	BC179
BC177	BC178	BC179	BC180
BC178	BC179	BC180	BC181
BC179	BC180	BC181	BC182
BC180	BC181	BC182	BC183
BC181	BC182	BC183	BC184
BC182	BC183	BC184	BC185
BC183	BC184	BC185	BC186
BC184	BC185	BC186	BC187
BC185	BC186	BC187	BC188
BC186	BC187	BC188	BC189
BC187	BC188	BC189	BC190
BC188	BC189	BC190	BC191
BC189	BC190	BC191	BC192
BC190	BC191	BC192	BC193
BC191	BC192	BC193	BC194
BC192	BC193	BC194	BC195
BC193	BC194	BC195	BC196
BC194	BC195	BC196	BC197
BC195	BC196	BC197	BC198
BC196	BC197	BC198	BC199
BC197	BC198	BC199	BC200
BC198	BC199	BC200	BC201
BC199	BC200	BC201	BC202
BC200	BC201	BC202	BC203
BC201	BC202	BC203	BC204
BC202	BC203	BC204	BC205
BC203	BC204	BC205	BC206
BC204	BC205	BC206	BC207
BC205	BC206	BC207	BC208
BC206	BC207	BC208	BC209
BC207	BC208	BC209	BC210
BC208	BC209	BC210	BC211
BC209	BC210	BC211	BC212
BC210	BC211	BC212	BC213
BC211	BC212	BC213	BC214
BC212	BC213	BC214	BC215
BC213	BC214	BC215	BC216
BC214	BC215	BC216	BC217
BC215	BC216	BC217	BC218
BC216	BC217	BC218	BC219
BC217	BC218	BC219	BC220
BC218	BC219	BC220	BC221
BC219	BC220	BC221	BC222
BC220	BC221	BC222	BC223
BC221	BC222	BC223	BC224
BC222	BC223	BC224	BC225
BC223	BC224	BC225	BC226
BC224	BC225	BC226	BC227
BC225	BC226	BC227	BC228
BC226	BC227	BC228	BC229
BC227	BC228	BC229	BC230
BC228	BC229	BC230	BC231
BC229	BC230	BC231	BC232
BC230	BC231	BC232	BC233
BC231	BC232	BC233	BC234
BC232	BC233	BC234	BC235
BC233	BC234	BC235	BC236
BC234	BC235	BC236	BC237
BC235	BC236	BC237	BC238
BC236	BC237	BC238	BC239
BC237	BC238	BC239	BC240
BC238	BC239	BC240	BC241
BC239	BC240	BC241	BC242
BC240	BC241	BC242	BC243
BC241	BC242	BC243	BC244
BC242	BC243	BC244	BC245
BC243	BC244	BC245	BC246
BC244	BC245	BC246	BC247
BC245	BC246	BC247	BC248
BC246	BC247	BC248	BC249
BC247	BC248	BC249	BC250
BC248	BC249	BC250	BC251
BC249	BC250	BC251	BC252
BC250	BC251	BC252	BC253
BC251	BC252	BC253	BC254
BC252	BC253	BC254	BC255
BC253	BC254	BC255	BC256
BC254	BC255	BC256	BC257
BC255	BC256	BC257	BC258
BC256	BC257	BC258	BC259
BC257	BC258	BC259	BC260
BC258	BC259	BC260	BC261
BC259	BC260	BC261	BC262
BC260	BC261	BC262	BC263
BC261	BC262	BC263	BC264
BC262	BC263	BC264	BC265
BC263	BC264	BC265	BC266
BC264	BC265	BC266	BC267
BC265	BC266	BC267	BC268
BC266	BC267	BC268	BC269
BC267	BC268	BC269	BC270
BC268	BC269	BC270	BC271
BC269	BC270	BC271	BC272
BC270	BC271	BC272	BC273
BC271	BC272	BC273	BC274
BC272	BC273	BC274	BC275
BC273	BC274	BC275	BC276
BC274	BC275	BC276	BC277
BC275	BC276	BC277	BC278
BC276	BC277	BC278	BC279
BC277	BC278	BC279	BC280
BC278	BC279	BC280	BC281
BC279	BC280	BC281	BC282
BC280	BC281	BC282	BC