KS 348

1/4 GHz counter
mini frequency counter
easy music

ELEKTOR

1/4-GHz-COUNTER

elektor 38 decoder

What is a TUN?
What is 10 n?
What is the EPS service?
What is the TD service?
What is a missing link?

Semiconductor types

Very often, a large number of equivalent semiconductors exist with different type numbers. For this reason, 'abbreviated' type numbers are used in Elektor wherever possible:
● a '741' stand for µA741, LM741, MC641, MIC741, RM741, SN72741, etc.
● 'TUP' or 'TUN' (Transistor, Universal, PNP or NPN respectively) stand for any low frequency silicon transistor that meets the following specifications:

	UCEO, max	20V
	IC, max	100 mA
	hfe, min	100
	Ptot, max	100 mW
	fT, min	100 MHz

Some 'TUN's are: BC107, BC108
and BC109 families; 2N3856A,
2N3859, 2N3860, 2N3904,
2N3947, 2N4124. Some 'TUP's
are: BC177 and BC178 families,
BC179 family with the possible
exception of BC158 and BC179;
2N2412, 2N3251, 2N3906,
2N4126, 2N4291.

● 'DUS' or 'DUG' (Diode Universal, Silicon or Germanium respectively) stand for any diode that meets the following specifications:

	DUS	DUG
UR, max	25V	20V
IF, max	100mA	35mA
IR, max	1µA	100µA
Ptot, max	250mW	250mW
CD, max	5pF	10pF

Some 'DUS's are: BA127, BA217,
BA218, BA221, BA222, BA317,
BA318, BAX13, BAY61, 1N914,
1N4148.
Some 'DUG's are: OA85, OA91,
OA95, AA118.

● 'BC107B', 'BC237B', 'BC547B'
all refer to the same (electrical better-quality
silicon transistors. In general,
any other member of the same
family can be used instead.

BC107 (-8, -9) families
BC107 (-8, -9), BC147 (-8, -9),
BC207 (-8, -9), BC237 (-8, -9),
BC317 (-8, -9), BC347 (-8, -9),
BC547 (-8, -9), BC171 (-2, -3),
BC182 (-3, -4), BC382 (-3, -4),
BC437 (-8, -9), BC414

BC177 (-8, -9) families
BC177 (-8, -9), BC157 (-8, -9),
BC204 (-5, -6), BC307 (-8, -9),
BC320 (-1, -2), BC350 (-1, -2),
BC557 (-8, -9), BC251 (-2, -3),
BC212 (-3, -4), BC512 (-3, -4),
BC261 (-2, -3), BC416.

Resistor and capacitor values

When specifying component values,
decimal points and large numbers

of zeros are avoided wherever
possible. The decimal point is
usually replaced by one of the
following abbreviations:

p (pico-) =	10^{-12}
n (nano-) =	10^{-9}
µ (micro-) =	10^{-6}
m (milli-) =	10^{-3}
k (kilo-) =	10^{3}
M (mega-) =	10^{6}
G (giga-) =	10^{9}

A few examples:
Resistance value 2k7: 2700 Ω.
Resistance value 470: 470 Ω or
0.000 000 000 004 7 F . . .
Capacitance value 4p7: 4.7 pF, or
0.000 000 000 004 7 F . . .
Capacitance value 10n: this is the
international one of writing
10,000 pF or .01 µF, since 1 n is
10^{-9} farads or 1000 pF . . .
Resistors are ¼ Watt 5% carbon
types, unless otherwise specified.
The DC working voltage of
capacitors (other than electrolytics) is normally assumed to be
at least 60 V. As a rule of thumb,
a safe value is usually approximately twice the DC supply
voltage.

Test voltages

The DC test voltages shown are
measured with a 20 kΩ/V instrument, unless otherwise specified.

U, not V

The international letter symbol
'U' for voltage is often used
instead of the ambiguous 'V'.
'V' is normally reserved for 'Volts'.
For instance: $U_b = 10$ V,
not $V_b = 10$ V.

Mains voltages

No mains (power line) voltages
are listed in Elektor circuits. It is
assumed that our readers know
what voltage is standard in their
part of the world!
Readers in countries that use
60 Hz should note that Elektor
circuits are designed for 50 Hz
operation. This will not normally
be a problem; however, in cases
where the mains frequency is used
for synchronisation some modification may be required.

Technical services to readers
● EPS service. Many Elektor
articles include a lay-out for a
printed circuit board. Some — but
not all — of these boards are available ready-etched and predrilled.
The 'EPS print service list' in the
current issue always gives a complete list of available boards.
● Technical queries. Members of
the technical staff are available to
answer technical queries (relating
to articles published in Elektor)
by telephone on Mondays from
14.00 to 16.30. Letters with
technical queries should be
addressed to: Dept. TD. Please
enclose a stamped, self addressed
envelope; readers outside U.K.
please enclose an IRC instead of
stamps.
● Missing link. Any important
modifications to, additions to,
improvements on or corrections
in Elektor circuits are generally
listed under the heading 'Missing
Link' at the earliest opportunity.
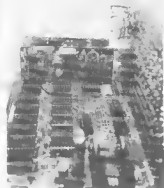
Despite being relatively inexpensive and simple to build, the performance of the ¼ GHz counter puts it safely in the 'professional' category. Its features include: five measurement ranges, from 15 Hz to 250 MHz; a preset facility for use as a digital tuning indicator; up and down count modes; automatic range indication and flicker-free last digit. p. 6-01

The time has come for software support for µP users in the form of ready-to-run programmes. Most readers possess a record player, so disc was chosen as the recording medium. It is hoped that the Elektor Software Service will prove a welcome addition to the existing range of reader services.

p. 6-20

The versatile traffic light controller should prove a welcome addition to model town, road or railway layouts, and could also be used as an aid to road safety demonstrations in schools. The design has provision for both British and European traffic light sequences, and can also be adapted to control a 'Pelican' crossing.

p. 6-36

Only 50 years ago, this type of cash register was an example of up-to-date technology and High Frequencies started at 10 kilocycles. Now, a 250 Megahertz frequency counter is a home construction project. . . . Just think about that for a minute.

1/4 GHz counter

It is often difficult, if not downright impossible, for the hobbyist to construct test equipment which can lay claim to offering truly professional performance. The 1/4 GHz counter described in this article however, not only more than meets that requirement, but is also extremely easy to build. Once the components have been mounted on the four printed circuit boards, and once they have been interwired, all that remains to be done is to connect up the mains transformer. Calibration is limited to three noncritical points in the circuit. Switching between measurement ranges is accomplished by means of DC control voltages. The main component in the circuit, the LSI (Large Scale Integration) counter, is controlled by means of a system of buses which also carry the control signals for the timebase circuit, the input divider, and for decimal point and range indication.

Despite being relatively inexpensive and simple to build, the performance of the frequency meter described in this article puts it safely in the 'professional' category. Its features include: five measurement ranges, from 15 Hz to 250 MHz; a preset facility for use as a digital tuning indicator; up and down count modes; automatic range indication and flicker-free last digit.

Block diagram

The block diagram of the complete counter is shown in figure 1. As can be seen, the circuit has two inputs, one for low frequency signals and another for high frequency signals. The low frequency range covers 20 Hz to 10 MHz and has an input impedance of approximately 1 MΩ. The high frequency input measures between 8 MHz and 250 MHz and has an impedance of 50 Ω. An ECL (Emitter-Coupled Logic) prescaler and a TTL counter are used to divide down the high frequency input signals by a factor of 100.
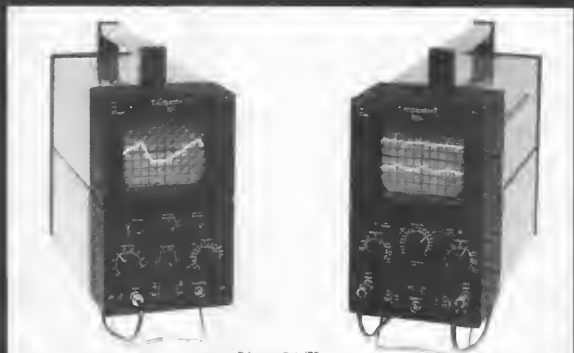
After being amplified and boosted to TTL level, the input signal is fed via the divider select bus to a decade counter, which, for certain measurement ranges, can be bypassed by means of a system of gates, so that the signal frequency is unaltered.

The timing cycle for the timebase is determined by the range/display decoder. The timebase supplies gate control pulses, which determine how long the counter gate is open, and the control signals for the store and load inputs of the LSI counter. The store input latches the count data into the

display, whilst the load input enables the counter to be preset to a particular value, so that it can be used as a digital tuning indicator for FM receivers. The input signal is fed from the output of the decade divider to a sync gate, which synchronises the input and timebase signals. This ensures that the gate pulse always maintains the same phase relationship with the input signal. For a fixed input frequency successive counts will therefore be identical, thus eliminating flicker on the last digit of the display.

At the same time, the range/display decoder provides the necessary control signals for correct indication of measurement range and decimal point. The LSI counter contains an internal scan oscillator which controls the multiplexing for the displays. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} or V_{DD} and scan input. Another bus system connects the counter to a number of dual-in-Line switches, by means of which the counter can be preset to the desired frequency using BCD code. The counter is switched between the 'preset' and 'count' modes by means of S2, whilst S3 switches between the 'up' and 'down' count modes.

The MK 50398N

Figure 2 shows the internal block diagram of the component which forms the heart of the 1/4 GHz counter, namely the MK 50398N, a six decade counter/display driver. The diagram also shows the system of bus lines used to drive the seven-segment displays and the BCD switches for preloading the counter.

When the load counter input is high, each of the digits corresponding to the BCD counter inputs is loaded in turn, starting with the most significant digit. This process is illustrated in the timing diagram shown in figure 2b.

The clear input is asynchronous and will reset all counter decades to zero when taken high. However this input does not affect the six digit latch or the scan counter. As long as the store input is
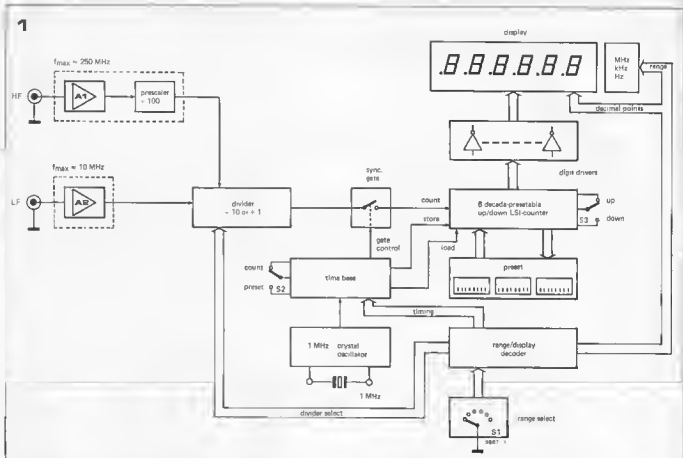
Figure 1. Block diagram of the 1/4 GHz counter. In order to simplify the wiring and to reduce the chance of crosstalk, DC control voltages are used to switch (electronically) between the different measurement ranges. All the control signals (for the preamps, the timebase and for correct indication of range and decimal point) are carried via a system of buses. The circuit contains a sync gate, which synchronises the timebase with the input signal, thereby preventing right-hand digit flicker.

Figure 2. The internal functional diagram of the MK 50398N, a six-decade counter/display driver. The counter can be preset to any desired value by means of the BCD switches connected between the digit strobe outputs and the BCD inputs. The counter is then loaded digit by digit corresponding to the digit strobe outputs. This process is illustrated in the timing diagram shown in figure 2b.
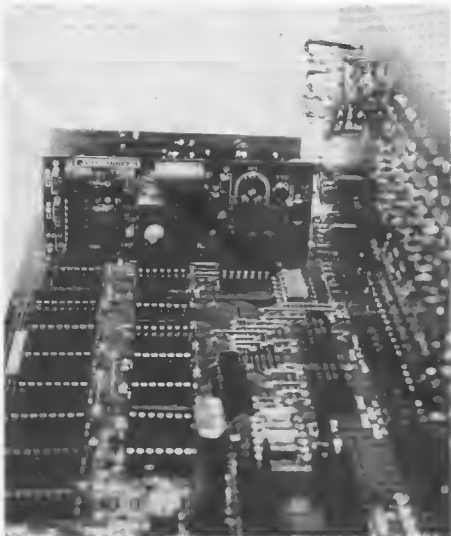
low, data is continuously transferred from the counter to the displays. Data in the counter will be latched and displayed when the store input is taken high.

Range selection

The degree of prescaling and the position of the decimal point for the differing gate times and measurement ranges is shown in figure 3.

Figure 3a shows the situation for the lowest frequency range (Hz), which has a gate time of 10 seconds and a resolution of 1/10 Hz. In this case the LF amplifier is connected direct to the sync gate.

With the arrangement shown in figure 3b, the counter will measure up to 1 MHz; the gate time here is 1 second. Figure 3c illustrates the highest of the low frequency ranges, namely up to 10 MHz. Since the MK 50389N cannot count frequencies higher than about 1 MHz, a decade divider is connected between the preamp and sync gate. This divider is either bypassed or switched into circuit by the arrangement of gates shown in figure 4.

Figure 3d, -e, and -f depict measurements made in the HF-range. Once again the decade divider is either bypassed (figure 3d and 3f) or connected in circuit (figure 3e) by means of the associated gating.

The situation in figure 3f shows the counter used as a digital tuning indicator for FM receivers. With a view to using the counter for this particular application, the counter was designed so that in this configuration the gate time is only 0.1 s, with the result that the display closely tracks the tuned frequency. In addition, the least significant digit is blanked, since small variations in the oscillator frequency of the receiver would cause this digit to be continuously flickering between different numbers.

Timebase and control signals

The simplified circuit diagram in figure 5 shows how the control signals for the counter are generated from the timebase. A signal, the frequency of which is 1000 times lower than that of the timebase (1 kHz), is presented to the input of IC13. This IC simultaneously clocks the three decade dividers IC14 . . . IC16. The gate times are determined by means of switch S_X, which in reality consists of a number of gates, these being clocked in turn by control pulses from the timing bus. The positive transitions of the signal is selected by SX trigger flip-flop FF1, so that the Q output goes low. At the same time, the Q̄ output of FF2 is also taken low, with the result that gates A, B and C are inhibited. As long as the Q̄ output of FF1 is held low, the sync gate, IC19, remains open, and the clock pulses from the input signal are fed to the count input of the LSI counter. As was already mentioned, the

2a

2b

3

4

5
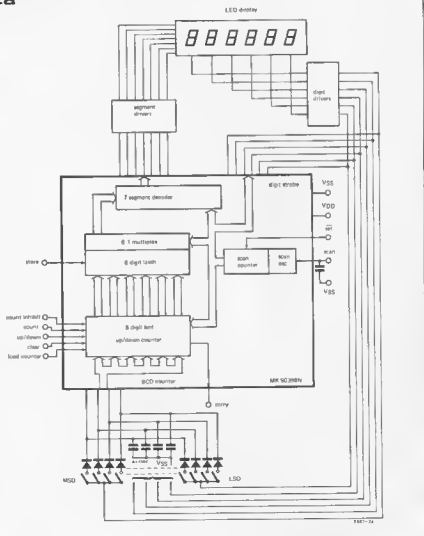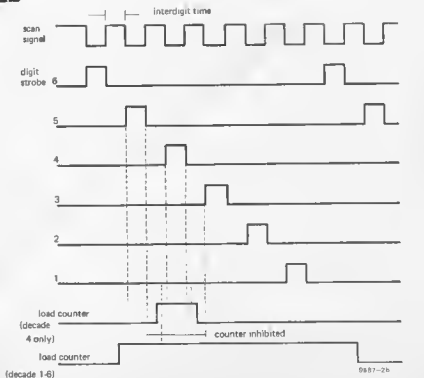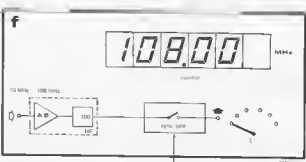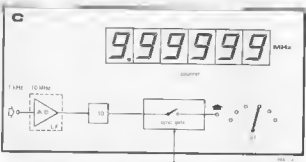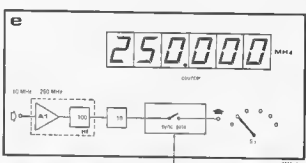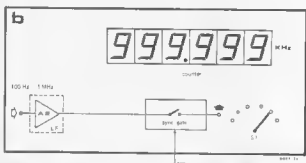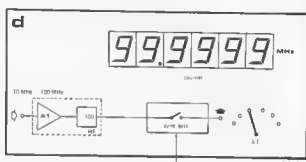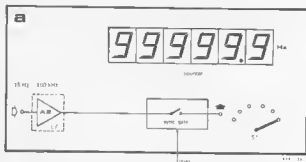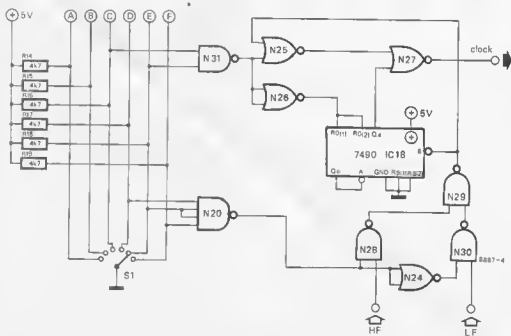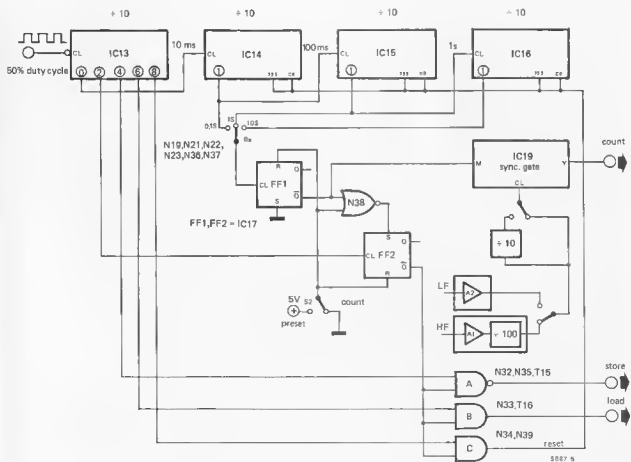
Figura 3. This diagram illustrates the different degrees of prescaling used for each of the measurement ranges. Figuras 3a . . . 3c show the low frequency ranges, whilst 3d and 3e show two high frequency ranges. Figure 3f illustrates the HF range intended for digital tuning indication for VHF-FM receivers. In this mode, the right-hand digit is blanked.

Figura 4. The gating circuit which decodes the position of the range select switch and routes the input signal either through or past the extra decade divider.

Figure 5. This simplified diagram shows how the control pulses for the counter are derived from the timebase signal.

clock pulses are synchronised to the timebase, so that, for a given input frequency, the counter will always count the same number of whole pulses. The sync gate is formed by a special TTL IC, the pulse synchroniser 74120. The sync gate will continue to feed clock pulses to the count input of the 50398N until a second positive going edge of the gate signal clocks FF1; this causes the Q output of FF1 to once more swing high, thus inhibiting the sync gate, and, via gate N38, it also enables the clock input of FF2, so that, on the next positive going edge of output 2 of IC13, the Q output of FF2 will go high. This removes the inhibition on gates A, B and C, and hence on outputs 4, 6 and 8 of IC13. The reset pulse at the output of gate C resets IC14 . . . IC16. A new gate period commences after approx. 1 ms.

Control- and counter circuits

Figure 6a shows the detailed circuit diagram of the control- and counter circuits of the 1/4 GHz counter.
Inverters N13 . . . N15, together with their associated components, form the crystal oscillator, the frequency of

which can be slightly varied by means of trimmer capacitor C2. By means of the three decade counters IC10 . . . IC12, the oscillator frequency is divided down from 1 MHz to 1 kHz. As has already been explained, the control signals are derived from the timebase with the aid of IC13 and the circuit shown in figure 5.
Together with transistors T15 and T16, gates N32 . . . N35 and N39 perform the functions of gates A, B and C in figure 4. Gate periods of 0.1 s, 1 s and 10 s are available at output 1 of IC14, IC15 and IC16 respectively. In the final version of the circuit switch S_X in figure 5 is replaced by gates N19, N21 . . . N23, N36 and N37. As explained above, flip-flop FF1 is triggered at the end of the gate period selected by switch S1. Depending upon the position of the range switch, gates N25 . . . N27 and N31 switch the decade divider IC18 either into or out of circuit. Gates N20, N24, N28 . . . N30 are used to switch between the low- and high frequency inputs. The use of electronic switching ensures that inductive crosstalk between the inputs is effectively eliminated.
The decimal points in the displays are driven via buffers N1 . . . N6, whilst

6a

6b

Figure 8a. Detailed diagram of the main circuits of the 1/4 GHz counter, which are mounted on the boards shown in figures 7 and 8.

Figure 6b. The power supply.

N7 . . . N12 buffer the LED displays for range indication (MHz, kHz, Hz). As is apparent from the diagram, switching between ranges is effected via the six-line bus which is controlled by the range switch, S1. When one of the six lines is taken low, this state is decoded by the above-described logic gating, so that the correct gate time, input amplifier and decimal point are chosen.

The counter can be preset to any desired value by means of the dual-in-line switches S4 . . . S6. At the beginning if each count cycle the counter will then increment starting from that figure. By setting S2 to the 'preset' position the preset frequency can be shown on the displays. When S2 is set to 'count', the counter begins a new count cycle, thus S2 can also be used as a reset switch. If desired, the DIL switches and diodes D1 . . . D24 can be omitted, in which case the counter is reset to zero after every 'load' pulse.

Via transistors T1 . . . T6, the commoned anodes of displays DP1 . . DP6 are connected in turn to the supply voltage. The segments are driven by transistors T7 . . . T13. Inverters N17, N18 and transistor T14 ensure that the least significant digit is blanked when the counter is operated as a digital tuning indicator.

The 'carry' output of the 50398N is available externally for possible extension of the circuit to include automatic ranging.

Wherever possible, CMOS devices were used for the gate- and divider ICs. Where the frequencies involved were too high for CMOS, TTL was used.

The power supply (figure 6b) provides two supply voltages. IC21 stabilises the rectified transformer voltage to 12 V, whilst IC20 together with the series transistor T26 provide a regulated 5 V supply.

Printed circuit boards for counter, displays and control circuits

The entire circuit shown in figure 6 is mounted on two printed circuit boards. The board for the left hand portion of the circuit, which includes the timebase and associated control circuitry, is shown in figure 7, whilst that for the right-hand section of the circuit, comprising the counter proper and the displays, is given in figure 8. To ensure good solder connections all the boards for the counter are tinned.

The HF amplifier

Figure 9 shows the circuit diagram of the preamp for the high frequency input (8 . . . 250 MHz). The two-stage transistor amplifier consisting of T27 and T28 provides a gain of around 60. After being amplified, the high frequency input signal is fed to the decade divider, IC24. This is an ECL (emitter-coupled logic) device, which can operate at the very high frequencies involved. The trigger level of the divider is set by means of P2. It is essential that a cermet (preferably multi-turn) preset be used for P2, to permit the threshold level of the divider to be set accurately. Transistor T29 boosts the signal to TTL level, whereupon it is fed to a second divider, IC25, a 'normal' TTL IC. The frequency of the output signal of the HF amplifier is thus 100 times lower than that of the input signal. The printed circuit board of the HF amplifier is shown in figure 10, the preamp and both decade dividers being mounted on the same board.

The LF amplifier

The circuit of the low frequency input preamp is given in figure 11. The input signal is fed via a super source follower, consisting of T17 . . . T19, to the cascode amplifier, T20 . . . T23. An integrated transistor array, the CA 3086, is used to form this amplifier, since the integrated transistors have an extremely small feedback capacitance. In this way it is relatively easy to obtain a reliable 10 MHz broadband amplifier. The low impedance output of the cascode amplifier drives two series-connected Schmitt triggers (N46, N47), which buffer the amplified input signal to TTL level.

Figure 12 shows the printed circuit board for the low frequency amplifier. An MKM or MKH type capacitor should be used for C26.

Parts list for the complete 1/4 GHz counter

Resistors:
R1,R3,R76 = 1 k
R2,R4,R5 = 390 Ω
R6 = 15 Ω
R7,R12,R13,R20,R31, R65,R73 = 2k2
R8,R10 = 8k2
R9,R11,R61,R70,R74 = 3k3
R14 . . . R19,R68,R75 = 4k7
R21,R23,R25,R27,R29,R32, R42,R44,R46,R48,R50,R52, R54 = 6k8
R22,R24,R28,R28,R30,R33, R43,R45,R47,R49,R51,R53, R55 = 2k7
R34 = 270 Ω
R36 . . . R41,R56 . . . R59, R88 = 180 Ω
R60,R72 = 1k5
R62 = 56 Ω
R63,R64 = 1Ω8
R66 = 1 M
R67,R80,R81 = 100 Ω
R69 = 39 k
R71 = 33 k
R77,R85,R89 = 470 Ω
R78,R82 = 22 k
R79,R83 = 220 Ω
R86 = 47 k
R87 = 120 Ω
R$_x$ = 8k2
P1 = preset potentiometer 1 k
P2 = cermet preset 5 k

Capacitors:
C1 = 10 n MKH, MKM
C2 = 45 p trimmer
C3 = 680 p ceramic
C4 = 330 p ceramic
C5 = 22 μ/16 V tantalum
C6,C37 = 47 n ceramic
C7 . . . C10 = 150 p ceramic
C11 = 1 μ/6 V tantalum
C12,C13,C16,C18,C20,C22,C24, C28,C30,C32,C43,C44, C45 = 100 n MKH
C14,C15 = 2200 μ/25 V
C19 = 470 μ/6 V
C21 = 1 n ceramic
C23,C29,C31 = 10 μ/16 V tantalum
C17,C25 = 220 μ/16 V
C26 = 1 μ MKH, MKM
C27 = 47 μ/16 V
C33 . . . C36, C38 . . . C42 = 10 n ceramic

Semiconductors:
D1 . . . D24,D34,D35 = 1N4148
D25,D26,D27 = LED (red)
D28 . . . D31 = 1N4004
D32,D33,D36 = zener 2V7, 400 mW (note that if this value should prove difficult to obtain, each zener diode may be replaced by a series-connection of three 1N4148s)
D37 = zener 10 V, 400 mW
T1 . . . T6,T14 = BC 516
T7 . . . T13,T15,T16 = BC 517
T17 = E 300
T18,T19 = BC 557A
T25 = BC 547B
T26 = BD 242
T27,T28 = BFY 90
T29 = BF 451
IC1,IC2 = 7407
IC3 = 7406
IC4 = 7420
IC5 = 4000

7
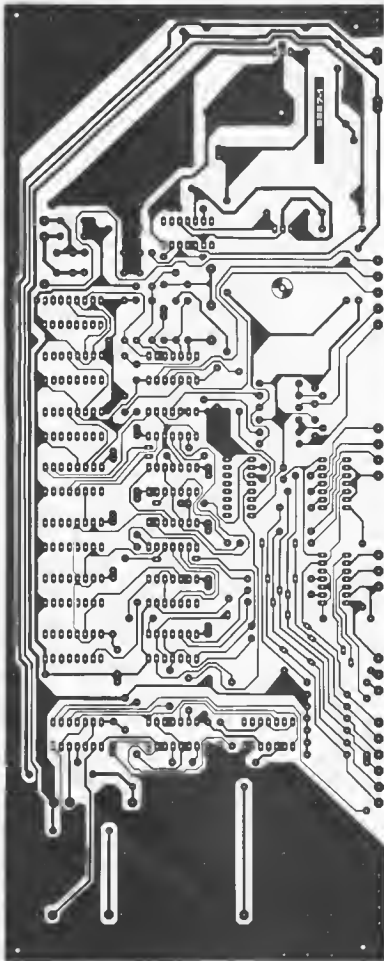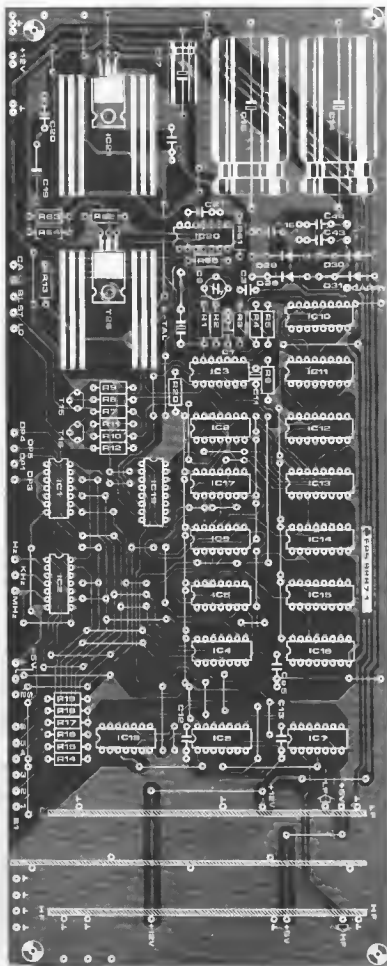
IC6 = 7402
IC7 = 7400
IC8 = 4011
IC9 = 4001
IC10 ... IC16 = 4017
IC17 = 4013
IC18 = 7490
IC19 = 74120
IC20 = 723
IC 21 = 7812
IC22 = MK 50398N (Mostek)
IC23 = 4049
IC24 = 95H90
IC25 = 74196
IC26 = T20 ... T24 = CA 3086 (DIP)
IC27 = 7413

Miscellaneous:
L1 ... L4 = chokes 10 µH
Xtal = 1 MHz series-resonant crystal
DP1 ... DP6 = HP 5082-7750 (common anode)
S1 = 1 way 6 position switch
S2,S3 = SPDT switch
S4,S6 = 8 way SPST DIL switch, if preset facility is required.
Transformer 15 V/1 A

Figure 7 and 8. Track pattern and component layout of the printed circuit boards for the circuit given in figure 6 (in view of the limited space, these boards are shown to .88 scale). Figure 7 shows the board for the timebase and control circuitry (EPS 9887-1), whilst figure 8 contains the counter and the displays, (EPS 9887-2).
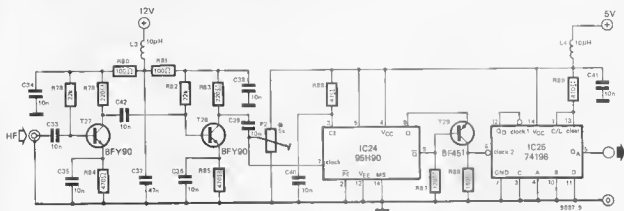
Figure 8. Printed circuit board and component layout (to .88 scale) for the counter and display circuitry (EPS 9887-2).

Figure 9. Circuit diagram of the high frequency input amplifier, which is followed by two decade dividers, IC24 and IC25.

Figure 10. The printed circuit board for the high frequency input stage (EPS 9887-4). The ECL decade divider, IC24, should be soldered direct to the board; using an IC socket would result in undesirable parasitic capacitances being produced.

11

T20 ... T24 = IC26 = CA 3086
N46, N47 = IC27 = 7413
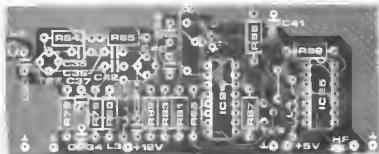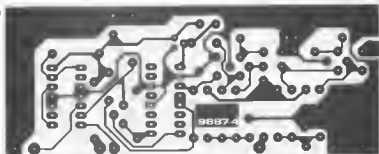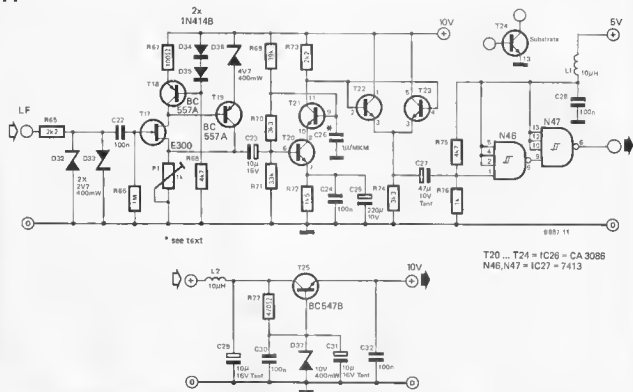
12
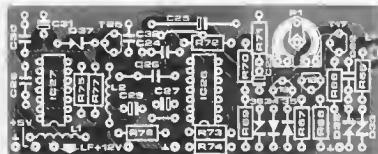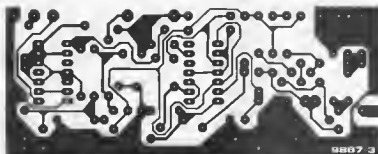
Construction of the complete counter

When mounting the components on the four boards, it is best to begin with the wire links, and then solder the resistors, capacitors and diodes into position, leaving until last the ICs. All the ICs which are to be mounted on the counter board (figure 7) should be soldered direct, i.e., no sockets should be used.

Figure 11. The circuit diagram of the low frequency input amplifier.

Figure 12. Printed circuit board for the circuit of figure 11 (EPS 9887-3).

Figure 13. A suggested layout for the front panel of the 1/4 GHz counter (to .88 scale).

This allows the front panel to be mounted within a reasonable distance of the displays. With the exception of the ECL divider, IC24, on the HF amplifier board, the rest of the ICs on the three other boards can be mounted using sockets. In order to avoid parasitic capacitances, IC24 must be soldered direct to the board.

Once the components have been mounted on all four boards, they should then be interwired. For preference, it is recommended that 1 mm tinned connecting wire be used. Space has been left between the boards for the high- and low frequency inputs for a panel of screening material, such as, e.g., a piece of copper laminate board.

After connecting up switches S1 ... S3 and the BNC-sockets all that remains to be done is to connect the circuit to the transformer voltage (15 V, 1 A) and the counter is then ready for use.

Calibration

The calibration procedure for the 1/4 GHz counter is extremely simple. If one can get hold of another accurate frequency counter, then the frequency of the crystal oscillator can be set to exactly 1 MHz by means of the trimmer, C2. This frequency can be measured at the clock input (pin 14) of IC10. If a second frequency meter is unavailable, then the trimmer should simply be set to its mid-position, halfway between the end stops. Alternatively the 200 kHz Droitwich transmissions can be used to calibrate the counter if a suitable receiver is available.

The HF amplifier can be tuned with the
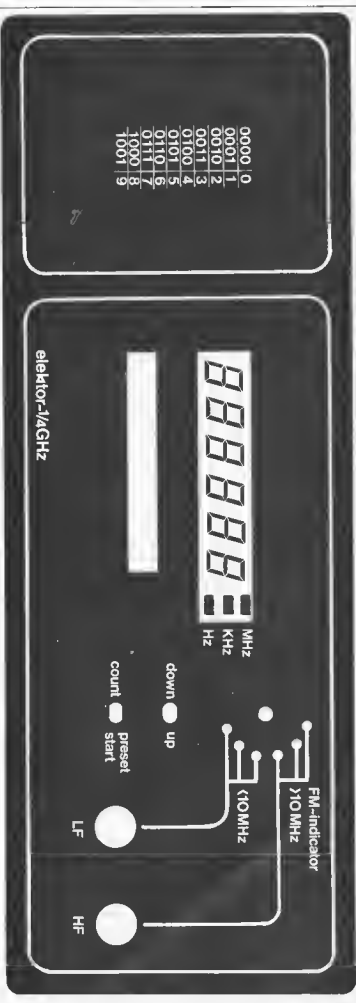
aid of a normal FM receiver. The input of the HF amplifier is connected via a length of 50Ω coaxial cable to a simple coil, consisting of one or two turns of insulated connecting wire and with a diameter of 10 mm. This coil is then placed near the oscillator coil of the FM receiver. It should then be possible to measure the oscillator frequency of the receiver (depending upon the tuning of the receiver, this should be somewhere between 70 and 120 MHz. By means of P2, the HF amplifier can be tuned for maximum sensitivity by gradually moving the pickup coil away from the oscillator coil in the receiver, and adjusting P2 for a stable display on the counter. Only when the display is completely stable will the sync gate (IC19) on the main board be receiving a jitter-free signal.

The LF amplifier is even simpler to tune. In most cases it will be sufficient simply to set P1 to the midposition. If desired, the LF amplifier can be tuned for maximum sensitivity by using a 10 kHz test signal with an amplitude of 50 mV.

Using the 1/4 GHz counter

Since the 1/4 GHz counter is equipped with a preset facility and may count either up or down, it is considerably more versatile than a simple frequency meter. One possible application is null method tuning. If, for example, one wishes to tune an oscillator to a frequency of exactly 145.163 MHz, then it is not easy to tell at a glance just how far the oscillator frequency is from the desired figure. In such a case it is simpler to preset the counter to 145.163 MHz and then let it count down. The oscillator in question is then adjusted until the counter displays 0 Hz. When using this method of tuning, the null point can be approached from both sides.

The 1/4 GHz counter can also be used as a digital tuning indicator for FM and AM receivers. As is well known, the intermediate frequency in an FM receiver is 10.7 MHz. The oscillator frequency in the tuner is thus 10.7 MHz greater or smaller than the carrier frequency. If one were to measure the oscillator frequency directly, the displayed result would obviously deviate from the carrier frequency by that figure. To obtain an accurate reading of the carrier frequency the counter should be preset to compensate for the i.f.; i.e. a preset of 989.300 MHz in the case where the i.f. is greater than the carrier frequency, and a preset of 010.700 MHz where the oscillator frequency is lower than the carrier frequency.

It is clear from the above mentioned possibilities that the 1/4 GHz counter should prove a highly useful tool for both hi-fi enthusiasts and radio amateurs. Not only that, but the counter offers the hobbyist a standard of performance which compares favourably with commercially available frequency meters which are considerably more expensive.   **H**

constant amplitude squarewave to sawtooth converter

Most electronic organs use octave dividers, which produce a symmetrical squarewave output. The harmonic content of this waveform is then altered by filtering to give the required organ voices. However, a symmetrical squarewave contains only the odd harmonics of the fundamental frequency, and those voices requiring even harmonics cannot be realistically imitated, since no amount of filtering can add harmonics which are absent. For this reason a sawtooth waveform, which contains both odd and even harmonics, is preferred as the 'raw material' for many organ voices.

A sawtooth waveform can be obtained from a squarewave as illustrated in figure 1. A capacitor is allowed to charge, either from a voltage source in series with a resistor or from a constant current source. The positive-going edge of the squarewave is used momentarily to close a (electronic) switch, which rapidly discharges the capacitor. This charging and instantaneous discharging of the capacitor produces the familiar sawtooth waveform.

Figure 2 illustrates the differences in the spectra of the square and sawtooth waveforms. If the capacitor is charged from a voltage source then a sawtooth with an exponential curvature results, the spectrum of which is shown in figure 1b. If a constant current source is used then the sawtooth is linear, and has the spectrum shown in figure 1c. For musical purposes an exponential sawtooth is preferred.

The disadvantage of this simple method is that the amplitude of the sawtooth waveform falls as the frequency of the input squarewave is increased, since the capacitor has less time to charge. This means that a different capacitor or charging resistor value would have to be used for each note of the organ to maintain equal amplitude over the entire compass of the instrument.

This problem can be overcome by arranging that the voltage of the source from which the capacitor is charged automatically increases as the frequency increases. This increases the charging current, which causes the capacitor to charge more rapidly and thus maintains a constant amplitude. A practical,

Most electronic organs use squarewaves as the basic signal from which all the organ voices are obtained by filtering, simply because squarewaves are easy to generate and process. However, from a musical point of view, the sawtooth is a much more useful waveform, since it contains both odd and even harmonics of the fundamental frequency, whereas the squarewave contains only the odd harmonics. The main problems involved in generating sawtooth waveforms for organ circuits have been those of cost and reproducibility. However, the circuit described here, for which a patent is pending, suffers from none of these drawbacks and could, in principle, be integrated into a microcircuit.

constant amplitude, squarewave-to-sawtooth converter is shown in figure 3. Capacitor C3 is charged via R4 from the voltage U_2, present on C4. The leading (positive-going) edge of the input squarewave is differentiated by C2 and R2, producing a short pulse which briefly turns on T1 to discharge C3.

The trailing edge of the squarewave is differentiated by C1 and R1, producing a short pulse which briefly turns on T2 and charges C4 via R3. Since T2 is turned on for a fixed time, as the input frequency increases T2 will be turned on for a greater proportion of the total time, so that C4 will charge to a higher voltage. This causes the charging current into C3 to increase, thus compensating for the fact that C3 charges for a shorter time as the frequency increases.

The circuit given in figure 3 will produce a sawtooth of constant amplitude over the frequency range 60 Hz to 10 kHz.

A slight disadvantage of this circuit is that the shape of the sawtooth (and hence the harmonic content) alters as the frequency changes. This is no great drawback from a musical point of view. However, in some applications a linear sawtooth is preferred, and this can be achieved by replacing R4 with a current mirror (T3, T4) as shown in figure 4. This circuit is also equipped with a FET-source-follower, T5, which acts as buffer between C3 and the output and allows low impedance loads to be driven without degrading the sawtooth linearity.

The performance of this circuit is better

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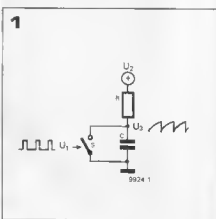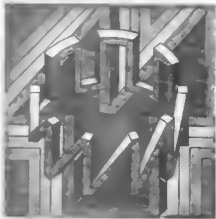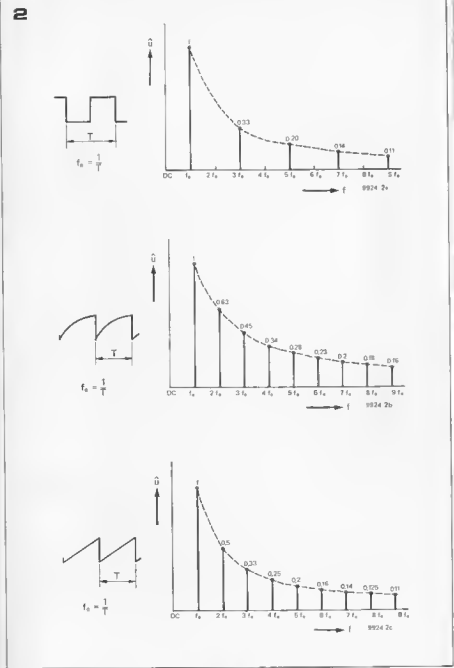
Figure 1. A sawtooth can be generated by charging a capacitor through a resistor and rapidly discharging it at regular intervals.

Figure 2. Comparison of the spectra of square, exponential sawtooth and linear sawtooth waveforms.

Figure 3. Circuit for converting a squarewave to a constant amplitude exponential sawtooth.

than that of the simpler circuit in that it will produce a constant amplitude sawtooth over the frequency range 10 Hz to 20 kHz.

The sawtooth output may be switched on and off by a switch at the input or output of the circuit, or by a switch in the supply line. This latter method is particularly useful if several sawtooth converters are in use, since it allows them all to be controlled by a single switch. However, if switching of the supply line is employed then D1 must be included to prevent the squarewave signal from breaking through the base-collector junction of T1 when the supply is switched off.

C4' can also be included to ensure that the sawtooth has a finite initial amplitude at switch-on. The amplitude depends on the value of C4', which should be no more than 4.7 μ maximum. Figure 5 shows the effect of different values of C4'. If C4' is omitted then the
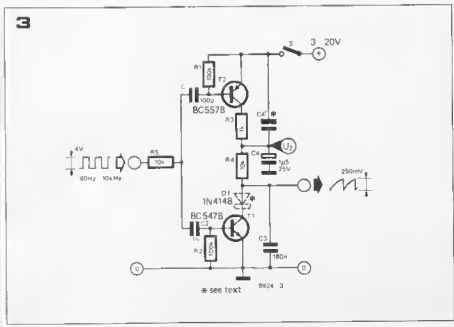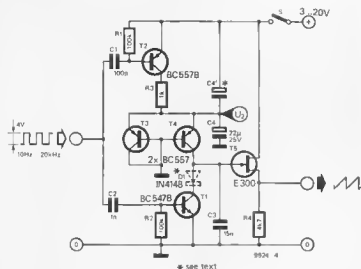
Figure 4. By replacing R4 with a current mirror a linear sawtooth may be generated. This circuit also has an output buffer, T5.

Figure 5. Showing the effect of different values of C4' on the attack and decay characteristics of the sawtooth.

servo polarity changer

Many model enthusiasts will be familiar with situations in which they discovered that moving a servo control in one direction prompted the model to steer in the opposite direction! The circuit described here is intended to offer a simple solution to just this problem.

amplitude of the sawtooth builds up slowly after switch-on as C4 charges via T2 (figure 5a). After switch-off the sawtooth will decay gradually as C4 discharges.

The times taken for the sawtooth to build up to its steady-state value and to decay are dependent on the input frequency, being longest at low frequencies and shortest at high frequencies. This behaviour corresponds quite closely to that of conventional musical instruments.

If C4' is included then the sawtooth signal will assume a finite amplitude immediately after switch-on. In figure 5b this is shown as being equal to the steady-state amplitude. However, if the value of C4' is made very large then the initial amplitude will exceed the steady-state amplitude, as shown in figure 5c. This effect will be more noticeable at low input frequencies.

In conclusion, it can be said that these circuits offer an economic solution to the problem of providing a sawtooth signal in squarewave divider instruments. By taking advantage of the high input resistances offered by MOS technology it should be possible to make the capacitor values sufficiently small to allow total integration of the circuit. ◄

servo polarity changer

Figure 1. The circuit diagram of the servo polarity changer.

Figure 2. The finished circuit when mounted on a board occupies very little space.

Figure 3. In order to set the servo in the neutral position a pulse duration of 1.5 ms is required. The top channel shows the input signal of the circuit, whilst the bottom channel shows the output pulse. The pulse is shifted along the time axis, but this has no effect upon the operation of the servo.

Figure 4. This photo shows the output pulse obtained for an input pulse duration of 1 ms. As is apparent the duration of the output pulse is 2 ms, so that the servo will now be moved exactly the same amount (the distance corresponding to a pulse of 0.5 ms) as in the case of the input signal, but in the opposite direction.

The best results are usually obtained from a servo mechanism if it is mounted in the model so there are as few joints and bends in the steering rod as possible. However the direction in which the servo moves should be such that it coincides with the direction of the control knob or joystick, i.e. moving the joystick to the right causes the model to steer to the right. However, in certain cases these two conditions prove mutually incompatible. Often the result is that the model builder has to tamper with the delicate mechanics of the steering system or with the finnicky electronics of the servo.

Servos are generally controlled by means of pulse width modulation; a pulse width of 1.5 ms corresponds to the neutral or 'straight ahead' position, whilst 1 and 2 ms represent the extreme settings of the control. The polarity of a servo can simply be reversed, so that a pulse width of 1 ms causes the servo control to assume the position that was previously adopted with a pulse width of 2 ms, and vice-versa, by modifying the width of the control pulses.

Since in both cases the neutral position of the control will correspond to a pulse width of 1.5 ms, it is possible to calculate the pulse width for all other positions on the basis of this figure. This can be done quite simply by subtracting the original pulse width from 3 ms in order to obtain its counterpart in the opposite direction. Thus in order to reverse the polarity of the servo one simply arranges for the control pulses to be subtracted from a reference pulse of 3 ms.

There are two different types of servo which are currently available, namely those which operate with positive going control pulses, and those which require a negative going pulse. The circuit described here can only be used with servos which use positive going pulses, however this represents the large majority of commercially available devices. The finished circuit occupies very little space (see figure 2) and hence there should be no problems mounting it in whatever model is under construction.
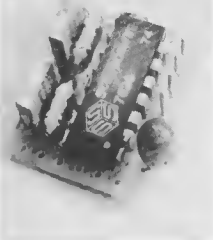
The circuit

N3 and N4 along with C1, C2, R1, R2 and D1 form a monostable with a pulse duration of approx. 3 ms. This monostable is triggered by the control signal, which is also fed to one of the inputs of N1 and N2. The other inputs of these two gates receive negative going pulses of approx. 3 ms. Since N1 and N2 (like N3 and N4) are NOR gates, their output will produce a positive going pulse, the duration of which is equal to the difference between 3 ms and the original control pulse. N2 is connected in parallel with N1 to increase the fan-out of the circuit.
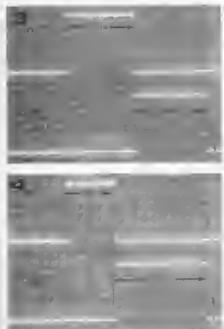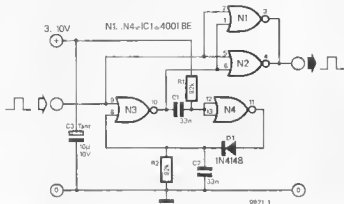
The oscilloscope photos show the result before and after a pulse has been processed by the circuit. In the prototype model the duration of the monostable pulse was 3.15 ms. In most applications where the servo is permanently built into the model, allowance for slight tolerances in pulse width can be made at the transmitter. However, if a pulse duration of exactly 3 ms is required, then a value of 27 should be chosen for C1 and C2. Smaller capacitors can then be connected in parallel with these until a pulse of precisely 3 ms is obtained on the scope. Without a scope the pulse width can still be accurately set by altering the value of C1 and C2 in the above fashion until, with or without the polarity changer, the servo remains in exactly the neutral position.

The circuit consumes very little current (1 mA), and is unaffected (< 2%) by variations in the supply voltage between 3 and 10 V. In order to reduce the dimensions of the circuit to a minimum, a tantalum type is recommended for C3. As a result of the symmetrical construction (R1 = R2, C1 = C2) the circuit has a very low temperature coefficient.

monopoly dice

Many circuits for electronic dice have previously been published, and it might be thought that the possibilities of the subject have been thoroughly exhausted. However, the dice described in this article incorporate one or two little refinements. The single die circuit incorporates a concealed 'cheat' switch, which allows the die to be stopped at any desired number, whilst the double 'Monopoly™ dice' circuit is equipped with an 'extra turn' lamp, which lights when a double has been thrown.

W. Pamler

H.A. Westra

The basic die circuit is given in figure 1. A 555 timer, IC1, is connected as an astable multivibrator. This feeds clock pulses to a divide-by-six counter, IC2, the outputs of which are decoded by gates N1 to N6 to drive an array of LEDs in the familiar die pattern.

When switch S1 is in position (b) the reset input of IC1 is pulled low and the oscillator is inhibited. Power is fed to the LEDs via S1b so that the display is activated. When the die is 'rolled' by switching S1 to position (a) the display is blanked. C4 is connected to positive supply via S1a, producing a short pulse which resets IC1 via R5. The reset input of IC1 is pulled high via R5, so the multivibrator is free to oscillate and feeds clock pulses to IC2 via N5. When S1 is switched back to position (a) the multivibrator is again inhibited so that the counter stops, whilst power is applied to the LEDs which display the value of the 'throw'.

Loaded die

Operation of the 'cheat' switch is extremely simple. The base of T1 is connected via R1 to a pair of (disguised) touch contacts. When these are bridged by a finger, current flows from the positive supply rail into the base of T1, turning on T1 and T2. This connects a large value capacitor, C1, in parallel with C2, which lowers the clock frequency to between 1 Hz and 2 Hz. If the die is now rolled it is quite easy (with a little practice) to count in time with the clock and to switch S1 to position (a) at the appropriate time to stop the counter at any desired number. The touch contacts may easily be disguised as a pair of screwheads in the housing of the die.

Monopoly dice

Board games such as Monopoly™ frequently use a pair of dice, and the rules of such games often allow a player a second throw if a 'double' is scored (i.e. both dice show the same number). The principle of a pair of dice, controlled by a single start switch, and with an 'extra

throw' indicator, is illustrated in figure 2. Each dice circuit is a duplicate of the circuit of figure 1, the only difference being that switch S1 is common to both circuits.

The four outputs of the counter (IC2) of each die are connected to the inputs of a 7485 four-bit comparator. The 'extra throw' LED, D15, is connected to the A = B output of the comparator. When both dice register the same score, the two, four-bit binary numbers fed to the inputs of the comparator will be identical, the A = B output will go high and D15 will light.

Testing the dice

A great deal of care goes into the manufacture of a conventional cubical die to make it perfectly symmetrical. This ensures that there is an equal probability of throwing any number from 1 to 6, i.e. the die is unbiased. Since the total probability of throwing a number at all is 1 (barring accidents) the probability of throwing a particular number is, of course, 1/6.

An electronic die must also obey the laws of probability, and it is quite easy to test the single die by making several hundred throws to check that each score occurs with equal frequency.

With a pair of dice the situation becomes considerably more complicated. Since two dice are being thrown the possible scores range from 2 to 12, but the number of ways in which the dice can be thrown is 36. Some scores can be thrown in more than one way, and thus have higher probabilities. For example, 2 can only be thrown in one way, (1+1) as can 12 (6+6). The probability of throwing 2 (or 12) is thus 1/36. A score of 3 can be thrown in two ways, (1+2, 2+1), as can a score of 11 (5+6, 6+5). These scores each have a probability of 2/36 or 1/18. A chart showing the 36 possible results of throwing two dice is given in figure 3, and the probability of each of the twelve possible scores is shown in figure 4.

If a pair of electronic dice is to obey the laws of probability it is essential that each die should function independently. When two dice circuits are built on the
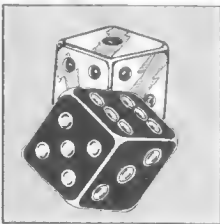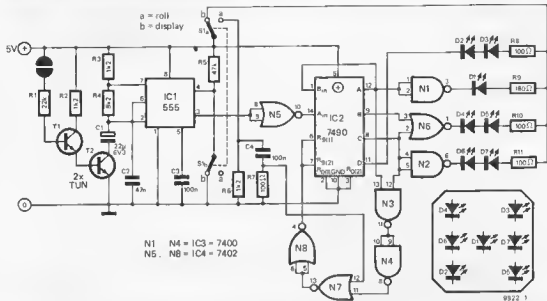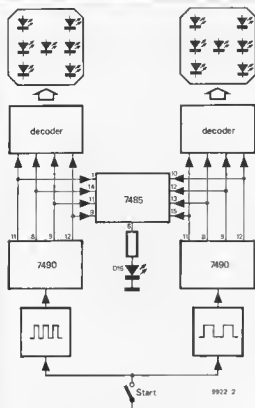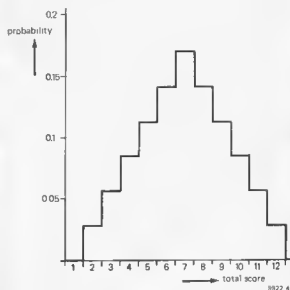
Figure 1. Circuit of electronic die with 'cheat' switch.

Figure 2. Block diagram showing the interconnection of two die circuits and a four-bit comparator to form a pair of 'Monopoly dice'.

Figure 3. Showing the 36 possible ways of throwing two dice.

Figure 4. Graph showing the probability of each possible total score when two dice are thrown.

same board and operate from the same power supply, great care must be taken to ensure that they do not interact. This means that careful attention must be paid to circuit layout and supply decoupling.

Because of the large number of throws possible with two dice, checking that a pair of electronic dice obey the laws of probability is inevitably a time-consuming process, since several thousand throws would have to be made to obtain a true assessment of the probability of each score. In practice this test is not really necessary, since any gross bias in the dice will be noticed fairly quickly when they are used. ◄

Elektor Software Service

coming soon

ESS

The ready-made printed circuit boards available from the Elektor p.c.b. service (EPS), which greatly simplify the construction of Elektor projects, have always been extremely popular with readers, for obvious reasons. Having printed circuit boards available just like any other component eliminates the time-consuming chore of designing and producing a suitable p.c.b., and the high-quality EPS boards mean that projects can be given a really professional finish. With the rapidly-growing interest in microprocessors it was felt that this 'hardware' service should be complemented by software support for µP users in the form of ready-to-run programmes for various applications. Simple programmes for the Elektor SC/MP system have previously been given in the form of a hexadecimal listing, but for longer programmes this is not really feasible, for a variety of reasons. Firstly, programmes published in this way must be loaded by hand. If the programme is of an appreciable length, and this can be extremely tedious, and furthermore there is the possibility of entering data incorrectly. Secondly, and perhaps more importantly from the reader's point of view, such programme listings take up a great deal of space, and certainly do not make compulsive reading. It was felt that to monopolise magazine pages in this way would be unfair to those readers who do not possess a microprocessor. Such readers might study a practical microprocessor article out of casual interest, but it is unlikely that they could find much interest in a programme listing!

For the above reasons it was decided to look for some alternative method of supplying software. The possibility of using optical barcodes was examined. This would have solved the problem of tedious manual loading and errors, but barcodes still occupy a lot of magazine space, and a special 'light pen' is required to read them.

However, most readers possess a record player or cassette recorder, so the possibility of recording programmes on disc or cassette was investigated. This could be played into the microprocessor via a cassette interface such as that described in the April issue for the SC/MP system.

After much discussion, disc was chosen as the recording medium, since discs are cheaper to produce than cassettes and, if reasonably well-treated, will retain the recorded information indefinitely.

As the only µP system so far described in Elektor is the SC/MP, programme discs will initially be available mainly for this system. Since a disc has a large storage capacity compared to the length of the average programme, several different programmes can be recorded on each discs. In most cases it will be possible to record each programme at least twice so that, in the event of damage to a section of the disc, the programme will not be lost. Nevertheless, it is recommended that if a programme is frequently used it should be transcribed onto a cassette and the disc stored safely as a 'master copy'.

It seems an obvious choice to record data on the discs in the form of an FSK (frequency-shift keyed) signal to CUTS standard (300 baud, $\emptyset$ = 8 cycles at 1200 Hz, 1 = 4 cycles at 2400 Hz).

The first disc will include the 'Reaction Tester' and 'Clock' programmes listed elsewhere in this issue. Three further programmes are presently under consideration, so that the first disc should contain four or five programmes.

It is hoped that the Elektor Software Service will prove a welcome addition to the existing range of reader services.

Summer circuits:
car battery monitor
power flasher
stereo width control
pseudo random running lights
symmetrical supply
butterworth hi/lo pass
headphone amplifier
touch tone control
variable power supply
metronome
hum filter
cable tester
dishwasher watcher
fluid detector
electronic soldering iron
a/d converter
marker generator
roger squawker
slide synchroniser
cold shower warning
stereo vectorscope
railway crossing bell
front and back door chime
trafficator warning
bicycle speedometer
loudspeaker protection
video combiner
brake efficiency meter
kojak siren
mini stabilisers
bat receiver
programmable address decoder
hf gain tester
model railway lighting
touch controlled dimmer
infrared light gate
power-fet amplifier
sc/mp interface
quadrature oscillator
aquarium light control
fet millivoltmeter
zero crossing detector
universal data-bus buffer
square-to-triangle converter
ultrasonic alarm system
ic fm tuner
broadband rf amplifier
automatic battery charger
voltage controlled audio mixer
digital delay line
disc jockey killer
disc preamp
data multiplexer
and some 50 other circuits!
(Commercial note:
How about a subscription?)

mini-counter

The mini-counter is a simple, but nonetheless highly functional, frequency counter which will measure signals between 10 Hz and 1 MHz and display them on a four-digit readout. The counter consists of six ICs, four seven-segment displays and a handful of discrete components. The entire instrument, with the exception of the mains transformer, can be mounted on a relatively small p.c. board. The mini-counter does not use a crystal timebase oscillator, but takes its reference frequency from the mains, so the accuracy of this circuit will obviously be inferior to that of the quarter-gigaherz counter. However, for non-professional applications its performance should prove more than adequate.

Figure 1 shows the complete circuit diagram of the mini-counter. The heart of the circuit is the MK 50398N IC (Mostek). This LSI (Large Scale Integration) chip contains a six-digit BCD counter and latch (memory), a BCD-to-seven-segment decoder, and the multiplexing for the displays. A more detailed description of this IC is given in the 250 MHz counter article.

The mini-counter actually only uses four of the six available digits. This is not only to reduce the dimensions of the counter to a minimum, but also because the accuracy of the counter does not warrant the use of more than four digits. The displays are multiplexed in the usual fashion, the common cathodes of the four digits being connected to ground via inverters N1 ... N4, which in turn are enabled by the strobe outputs D5 ... D2 of the 50398N. The anodes of the segments receive their supply voltage via resistors R3 ... R9 from the segment outputs a ... g. The multiplexing is controlled by the 50398N itself. The digit scan-frequency is determined by C11, and is in the region of 2 kHz.

The input signal is fed via the input stage T1 to the clock input of the counter; diode D6 protects this input against large negative voltages.

The counter counts the pulses at the clock input as long as the count-inhibit input is at logic '0', i.e. as long as the Q output of flip-flop FF2 is at logic '0'. This flip-flop is in turn gated by the

Elsewhere in this issue a highly sophisticated 250 MHz counter is described. The heart of that instrument is an LSI counter IC from Mostek, the MK 50398N. By using the same IC it is possible to build a more modest counter which should prove more than adequate for most home constructors.

actual clock generator of the mini-counter. The clock pulses are derived from the mains frequency. By means of inverters N5 and N6, which together form a Schmitt-trigger, the mains sinewave voltage is squared up to a CMOS level signal, which is then divided down to 10 and 1 Hz squarewaves by IC4 and IC5 respectively. (N.B. the mini-counter can be used with either 50 Hz or 60 Hz mains frequencies. This is accomplished by using the proper jumper connection on the p.c. board). Depending upon the position of the range switch S1, either the 10 Hz or the 1 Hz signal is fed to the clock input of flip-flop FF2. In the former case the Q output of this flip-flop goes high for 0.1 s, whilst in the latter case it is low for a period of 1 s (these are the two gate periods of the counter).

At the end of this interval the Q output of FF2 swings high, the count stops and FF1 is triggered. The result of this is that the store-input of the 50398N goes low, the status of the six BCD counters is transferred to the latch, and the four middle digits are displayed.

After a short time capacitor C7 charges up and FF1 resets itself (FF1 along with C7 and R11 thus actually functions as a monostable). Q once more goes high, so that the store-input of the 50398N is also taken high and the contents of the counter are retained. Shortly after FF1 has reset, capacitor C2 will charge up and the clear-input of the counter will be taken high. This zeroes the six BCD counters in preparation for the next count cycle, but has no effect upon the latch, so that the display data are not lost. Diode D5 protects the clear-input against negative pulses.
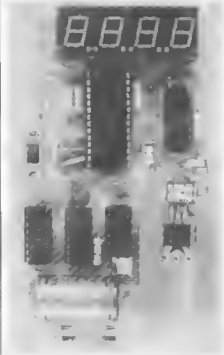
Specifications:

sensitivity	: 1 V peak
max. input voltage	: ± 5 V peak
input impedance	: min. 4k7
max. measurement range	: 1 MHz

It should be noted that the counter cannot measure the frequency of input signals with a (superimposed) DC voltage component.

1

In addition to the frequency of the clock pulse fed to flip-flop FF2, the range switch S1 also controls the position of the decimal point. The maximum values which can be displayed on these two ranges are 99.99 kHz (gate period 1 s) and 999.9 kHz (gate period 0.1 s) respectively.

The power supply for the mini-counter simply uses the common voltage regulator IC type 7812.

Printed circuit board

The printed circuit board, the track pattern and component layout of which are shown in figure 2, will accomodate all the components shown in figure 1, with the exception of the mains trans-

Figure 1. Complete circuit of the mini-counter.

Figure 2. Printed circuit board and component layout for the mini-counter (EPS 9927).

former and the mains switch S2. If the components are mounted fairly low on the board, then the result should be a compact and handy little instrument.

For use with 50 Hz mains frequency the wire link shown as a continuous line next to C8 on the p.c.b. should be mounted; in the case of a 60 Hz power line frequency (North America), the 'dotted' link is used.

The voltage regulator IC6 should be fitted with a heat sink.

The frequency range of the mini-counter can be extended to 10 MHz by connecting a 7490 decade counter between T1 and the clock input of IC1. If desired, the accuracy of the mini-counter can be increased by using a crystal timebase.

2
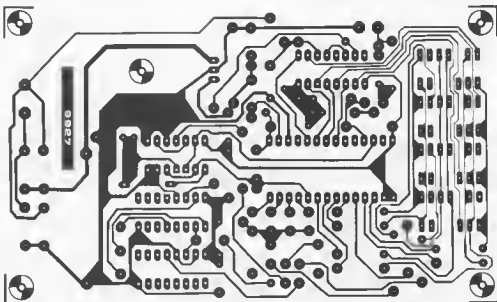
Parts list to figures 1 and 2

Resistors:
R1,R14 = 4k7
R2 = 2k2
R3 . . . R9 = 270 Ω
R10,R13 = 10 k
R11 = 22 k
R12 = 330 Ω
R15 = 47 k

Capacitors:
C1,C11 = 1 n
C2,C10,C12 = 100 n
C3 . . . C6 = 150 p
C7 = 470 n
C8 = 1000 µ/25 V
C9 = 47 µ/16 V

Semiconductors:
IC1 = MK 50398N (Mostek)
IC2 = 4049
IC3 = 4013
IC4,IC5 = 4017
IC6 = 7812
T1 = BF 494
D1 . . . D4 = 1N4004 or equ.
D5,D6 = 1N4148 or equ.

Miscellaneous:
DP1 . . . DP4 = display HP 7760
  (common cathode)
Tr = mains transformer
  12 . . . 18 V/500 mA
S1 = DPDT switch
S2 = DP mains switch
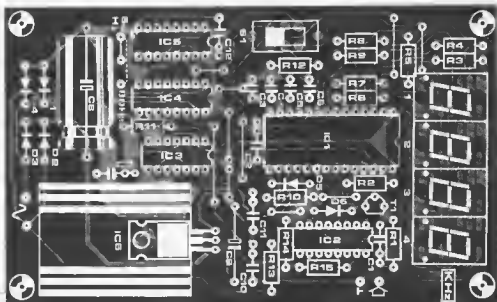
Mains frequency stability

Under normal conditions, the mains frequency in the whole of Europe is maintained at 50 Hz ± 0.1 Hz, i.e. to within 0.2%. In exceptional cases the error may increase to 0.4%, but this happens so rarely that the possibility may safely be ignored when using the mains frequency as a reference for frequency counters and the like.

For electric clocks, the cumulative long-term error is important. For instance, if the frequency were to remain at 50.1 Hz for one full day, this would lead to a total error of nearly 3 minutes. However, such errors are compensated for in such a way that the total error over any period (day, month or even year) rarely amounts to more than one minute.

For equipment using the mains frequency as a reference or timebase, the accuracy is as follows:
• instantaneous accuracy, important for frequency counters and the like, nominal: ± 0.2%
  worst-case: ± 0.4%
• long-term accuracy, important for clocks: ± 1 minute

digital clock using the SC/MP

Nowadays digital clocks are something of a commonplace. For some time now ICs have been available which contain all the necessary logic for a digital clock, and frequently these ICs also include decoder- and display driver circuits, so that one simply has to connect up the displays to have a digital clock which is fully operational. However it is also a fairly simple task to write a programme which will enable a microprocessor to perform all the complex functions of a clock chip. Naturally enough, one does not build a microprocessor system with the sole intention of using it as a digital clock. However if such a system is already available, then a clock programme represents an interesting and useful example of the possibilities afforded by a microcomputer.

The flow diagram of the software clock is shown in figure 1. Basically the programme sets up a software counter for each of the three variables involved, i.e. seconds, minutes and hours. For each of these counters a byte is reserved in memory, the contents of which are continually incremented.

When the programme is started, the clock must be set to the correct time. This is done by presetting the counters to the desired values.

The state of the counters is displayed on the HEX I/O unit, with, as is normal in the case of digital clocks, the digit furthest to the right indicating seconds (units), whilst the digit on the extreme left on the display indicates hours (tens). The contents of the seconds counter are incremented by 1 every second, and the new value indicated on the displays. When the seconds counter reaches 60 (decimal), then this counter is reset to zero and the minutes counter is incremented.

The new contents of the seconds- and minutes counters are then displayed, whereupon the seconds counter is once more incremented, and so on. When the minutes counter reaches 60 (decimal), this counter is reset and the hours counter incremented. The hours counter of course counts only to 24, and is then reset to zero.

Programme

The simple flow diagram of figure 1

One of e number of programmes which will shortly appear on disc, under the ESS label (see elsewhere in this issue), is the following clock programme, which enables the SC/MP to be used as a digital clock.

M. Reimer

1

START

set counters and display

Delay

increment sec counter

< 60 — yes → Display sec counter

reset sec counter increment min-counter

< 60 — yes → Display min counter

reset min-counter increment hour-counter

< 24 — yes → Display hour-counter

reset hour-counter

9542 1

Table 1.

Address	Code	Mnemonic
		DIS: display routine
0F00	08	NOP
0F01	01	XAE
0F02	C40F	LDI 0F
0F04	50	ANE
0F05	01	XAE
0F06	1C	SR
0F07	1C	SR
0F08	1C	SR
0F09	1C	SR
0F0A	C80F	ST BYTE
0F0C	C280	LD-128 (2)
0F0E	C900	ST 00 (1)
0F10	C009	LD BYTE
0F12	01	XAE
0F13	C280	LD-128 (2)
0F15	C901	ST 01 (1)
0F17	3F	XPPC 3
0F18	90F7	JMP DIS
0F1A	•	BYTE
		TA8: table of 7-segment code
0F1B	3F	
0F1C	8B	
0F1D	5B	
0F1E	4F	
0F1F	66	
0F20	6D	
0F21	7D	
0F22	07	
0F23	7F	
0F24	6F	
0F25	08	NOP; start address
0F26	C417	LDI 17
0F28	33	XPAL 3
0F29	C40F	LDI 0F
0F2B	37	XPAH 3
0F2C	C407	LDI 07
0F2E	35	XPAH 1
0F2F	C400	LDI 00
0F31	31	XPAL 1
0F32	C41B	LDI 1B
0F34	32	XPAL 2
0F35	C40F	LDI 0F
0F37	36	XPAH 2
0F38	C07A	LD SEC
0F3A	3F	XPPC 3
0F3B	C403	LDI 03
0F3D	31	XPAL 1
0F3E	C075	LD MIN
0F40	3F	XPPC 3
0F41	C406	LDI 06
0F43	31	XPAL 1
0F44	C070	LD HOU
0F47	3F	XPPC 3
0F49	C400	LDI 00
0F49	C9FC	ST-4 (1)
0F4B	C9FF	ST-1 (1)
0F4D	00	HALT
		$ 1
0F4E	C407	LDI 07
0F50	8F01	DLY 01
0F52	08	NOP
		$ 2
0F53	C402	LDI 02
0F55	8F01	DLY 01
		$ 3
0F57	C461	LDI 61*
0F59	8F00	DLY 00
		$ 4
0F58	C482	LDI 82
0F5D	8FC9	DLY C9
0F5F	8FFF	DLY FF
0F61	8FFF	DLY FF
0F63	8FFF	DLY FF
0F65	C400	LDI 00
0F67	31	XPAL 1
0F68	C84A	LD SFC
0F6A	02	CCL
0F6B	EC01	DAI 01
0F6D	C845	ST SEC
0F6F	3F	XPPC 3
0F70	C042	LD SEC
0F72	03	SCL
0F73	FC60	CAI 60
0F75	9CD7	JNZ $ 1
0F77	C83B	ST SFC
0F79	3F	XPPC 3
0F7A	08	NOP
0F78	08	NOP
0F7C	08	NOP
0F7D	08	NOP
0F7E	08	NOP
0F7F	08	NOP
0F80	C403	LDI 03
0F82	31	XPAL 1
0F83	C030	LD MIN
0F85	02	CCL
0F86	EC01	DAI 01
0F88	C828	ST MIN
0F8A	3F	XPPC 3
0F88	C828	LD MIN
0F8D	03	SCL
0F8E	FC60	CAI 60
0F90	08	NOP
0F91	08	NOP
0F92	9CBF	JNZ $ 2
0F94	C81F	ST MIN
0F96	08	NOP
0F97	08	NOP
0F98	08	NOP
0F99	3F	XPPC 3
079A	C406	LDI 06
0F9C	31	XPAL 1
0F9D	C017	LD HOURS
0F9F	02	CCL
0FA0	FCB1	DAI 01
0FA2	CB12	ST HOURS
0FA4	3F	XPPC 3
0FA5	C00F	LD HOURS
0FA7	03	SCL
0FA8	FC24	CAI 24
0FAA	08	NOP
0FAB	08	NOP
0FAC	9CA9	JNZ $ 3
0FAE	C806	ST STD
0FB0	3F	XPPC 3
0FB1	90A8	JMP $ 4
0FB3	•	SEC
0FB4	•	MIN
0FB5	•	HOURS

*see text

Figure 1. This figure gives the simplified flow-diagram of the clock programme.

Table 1. The detailed listing of the programme in machine code together with mnemonics.

provides an overview of the programme. A detailed listing of all the programme steps in machine code is given in table 1. Since the programme runs to more than 200 bytes, it was considered long enough to be recorded on disc.

The section of memory from 0F00 to 0FB6 is reserved for the programme. The first section of the programme, from 0F00 up to and including 0F24 represents the display routine, which converts the contents of the various counters into the correct 7-segment code for the displays. This means that the start address of the programme is not 0F00, but 0F25. Before the programme is run, the correct time should be entered at addresses 0FB3 (seconds), 0FB4 (minutes) and 0FB5 (hours). Since the programme treats the contents of these locations as decimal numbers, one simply has to enter the correct time

in decimal by means of the MODIFY routine.

When the programme is started, the values entered at these locations will appear on the display, but the clock does not run. The clock is started at exactly the right moment by means of the HALT-RESET key.

If, after a certain period, the clock starts to run fast or slow, the reason for this is that the clock frequency of the SC/MP is not exactly 1 MHz. To correct the clock, the contents of location 0F58 (in the listing, this is the second half of the instruction at address 0F57) should be altered accordingly. If the clock is running fast, then the contents should be increased, whilst if the clock is running slow then they should be decreased.

M

programmable call generator

The earlier version of the automatic call-sign generator was designed to transmit a morse-encoded version of a station's call-sign every 5 or 10 minutes. The morse code for the call sign was stored in a diode matrix memory. This means that in order for the unit to transmit other messages it is necessary to set up new diode matrices. The matrix is thus similar to a ROM- (Read Only Memory) type of storage, in that the contents of the memory cannot be altered or replaced, but only read out. However it would be perfectly feasible to replace the ROM by a RAM (Random Access Memory), the contents of which can easily be altered, and hence used to store different messages. In addition it is possible to arrange matters such that the basic function of the call-generator, i.e. to automatically transmit the station's call-sign, remains unaffected.

The modified version of the circuit is shown in figure 1. The most important difference between it and the original circuit is that two pairs of analogue switches are incorporated into the connections leading from the call generator to the diode matrix. When the selector switch is in the 'ROM' position, the corresponding pair of switches simply forms a through connection, and the call generator continues to regularly transmit the call-sign stored in the diode matrix. When the selector switch is moved to the 'RAM' position, the other pair of switches is activated, with the result that the B and C inputs of the call generator are connected to the outputs of two RAMs. For these it was decided to use the relatively inexpensive 2102, a 1024 x 1 bit static RAM, which means that the length of the message which is to be automatically transmitted is limited to a maximum of 1024 morse characters (dot, dash or space).

In order to read out the contents of each location in the RAMs, two counters are used to continuously increment the address of the RAMs.

The circuit diagram of the add-on circuit to the call generator plus part of the address circuitry is shown in figure 2. The counters used to address the RAMs are 4029's. They are equipped with a preset-facility, and this
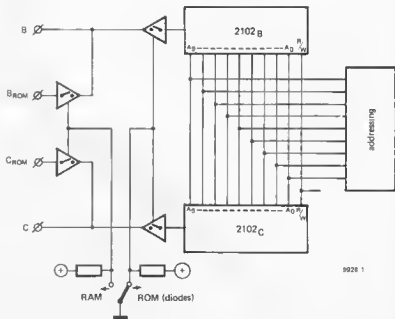
The automatic call-sign generator, which was published in Elektor 10, February 1976, relieved radio amateurs of the chore of having to periodically repeat their call-sign during e QSO. The circuit described here, which is an extension to the above call generator, allows the operator to automatically transmit a number of pre-programmed morse-encoded messages.
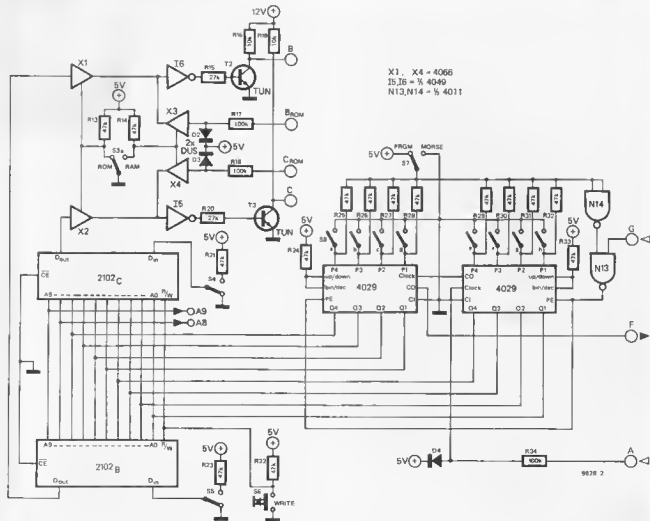
is used to actually programme the RAMs. The desired address of a particular bit of data is set up by means of switches S8a ... S8h, whilst the data itself is determined by switches 4 and 5. Table 1 shows how the various combinations of morse characters are encoded digitally. For a '0', the D inputs of the RAMs should be connected to earth (using switches S4 and S5), whilst a '1' is obtained by connecting them via a resistor to plus supply (+5 V). As long as switch S7 remains in the 'prgrm' position, successive addresses can be entered using S8a ... S8h.

With 8 address switches it is only possible to address 256 bits of memory,

MORSE CODE	2102C	2102B
dot	0	0
dash	1	0
dot + sp	0	1
dash + sp	1	1

1

Figure 1. The block diagram of the add-on 'programmer' circuit for the automatic call-sign generator.

Figure 2. The circuit diagram of the add-on circuit minus the logic gating for the two highest address bits of the RAMs.

whilst the two RAMs have a combined capacity of 1024 bits. To be able to address all of the available memory, it is divided into four sections of 256 bits, each of which can be selected by means of switch S9 (see figure 3). This arrangement was chosen for practical reasons, since it means that four different messages can be stored in memory.

For this system to operate however, the two highest address bits of the RAMs must be addressed separately. The circuit which performs this function is shown in figure 3. Whilst the RAMs are being programmed, or before a message is to be transmitted, the section of memory to be accessed can be selected by means of switch S9. When in position '1', only the contents of the corresponding section of RAM will be transmitted, and the same is true for positions 2, 3 and 4. However it is also possible to automatically transmit several messages one after another. This is done by selecting the appropriate combination-position for S9. For example, in position 3 + 4, the contents of sections 3 and 4 are transmitted successively.

The state of the two highest address bits is controlled by the outputs of two flip-flops (FF1 and FF2), which can be set or reset (via N1 . . . N4) by selecting one of the first 4 positions of S9. When the call-generator is switched on, the monostable round N12 ensures that both flip-flops are reset. When the third and fourth sections of memory are to be transmitted, the monostable round N11 presets flip-flop FF2.

It may, of course, be the case that the message stored in memory is considerably shorter than the available 256 bits. It is then necessary to interrupt the transmission immediately after the message in question by operating the reset switch (S2) on the call generator.

Wiring and power supply

The wiring diagram for the connections between the call generator and the add-on circuit is given in figure 4. As has already been mentioned, the extra circuit is situated between the call generator proper and the diode matrix. The original connections between these two points are therefore broken, and
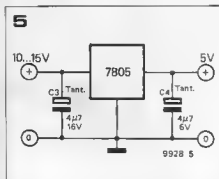
Figure 3. The address circuitry for the two highest address bits of the RAMs. This arrangement enables the available memory capacity to be divided into four separate blocks.

Figure 4. The wiring diagram for the connections between the cell generator and the add-on circuit.

Figure 5. A suggested power supply for the add-on circuit, whereby the required voltage is derived from the existing supply voltage of the call generator.

the points marked B$\overline{ROM}$ and C$\overline{ROM}$ are joined to the diode matrix. Outputs B and C in figure 2 are taken to the corresponding inputs of the call generator, whilst input A is taken to point A of the call generator. Points F and G and address bits A8 and A9 in this figure refer to the diagram of figure 3.

Points D and E in figure 3 are connected to the corresponding points in the call generator. In the case of point E a small modification affecting the reset switch, S2, in the call generator is required. Originally this switch was connected in parallel with capacitor C3. For use with the add-on circuit however, the contact of S2 which was joined to point E should be disconnected and joined to earth. This step ensures that the reset facility is preserved.

The complete add-on circuit is fed from a 5 V supply, this being the voltage required by the two RAMs. Since the original call generator operated at a supply voltage of between 10 and 15 V, an extra supply stage is required. Figure 5 shows a suitable circuit which derives the necessary 5 V from the existing supply voltage of the call generator.

Literature:
Elektor 15, February 1976, Automatic call-sign generator.

TV sound modulator

When used in conjunction with the UHF modulator described in the December 1977 issue of Elektor, or other UHF modulators, this sound modulator will allow audio signals to be fed to the antenna input of a domestic TV set and reproduced via the audio circuits of the receiver.

A video signal can be fed into the antenna socket of a domestic TV receiver by amplitude modulating the signal onto a UHF carrier. This is the function of the UHF modulator described in the December 1977 issue of Elektor. However, if it is also necessary to feed a sound signal into the receiver, this cannot be modulated directly onto the UHF carrier, since an audio signal lies within the spectrum of the video signal, and the two would interact. It is first necessary to place the sound signal outside the video signal band by modulating it onto a subcarrier, using frequency modulation for better sound quality. The frequency-modulated subcarrier is then modulated onto the UHF carrier together with the video signal.

Since the sound subcarrier is itself not usually amplitude modulated (see table 1) it does not produce amplitude modulation of the UHF carrier, but causes the appearance of a second carrier (frequency-modulated) whose centre frequency differs from the video carrier by 6 MHz. This is illustrated in figure 1 and clarified in table 1.

In a broadcast TV system most of the lower sideband (LSB) is suppressed. This suppression generally starts at about 1 MHz from the carrier, leaving only a small part of the video sideband and none of the sound. However, for a modulator which is to be used in the home, no suppression is necessary.
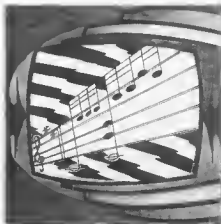
Block diagram

Figure 2 shows a block diagram of a sound modulator. The first stage of the modulator is a high-frequency pre-emphasis network, which boosts the high end of the audio spectrum to improve the signal-to-noise ratio. A

Specifications

The specifications given below are based on measurements made on the prototype at a supply voltage of 15 V.
Frequency deviation: 25 kHz/V. Maximum ± 75 kHz for 6 V p-p input.
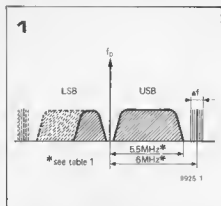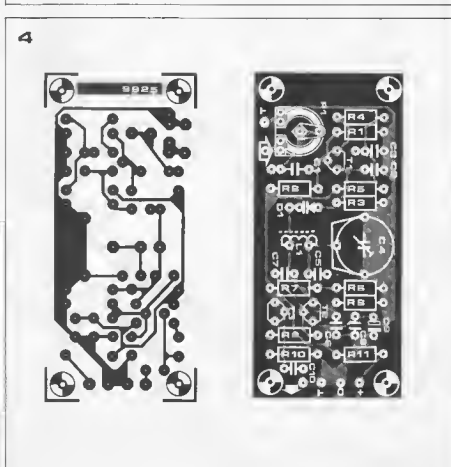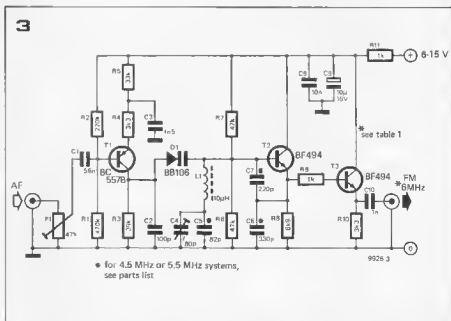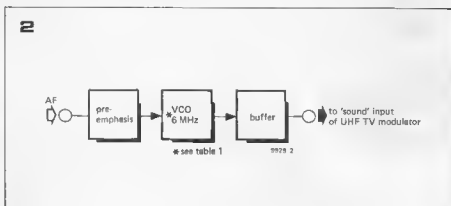Output level: 3 V p-p from 1 k.

Figure 1. Showing the relationship of the FM sound carrier to the AM vision carrier and its sidebands.

Figure 2. Block diagram of a sound modulator.

Figure 3. Complete circuit of the 6 MHz TV sound modulator.

Figure 4. Printed circuit board and component layout for the modulator (EPS 9925).

Parts list

Resistors:
R1 = 470 k
R2 = 220 k
R3 = 39 k
R4,R10 = 3k3
R5 = 33 k
R6,R7 = 47 k
R8 = 6k8
R9,R11 = 1 k

Capacitors:
C1 = 56 n
C2 = 100 p ceramic
C3 = 1n5
C4 = 7 . . . 80 p trimmer
C8 = 10 n ceramic
C9 = 10 µ/16 V
C10 = 1 n ceramic

	6.0 MHz	5.5 MHz	4.5 MHz
C5	82 p	100 p	180 p
C6	330 p	390 p	680 p
C7	220 p	270 p	390 p

Semiconductors:
T1 = BC 557B
T2,T3 = BF 494
D1 = BB 106

Miscellaneous:
P1 = preset potentiometer 47 k
L1 = r.f. choke 10 µH

complementary de-emphasis network in the TV set cancels this boost to give a flat frequency response.

The heart of the sound modulator is a 6 MHz voltage-controlled oscillator, whose frequency varies in sympathy with the amplitude of the audio input signal.

The final stage of the modulator is an output buffer which allows the 6 MHz output to be fed direct to the second input of the UHF modulator.

Complete circuit

The full circuit of the TV sound modulator is given in figure 3. The input stage around transistor T1 functions as an input buffer and pre-emphasis filter. This has unity gain at low frequencies, rising to 10 at the high end of the audio spectrum. The pre-emphasis is determined by the time constant R5/C3, and corresponds to the European standard of 50 μs.

The oscillator section 'T2' is a standard Clapp circuit, chosen for its exceptional stability. The frequency of this oscillator is modulated by using the audio signal from T1 to alter the capacitance of a varicap diode, D1.

The circuit is completed by an output buffer, emitter follower T3.

Construction

Construction of the sound modulator is extremely straightforward using the printed circuit layout of figure 4. To minimise stray radiation and frequency drift the circuit board should be built into a screened, i.e. metal, box. Connection from the output of the sound modulator to the input of the UHF modulator should be by coaxial cable as shown in figure 5. The current consumption of the circuit is extremely low (1 mA) so power can be taken from the existing supply to the UHF modulator.

Adjustment

Setting up the modulator is extremely simple, since incorrect adjustment is immediately apparent. Firstly, a suitable video signal is fed into the TV set via the UHF modulator and the set is correctly tuned to this.

The sound signal is then fed in and C4 is adjusted to tune the centre frequency of the modulator. Incorrect tuning will manifest itself as distortion, intercarrier buzz or no sound at all being present. Distortion may also occur if the audio input level is too high, but this can be adjusted using P1 on the sound modulator board.

The sound carrier level may be set by adjusting P2 on the UHF modulator board.

Figure 5. Connection from the output of the sound modulator to the input of the UHF modulator should be by coaxial cable.

Figure 6. Photograph of the completed board.

Table 1. A list of the various sound intermediate frequencies used by different countries. Also listed is the mode and deviation which is used. Note that the unit described here is not suitable for use in France, Luxembourg and Monaco.

Table 1.

sound IF	mode and deviation (Δf)	country or region
4.5 MHz	FM, 25 kHz	North and South America, Japan
5.5 MHz	FM, 50 kHz	Most of Western Europe, East Germany, Yugoslavia, most of north Africa.
6.0 MHz	FM, 50 kHz	UK, Northern Ireland, most of the southern part of Africa.
6.5 MHz	FM, 50 kHz	USSR, and most east European countries.
6.5 MHz	AM	France, Luxembourg, Monaco

Note: this table is only valid for audio systems, not video!

reaction timer

Like digital clocks, reactions timers have conventionally been built using TTL- or CMOS logic ICs. However, providing it does not operate at excessively high speeds, the function of any logic circuit, including that of a reaction timer, can be duplicated by a suitably programmed microprocessor.

In most reaction timers the user simply has to respond as quickly as possible to a signal generated by the timer after a random lenght of time. By using the SC/MP system however, it is possible to add an extra twist to the challenge.

Instead of having only one button to push, the user must select the correct data key from all those on the HEX I/O unit, never knowing in advance just which key it will be.

How the programme works can be gathered from the flow diagram shown in figure 1. Once the programme is started the text 'START' will appear on the displays on the HEX I/O unit, whereupon one of the data keys (O - F) can be pressed. After an undefined length of time a random (hexadecimal) number will appear in display 2. As quickly as possible the user must then depress the corresponding key on the keyboard. For example, if the display shows '7', then key '7' should be pressed, and so on. If, within 10 seconds of the number appearing on the display, no key or an incorrect key has been pressed, then the text 'START' will be regenerated on the display. If however the correct key has been pressed, then the time between the number appearing on the display and that key being pressed will be displayed. This interval is measured by a software counter which is incremented every millisecond, which means that the reaction time shown on the displays is also in milliseconds. If the reaction time is less than the previous best time, T_0, the SC/MP will express its admiration by displaying the text 'SPLENDID'. The displays will then alternately show this text and the reaction time until one of the keys is pressed, causing 'START' to reappear on the displays.

If the reaction time is greater than T_0 however, then it alone will remain on the displays until one of the data keys is pressed, whereupon 'START' will re-

Another programme which will shortly be made available on the same disc as the clock programme is for a reaction timer. With the aid of the SC/MP this programme allows a person's reactions to be timed down to the last millisecond.

H. Huschitt

appear.

For the first test T_0 equals 1 second. If the reaction time is longer than 1 second then T_0 remains at this value. If, however, it is shorter than 1 second, then the initial reaction time of the user is taken as the new value of T_0, so that, at the second attempt, he must be faster than his previous time to elicit 'SPLENDID' from the SC/MP.

The text 'START' must always appear on the displays before another attempt can be made to improve one's previous score. When no further improvement is possible the programme can be started again by means of the NRST switch.

Listing

In conclusion, the listing for the reaction timer programme is given in table 1. Although the programme is not complicated, it is nonetheless considerably longer than the clock programme. In order to take up a minimum of page space therefore, the listing contains only the programme addresses and the instructions in machine code, so that if necessary they can be entered by hand. The section of memory reserved for the programme runs from ØC00 up to and including ØCFF, and the start address is ØCØØ. Like the clock programme, the reaction timer is intended for systems with SC/MP 1 and a 1 MHz crystal or SC/MP 2 and a 2 MHz crystal.
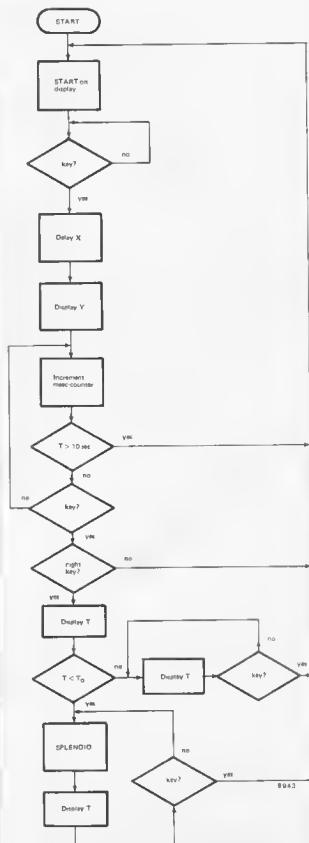
Figure 1. Flow diagram of the reaction timer programme.

Table 1. The programme listing together with addresses.

Table 1.

0C00	C400	0C82	CA1D
0C02	C857	0C84	3F
0C04	C410	0C85	C901
0C06	C854	0C87	D40F
0C08	C46D	0C89	E209
0C0A	C904	0C8B	9CD1
0C0C	C478	0C8D	C9CE
0C0E	C900	0C8F	CA01
0C10	C903	0C91	C9CB
0C12	C45F	0C93	CA02
0C14	C902	0C95	C4A0
0C16	C450	0C97	CA1D
0C18	C901	0C99	3F
0C1A	C400	0C9A	C400
0C1C	C905	0C9C	C9FF
0C1E	C906	0C9E	C900
0C20	C9FF	0CA0	C408
0C22	A838	0CA2	C8B6
0C24	C108	0CA4	8FFF
0C26	94FA	0CA6	88B2
0C28	8FFF	0CA8	9CFA
0C2A	C400	0CAA	C40A
0C2C	C900	0CAC	CA1D
0C2E	C901	0CAE	03
0C30	C902	0CAF	C0AA
0C32	C903	0CB1	F8AA
0C34	C904	0CB3	C0A7
0C36	C022	0CB5	F8A7
0C38	CA01	0CB7	9403
0C3A	C4A0	0CB9	3F
0C3C	CA1D	0CBA	90A2
0C3E	8F20	0CBC	C09F
0C40	B818	0CBE	C898
0C42	9CFA	0CC0	C09C
0C44	C400	0CC2	C898
0C46	37C4	0CC4	C46D
0C48	5533	0CC6	C906
0C4A	3F	0CC8	C473
0C4B	C400	0CCA	C905
0C4D	C9FF	0CCC	C438
0C4F	C900	0CCE	C904
0C51	C902	0CD0	C479
0C53	C903	0CD2	C903
0C55	C904	0CD4	C437
0C57	9907	0CD6	C902
0C59	00	0CD8	C45E
0C5A	0000	0CDA	C901
0C5C	0000	0CDC	C408
0C5E	90A8	0CDE	C820
0C60	C400	0CE0	C430
0C62	C8F9	0CE2	C900
0C64	C8F8	0CE4	0808
0C66	02	0CE6	C45E
0C67	C401	0CE8	C9FF
0C69	E8F2	0CEA	C108
0C6B	C8F0	0CEC	9403
0C6D	C400	0CEE	3F
0C6F	E8ED	0CF0	99C7
0C71	C8EB	0CF1	8808
0C73	06	0CF3	9CE9
0C74	9402	0CF5	C400
0C76	90E6	0CF7	C905
0C78	C4A6	0CF9	C906
0C7A	8F90	0CFB	908E
0C7C	C108	0CFD	00
0C7E	94E7	0CFF	
0C80	C40A		

1

automatic mono stereo switch

When an FM stereo transmission has been demodulated, but before it has been decoded, it consists of two distinct channels. The left plus right (L + R) signal occupies the frequency band 0 ... 15 kHz. This signal is essential for mono compatibility, as it is the only part of the stereo signal that a mono radio can receive. The frequency band from 23 ... 38 kHz is occupied by the lower sideband of a 38 kHz subcarrier, onto which the L−R (left minus right) signal is modulated. In principle the stereo signal is decoded by demodulating this signal, adding it to the L + R signal to get 2L, and subtracting it from the L + R signal to get 2R. Since the 23 ... 38 kHz signal is absent during a mono transmission, a circuit which can detect this signal will be able to distinguish between mono and stereo transmissions. This is the principle of the automatic mono-stereo switch.

Block diagram

The principle of the automatic mono-stereo switch is illustrated in the block diagram of figure 1. A portion of the signal from the output of the detector stage of the tuner is fed to a selective amplifier with a centre frequency of 35 kHz. If a signal is present in its passband it will be amplified, then rectified by an envelope detector. The resulting positive voltage is applied to a comparator, whose output swings negative and switches on the stereo decoder. If the transmission is mono then no signal will be fed through the selective amplifier and the comparator output will remain high, switching off the stereo decoder.

Complete circuit

The circuit of the mono-stereo switch is shown in figure 2. A1 to A4 are the four sections of a TL084 quad FET op amp. The selective amplifier is built around A1 and A2, the passband being determined by L1, L2, C4 and C5. A positive bias voltage of just less than half supply voltage is applied to the selective amplifier from the junction of R2 and D1. This is fed through the rectifier A3 to appear on capacitor C6 and hence to the inverting input of comparator A4. The non-inverting input of A4 receives a

Since the end of February, owners of FM stereo receivers will have noticed that the stereo indicator lamp stays on continuously. This is due to a decision by the BBC to transmit the 19 kHz pilot tone with all programmes, ostensibly to eliminate annoying clicks that occur when switching the pilot tone on and off. The commercial radio stations have, of course, followed this practice for some time.

As the mono-stereo switch in a stereo receiver operates by detecting the pilot tone, this means that such receivers are now incapable of distinguishing between mono and stereo transmissions and will be permanently switched to stereo unless the 'mono' switch is pressed. Apart from the minor annoyance of not knowing if a programme is in stereo (unless one buys the Radio Times) there is the greater inconvenience of listening to mono transmissions with the poorer signal-to-noise ratio inherent in stereo transmission. This is particularly a problem in areas of fringe reception.

The circuit described in this article distinguishes between mono and stereo transmissions by detecting whether or not stereo information is present in the received signal, independent of the pilot tone.

positive bias slightly higher than half supply voltage from the junction of R1 and D1. Under no-signal conditions the output of A4 is therefore positive. The output signal of the tuner is fed to the input of A1 via sensitivity control P1 and C3. If stereo information is present this will be amplified by A1 and A2 and rectified by A3, causing the voltage on C6 to rise above that at the non-inverting input of A4. The output of A4 will thus swing down to 0 V, turning on the stereo decoder.

The attack time of the rectifier is extremely short, about 2.7 ms, so the decoder will be switched to stereo immediately a stereo signal is received. However, to avoid the decoder switching back to mono during pauses in the audio signal, the decay time constant, R7-C6, is made fairly long, and the circuit will not switch back to mono operation until about 20 seconds after the cessation of a stereo signal.

The mono-stereo switch can be connected to most IC stereo decoders, such as the MC1310P, as shown in figure 3. Operation of the manual mono switch,

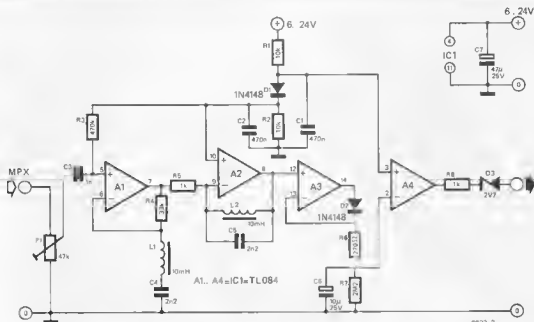Figure 1. Block diagram of the automatic mono-stereo switch.

Figure 2. Complete circuit of the mono-stereo switch.

Figure 3. Showing the connection of the mono-stereo switch to an IC stereo decoder.
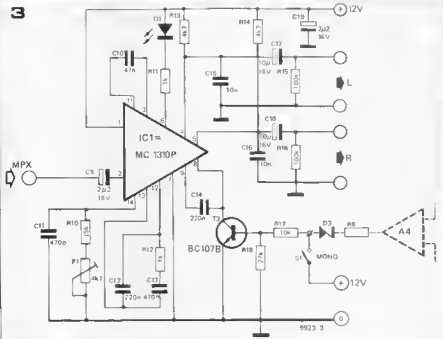
Figure 4. Printed circuit board and component layout for the circuit of figure 2 (EPS 9923).
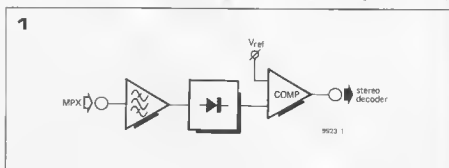
Figure 1

2

3

Parts list for figure 2 and 4

Resistors:
R1,R2 = 10 k
R3 = 470 k
R4 = 33 k
R5 = 1 k
R6 = 270 Ω
R7 = 2M2
R8 = 1 k

Capacitors:
C1,C2 = 470 n
C3 = 1 n
C4,C5 = 2n2
C6 = 10 μ/25 V
C7 = 47 μ/25 V

Semiconductors:
IC1 = TL 084
D1,D2 = 1N4148
D3 = zener 2V7

Miscellaneous:
P1 = 47 k preset
L1,L2 = 10 mH choke

which allows selection of mono operation if stereo reception is too noisy, is unaffected.

Construction

A printed circuit board and component layout for the mono-stereo switch are given in figure 4. This p.c.b. should be sufficiently compact to be built into most FM tuners, and the wide supply voltage range should allow the circuit to be powered from the supply rail of almost any tuner.

The circuit has only one adjustment, the sensitivity control P1. This should be adjusted so that the circuit operates on any stereo signal which is sufficiently strong for noise-free stereo listening. On the other hand, the sensitivity of the circuit must not be so great that it switches on spurious noise.   ◼

4
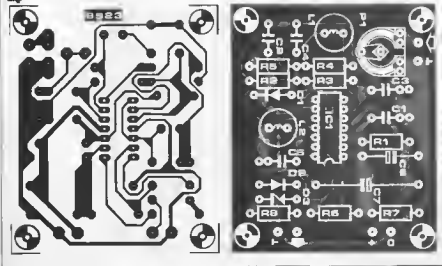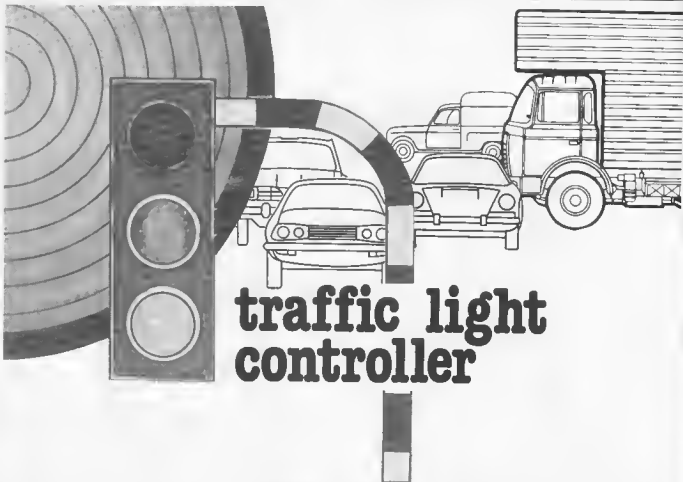
traffic light controller

The heart of the traffic light controller is a pulse sequence generator based on a self-shifting register, the basic circuit of which is given in figure 1. N1 and N2 form an input monostable. A positive pulse, of arbitrary length, applied to the input, will be differentiated by C1 and R1 to give a short positive spike at the input of NOR gate N1. The output of N1 will thus go low, pulling the input to N2 low via C2. The output of N2 will go high, which will take the other input of N1 high. The output of N1 will thus remain low even after the input pulse has terminated.

C2 will now charge via R2 until the logic 1 threshold of N2 is exceeded, when the output of N2 will go low and the monostable will reset. The input of N3 is now pulled low via C3, and its output will go high. C3 will charge via R3 until the logic 1 threshold of N3 is exceeded, when the output of N3 will go low, pulling the input of N4 low via C4, and so on. The result is that a positive-going pulse appears at the outputs of N2 to N6 in turn. The length of each pulse is individually determined by the RC time constant at the input of the relevant inverter. This makes the system much more versatile than designs which rely on clocked digital counters, since each pulse length, and hence the duration of each phase of the traffic lights, can be individually adjusted. N6 produces a short pulse at the end of the sequence, which is used for trigger purposes.

To simulate a traffic-light controlled

This versatile traffic light controller should prove a welcome addition to model town, road or railway layouts, and could also be used as an aid to road safety demonstrations in schools. The design has provision for both British and European traffic light sequences, and can also be adapted to control a 'Pelican' crossing.

pedestrian (Pelican) crossing a phase of the lights is needed where the amber light flashes. This is provided for by an astable multivibrator (N7, N8) which oscillates at approximately 2 Hz.

The sequence of pulses generated by the circuit of figure 1 is shown in the timing diagram of figure 2a, the output pulses from N2 to N6 being labelled A to E respectively, and the astable output being labelled F. Any desired sequence for a single set of traffic lights can be derived from these pulses by simple logic gating, always remembering that the length of each pulse can be individually varied to suit particular requirements.

Pelican crossing

The Pelican crossing probably has the most complicated lamp sequence that is likely to be encountered. In the quiescent state the traffic lights are green, whilst a red, standing figure is illuminated to warn pedestrians not to cross. When a pedestrian presses the push-button there is an initial waiting period, during which a WAIT sign is illuminated in the control console. The waiting period in a full-size Pelican crossing depends on when the crossing was last activated, but for the purposes of the model a fixed delay is simpler.

At the end of the waiting period the traffic lights change to amber, then to red. When the traffic lights are red the WAIT sign is extinguished, the green,
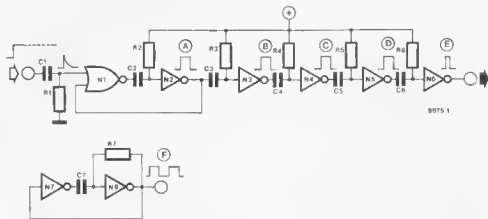
Figure 1. Showing the principle of a pulse sequence generator using a 'self-shifting register'. An astable multivibrator provides 2 Hz pulses for the 'flashing amber' phase of the Pelican crossing.

Figure 2a. Timing diagram of the pulse sequence generator.
Figure 2b. Timing diagram of the Pelican crossing.
Figure 2c. Timing diagram of one set of traffic lights at a crossing.
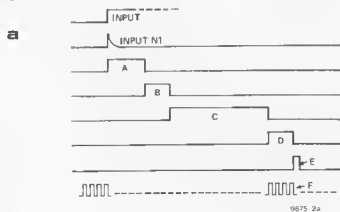
walking figure is illuminated and an audible warning sounds. After several seconds the audible warning ceases and the green figure and amber traffic lights begin to flash. The traffic lights then change to green and the red figure is illuminated.

By drawing a timing diagram for this sequence of events, as shown in figure 2b, it is easy to calculate the necessary logic functions. The wait sign is illuminated during pulses A and B, therefore WAIT = A + B (A OR B). The amber traffic light is lit during B and flashes during D, so AMBER = B + D · F. [B OR (D AND F)] The red traffic light is illuminated only during C, so RED = C. The green figure is lit during C and flashes during D, therefore GREEN FIGURE = C + D · F.

The two last conditions, the red figure and green traffic light, are slightly less obvious. The only time the red figure is NOT illuminated is during C and D. Therefore RED FIGURE = $\overline{C + D}$. Similarly, the only time the green traffic light is NOT illuminated is during B, C and D. Therefore, GREEN LIGHT = $(\overline{B + C + D})$.

Since the logic functions required are mostly OR and NOR functions, the practical circuit is most easily designed using NOR gates. CMOS gates were chosen because their high input resistance allows the use of large value resistors in the shift register, which allows long delays to be achieved even with small, non-electrolytic capacitors.

Since NOR gates are used in the circuit,

3

N1 ... N5,N7   N13 = 3 x 4001
T1,T2,T4 = BC 159C,BC 559C
T3,T5,T6 = BC 109C,BC 549C
D1 ... D4 = DUS
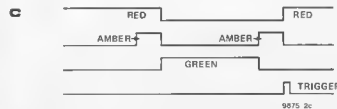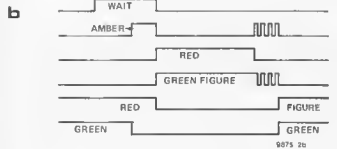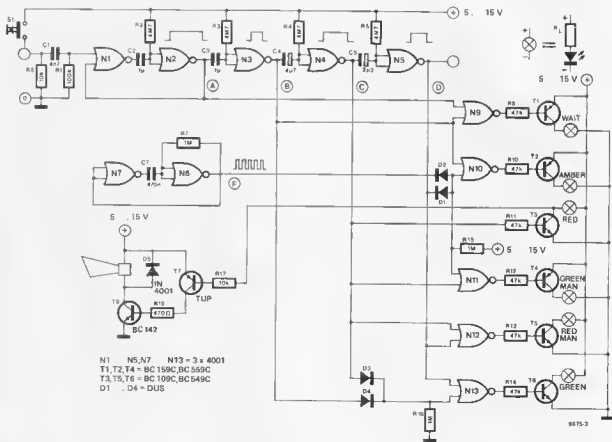
where an OR function is required a PNP transistor is used as an inverter/lamp driver. When the input to the transistor is high it is turned off and the lamp is extinguished; when the input is low the transistor is turned on and the lamp lights. For example, the WAIT sign requires A + B, so NOR gate N9 is used to drive a PNP transistor. When a NOR function is required an NPN transistor is used as a lamp driver, and does not invert the output of the NOR gate. Diodes D1 and D2 at the input of N10 perform the AND function required for the amber lamp (B + D · F) while diodes D3 and D4 at the input of N13 perform an OR function to turn N13 into a 3-input NOR-gate for the green lamp (GREEN LIGHT = B̄ + C̄ + D).

Since operation of the Pelican crossing is a 'one-shot' affair initiated solely by the pushbutton, the trigger oscillator from N6 is not required, so only 12 gates (3 ICs) are required.

The maximum current that can be supplied to the transistors before the drive transistors come out of saturation is limited by two factors; the base current which the CMOS gates can supply to the transistors, and the gain of the transis-

tors. With a 5 V supply and a transistor gain of 400, the maximum lamp current is about 37 mA. This improves as the supply voltage is increased to about 122 mA at 15 V. If incandescent filament lamps are to be driven then it is preferable to use the higher supply voltage. Otherwise higher gain (e.g. Darlington) transistors could be used. If LEDs are used they must be equipped with a suitable series current limiting resistor. The value of the resistor is given by:

$$R_L = \frac{\text{supply voltage} - \text{LED forward voltage}}{\text{required LED current}}$$

$$(k\Omega, V, mA)$$

The number of lamps connected to each driver transistor depends on the actual physical arrangement of the crossing. For example, on a two-way street with no central reservation there would be four traffic lights of each colour and two sets of pedestrian lights. The lamps may be connected in series or parallel, but series operation is preferable to

reduce current consumption. Of course, if four LEDs are connected in series the supply voltage would be greater than the sum of their forward voltage drops. (Note that in a real crossing series operation would not be used, since if one lamp failed all would be extinguished.) For the audible signal a 'sonalert' or similar audible warning device may be used, driven by T7 and T8.

Traffic-light controlled road junctions

There are many variations of traffic light sequences at road junctions, depending on the complexity of the junction and the whim of the engineer. However, the discussion here will be confined to a simple crossing, which should be adequate for most modelling applications. Here, the operating sequence is as follows: one set of lights remains at red whilst the other set goes through its sequence from red, through green, back to red again. There may then be a short delay (though frequently not) during which both sets of
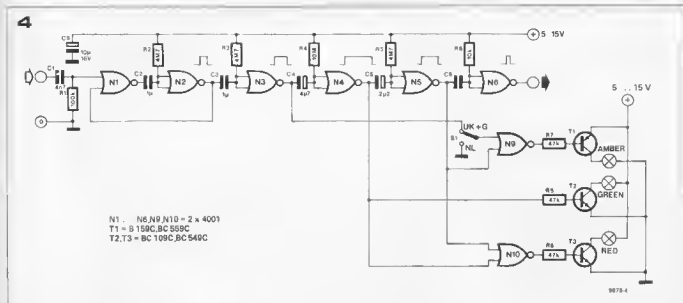
Figure 3. Circuit diagram of the Pelican crossing controller.

Figure 4. Circuit diagram of the traffic light controller.

Figure 5. Two traffic light modules are required to control both sets of lights at a crossing.
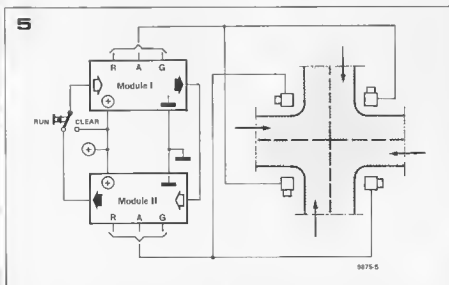
lights are red.

The first set of lights then changes to red + amber, then green, then back through amber to red. After a short delay the second set repeats the same sequence, and so on. In some countries the red + amber phase is omitted and the lights change straight from red to green.

The timing diagram for this sequence is shown in figure 2c, and it can be seen that it bears a great similarity to that for the Pelican crossing, although it is simpler and the duration of some of the phases is different. The required logic gating is quite simple: GREEN = C, AMBER = B + D and RED = $\overline{C}$ + D. If the red + amber phase is omitted then AMBER = D.

The practical circuit for one set of traffic lights is given in figure 4. The two different possibilities for amber are catered for by switch S1. Two sets of lights are required to control a crossing, so the circuit of figure 4 must be duplicated. The two circuits are then arranged to trigger each other by connecting them in a loop as shown in figure 5.

Since it is possible that the circuit may

start in an invalid sequence at switch-on, S2 is included. When this is switched to the clear position it applies a trigger pulse to the input and also breaks the loop so that the register can be cleared of any invalid states. Once the lights have ceased to change, S2 is switched back to the run position, then briefly back to the clear position to start the circuit in the correct sequence, and finally back to the run position.

The comments that were made about lamp driving with regard to the Pelican crossing apply equally to this circuit.

Calculation of time delays

The time delay (t) generated by each section of the shift register is determined by the exponential charging of the capacitor to the voltage at which the inverter output changes from logic 1 to logic 0. For this application, the equation

$$t = \frac{RC}{2}$$

is sufficiently accurate.

Using this equation the value of RC

time constant can be calculated for any given delay time. However, it should be noted that the threshold voltage of a CMOS gate is subject to a considerable tolerance, so the actual time delays obtained in practice may vary by ± 50%. **K**

easy music

The principle of 'Easy music' is extremely simple, as can be seen from the block diagram of figure 1. The 'musician's' whistle is picked up by a crystal microphone and amplified by op amp A1. A portion of the signal is fed to an envelope follower, which rectifies and filters it to produce a positive voltage that follows the amplitude envelope of the input signal. The signal is also fed to two limiting amplifiers, which convert the variable amplitude sinewave of the input signal into a constant amplitude squarewave having the same frequency

For those who do not have the time (or perhaps the patience) to mester a musical instrument, but would nonetheless like to make their own music, this simple circuit may provide the answer. The only musicel accomplishment necessary is the ability to whistle in tune.

P.J. Tyrrell

as the input signal. This squarewave is used to clock a binary counter whose division ratio can be set to 2, 4, 8 etc., so that the output is one, two, three etc. octaves below the input signal.
The counter output is used to switch transistor T1 on and off, and the collector signal of T1 is fed to the output amplifier A4. Since the collector resistor of T1 receives its supply from the output of the envelope follower, the amplitude of the collector signal, and hence of the output signal, varies in sympathy with the amplitude of the

1
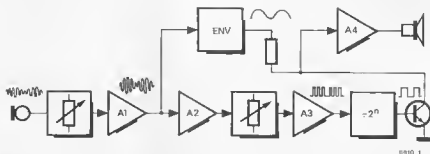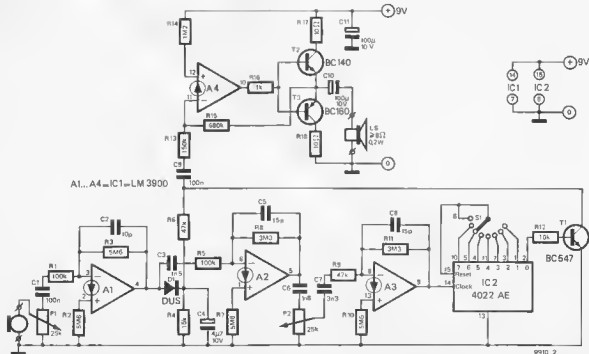
2

Figure 1. Block diagram of 'Easy music'.

Figure 2. Complete circuit diagram.

link 77

The Link appears each year in the June issue of Elektor. It contains an index to all 'Missing Links' published in 1977 plus all 'Missing Links' published so far this year. The intent of the Link is to assist the home constructor by listing corrections and improvements to Elektor circuits in one easy to find place. A simple check of the Link will show whether any problems were associated with a project. Don't forget to check Link 76 and Link 75 if the project in question was published before January 1977 or January 1976, respectively.

original input signal.

The output is therefore a squarewave whose frequency may be one or more octaves lower than the input signal and whose amplitude dynamics follow the amplitude of the input signal.

Complete circuit

The complete circuit is given in figure 2, and the sections of the circuit shown in the block diagram are easily identified. The output of the crystal microphone is fed to P1, which functions as a sensitivity control. A1 is connected as a linear amplifier with a gain of approximately 56. A portion of the output signal from A1 is rectified by D1 and the resulting peak positive voltage is stored on C4. The output signal from A1 is further amplified by A2 and A3, the combined gain of A1 to A3 being sufficient to cause limiting at the output of A3, even with very small input signals. P2 is used to adjust the gain of the limiting amplifier so that limiting just occurs with the smallest input signal, this avoiding limiting caused by extraneous noises.

The output of A3 is used to clock a CMOS binary counter, whose division ratio may be set by means of S1. The output of IC2 switches transistor T1 on and off. Since the collector resistor of T1 (R6) receives its supply voltage from C4, the amplitude of the collector signal varies in sympathy with the input signal. This signal is amplified by a small audio power amplifier built around A4, which drives a small loudspeaker.

Additions to the basic circuit

However, the possibilities do not end there. The more ambitious constructor may wish to add filters and other circuits to produce different output waveforms which will extend the tonal possibilities of the instrument. Such variations on the basic design are, however, beyond the scope of this short article, and are left to the ingenuity of the individual reader.

market

Programmable pulse generator

Programmable timing accuracies of 2% of programmed value with a repeatability of 0.5% is available in this new Hewlett-Packard Model 8160A Programmable Pulse Generator. All pulse parameters are programmable – width, period, delay, transition times, amplitude with both high and low levels separately setable while holding the other level stable. Pulses are generated from 1 Hz to 50 MHz. Transition time of ± 1% is specified for programmed repeatability.

The basic pulse generator is single channel with a dual channel option available. The ability to store and recall up to nine complete instrument settings is one of the features in the 8160A. Complete operating mode settings, pulse parameters and output settings are recalled by simply pressing two buttons, or by addressing one of nine storage registers via the HP-IB (IEEE-488) interface bus. This built-in versatility in a precision pulse generator lets the user switch rapidly between different pulse parameters without knob twisting and verification of pulse parameters with an oscilloscope. Built-in batteries maintain data storage when the instrument is turned off. Because both keyboard and bus operation are possible, the Model 8160A is
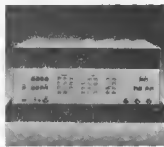
suited for both bench and system applications. Pulse period is settable from 10.0 ns to 999 ms with three digits of resolution (100 ps min.). Internal and external trigger modes as well as external gate and counted burst are provided. Up to 49.9 ns, pulse width and delay are set using delay lines which provides pulses with negligible jitter.

The delay lines also allow delays longer than one period. Above 50 ns, delay and width are generated using a combination of an internal 20 MHz clock and the delay lines. Delay is from zero to 999 ms, pulse width is from 3 ns to 999 ms both with three digits of resolution.

Transition times, with both leading and trailing edges independently programmable within a ratio of 1 to 20, are from 5 ns to 9.90 ms with three digits of resolution. Programmed accuracy is ± 5% with a repeatability of ± 1%. Both upper and lower levels of the output may be separately set from +9.99 V to −9.89 V and +9.89 V to −9.99 V respectively. Maximum difference between levels with a 50 ohm load and source is 9.99 V both with a minimum difference of 0.1 V. All output levels may be doubled by operating with the internal load disabled.

In the two channel version, an A+B mode allows doubled output amplitude with a 20 V swing within a ± 20 V window from 50 ohms into 50 ohms. In addition, the A+B mode permits variable, three-level signals. It costs $11,000 (Domestic U.S.).

*Hewlett-Packard Ltd.,
King Street Lane, Winnersh,
Wokingham, Berkshire, England.*

(722 M)

Low-cost computer kit

A new low-cost do-it-yourself computer kit, the COSMAC VIP (Video Interface Processor), has been launched by RCA Solid State. The new system, designed to interface with a cathode-ray display or, via a suitable modulator, with a TV receiver, allows the user to assemble a complete microcomputer for creating and playing video games, generating computer graphics and developing microprocessor control functions.

The VIP offers a complete

computer system on a printed-circuit card, with a powerful, uncluttered operating system using only 4k bits of read-only memory. Programs can be generated and stored in an audio cassette tape recorder for easy retrieval and use.

The heart of the VIP is RCA's COSMAC CDP1802 microprocessor, incorporating C-MOS circuitry for low power consumption and an 8-bit architecture for ease of application. The VIP is based on a single 8½ x 11 inch card containing the CDP1802 microprocessor chip, a 2048 byte random-access memory, a single-chip graphic video display interface, a built-in hexadecimal keyboard, a 100 byte/s audio tape cassette interface, power supply and facilities for expanding both memory and input/output interfaces.

An interpretive programming language known as CHIP-8 simplifies the programming of video games using hexadecimal code. Extremely compact CHIP-8 programs can be stored on cassette tape for immediate use. CHIP-8 has 31 easy-to-use instructions in a 2-byte format for such programming tasks as displaying a pattern on the cathode-ray video display, adding a random byte, sounding a tone, providing 16 one-byte variables, and allowing subroutine nesting.

The 512-byte read-only memory operating system simplifies tasks such as loading program into the random-access memory via the hexadecimal keyboard, recording random-access memory contents on cassette tapes, transferring tape-recorded programs into random-access memory, displaying memory bytes in hexadecimal format on a cathode-ray tube, stepping through random-access memory contents, and examining the contents of the central-processor registers.

The VIP system is readily expandable, both on the printed-circuit card and through connectors. Random-access-memory capacity can be doubled on the card to 4096 bytes by adding four 4k bit devices, and can be expanded to 32k bytes by adding further memory capacity through a 44-pin connector socket on the card. Parallel input/output expansion to 19 lines can be achieved for use with music synthesisers, relays, a low-cost printer or an ASCII keyboard. The 44-pin connector socket on the board also allows the addition of other circuitry for miscellaneous applications.

A VIP hobbyist manual contains detailed information on kit assembly, VIP operating procedures, CHIP-8 interpreter programming technique, machine-language programming, logic description, test programs, troubleshooting guides and

system expansion. The manual also includes program listings for 20 video games, with simple instructions to nonprogrammers for using the hexadecimal keyboard.

At present, the VIP is available in a form compatible with American NTSC monochrome television standards, but a PAL interface chip with full colour and programmable sound capability will be available shortly.

*RCA Solid State– Europe,
Sunbury-on-Thames,
Middlesex, TW16 7HW, England.*

(720 M)

3-Terminal adjustable negative regulators

National Semiconductor Corp. has developed a series of negative three-terminal adjustable voltage regulators.

The LM 137/LM 237/ LM 337 are adjustable 3-terminal negative voltage regulators capable of supplying an excess of −1.5 A over an output voltage range of −1.2 V to −37 V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM 137 series features internal current limiting, thermal shutdown and safe area compensation, making them virtually blowout-proof against overloads.
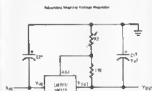
The LM 137/LM 237/ LM 337 serve a wide variety of applications including local on-card regulation, programmable output voltage regulation or precision current regulation. The LM 137/LM 237/ LM 337 are ideal complements to the LM 117/LM 217/LM 317 adjustable positive regulators.

Features

- Output voltage adjustable from −1.2 V to −37 V
- 1.5 A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W

*National Semiconductor
19, Goldington Road
Bedford MK40 3LF
England*

(727 M)

DC standard

The YEW Type 2554 is a new DC Voltage and Current Standard designed for bench or field use. The unit is housed in a compact and rugged case, and may be powered by mains or rechargeable batteries. The five voltage ranges are from 12 mV to 120 V, and current ranges are from 12 mA to 120 mA.

Resolution on the lowest ranges is 1μV and 0.1μA respectively, and stability is 0.001%/hr. Accuracy is 0.05% making the instrument suitable for calibration of most general purpose measuring instruments, recorders, data acquisition systems, and process control recording and controlling instrumentation. Functions include polarity reversal switch, over-voltage and over-current protection and warning systems, and an optional reference junction compensator unit for use when thermocouple systems are being calibrated.

Martron Ltd., 20 Park St., Princes Risborough, Bucks, England

(769 M)

.6" Leds

Industrial Electronic Engineers, Inc., (IEE), is now offering a new line of red '63' LED digital displays designated as IEE-HERCULES Series 1800. Series 1800 makes available high brightness, dual element models, and also, economy, single element models. The dual element LEDs consist of two chips of light emitting material which are electrically interconnected in series and act functionally as single segments. Both types of red LEDs have wide angle and long distance viewing with a high contrast ratio. Common anode and cathode versions are available with right and left hand decimal points and a 1 overflow. These IC compatible LEDs offer reliability and long operating life with low power consumption and low forward voltage.
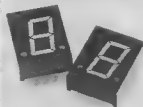
Series 1800 LEDs are directly interchangeable with Litronix. Delivery is immediate; these devices are available through IEE Stocking Distributors.

IEE, 7740 Lemona Avenue, Van Nuys, California, 91405, USA

(770 M)

Plastic boxes

Vero Electronics Limited have expanded their range of plastic enclosures for electronic equipment by the introduction of the Verobox Series II Case Boxes. These boxes are moulded in light grey high-impact polystyrene in an attractively-styled bezel. The anodised aluminium front panel supplied with the box is retained between the two halves, avoiding the need for fixing screws. Slots and bosses are moulded into the interior of the box, so that a wide choice of mounting positions, either horizontal or vertical, is available for circuit boards or component decks. Many of the boxes have a battery compart-

ment which is accessible without dismantling the box.
The standard range consists of fifteen boxes, varying from 110 mm x 68 mm x 33 mm to 190 mm x 138 mm x 91 mm, and other sizes are available to special order at a minimum quantity of 100.
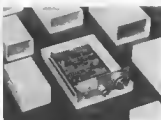
Vero Electronics Limited, Chandler's Ford, Eastleigh, Hampshire, SO5 3ZR, England

(766 M)

Stickies

Concept Electronics, producers of TTL Stickies, the IC-size self-adhesive labels showing pin-outs for most frequently used TTL ICs, announce the addition of CMOS Stickies to their range of aids for users of digital ICs.
CMOS Stickies are packed in sets of 480 labels, each set covering 65 different 4000-series ICs. Both TTL and CMOS Stickies are available from Concept Electronics at £ 2.80 per set, 2-10 sets at £ 2.50 each.
The company have also introduced 120-label sets for TTL or CMOS. Designed especially for
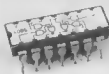
hobbyists, they sell at 80p per set. Each set of Stickies is packed in a sturdy plastic wallet, complete with data sheet and full instructions.
As a new service for specialised industrial applications, Stickies can be custom produced in a wide range of materials and adhesives.

Concept Electronics, 8 Bayham Road, Sevenoaks, Kent, England

(773 M)

De-soldering

To complement its professional range of de-soldering guns, A.B. Engineering Company has introduced two new models.

Both feature single handed operation, a plunger is depressed then the tool is placed over the joint to be desoldered — a soldering instrument is used to melt the solder. A press button releases the plunger creating sufficient suction to remove the molten solder.
The new Popular model is designed for field engineers and it fits easily into a pocket. Two versions are available, the Standard has an orange body fitted with 3/4" long by 1/2" diameter nozzle, and the Micro has a red body and a 1" by 1/16" diameter nozzle.
The 'Top of the Range' De-luxe model incorporates an anti-recoil system to eliminate the jolt caused by the return of the plunger and it features three guide rods for smooth action.

A removable guard is fitted to aid precise control. With the guard removed the De-luxe can be reset single handed by simply pressing the plunger against the bench. The Popular Standard and Micro De-soldering guns are priced at £ 4.75 and the De-luxe is priced at £ 7.25. All prices are plus V.A.T.

A.B. Engineering Company, Apem Works, St. Albans Road, Watford, Herts, WD2 4AN. England

(767 M)

04 guard

Licon's 04 illuminated push button series has now been fitted with a switch guard which can be specified with their bezel barrier lighted switches and indicators (for uniform display appearance).
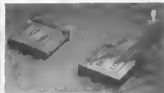
The integral hinged cover prevents accidental depression of the display screen.
Both clear and smoky hidden legend versions are available.

Licon, Norway Road, Hilsea Industrial Estate, Portsmouth PO3 5HT, England

(772 M)

Ink-jet

A unique ink-jet system for creating alphanumeric characters on moving recorder charts has been introduced by Gould Instruments Division. The ink-jet annotation device, available as an option on Gould Mk 2000 Series and Mk 200 oscillographic recorders, prints uniform, highly readable alphanumeric characters in a 5 x 7 dot matrix along the edge of the chart over a wide range of chart speeds.

With the new ink-jet annotation system, the user no longer has to stop the recorder (and possibly lose valuable analogue data) to make manual notations. Printing and analogue recording occur simultaneously, so that annotations are closely associated with the analogue traces to which they refer.

The device also facilitates use of the recorder on an 'exception' basis, rather than consuming chart paper whether or not an important signal is coming in. Printing and recording can be operator-, event- or computer-initiated in either attended or unattended service, and the device eases the incorporation of recorders into automated computer controlled test systems.

Important measurement parameters such as instrument sensitivity settings and chart speed can also be entered on the keyboard and automatically noted on the chart along with the analogue traces to become a part of the permanent record.

The patented Gould ink-jet

mechanism is a capillary 'drop-on-demand' system which forms and ejects an individual droplet of fluid only when its piezoelectric transducer is pulsed by the drive electronics. Unlike continuous-stream systems, which require a catcher to collect drops not required for character formation, the Gould system eliminates the need for ink pumping, filtering and recirculating.

Ink consumption is very low. One 10 cm³ cartridge will print over two million characters, and is easily replaced.

Standard ASCII characters are formed by electrostatically deflecting each drop to a preassigned position in a character column. Characters are formed by scanning each of the five 7-dot character columns from the bottom up in raster fashion, and either depositing or omitting an ink drop in each of the 35 possible matrix positions. Character width is held constant over a 1 000 : 1 chart-speed range (from 0.05 mm/s to 50 mm/s) by electronically synchronising the character-generation rate with chart speed.

An optional Gould real-time clock module is also available and an interface allows time to be printed from other clock modules. All inputs are TTL-compatible.

Gould Instruments Division, Roebuck Road, Hainault, Essex, England.

(765 M)