September 1977
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elektor

up-to-date electronics for lab and leisure

CCIR standard TV test pattern generator

darkroom timer with logarithmic scale

FM mains intercom system with 'babyphone' extension

elektor

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decoder

What is a TUN?
What is 10 n?
What is the EPS service?
What is the TD service?
What is a missing link?

Semiconductor types
Very often, a large number of equivalent semiconductors exist with different type numbers. For this reason, 'abbreviated' type numbers are used in Elektor wherever possible:

- '741' stand for µA741, LM741, MC841, MiC741, RM741, SN72741, etc.
- 'TUP' or 'TUN' (Transistor, Universal, PNP or NPN respectively) stand for any low frequency silicon transistor that meets the following specifications:

U_{CEO}, max	20V
IC, max	100 mA
hfe, min	100
Ptot, max	100 mW
fT, min	100 MHz

Some 'TUN's are: BC107, BC108 and BC109 families; 2N3856A, 2N3859, 2N3860, 2N3904, 2N3947, 2N4124. Some 'TUP's are: BC177 and BC178 families; BC179 family with the possible exception of BC159 and BC179; 2N2412, 2N3251, 2N3906, 2N4126, 2N4291.

- 'DUS' or 'DUG' (Diode Universal, Silicon or Germanium respectively) stands for any diode that meets the following specifications:

	DUS	DUG
U_R, max	25V	20V
IF, max	100mA	35mA
IR, max	1µA	100 µA
Ptot, max	250mW	250mW
CD, max	5pF	10pF

Some 'DUS's are: 8A127, BA217, BA218, BA221, BA222, BA317, BA318, 8AX13, BAY61, 1N914, 1N4148.
Some 'DUG's are: OA85, OA91, OA95, AA116.

- 'BC107B', 'BC237B', 'BC547B' all refer to the same 'family' of almost identical better-quality silicon transistors. In general, any other member of the same family can be used instead.

BC107 (-8, -9) families:
BC107 (-8, -9), BC147 (-8, -9), BC207 (-8, -9), BC237 (-8, -9), BC317 (-8, -9), BC347 (-8, -9), BC547 (-8, -9), BC171 (-2, -3), BC182 (-3, -4), BC382 (-3, -4), BC437 (-8, -9), BC414

BC177 (-8, -9) families:
BC177 (-8, -9), BC157 (-8, -9), BC204 (-5, -6), BC307 (-8, -9), BC320 (-1, -2), BC350 (-1, -2), BC557 (-8, -9), BC251 (-2, -3), BC212 (-3, -4), BC512 (-3, -4), BC261 (-2, -3), BC416.

Resistor and capacitor values
When giving component values, decimal points and large numbers of zeros are avoided wherever possible. The decimal point is usually replaced by one of the following abbreviations:

p (pico-) = 10^{-12}
n (nano-) = 10^{-9}
µ (micro-) = 10^{-6}
m (milli-) = 10^{-3}
k (kilo-) = 10^{3}
M (mega-) = 10^{6}
G (giga-) = 10^{9}

A few examples:
Resistance value 2k7: 2700 Ω.
Resistence value 470: 470 Ω.
Capacitance value 4p7: 4.7 pF, or 0.000 000 000 004 7 F . . .
Capacitence value 10n: this is the international way of writing 10.000 pF or .01 µF, since 1 n is 10^{-9} farads or 1000 pF.
Resistors are ¼ Watt 5% carbon types, unless otherwise specified.
The DC working voltage of capacitors (other than electrolytics) is normally assumed to be at least 60 V. As a rule of thumb, a safe value is usually approximately twice the DC supply voltage.

Test voltages
The DC test voltages shown are measured with a 20 kΩ/V instrument, unless otherwise specified.

U, not V
The international letter symbol 'U' for voltage is often used instead of the ambiguous 'V'. 'V' is normally reserved for 'volts' For instance: U_b = 10 V, not V_b = 10 V.

Mains voltages
No mains (power line) voltages are listed in Elektor circuits. It is assumed that our readers know what voltage is standard in their part of the world!
Readers in countries that use 60 Hz should note that Elektor circuits are designed for 50 Hz operation. This will not normally be a problem; however, in cases where the mains frequency is used for synchronisation some modification may be required.

Technical services to readers
- **EPS service.** Many Elektor articles include a lay-out for a printed circuit board. Some — but not all — of these boards are available ready-etched and predrilled. The 'EPS' print service list in the current issue always gives a complete list of available boards.
- **Technical queries.** Members of the technical staff are available to answer technical queries (relating to articles published in Elektor) by telephone on Mondays from 14.00 to 16.30. Letters with technical queries should be addressed to: Dept. TQ. Please enclose a stamped, self addressed envelope; readers outside U.K. please enclose an IRC instead of stamps.
- **Missing link.** Any important modifications to, additions to, improvements on or corrections in Elektor circuits are generally listed under the heading 'Missing Link' at the earliest opportunity.

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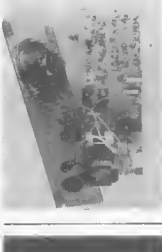
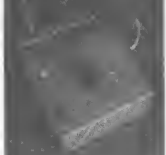
Number 9



A complete station of the **FM mains intercom** consists of a transmitter, a receiver and a power supply. All three can be mounted on a single p.c.board.



The control switches and indicator lights of the **logarithmic darkroom timer** are laid out in such a way that the unit should be easy to operate even when working in complete darkness.

The line and field sync pulses produced by a television test generator must conform to a precisely defined international standard. The **CCIR tv pattern generator** uses a quartz oscillator and TTL divider stages to produce a video waveform that is well within the limits defined by the European CCIR.

The Japanese influence on electronics is becoming more and more widespread. An obvious further step in the right direction would be to paint the components in traditional oriental fashion, as illustrated by this month's cover . . .

Where are those buses?

Coras Iompair Eireann (CIE), Ireland's national transport company, are installing a fully automatic vehicle monitoring (AVM) system for Dublin City Bus Services' entire fleet of some 900 buses which carry over 216 million passengers and operate over 32 million miles each year.

Storno Limited of Camberley, Surrey are the main suppliers for the system which will enable the entire fleet to be monitored by Control Inspectors from seven garages. The system is based on a dual computer arrangement which automatically collects location data from each bus on a route. The results are presented on visual display units (VDU's) so that Control Inspectors in each garage can see at a glance the actual, and scheduled, position on all buses on a particular route.

Although the collection of location data is automatic, and does not require the driver to answer queries, normal speech contact between driver and Control Inspector is also provided in this complete radio communications system. This system will enable CIE to provide improved services for passengers by reducing bus waiting times, operating services on time, and by having the facility to summon aid in cases of emergency, or passenger illness. Significant benefits are also being provided for the CIE management and 4,000 workforce. Of the utmost importance, the system generates valuable statistical information which is available within 24 hours and forms the basis of a comprehensive management information service for the scheduling, maintenance and operating departments.

The Control Inspectors, who are now being removed from often unpleasant outdoor work, are achieving a re-newed sense of job satisfaction and involvement from being able to control a full bus route, or group of routes without assistance, or interference.

Improved morale has been achieved for the operating staff who will now be responsible to a single Control Inspector instead of reporting to several Control Inspectors located at different parts of their route. The greater control achieved with radio is providing an equalisation of workload between crews, enabling them to take their mealbreaks at correct times, and providing immediate assistance in the event of assault, or vandalism.

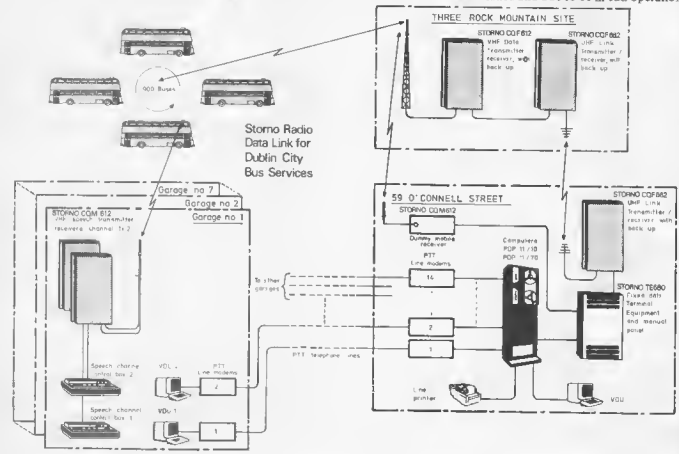
Dublin Bus Services first started experimenting with radio telephones in 1970. Tests proved so satisfactory that there are now 740 radio equipped buses in service using 14 voice channels.

Due to the limited availability of VHF channels, expansion to the remainder of the fleet could only be achieved through higher utilisation of existing allocation, and the solution appeared to lie in the automation of the existing scheme.

Major trials took place in 1975 on all aspects of automatic vehicle monitoring on 100 buses from the Phibsborough garage. The buses were fitted with Stornophone CQM612 semi-duplex VHF FM mobile radio telephones, designed to facilitate data transmission. A telemetry unit stored the data message and facilitated transmission when interrogated by the computer located at the CIE headquarters in O'Connell Street. Results were presented on two VDU's at the Phibsborough garage. A printer provided hard copies of specific information.

The data link comprised a base station at the computer site, and a station at Three Rock Mountain, approximately seven miles away to relay the information from the computer to the mobile bus units and vice versa.

These comprehensive tests included location accuracy, facilities tests, tests on voice communications, computer system and display responses, equipment reliability, Control Inspectors' and operatives' reactions. The results obtained paved the way for the complete AVM system now being installed and due to be in full operation



selektor

by mid 1979.
When fully operational a 'front end' PDP 11/10 computer will interrogate each bus in turn at the rate of 900 buses/minute via a fully duplicated radio system. It will also handle requests to speak. Once verified the bus replies are fed into a larger PDP 11/70 machine which presents the results as actual and scheduled positions of the buses on individual routes on 2000 character screen VDU's — a number of which with a printer are being located at each of the seven garages.
This will enable Control Inspectors in each garage to see at a glance the positions of all buses on a particular route so that they get an accurate picture of the situation as it is, and as it should be, to allow them to accurately make any changes that may be necessary to maintain, or improve services.
Additionally, as part of the improvement of control techniques a number of closed circuit television cameras (CCTV's) are being installed at city centre points. These will provide Control Inspectors with an awareness of traffic conditions and build-up of passenger queues. Route Control Inspectors can operate the CCTV's which incorporate low light level lenses for night operation together with pan, tilt, zoom and focus facilities.
The bus radio is being modified to accept and transmit the computer data and this, together with a bus data unit and control head comprises the bus equipment.
The control head provides the means of establishing voice communications between the driver and the Control Inspector and also feeding in the odometer reading at commencement of each journey to identify its precise location. Thereafter, location identification is automatic as the odometer is fitted to the final drive in parallel with the normal speedometer drive unit and generates pulses to the data unit at 44 yard intervals. The control head also incorporates an input for emergencies. The computer can also make direct inputs to the odometer.
The bus data unit stores the location of the bus and passenger loading. It also incorporates facilities to record up to

The Storno bus date control head provides the means of feeding in the three-digit code odometer reading at commencement of each journey to identify the precise location of the bus. Thereafter, location identification is automatic. When the driver wishes to speak he uses the RTS button which informs the Control Inspector through a VDU of his request. Up to eight such requests may be displayed at any one time.
Every 20 seconds a general call is sent to all Storno bus data units searching for an 'alarm' condition. Should any bus have its 'alarm' button depressed it will respond by causing its number and location to flash continuously on the Control Inspectors VDU. At the same time the computer automatically switches the bus to the speech mode thus giving drivers speech contact with their respective Control Inspectors on average within ten seconds of pressing the 'alarm' button.

Close-up of typical map shown on the VDU's and up-dated automatically at least every two minutes. The route is shown as two horizontal lines — one for each direction of travel. The scheduled positions for the buses operating on the route are shown on the inside of the diagram. Actual positions are plotted on the outside of the diagram and are represented by the duty number of the bus concerned.
deemed to be under the first character of the duty number. Time and route numbers are shown on the first line of the screen. Driver 'alarm' calls are flashed on and off on the first line until answered by the Control Inspectors. Requests to speak by bus crews appear on the last line and again will remain there until cleared by the Control Inspectors. Columns on the right-hand side of the screen give additional information on buses being monitored.

```
TIME 10 58      05-APR-77       ROUTE 10       ALARM10/19 CHECK40/01
                                   OFX                                   SET ODO
                                   15A                                   1015 0411
                                  07A                                    4005 1003
                                   18
 06V       14A      24     21A     16V
•---- -------•------ ----|--------•---------•---•------•-------•-----•  GARAGE
06-      14A·          24         21A•         16•      18       08-    0410 4011
           17                                          07A•             1009 1021
                SHLRD             S1GRN                         ANARD
  BELFD     DBRCH        WA1RD               OCOS1    STPET      PHXPK
                          22•                            09A•            NO REPLY
       01A      19•     13A•          04      11A     03·       15A       15 20 06
       •-----------|------•------|---------•------•--------|------•--•  17 12 19
            01A            13A   22 04V          11A
             19
                                                                         INVALID
                                                                          01 18 16
                                                                          13 22 07
OVERFLOW X 03,09A,08,17

COMMAND?          COMMAND LINE
                  PRINTER LINE
REQUEST 10 SPEAK 10/02 10/03 10/18 4/01 40/15
```

ten different mechanical and operating features, such as, excessive engine temperature and oil pressure. It also checks all incoming messages and controls the radio from receive to transmit.

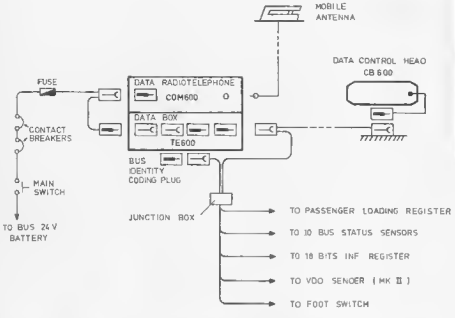
The data link is similar to the one used in the 1975 trials, and again comprises a data base at the central computer site, and a relay station on Three Rock Mountain. The link is in two parts — a VHF link between the relay station and the mobile unit, and a UHF link between the relay station and the central computer site.

The VHF equipment consists of a Stornophone CQF612 FM duplex base station giving 25 watts RF output. It operates on a 25 kHz channel spacing and is modified to permit the transmission of data signals.

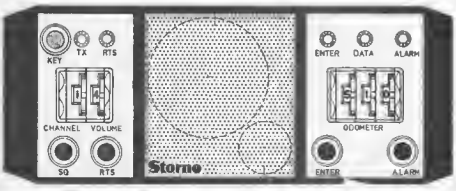
The relay station transmitter outputs to an omnidirectional antenna and the receiver outputs to the adjacent UHF unit. The UHF link comprises two CQF662 duplex base stations — one on Three Rock Mountain and the other in O'Connell Street. The RF output is one watt and is fed into a directional antenna.

The data base station and data link are duplicated throughout and the standby link may be selected remotely from the O'Connell Street headquarters or from a garage based VDU.

The improved radio communications being introduced are helping to provide a reasonable level of public transport service under difficult congested operating conditions.



bus radio/data box installation layout



Inventions

The current Jubilee Year passion for discovering the best of British inventions and techniques is to be given an unique audience in November that will provide United Kingdom ingenuity and technology with its biggest-ever world boost: the Sixth International Exhibition of Inventions in Geneva from 25 November to 4 December 1977. This Swiss Government-backed exhibition is the world's leading inventors' showplace where more than 1,000 new ideas and developments will be exhibited from 26 countries and where last year 350 licences were negotiated and exhibitors did £5-million worth of business during the 10-day exposition. There are 22 classes of exhibits, from general mechanical engineering through clothing and footwear to games and toys. An international jury representing 10 nations awards prizes from Grand Prix to bronze medals, visitors vote an Oscar award, the world Press presents its own prize, there are special awards for environment, transport, clock and watch-making, for the best foreign invention and prizes from the French, Spanish and Dutch Chambers of Commerce for their best national invention.

The reputation of the Geneva exhibition is now so high that it attracts more exhibits than all other international inventors' exhibitions put together. But exhibitions in general, and international events in particular, have the limiting disadvantage of cost. Two-metres all round stand space will cost at least £200. Carpets, furniture and decorations another £150.

International Commercial Network of Harrowgate now offer a unique solution to this problem. They have arranged a special British inventions show stand where they will display a group of special television-type monitor screens on which will be shown a series of three-minute colour films of each British invention or new development. These films will be accompanied by sound commentary in English, French, German and Italian. Visitors can select the invention they wish to see and choose the language of commentary. Inventors and companies may provide their own already-made Super-8 or 8 mm three-minute colour films with English commentary either on tape or script. Translated recordings will then be made at no charge. If there is no film this will be produced by Inter-View Productions. The cost of taking a film that already exists to Geneva and representing the British interests at the 10-day show is around £200. If a film is specially produced the total cost will be under £500, perhaps much less if film demands are simple.

(203 S)

selektor

Optical waveguides used in Air Force's data-carrying cable

Optical waveguides made by Corning are an essential part of a cable installed at the U.S. Air Force Arnold Engineering Development Center in Tennessee.
The glass waveguides are contained in a custom-made cable of the General Cable Corporation that connects rocket engine test sites with a central data processing facility.
The cable contains six waveguides, along with several copper conductors. Each waveguide may be employed independently for transmitting, at high-speed, data signals or any other information, including voice and video signals.
The waveguides transmit data from the engine test sites to the base computer center, located approximately two kilometers away.
The optical waveguides were chosen for the installation because of their large data-carrying capability, and because they are immune to hostile environments, particularly electromagnetic interference.
Measuring about 0.005-inch (0.127 mm) in diameter, or about the thickness of a human hair, the waveguides are well protected by other cable components. Because the cable is buried for most of its 7,000-foot (2,100-meter) length, special steps were taken to make it suitable for such an environment.
The cable consists of a welded tubular aluminium sheath surrounding the fibers and their support structure, a polyethylene inner jacket, a corrugated steel wrapping and a polyethylene outer jacket. The cable is suitable for installation in ducts or can be buried directly in the ground.
The installation at the Arnold Center is particularly significant because it is intended as an operational system, not an experimental one. The complete system is expected to be in service by mid-1977, when installation of other elements of the system is complete.
The graded-index optical waveguides used in this cable system were made by a patented Corning doped deposited silica process. In this process, carefully controlled materials that raise the refractive index of the core glass are introduced during deposition of the core.
Freedom from electromagnetic interference is a characteristic of optical waveguides that is particularly desirable in the Arnold Center installation, where accurate data transmission is essential. The characteristics are particularly important because real-time transmission reduces opportunities for error correction. Neither natural interference, such as lightning, nor man-made interference, such as that created by adjacent electromechanical equipment or cross-talk between fibers in the same cable, affects signals carried in optical waveguides. Also, waveguides do not radiate energy that might interfere with other equipment.
The practical application of waveguides on a demanding installation such as that at the Arnold Centre has only been possible recently. Six years ago the purest glass fibers of one-kilometer length could deliver only one per cent of the light introduced into them. However, steady improvement has been made, so that today as much as 80 per cent transmission has been achieved in the best optical waveguides of comparable length.

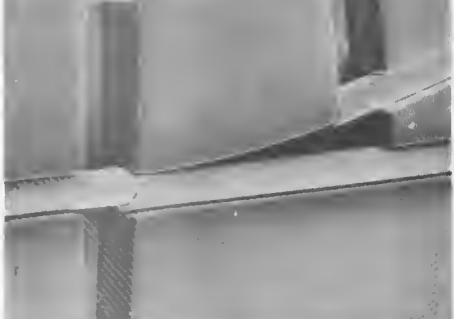
(205 S)

Optical fibers are branching out

The purpose of telecommunication systems is to transmit information and data to specific destinations. For certain transmission applications, optical fibers are well on the way to competing effectively with conventional metal conductors. Viable methods of optical distribution of communications are also being established, and Siemens is now presenting a branching unit for optical waveguides, developed with the support of the Federal Department of Research and Technology.
In an optical-fiber communication network, definite light components have to be branched off from the main optical waveguide. Since optical fibers do not readily lend themselves to branching, it was necessary to find a suitable optical distributor. Using a planar thick-film technology, research engineers at Siemens succeeded in realizing novel branching structures for optical fibers, based on the use of a light-sensitive plastic foil with a thickness of approximately 0.1 mm, corresponding to the diameter of the fibers. Any desired structure can be etched into this foil by photolithographic processes.
The structure required for the waveguide branch is such that the two ends of the cut fiber meet with a slight offset. The light component escaping at the interface enters the foil and is guided along a curvature to a branching fiber. The amount of optical power coupled out depends on the offset of the ends of the main waveguide at the interface. The advantage of the described technology is that the light-guiding structure in the foil, and the guiding channels for the fibers, can be produced in a single operation. This fabrication method is very simple, while at the same time fulfilling the stringent requirements specified with respect to the accuracy of fiber alignment (tolerances of approximately ± 3 μm).

(204 S)

Alternating current flow can be detected and indicated using only four components. How?
See the inside of this month's mailing wrapper!



introducing microprocessors (1)

Over the past two decades increasing miniaturisation, and in particular the advent of integrated circuits, has revolutionised the electronics industry. Nowhere is this more true than in the field of digital electronics, especially in the area of data processing and calculating machines, where large-scale integration (LSI) has made possible low price units of a small size and high performance unheard of even ten years ago. Currently, microprocessors are the 'in thing', so this series of articles is intended to provide a simple introduction to these extremely versatile devices.

A microprocessor is simply an extremely small processor, and a processor is part of a computer or other data processing system, so before delving into the intricacies of microprocessors it is first necessary to understand the operating principles of computers, and the function of a processor in a computer system.

A computer is basically a machine for processing data. The data to be processed is fed into the computer, and the results of the data processing are obtained at the output. The operations that are to be performed on the data are contained in a sequence of instructions known as the programme.

Apart from complexity, the major difference between a computer and say a simple pocket calculator lies in the programming. A calculator possesses a number of pre-programmed mathematical functions that can be called up at the push of a button, e.g. $\cos x$, y^x, $\log x$, as well as the basic arithmetic functions $+$, $-$, $\times$, $\div$. A computer, however, possesses only basic arithmetic and manipulative logic functions 'if $x > y$, then . . .', and these must be written into the programme step by step. However, this makes a computer infinitely more versatile than a calculator. A calculator is limited in its operation to the mathematical functions available on its keyboard, whereas (within reason) any desired manipulation of data or complex mathematical operation may be performed by a computer by building the correct sequence of instructions into the programme.

A typical computer system might consist of four units.

1. A separate (or sometimes peripheral) unit for preparation (and sometimes even verification) of programmes. This might consist of a teletype or visual display unit (VDU) and punched tape or card equipment.

2. A peripheral input/output unit such as tape/card reader to read in the programme and data, and tape/card punch to output the results.

The programme preparation and input/output units may frequently be combined, especially in applications where the computer and the user interact directly, e.g. by means of light pens, voice recognition units etc.

3. A memory unit to store the data and programme instructions. The same memory may be used to store both data and programme, especially in small computers, or there may be separate programme and data memories.

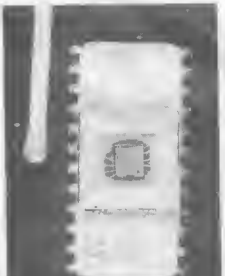
4. A central processing unit (CPU). This carries out arithmetic operations, data comparison, manipulation and movement in accordance with the programme instructions.

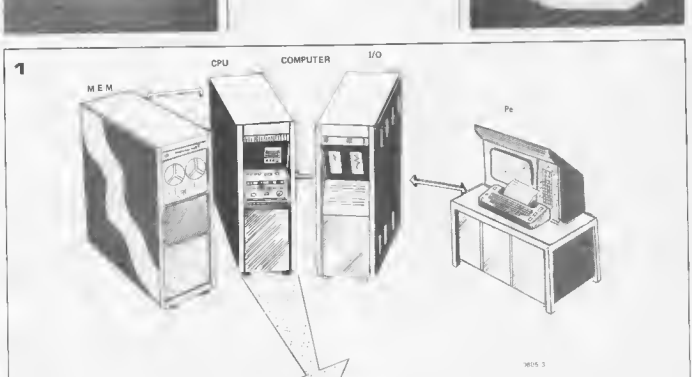
Many readers will have seen photographs of early computers built using valves, and may have marvelled at their apparent complexity and wondered just why they were so complex. The answer is really very simple. After a few initial attempts to build computers operating in decimal notation it was quickly realised that to represent decimal numbers 0 to 9 electronically was not a very practical proposition when applied to a large computer system. It soon became apparent that it was much simpler to make computers operate in the binary number system, since this system uses only digits 1 and Ø ('Ø' is used instead of '0' for the digit, to clearly distinguish it from the letter 'O'), which can be represented electronically by 'on' and 'off' conditions.

A computer system must be able to handle and store large amounts of information (i.e. numbers), and to store one digit of a binary number requires an electronic circuit that can be set in one state or another depending on whether the digit is Ø or 1. Such a circuit is the common flip-flop. To store and handle many large numbers requires a correspondingly large number of flip-flops, and when one considers that in the days of valves each flip-flop would require one double-triode valve, it is not difficult to see why valve computers were so bulky.

In those days each of the four units of a computer might have occupied a room to itself, depending on the complexity of the computer system. The introduction of transistors made possible much smaller computers, and after the introduction of TTL and later MOS integrated circuits the size of computers could be reduced even further. Finally, with the perfection of LSI MOS tech-

Figure 1. A computer system comprises a memory unit (MEM), CPU, input/output unit (I/O) and peripherals. Development of LSI technology now means that the CPU can be integrated into a single IC – the microprocessor.





nology the microprocessor appeared on the scene. Thus the functions of the CPU, which in the days of valves occupied several racks of equipment, and in the days of TTL occupied several printed circuit boards, could now be integrated onto a single chip.

Of course large scale integration has also brought about a reduction in the physical size of memories, and large amounts of memory capacity can also be accommodated on one chip.

Applications of Microprocessors

The most obvious use to which a microprocessor can be put, is to couple it to a memory and peripherals to build a microcomputer system. However, much more exciting applications are possible where the microprocessor is 'dedicated' to a particular task.

A good example of this is the electronic sewing machine recently introduced by the Singer company. Until the advent of this machine patterned sewing was accomplished by purely mechanical arrangements of cams and levers operating in a fixed sequence. Once the production line was tooled up to produce a machine it was an extremely costly business to make any alterations to the patterns that could be produced. Using a microprocessor to control the sewing patterns all that needs to be changed is the programme.

A similar argument applies to automatic washing machines, which normally use cam timers to control the washing sequence. Here again the introduction of any new washing sequences would be extremely costly once the machine was past the prototype stage. Using microprocessors the design can be made much more flexible. During the development phase the programme can be changed many times at relatively little cost and once it is perfected it can be 'frozen' into a memory for production use. Even if a design change is necessary during production it is simply a matter of substituting a memory with a new programme, which is considerably less costly than re-tooling to produce a new mechanical part.

In general, it is safe to say that microprocessors offer considerable advantages in applications where they can replace a large number of mechanical, electromechanical or electronic parts, such as in control applications in industry, in domestic appliances and in automobiles.

(to be continued)

FM-mains intercom

The disadvantage of conventionel AM-mains intercoms is that they are subject to the often highly disruptive effect of mains interference. The system described in this article however, obviates this problem by employing FM; in addition, by reducing the bandwidth to a minimum, the number of available channels is thereby greatly increased, so that there is little chance of interference ('splatter') between different intercom systems caused by channel overlap.

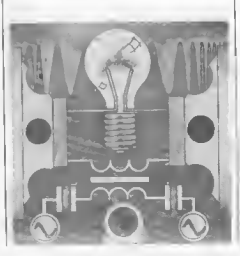
A design for a simple mains intercom has already been published in the June '76 issue of Elektor. It was stated then that a future issue would contain a design for an improved version, which in a number of respects, would 'offer considerably better performance.

The original design was for an AM-system with roughly the same characteristics as most commercially available (AM-) devices. However, since there is very little that can be done to alleviate the problem of mains interference with such a system, it is often the case that users soon revert back to 'normal' intercom-installations.

The superior performance of the mains intercom described here is due almost entirely to its reduced sensitivity to interference. This is achieved by using an FM system. The advantages of using an FM- as opposed to an AM-transmission system.. were extensively discussed in the article 'modulation systems' which appeared in the February '75 issue of Elektor. Although the system does in fact employ a transmitter and a receiver, it is somewhat uncommon to use these terms when talking of an intercom system since it is the mains wiring which is being used as the medium to carry the signals.

An intercom system is used in the first instance for the transmission of the spoken word, so that high fidelity reproduction is not required. This means that narrowband FM will give sufficient intelligibility for spoken signals. The use of a very narrow bandwidth has the advantage that, if the transmission and reception frequency is made adjustable over a reasonable range, then the number of avadable channels is thereby greatly increased. The system described here takes advantage of this possibility, since increasing the number of channels reduces the chance of one frequency overlapping with another and producing interference or 'splatter'.

The transmitting power of the intercom has to be fairly high to take account of the potentially very severe mains interference. However, under normal circumstances the output power (which may be varied) will be kept to a fairly low level in order to prevent the transmitter being picked up outside the building.



The construction of the intercom is simplified by the fact that a complete station, consisting of a transmitter, a receiver and a supply section, can be mounted on one printed circuit board. In addition the circuit is simplicity itself as far as tuning is concerned.

Design

Figure 1 shows the block diagram for a complete intercom station. The transmitter and receiver sections interconnect at point B, so that the mains connection functions as both the in- and output of the station.

The transmitter section is shown on the upper half of the diagram. The signal from the microphone is first amplified, limited and filtered, then used to frequency modulate an oscillator. After being amplified, the resulting FM-signal is fed into the mains via an isolation transformer.

Signals transmitted from other stations are picked up by the transformer and fed to the receiver section. After being amplified and limited, the received signal is demodulated and fed, via a simple audio-amplifier, to a loudspeaker. Switching between 'speak' and 'listen', i.e. between transmit and receive, is accomplished by switching the supply voltage between the output stage of the transmitter and the AF-amplifier of the receiver.

The Transmitter

Figure 2 shows a more detailed block diagram of the transmitter section of the intercom. The circuit diagram for the first three blocks is reproduced in figure 3a, whilst figure 3b shows the circuit diagram for the rest of the transmitter.

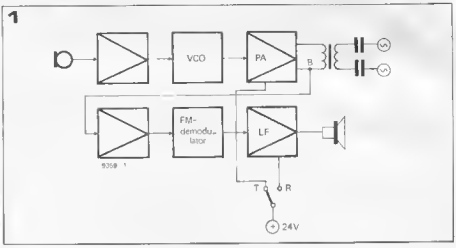
As is apparent from the block diagram, the signal from the microphone is first amplified by the stage round T1. In order to reduce the bandwidth of the transmitted signal to a minimum approx. 10 kHz in this case), T1 is followed by a clipper, consisting of the differential stage round T2/T3. Although the signal is severely clipped, the intelligibility of the audio signal is virtually unaffected. The clipper is

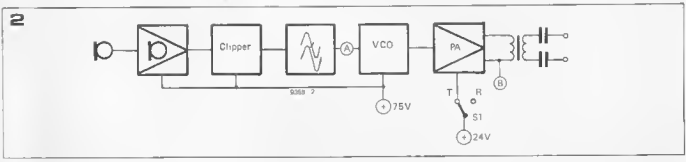
Figure 1. Block diagram of a complete station of the mains intercom. The station, together with the supply section, can be mounted on a single circuit board.

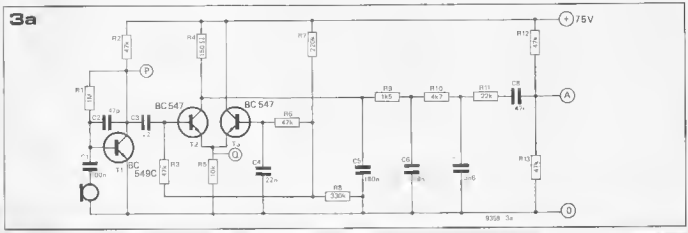
Figure 2. Block diagram of the transmitter. After being clipped and filtered, the microphone signal is used to modulate the frequency of a VCO. The resulting FM-signal is then amplified and fed to the mains via an isolation transformer.

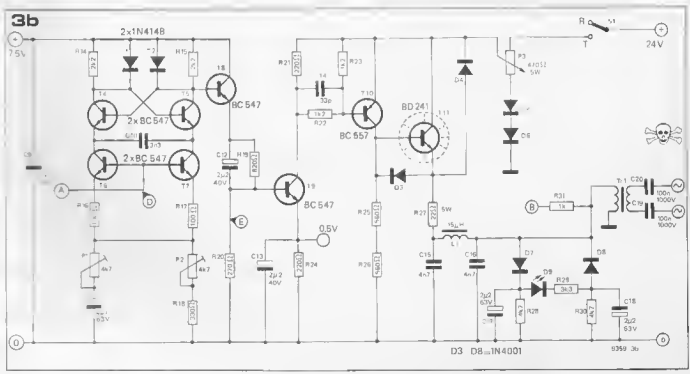
Figure 3a. The circuit diagram of the microphone preamplifier, clipper and lowpass filter.

Figure 3b. The circuit diagram of the VCO and the output stage of the transmitter.









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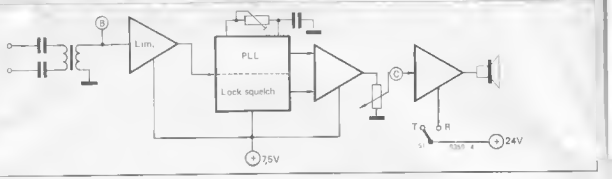
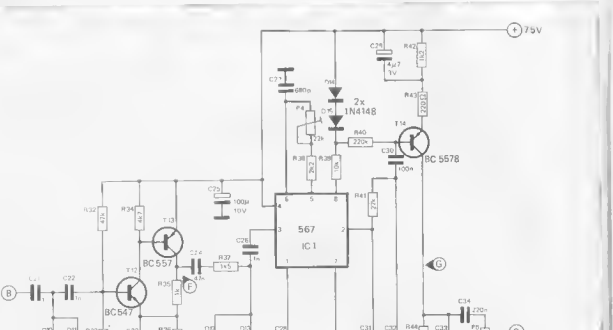


5a



followed by a lowpass filter (R9, R10, R11, C5, C6 and C7) with a cutoff frequency of approx. 5 kHz, which ensures that the sidebands of neighbouring channels do not overlap causing splatter.

The resulting signal (we have now reached figure 3b) is used to modulate the frequency of the VCO built up round T4, T5, T6 and T7. The size of the frequency deviation can be adjusted by means of P2. The frequency of the VCO (i.e. the desired channel) is tuned using P2; the range of the oscillator runs from approx. 70 kHz to approx. 500 kHz.

The frequency-modulated oscillator signal is then fed via the buffer stage T8 to a power amplifier consisting of T9, T10 and T11. The latter two transistors are connected as class-C amplifiers. However the efficiency of the output stage is not as great as one might expect, since the stage has no facility for tuning, thereby making it impossible to match to the load. Although an adjustable matching network would considerably increase the power of the transmitter, it was decided that it would not be practicable in this case. The reason for this is that when using more than one channel, it is not sufficient merely to alter the VCO-frequency to select a different channel, the matching of the output stage would also need to be adjusted accordingly, thereby making the system much more complicated to operate.

Operating the output stage in the wideband mode guarantees an output power of at least 1 W over the entire frequency range of the VCO. The transmitter power is adjusted by means of P3 (a 5 W type should be used).

Components D3, D4, D7, D8, C17 and C18 protect the output stage of the transmitter from possible voltage transients occurring on the mains. LED D9 is included to provide a visual indication of the transmitter power. Power transistor T11 should be fitted with a heat sink (for which sufficient room has been left on the printed circuit board).

The Receiver

Figure 4 shows the block diagram of the receiver section of the intercom. The circuit diagram of the most important part of the receiver, namely the phase locked loop, is given in figure 5a, whilst figure 5b shows the circuit diagram of the last block in figure 4, i.e. the AF-amplifier.

Incoming signals from other intercom stations are fed via the isolation transformer Tr1 (see figure 3b) to the input of the receiver. The output of the transmitter and the receiver input are thus connected directly to one another (point B). However, in order to prevent the clamping diodes at the input of the receiver from burning out when the station is transmitting, a series resistor (R31 in figure 3b), is included.

For the same reason that there is no facility for matching the transmitter output stage, the receiver input is also untuned. For the present application the receiver is sufficiently selective as it is, and a wideband input has the added advantage that it is less susceptible to shock excitation caused by transient voltage peaks.

The block marked 'Lim.' in figure 4 represents the stage which amplifies (to approx. 1 V_{pp}) and limits the input signal. This is done by T12/T13 and D12/D13 respectively. The signal is then demodulated using a phase locked loop fitted with 'lock squelch', i.e. the receiver will only deliver an output when the PLL is locked in.

As is apparent from figure 5a, this stage employs an IC (IC1). The IC used (available from, among other, Signetics

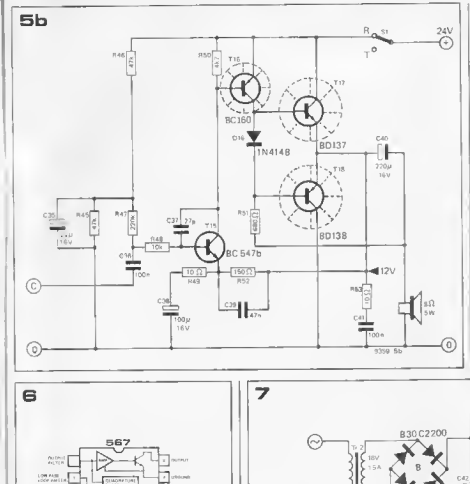


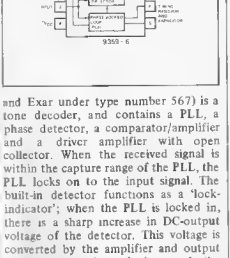
Figure 4. Block diagram of the receiver. After it has been amplified and limited, the received signal is demodulated in a PLL with 'lock squelch'. The demodulated signal is fed to the loudspeaker via a low-frequency amplifier.

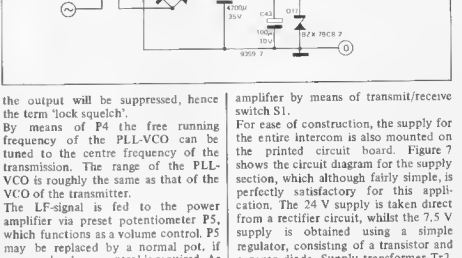
Figure 5a. The circuit diagram of the high-frequency section of the receiver. IC1 contains a PLL FM-demodulator. The output transistor of the IC, together with T14, forms the lock squelch.

Figure 5b. The low-frequency amplifier of the receiver.

Figure 6. Internal block diagram of the tone decoder IC, type number 567.

Figure 7. The supply, which, along with the receiver and transmitter is mounted on the circuit board.





and Exar under type number 567) is a tone decoder, and contains a PLL, a phase detector, a comparator/amplifier and a driver amplifier with open collector. When the received signal is within the capture range of the PLL, the PLL locks on to the input signal. The built-in detector functions as a 'lock-indicator'; when the PLL is locked in, there is a sharp increase in DC-output voltage of the detector. This voltage is converted by the amplifier and output driver transistor into a logic state. In the quiescent state pin 8 of the IC is high, whilst during lock, the logic state at this pin is low.

The FM-input signal is demodulated by taking as the LF-signal the control voltage for the PLL-VCO present at pin 2. The lowpass filter which is connected to this pin is formed by C31 (see figure 5a) together with a resistor in the IC. The LF-signal is fed via R41 and C30 to the base of transistor T14. However the DC-bias voltage of this transistor is determined by the logic state at pin 8 of the IC. The transistor will turn on only when the PLL is in lock and pin 8 is low. If the input frequency band is outside the capture range of the PLL, the latter will not lock in, and the low frequency signal at the output will be suppressed, hence the term 'lock squelch'.

By means of P4 the free running frequency of the PLL-VCO can be tuned to the centre frequency of the transmission. The range of the PLL-VCO is roughly the same as that of the VCO of the transmitter.

The LF-signal is fed to the power amplifier via preset potentiometer P5, which functions as a volume control. P5 may be replaced by a normal pot, if a manual volume control is required. As figure 5b makes clear, the power amplifier is of a very simple design, given the fact that there is no need for hi-fi reproduction. In the absence of a signal no quiescent current flows through the output stage; with a supply voltage of 24 V the circuit will deliver 5 watts to an 8 ohm loudspeaker.

The Supply

It will have become clear from the foregoing that two separate supply voltages are needed for the intercom. Most of the circuit operates at 7.5 V, but for the output stage of the transmitter and the LF-amplifier in the receiver, a 24 V supply is necessary. The 24 V supply is switched between the transmitter-output stage and the LF-amplifier by means of transmit/receive switch S1.

For ease of construction, the supply for the entire intercom is also mounted on the printed circuit board. Figure 7 shows the circuit diagram for the supply section, which although fairly simple, is perfectly satisfactory for this application. The 24 V supply is taken direct from a rectifier circuit, whilst the 7.5 V supply is obtained using a simple regulator, consisting of a transistor and a zener diode. Supply transformer Tr2, which of course cannot be mounted on the p.c.b., should have a secondary voltage of 18 V and supply a current of 1.5 A.

Construction

Figure 8 shows the component layout and copper side of the printed circuit board. The construction of the intercom should present few difficulties, providing the listed component values are adhered to. The only problem may be the isolation transformer Tr1, which has to be selfwound. A pot core without an air gap, 30 mm in diameter and 19 mm high, should be used. The primary winding consists of 48 turns of enamelled copper wire 0.3 mm thick; 24 windings of the same wire will suffice for the secondary

Parts list for figure 8: a complete station (figures 3a, 3b, 5a, 5b and 7)

Resistors:

R1 = 1 M
R2,R3,R6,R12,R13,R32,
R45,R46 = 47 k
R4,R52,R55 = 150 Ω
R5,R39,R44,R48 = 10 k
R7,R40,R47 = 220 k
R8 = 330 k
R9,R37 = 1k5
R10,R28,R30,R34,
R50 = 4k7
R11,R33,R41 = 22 k
R14,R15,R38 = 2k2
R16,R17 = 100 Ω
R18 = 330 Ω
R19 = 820 Ω
R20 = 270 Ω
R21,R24,R43 = 220 Ω
R22,R23, R42 = 1k2
R25,R26 = 560 Ω
R27 = 22 Ω/5 W
R29,R54 = 3k3
R31,R35,R36 = 1 k
R49,R53 = 10 Ω
R51 = 680 Ω
P1,P2 = 4k7 preset
P3 = 470 Ω/5 W
P4 = 22 k preset
P5 = 100 k preset

Capacitors:

C1,C30,C36,C41 = 100 n
C2 = 47 p
C3,C4 = 22 n
C5 = 180 n
C6 = 18 n
C7 = 5n6
C8,C24,C28,C39 = 47 n
C9 = 10 µ/10 V
C10,C33 = 3n3
C11 = 4µ7/63 V
C12,C13 = 2µ2/40 V
C14 = 33 p
C15,C16 = 4n7
C17,C18 = 2µ2/63 V
C19,C20 = 100 n/1000 V
C21,C22,C26 = 1 n
C23 = 1µ5/6 V
C25,C43 = 100 µ/10 V
C27 = 680 p
C29 = 4µ7/3 V
C31 = 15 n
C32 = 1n5
C34 = 220 n
C35 = 22 µ/16 V
C37 = 27 p
C38 = 100 µ/16 V
C40 = 220 µ/16 V
C42 = 4700 µ/35 V

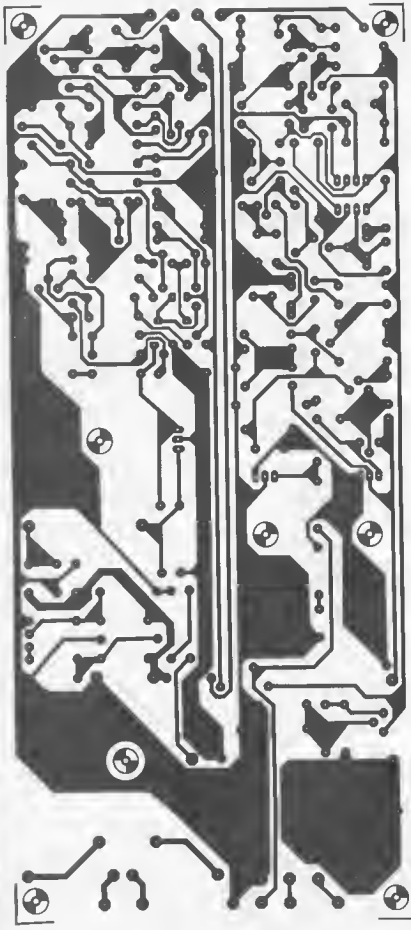
Semiconductors:

T1 = BC549 C
T2 . . . T9,T12 = BC547
T10,T13 = BC557
T11 = BD241
T14 = BC557 B
T15 = BC547 B
T16 = BC160
T17 = BD137
T18 = BD138
T18 = BC140
D1,D2,D10 . . . D16 = 1N4148
D3 . . . D8 = 1N4001
D9 = LED
D17 = BZX79-C 8V2
(or equ. 8V2 zener)
IC1 = 567

Miscellaneous:

L1 = choke 15µH
Tr1 = pot core tranformer (see text)
Tr2 = supply transformer 18 V/1.5 A
B = bridge rectifier B30C2200
S1 = SPDT switch

8



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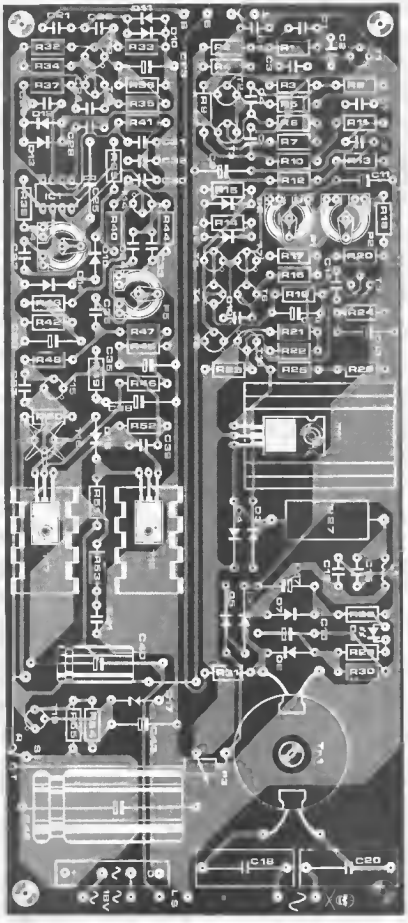


winding. The above pot cores are available from Mullard under type number FX 2241, and from Siemens, type number B65701-L0000-R026 (or equivalent).

The power transistor in the transmitter and the two power transistors in the LF-amplifier (T17 and T18) should be fitted with a heat sink.

Tuning

When two intercom stations have been completed and are functioning satisfactorily (which can be checked by measuring the voltages at the points indicated in the circuit diagram), the tuning procedure – which is not difficult – can begin:

* switch both stations on and set one to 'transmit' and the other to 'receive'.
* set P3 for maximum transmitting power; LED D9 on the transmitter should now light up.
* set P2 (transmission frequency) to mid-position.
* adjust P4 on the receiver until the PLL audibly locks in on the transmitted signal; continue to adjust P4 until the PLL goes out of lock; P4 should then be set to the position midway between these two points.
* connect a microphone to the transmitter and set P1 for maximum frequency deviation.
* hold the microphone of the transmitter close to the loudspeaker of the receiver thus producing 'howl round'. By means of P5, set the receiver to a reasonable volume.
* still holding the microphone close to the loudspeaker, use P1 to adjust the frequency deviation of the transmitter until the acoustic feedback produces a much smoother sound, with no audible evidence of overloading. The resulting position for P1 should give a reasonable volume with minimal distortion when receiving spoken signals.
* Finally, set the transmit/receive switch of both stations in the alternative position, and repeat the above procedure for the other transmitter and receiver. A different transmission frequency should be chosen in order to avoid possible interference.

Once the tuning procedure has been completed, it is advisable, in the event of severe interference or of heavy signal losses due to transmitting between different phases, to experiment with the system in order to find the optimum transmission frequency. This also avoids the potential problem of a number of users setting P2 in the identical mid-position, thereby increasing the likelihood of channel congestion.

In some cases, where severe mains interference is present, it may prove helpful to add a small resistor (say 56 Ω) in parallel with the primary of Tr1 – i.e. between the R31/D8 junction and supply common.

Figure 8. Copper side and component layout of the circuit board for the mains intercom.

In Conclusion

If, as is shown in figure 9a, a multi-way switch, along with a number of fixed resistors connected in series with preset potentiometers, is used to replace P2, then the result is a true multichannel transmitter. A similar alteration to the frequency-determining section of the receiver (figure 9b) thus converts the system into a complete mains-transceiver.

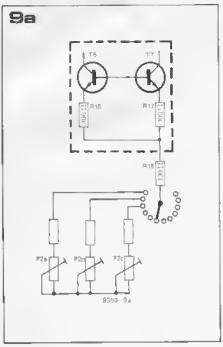
Should difficulties occur with the 5 W wirewound potentiometer (P3 in figure 3b) used to regulate the transmitting power, an alternative arrangement is shown in figure 10. The replacement circuit, shown on the right of the diagram, employs a more conventional type of potentiometer and a power transistor, which should of course be fitted with a heat sink.

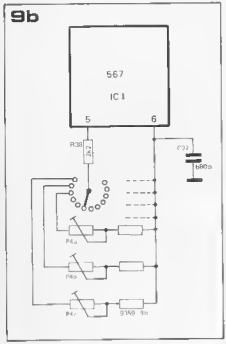
Babyphone extension

A large number of mains intercoms are used as babyphones or baby-alarms. It is important that, before an intercom is used for this purpose, it be fitted with a voice-operated control. If this is omitted, the result is that a continuous, more or less unmodulated carrier signal is being transmitted, which, in the case of widespread use, will soon lead to channel congestion. In addition, those present in the same room as the receiver station will be subject to a variety of background noises produced by the intercom.

For this reason the following add-on circuit (see figure 11) offers a babyphone extension for the mains intercom, which will ensure that the intercom is only switched on when the alarm has been actuated.

The signal from the microphone is first amplified by A1 and A2. The latter amplifier stage can also be used to amplify the signals from up to three separate alarm-signal sources of the type described in Elektor 19, November 1976, p. 1121 and 1141. A3, together with D2 and D3, functions as a





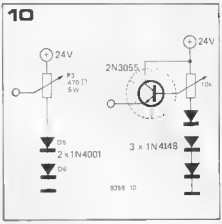
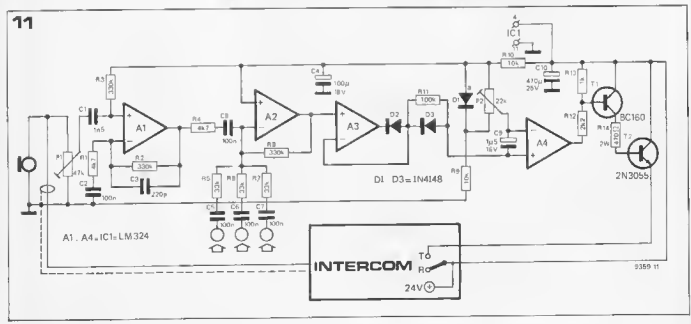


Figure 9. Extension to switchable multi-channel transceiver.
Figure 9a shows the necessary alterations to the frequency-determining section of the transmitter VCO; figure 9b shows the alterations to the VCO frequency in the PLL of the receiver.

Figure 10. On the left is the original circuit, whilst an alternative method of regulating the power of the transmitter is shown on the right (cf. figure 3b).

Figure 11. Circuit diagram of babyphone extension for mains intercom.



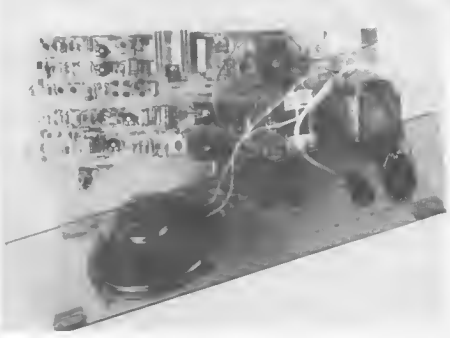
rectifier, and feeds a DC voltage to A4, which operates as a trigger, the threshold voltage of which may be adjusted by means of P2. With a sufficiently large input signal, the output of A4 is pulled low, causing T1 and T2 to turn on and switch the supply voltage to the intercom. The value of R14 is such that the maximum current through T2 is 1A, which should prove sufficient in the majority of cases.

The adjustment procedure is as follows: the slider of P2 is turned fully towards the anode of D1 and P1 is used to adjust the circuit to the desired sensitivity. If the circuit fails to trigger with P1 set for maximum sensitivity, then the trigger threshold can be lowered by means of P2.

In addition to its use with a mains intercom, the circuit can be adapted for radio ham applications, since:

- the circuit functions with supply voltages equal to or greater than 6 V
- the circuit offers the possibility of VOX (Voice operated transmission)
- A1 and A2 can be used as microphone amp and clipper.

M



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Multipurpose time switch

Summer Circuits 1977 (E27/28), circuit no. 6. The operation of this circuit is such that only half of the mains period is multiplied to obtain the required timing period. The maximum timing interval is therefore 0.01×2^{24} seconds, or approximately 46.6 hours. In the example given for a 24-hour timer, an extra nought should be added at the end of the binary number. It will be noted that the A1 . . . A8, B1 . . . B4 and C1 . . . C4 connections shown in the circuit diagram are correct for this application.

The last paragraph is perhaps misleading. The CMOS NAND gates mentioned are actually N8 and N4 in the circuit.

Automatic NiCad charger

Summer Circuits 1977 (E27/28), circuit no. 13. In the diagram, two resistors are shown as R6. The one in the top left hand corner should be R4 = 330 Ω.

Furthermore, it should be noted that although S1 is shown on the p.c.board, only one pushbutton is required for any number of boards as shown in the circuit diagram.

0 . . . 10 V supply

Summer Circuits 1977 (E27/28), circuit no. 24. A resistor R_X is shown on the component layout for the printed circuit board. If a wire link is used here, the circuit shown in figure 1 is obtained. Alternatively, a fixed resistor at this point can be used to reduce the maximum output voltage obtainable to any desired value.

Spot-frequency sinewave generator

Summer Circuits 1977 (E27/28), circuit no. 25. The input pinning of IC2 and IC3 are shown incorrectly. In both cases, the inverting input should be pin 2 and the non-inverting input should be pin 3.

Stereo pan pot

Summer Circuits 1977 (E27/28), circuit no. 35. The value of P1/P1' is not shown in the diagram. This should be a twin 10 k lin potentiometer.

Reaction speed tester

Summer Circuits 1977 (E27/28), circuit no. 54. Very little remains of the identification of the preset potentiometer between pins 6 and 7 of IC1 . . . This is P1, and the value is 100 k.

If desired, C1 can be reduced to 390 n and P1 can be readjusted until clock pulses are produced every 10 ms.

Short-wave converter

Summer Circuits 1977 (E27/28), circuit no. 64. In the text, for BFO read VFO (variable frequency oscillator).

Phaser

Summer Circuits 1977 (E27/28), circuit no. 70. T1 . . . T6 are given in the circuit as BC245Cs. This should have read BF245C.

Voltage controlled monostable

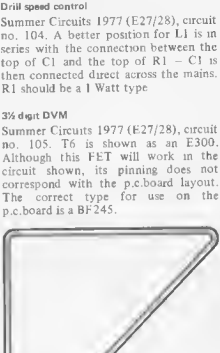
Summer Circuits 1977 (E27/28), circuit no. 82. The positive end of the electrolytic should be connected to pin 11 of the IC, the negative end to pin 10.

Drill speed control

Summer Circuits 1977 (E27/28), circuit no. 104. A better position for L1 is in series with the connection between the top of C1 and the top of R1 – C1 is then connected direct across the mains. R1 should be a 1 Watt type

3½ digit DVM

Summer Circuits 1977 (E27/28), circuit no. 105. T6 is shown as an E300. Although this FET will work in the circuit shown, its pinning does not correspond with the p.c.board layout. The correct type for use on the p.c.board is a BF245.



working perspex

Almost every electronics enthusiast likes to house his lovingly constructed projects in an attractive case or cabinet. Although a wide range of cabinets is now available from various manufacturers it is still often difficult to find a case which meets the exact requirements of a particular project, or is within the budget of the constructor. Attractive cabinets can be fabricated from acrylic sheet such as Perspex ™ or Plexiglas ™ with much simpler tools than those required for metalworking.

Acrylic sheet is relatively inexpensive, and is available both clear and opaque in a variety of colours. 3 mm thick sheet will normally be adequate for all but the largest cabinets. Acrylic sheet is normally obtained covered by a protective paper film. This simplifies marking out, and to avoid scratches the paper should be retained until after drilling and sawing operations are complete.

Drilling

A certain amount of care must be taken when drilling perspex to avoid splintering and cracking around the hole. Drills should always be kept as sharp as possible. When drilling small holes a normal twist drill may be used and the drill speed should be kept high. However, prolonged high-speed drilling should be avoided as friction may cause the perspex to melt. It is much better to drill a hole in several 'bites', allowing the drill and workpiece to cool down in between, and clearing swarf from the drill flutes.

Larger holes are best cut with a screw auger, since this cuts the hole from the outside inwards and splintering is less likely.

Very large circular holes may be cut using a hole saw or tank cutter. When cutting large holes, care should always be taken to clamp the work securely in case the drill or cutter should grab, which might otherwise lead to the loss of several fingers.

Sawing

Straight cuts can be made using a normal hacksaw or a power saw with a fine tooth blade. Large cut outs of any shape may be made using a jigsaw or padsaw, after first drilling a hole into which the saw blade can be inserted. As with drilling, care must be taken to avoid melting the acrylic sheet, and frequent stops should be made to clear swarf from the saw blade, since it has a marked tendency to clog the teeth.

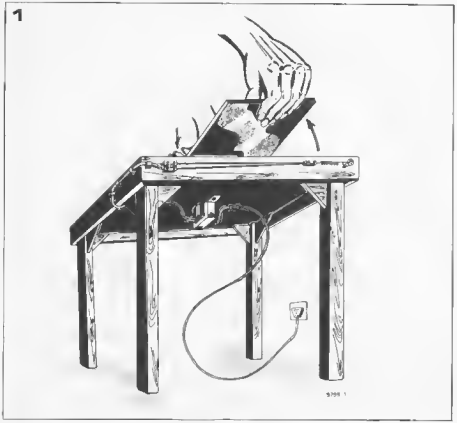
Bending

A useful quality of acrylic sheet is that it can easily be bent after softening by heat. Only the portion of the sheet where the bend is to occur is heated, and figure 1 shows a simple bending jig that can be mounted at the edge of a workbench. Current is passed through a length of resistance wire mounted along the edge of the bench just below the acrylic sheet. The wire, and hence the sheet, heats up, and the sheet can easily be bent upwards. If a sharp bend is required then a wooden batten may be clamped over the sheet along the bending line. However, sharp bends will cause some 'waisting' of the sheet at the bend.

The mechanical details of the bender are extremely simple. The current supply is brought to a 'chocolate block' connector which is fixed to the bench. The resistance wire is a loop which goes out from the connector to a second connector and back again. The second connector is fixed to a coil spring that keeps the wire under tension so that it will not go slack as it heats up and expands.

The power rating of the transformer

1



should be around 80 watts, and for safety reasons the secondary voltage should not exceed about 24 V. The resistance of the wire can easily be calculated from the equation:

$R = \frac{V^2}{P}$ where R = resistance
V = transformer voltage
P = transformer power

The length of wire required can then be found by dividing the required resistance by the specific resistance (ohms per metre) of the wire. For example, if the transformer secondary is 24 V at 80 W then $R = \frac{24^2}{80} = 2.81\ \Omega$. If the specific resistance of the wire is 2.5 Ω/m then the length required is $\frac{2.81}{2.5}$ or 1.12 m.

Alternatively, if a particular length of wire is required, for example to fit a certain bench, then the required specific resistance can be obtained by dividing the resistance by the length required. Obviously the wire gauge chosen should not be so thin that it will quickly burn out in use, but there is obviously much scope for individual ingenuity in constructing a bending jig.

The basic circuit of the bender is shown in figure 1a. The heating effect may be controlled by driving the transformer from a 100 VA Variac as shown in figure 1b, or by driving the heater direct from an isolating Variac as shown in figure 1c. On no account should the heater be driven direct from a normal Variac, however, as this is not isolated from the mains.

To use the bender the bend line is placed directly over the heater and the heater is switched on for about thirty seconds, after which the acrylic sheet should bend easily. Care should be taken not to bend at too low a temperature as this can cause stress lines and cracks. When making a right angle bend it is best to bend the sheet just past ninety degress as it will tend to 'unfold' as the material cools. With a little practice bends with very clean, straight edges can easily be achieved.

Bending is best carried out after all drilling operations have been completed, as otherwise the sheet cannot easily be supported while drilling. The only exception to this rule is if a large hole is to be cut very close to a bend. This should be cut after bending, as otherwise the bending operation may distort the hole.

Cabinets may be constructed from a single sheet in 'wrap-around' form with two endplates, as shown in the accompanying photograph. In this case only one seam is required on the main part of the box, and from an appearance point of view it is best to place this at the base of the cabinet. The end cheeks can be made of acrylic sheet or, for a contrasting appearance, wood. Wood also has the advantage that it can easily be grooved to accept the edges of the box. A transparent acrylic box with wooden end cheeks can make an attractive housing for an instrument such as a digital clock, allowing all the 'works' to be seen.

Another useful method of construction is to make three sides of the cabinet in a 'U' shape from a single acrylic sheet. The other three sides are also made in the form of a 'U' which mates with the first 'U'. The advantage of this method is that one part of the cabinet can form the front panel, base and back panel with components mounted on it, while the other part is simply a lift off lid.

Seams and joints may be made using acrylic adhesive which is available from suppliers of acrylic sheet.

Lettering

Acrylic cabinets, like any other cabinet, can be attractively labelled using instant dry transfer lettering. After rubbing down the letters firmly they can be sprayed with protective lacquer to prevent damage. The lacquer should be of a type that dries to a hard gloss finish, as the matt types of lacquer supplied for use with instant lettering tend to attract dirt very quickly.

TM-Perspex and Plexiglas are registered trade marks.

2

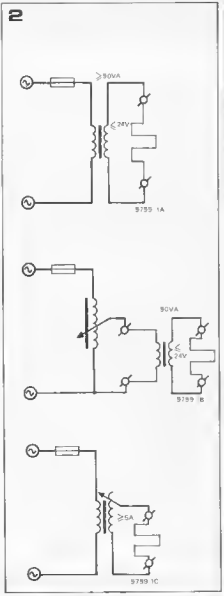
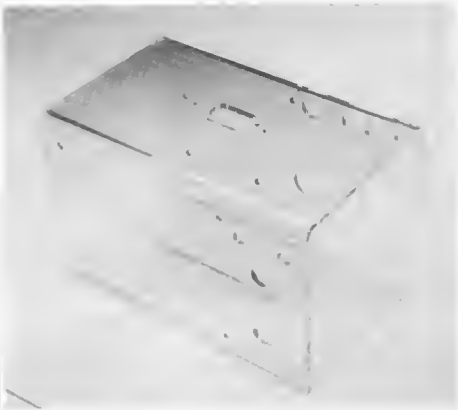


Figure 1. Construction of a simple bending jig for acrylic sheet work.

Figure 2. Three possible methods of powering the heater for the bending jig.

Photo. An almost complete acrylic sheet cabinet, showing the main assembly and the two end cheeks.



logarithmic darkroom timer

Although there is no shortage of designs for darkroom timers, many of these suffer from the twin drawbacks of a linear timing scale and inconvenient controls that leave the user fumbling about in the dark. The design presented here overcomes these disadvantages by having a logarithmic timing scale and ergonomically designed controls.

Linear or Logarithmic

When taking a photograph, the exposure of the film can be varied in two ways, by altering the shutter speed and by altering the aperture setting of the camera. Opening the aperture by one stop doubles the amount of light falling on the film, i.e. the aperture setting is calibrated logarithmically.

In the darkroom, when printing or enlarging, the exposure of the photographic paper is varied by altering the time for which the lamp is switched on. Here again, a logarithmic scale is appropriate. For example, consider a timer with a linear scale calibrated from 0 to 100 seconds in intervals of five seconds. The first 'stop', from 5 to 10 seconds, will double the exposure time. However, at the top end of the scale a change of exposure time from 95 to 100 seconds would have little effect on the final print, as this last stop represents only a 5% change in exposure time. This means that : a) the timing scale is too finely calibrated at the upper end, but is probably too coarsely calibrated at the lower end, and b) the range of such a timer is limited, since to extend it to say 200 seconds would require a 40-way switch[1].

This objection could admittedly be overcome by building a digital timer programmed by thumbwheel decade switches, but there would still remain the basic difficulty of having to estimate how much to increase or decrease the exposure time in order to obtain a lighter or darker print.

In the circuit given here, each increment of the timing switch doubles the exposure time, so each switch position will have the same effect on the density of the final print. If a finer increment is required a 'half-stop' position is provided that increases the exposure time by a factor of $\sqrt{2}$.

A block diagram of the timer is given in figure 1. Pulses from a 10 Hz clock generator are divided by a counter whose division ratio can be set to either 5 or 7 by means of S1a. This means that with S1a in the 'x 1.4' position the period of the output pulse is 7/5 (= 1.4) times the period of the output waveform with S1a in the divide-by-five position. Since 1.4 is a reasonable approximation to $\sqrt{2}$, the timing interval with S1a in the 'x 1.4' position is $\sqrt{2}$ times the timing interval with S1a in the 'x 1' position.

The divided-down clock frequency is then fed to the start/stop switching circuit, and also to a 12-bit binary counter. The start/stop circuit is provided with Q and $\bar{Q}$ outputs, and in the quiescent state the Q output is high, holding the binary counter in a reset condition.

When the start button is pressed the Q output goes high on the next positive-going edge of the clock pulse. This removes the inhibition on the counter which begins to count the clock pulses. S2 is used to select the particular output of the counter at which the timing interval is to stop. When that output goes high the Q output of the start/stop circuit goes low and the $\bar{Q}$ output goes high, which stops the count and resets the counter. A manual stop button is also provided for resetting the timer on initial switch-on, or for manual termination of the timing interval.

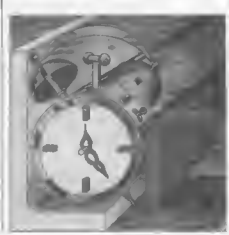
As each stage of the binary counter divides the output frequency of the previous stage by two, the output period of each stage is twice that of the preceding stage, and this is how the logarithmic timing scale is obtained.

The Q and $\bar{Q}$ outputs can be used to drive a relay or relays to switch on the enlarger/printer lamp during the timing interval and, if required, to switch off the darkroom safelight.

The complete circuit of the timer is given in figure 2. The clock generator is an astable multivibrator built around two NAND gates N1 and N2. The clock frequency is divided down by IC1, a 4017 decade counter.

Depending on the position of S1a this counter will count to 5 or 7 before resetting itself via N3 and N4. The divided down clock pulses are available at the output of N3.

The start/stop circuit comprises two D-flip-flops FF1 and FF2. In the quiescent state, for example when the stop button has been pressed, both these flip-flops will be in the reset state. The $\bar{Q}$ output of FF1 will hold the reset input of the binary counter IC3 high,



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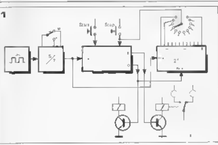
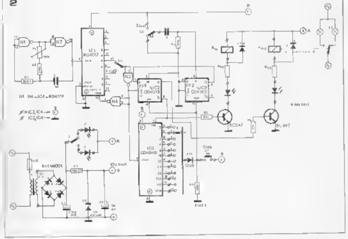
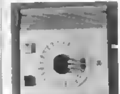


Figure 1 Block diagram of the timer. Clock pulses from an oscillator are divided by a factor of 5 or 7 in a prescaler. The start/stop circuit controls the application of divided down clock pulses to the main timing circuit, a 12-bit binary counter, which can be set to count to any power of 2 up to 2^{12} by means of S2.

Figure 2 Complete circuit of the darkroom timer. An alternative arrangement using a 24-way switch to replace S1 and S2 is shown in figure 2a.

2





2a

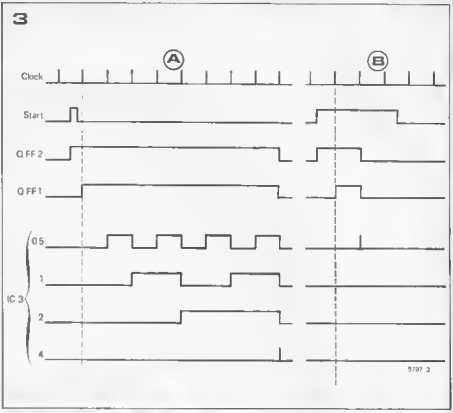
thus preventing it from counting.

When the start button is pressed C2 charges through R4 producing a short positive pulse to set FF2. The Q output of FF2 will now hold the D input of FF1 high so that on the next positive edge of the clock pulse the $\bar{Q}$ output of FF1 will go low allowing IC3 to begin counting. When the output of IC3 selected by S2 goes high, FF1 and FF2 will be reset via D10 and the counter IC3 will be reset. The range of timing intervals is from 0.5 seconds to 1024 seconds, but if desired this can easily be changed by altering the frequency of the clock generator.

During the timing interval T2 is turned on by the Q output of FF1 thus lighting D2 to indicate that the timing interval is in progress, and energising Re2 to turn on the enlarger/printer lamp. At the same time T1 is turned off, extinguishing D1 and de-energising Re1 to switch off the darkroom safelght. This of course assumes that relays with single-pole, normally-open contacts are used for Re1 and Re2. If a relay with a single-pole changeover contact is used then this can switch on the enlarger and switch off the safelight simultaneously, in which case Re1 can be omitted, and the Re1 terminals on the p.c.b. bridged by a wire link. The voltage and current capability of the relay contacts should be sufficient to handle the lamp currents. The coil rating of the relays should be 12 V 50 mA or less. In this case, R8 and R9 can be replaced by wire links. However, if a lower voltage relay is used, suitable values for R8 and R9 should be chosen to limit the LED current to 50 mA. For example, if a (nominally) 6 V/50 mA relay is to be used, R8 (or R9) should be $\frac{12-6}{50}\ k\Omega = 120\ \Omega$.

Figure 3 shows a timing diagram for the circuit. In the left-hand part of the diagram S2 has been set to a time of 4 seconds. After the start button has been pressed the Q output of FF1 goes high at the next clock pulse and remains high until output 4 of the counter goes high when the circuit resets. The right-hand part of the diagram illustrates that the timing interval is unaffected by inadvertently holding down the start button. In this case the timing interval is set to 0.5 second, which is achieved despite the fact that the start button has been depressed for longer than this.

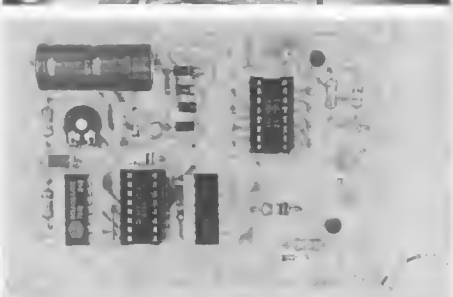
3



Construction

A p.c. board and component layout for the timer are given in figure 4. Careful attention to the construction is required if the timer is to be safe and easy to use. Figure 5 shows a suggested front panel layout. The twelve-position switch carries a knob to which is attached a perspex disc marked out with 24 timing intervals. D11 is positioned beneath the disc so that it illuminates the full-stop timing intervals, i.e. 0.5, 1, 2, 4, 8 seconds etc. while D12 is positioned so that it illuminates the half-stop intervals, i.e. 0.7, 1.4, 2.8 seconds etc. LEDs D1 and D2 are mounted so as to indicate which button should be pressed next, so D1, which is lit when the timer is quiescent, is mounted next to the start button, indicatng that this button should be pressed to start the timing sequence. D2, which is lit during the timing sequence, is mounted next to the stop button, so that this button can easily be found to stop the timer if necessary.

As an alternative to S1 and S2 a 2-pole, 24-way switch may be used, wired



Parts list for figure 4

Resistors:
R1 = 820 k
R2 = 270 k
R3,R4 = 100 k
R5,R6 = 22 k
R7 = 560 Ω
R8 = see text
R9 = see text

Capacitors:
C1 = 150 n
C2 = 10 n
C3 = 470 μ/25 V
C4 = 10 μ/16 V tantalum

Semiconductors:
D1,D2,D11,D12 = LED
D3 = zener 10 V/400 mW
D4, D5, D6, D7 = 1N4001 or equivalent
D8 = 1N4148 or aquivelent (see text)
D9 = 1N4148 or equivalent
D10 = DUS
T1,T2 = BC547
IC1 = CD4017
IC2 = CD4013
IC3 = CD4040
IC4 = CD4011

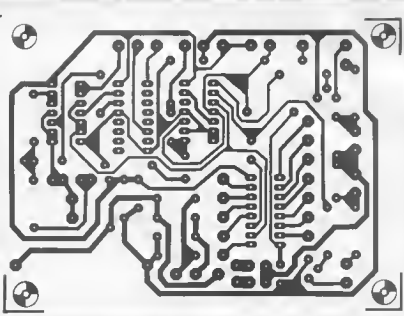
Miscellaneous:
S1 = DPDT toggle switch
S2 = single-pole 12-way switch
S3,S4 = pushbutton switch with change-over contacts
slow blow 100 mA fuse and holder
Re1 = relay. Nominal coil rating 12 V/50 mA, with single pole N.O. contact suitable for 240 V. (see text)
Re2 = as Re1, or with single pole changeover contact. (see text).
Tr = supply transformer 12 V/100 mA
2 mains sockets
perspex disc and rub-on lettering.

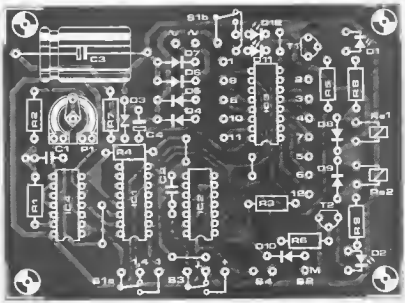
Figure 3. Timing diagram for the darkroom timer. For simplicity only the first four outputs of the binary counter are shown.

Figure 4. Printed circuit board and component layout for the timer. The mains transformer, relay(s) and controls are mounted external to the board.

Figure 5. Suggested front panel layout for the timer.

4





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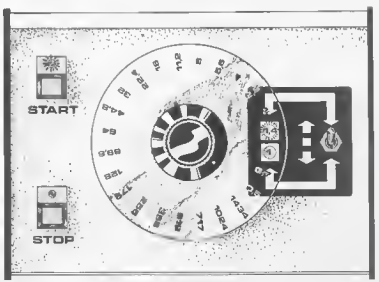


as shown in figure 2a. The bank of this switch that replaces S1a is wired so that it switches IC1 alternately between x1 and x 1.4, while the bank that replaces S2 is wired so that it changes the selected output of IC3 on every second position of the switch. S1b and D12 are then superfluous, and D11 is simply wired in permanently to illuminate the perspex disc. However, it should be stressed that 24-way switches are not very easy to obtain, which was why the two-switch approach was adopted in the first place.

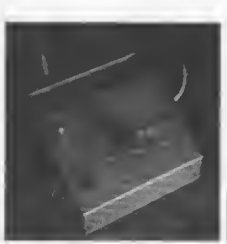
In view of the fact that one is frequently working with wet hands in a darkroom, and that there are probably several 'earthy' points such as water taps, the wiring and mechanical construction must be of a very high standard to avoid any danger of electric shock. Firstly, the case of the timer should be splashproof (no ventilation is required since the power consumption is low) and all metal parts should be securely bonded to mains earth. All mains wiring should be carried out using suitable, double insulated mains cable, and should be secured with cable clips so that there is no danger of a bare mains wire touching any metal part of the case should it come adrift.

The lamp outputs from the relays can be brought out to the back of the case on normal mains sockets.

As a final safety point, as with any electrical equipment that may be used in damp conditions, e.g. washing machines, lawnmowers, hedge trimmers etc., it is a good idea to have the house wiring system fitted with an earth current leakage trip.

Calibration

To calibrate the timer, simply set S1 and S2 to some convenient short interval such as 8 seconds and adjust P1 until the timer agrees with some standard such as a stopwatch. Then check the timer on the higher ranges, where the longer timing interval will allow a more precise check of the accuracy, and readjust P1 if necessary. ⋈



Monitor Switching for Two Tape Decks

Although modern audio amplifiers frequently sport an abundance of (seldom-used?) gimmicks, very few amplifiers possess comprehensive tape switching and monitoring facilities. Most have only a single tape socket, with facilities for making a recording onto one tape deck and monitoring that recording, and have no provision for a second tape deck.

The simple switching circuits described here will allow recording from disc or other sources onto two tape recorders, either one at a time or simultaneously, with monitoring of both recordings. In addition, transcription from either tape recorder to the other is possible, while at the same time a totally different source (disc, tuner, etc.) can be played through the amplifier.

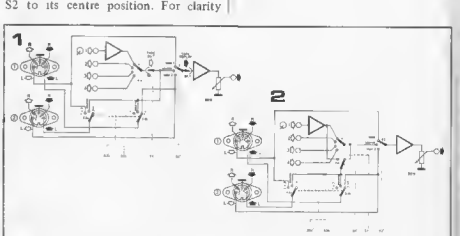
The switching circuit is shown in figure 1. The function selector switch of the amplifier (disc, tuner, aux, etc.) is represented by S1. S2 and S3 are part of the switching unit. With S3 in its centre position a signal can be taken from the source to the record inputs of both tape recorders. With S1 in position 1 → 2 the playback output of one tape deck is fed to the record input of the second, while in the 2 → 1 position the playback output of the second deck is fed to the record input of the first.

Whatever the position of S3, monitoring of tape 1, source, or tape 2 is possible by means of S2. Therefore, with S3 in position 1 → 2 or 2 → 1 it is still possible to listen to disc, tuner, etc. by setting S2 to its centre position. For clarity only the left channel is shown, but the right channel is identical.

The circuit may be incorporated into the amplifier by inserting it between the output of the function switch and the input of the next stage of the amplifier. The original tape monitor switch (if fitted) can be discarded and replaced by S2, while an extra hole must be drilled in the front panel for S3.

Alternatively the switching unit can be mounted in its own box and can be connected to the amplifier via the existing tape socket. The output to the unit is simply taken from the record pin of the tape socket, and the input back to the amplifier from the rotor of S2 is taken to the replay pin of the tape socket. The amplifier must then be operated with the tape monitor switch depressed.

A slight modification to the circuit, shown in figure 2, allows recording from disc while listening to a different source. With S4 in the left-hand position the output of the disc preamp can be tapped off and fed to the tape decks, while S1 can be in any of its four positions, thus allowing disc or some other source to be listened to at the same time. The recording may also still be monitored by setting S2 to 'tape 1' or 'tape 2'. ⋈



ccir tv pattern generator (1)

The basis of any television signal is a complex synchronisation wave form, which ensures that the scanning circuits of the TV receiver stay synchronised to the transmitted signal. Standards vary throughout the world, but in Europe the CCIR norm is used, and the basis of this design is a generator to provide a CCIR standard sync signal. Of course, such a sync signal is of very little use by itself, so the modular construction allows the addition of units to generate various video signals, the first of which is a test pattern generator giving a fully interlaced picture.

The letters CCIR stand for Comité Consultatif International des Radio communications which is an international standards committee in the field of telecommunications. The principal specifications of the European TV standards are:

number of lines per frame	625
line frequency	15625 Hz
field frequency	50 Hz
picture (frame) frequency	25 Hz
video bandwidth	5 MHz
channel width	7 MHz
vision - sound carrier separation	5.5 MHz

Even in Europe there are several slight variations on this standard, but these are mainly concerned with minor details such as channel width, video bandwidth and vision-sound carrier separation so they do not affect the basic characteristics of the sync signal. There are, of course, totally different systems (and receivers!) still in use such as the British 405 line system, the French 819 line system and the American 525 line system, and these are incompatible with the present design. However, the generator is broadly compatible with many systems based on a 625 line 50 Hz field standard. Discussion of colour signals will be limited to the PAL system.

Complete information on the standards mentioned can be found in the CCIR Report No 624 Vol XI, Geneva 1975, which as far as we are aware is the most recent publication on the subject of television standards. The present design is based on the CCIR 'B' and 'G' standards discussed in this report.

The TV picture

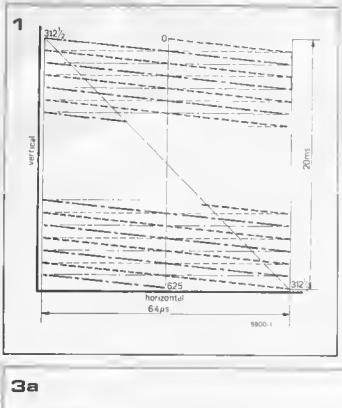
At the risk of boring those who are already au fait with the basic system of television (they can always skip this portion of the text) a brief description of the composition of a TV signal and picture will be given to assist those who are not 'clued-up' on this subject.

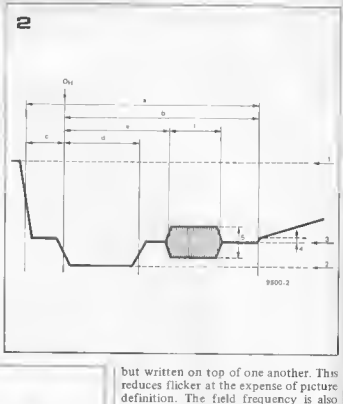
A TV picture is built up by an electron beam scanning 625 lines across the screen of a TV picture tube, the brightness of the picture at any point on the screen being determined by the beam current. Of course the picture does not have an existence in real time, since the top part of the picture is fading out as the bottom part is being scanned, but the afterglow of the 'phosphor' and persistence of vision combine to make the viewer see a stable picture that occupies the whole screen with equal brightness.

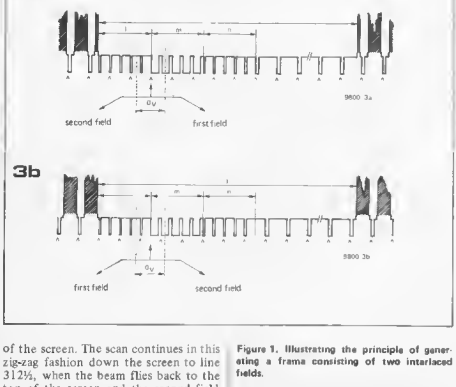
The bandwidth occupied by a TV signal is directly proportional to the line frequency, which in turn is proportional to the number of lines per second that are scanned (frame frequency). In the interests of the most economic use of the rf spectrum the minimum frame frequency must be chosen that gives an acceptable picture. As with cine photography, any movement that is being televised is not being presented continuously but is being sampled in a sequence of discrete frames. The frame frequency must thus be sufficiently high that any movement in the televised scene appears continuous and not a series of jerky steps. In cine photography this occurs at about 16 frames per second. The second limitation on frame frequency occurs because the picture is blanked out between each frame, and if the frame frequency is too low a noticeable flickering of the picture brightness occurs. In cine photography this problem is overcome by opening and closing the projector shutter, for instance three times on each frame, thus raising the flicker frequency to 48 Hz which is too fast for the eye to notice.

This procedure is not possible with a television picture since there is no way of storing a frame for subsequent replication, so the problem is overcome in a different way. Firstly, the frame frequency is 25 Hz which is more than adequate to overcome the jerkiness problem. Secondly, each frame is scanned, not in one 625 line sweep but in two *interlaced fields* of 312½ lines each. The field frequency is thus 50 Hz which is sufficiently high to overcome the flicker problem, but the frame or picture frequency is only 25 Hz so the video bandwidth is not excessive.

Figure 1 illustrates the principle of the interlaced scan. The first (odd) field starting with line 0 is shown dashed. Each line takes 64 µs to scan, and at the end of each line the electron beam rapidly flies back to the left-hand edge







of the screen. The scan continues in this zig-zag fashion down the screen to line 312½, when the beam flies back to the top of the screen and the second field starts with the second half of line 312. It is apparent that the second field fills in the gaps between the lines of the first field, i.e. the two fields are *interlaced*.

Although interlacing is a satisfactory method of reducing flicker on moving scenes, since any residual flicker is masked by the movement, flicker can still be quite annoying on stationary pictures such as test patterns, as the changeover from the odd field to the even field is quite noticeable. The pattern generator therefore offers the option of switching off the interlace, in which case the picture will consist of two fields of 312 lines, not interlaced but written on top of one another. This reduces flicker at the expense of picture definition. The field frequency is also slightly increased due to the loss of one line.

Figure 1. Illustrating the principle of generating a frame consisting of two interlaced fields.

Figure 2. Detail of the waveform during a line blanking interval showing the line sync pulse and chroma burst.

Figures 3a and 3b Showing a complete composite video + sync waveform for a) the end of an even field and start of an odd field, and b) end of an odd field and start of an even field.

The CCIR standard

Extensive text, diagrams and tables of rise and fall times and signal levels are used to define the video signal in the CCIR report on which the pattern generator is based. It is clearly impractical and unnecessary to reproduce all this information here, so only the more salient points will be discussed.

Figure 2 shows, in detail, a portion of the composite video waveform around the line blanking interval. The maximum amplitude of the video signal in this example is taken as being peak white level (1). The minimum signal level is sync level (2), and between these two lie blanking level (3), which is 30% of the total signal level, and black level (4). Picture information is distinguished from sync information by the fact that it occupies the portion of the waveform above black level, while sync information occupies the portion below blanking level. Black level and blanking level frequently coincide, but black level may be up to 2% above blanking level. At the beginning of the line blanking interval (a), which lasts for 12 μs, the video signal is clamped to blanking level, which ensures that the signal is below black level during the retrace (flyback) period. The retrace is thus not visible on the screen.

1.5 μs after the start of the line blanking interval the sync pulse (d) begins, and lasts for 4.7 μs. After the line sync pulse the chroma subcarrier burst in a colour transmission (f) is inserted on the 'back porch' of the sync signal. This consists of 10 cycles of the chroma (colour) subcarrier, which is suppressed during transmission of the picture information,

and facilitates demodulation of the chroma signal. How this is done is not important at this stage; the only thing to note is that the 'grass' on the back porch is only present during colour transmissions.

The specifications and tolerances of the line blanking interval waveform are given in table 1.

Field synchronization

The waveform of the video signal during the field blanking interval is shown for the end of an even field and the beginning of an odd field in figure 3a, and conversely, for the end of an odd field and the beginning of an even field in figure 3b. It is immediately apparent that this waveform is considerably more complex than the line blanking interval waveform. As a time scale on these diagrams one line period (64 μs) is equal to the distance between two Λ symbols.

The picture information is clamped to blanking level for the duration of the field blanking interval. Immediately after the start of the field blanking interval is a sequence of five *equalisation* pulses (i). This is followed by a sequence of five field sync pulses (m), then a further sequence of five equalisation pulses (n). The remainder of the field blanking interval is occupied by normal line blanking pulses.

The lines that occur during the field blanking interval carry no picture information, and are responsible for a black band just off the top or bottom of the television picture. Some of these lines may carry digital information for engineering purposes and for the transmission of Teletext. From figure 3 it is obvious that the period of a field sync or equalisation pulse is half of a line period, and this is shown in figure 4, which is an expanded version of the field blanking interval about the area O_Y. The specifications and tolerances of the field blanking waveform are given in table 2.

Design considerations

All pulse lengths and timing intervals in the generator are derived from a crystal oscillator by dividing down using digital counters. It is fairly obvious that the accuracy with which these intervals can be generated depends on the frequency of the oscillator signal, since the smallest time interval that can be generated is equal to the half-period of the oscillator signal. Looking at tables 1 and 2 it is clear that the smallest time interval is 0.05 μs, since the equalisation pulses are specified as 2.35 μs and the colour burst period as 2.25 μs, so it would appear that an oscillator frequency of 10 MHz is necessary.

In the interests of circuit economy (shorter counter chains) and to minimise undesirable effects due to logic circuit propagation delays, it is worth considering whether a lower clock frequency could be used. Taking into account the tolerances allowed in the various pulses and timing intervals, it becomes apparent that a clock frequency of 4 MHz is permissible. As the half-periods of the clock signal itself will be used to generate timing intervals it is necessary that the clock waveform should have a 50% duty-cycle, but even allowing for a 10% variation in the clock duty-cycle all pulses and timing intervals still fall well within the CCIR standards. Having decided on the clock frequency it is then possible to choose a suitable logic family on which to base the design. Obviously, the maximum clock frequency of any counters and flip-flops used must be well above 4 MHz, and propagation delays of gates must be sufficiently short not to have any adverse effect on any of the pulse lengths.

These considerations immediately rule out CMOS ICs, since they have an insufficiently high guaranteed minimum clock frequency and too long a propagation delay. The 74-series TTL logic family was therefore chosen. This has the advantage of being sufficiently fast, cheap, and fairly easy to obtain. The disadvantage of TTL is its relatively high power consumption. However this is no real problem in TV work, where a mains supply is generally available. If power consumption is a prime consideration then low power Schottky (74LS series) devices may be substituted in the circuit, though this will increase the cost.

Table 1.

Symbol	Characteristics	
H	Nominal line period (μs)	64
a	Line-blanking interval (μs)	12 ± 0.3
b	Interval between time datum (OH) and back edge of line-blanking signal (μs)	10.5
c	Front porch (μs)	1.5 ± 0.3
d	Synchronizing pulse (μs)	4.7 ± 0.2
e	Start of sub-carrier burst (μs)	5.6 ± 0.1 after OH
f	Duration of sub-carrier burst (μs)	2.25 ± 0.23 (10 ± 1 cycles)

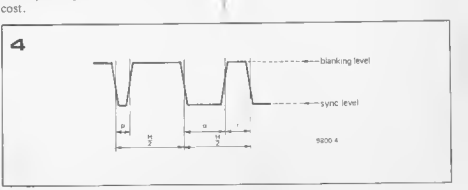
Table 2.

Symbol	Characteristics	
v	Field period (ms)	20
i	Field-blanking period (for H and e, see table 1)	25 H + e
l	Duration of first sequence of equalizing pulses	2.5 H
m	Duration of sequence of synchronizing pulses	2.5 H
n	Duration of second sequence of equelizing pulses	2.5 H
p	Duration of equelizing pulse (μs)	2.35 ± 0.1
q	Duration of field-synchronizing pulse (μs)	27.3 (nominal value)
r	Interval between field-synchronizing pulses (μs)	4.7 ± 0.2

Table 1. Extract from CCIR standards pertaining to the line blanking interval.

Table 2. Extract from CCIR standards with reference to the field blanking interval.

Figure 4. Details from figure 3 around point O_Y, showing the changeover from equelisation to field sync pulses.



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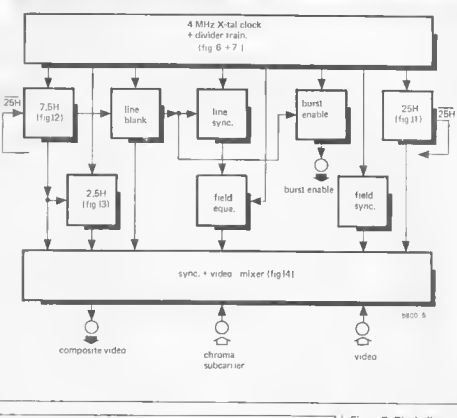

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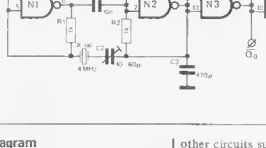


Figure 5. Block diagram of the sync generator.

Figure 6. The clock oscillator.

Figure 7. The divider chain.

Figure 8. Showing the principle of combining outputs of the divider chain to obtain the desired pulses.

Figures 9 and 10. The reference point in the sync waveform is when all counters start from zero, and this is taken as being the leading edge of a line blanking pulse and the trailing edge of the 25 H signal.

Block diagram

Most of the principal timing intervals in the generator may be obtained by simple division of the clock frequency, and the rest are achieved by suitable logic gating. For example, as there are 625 lines per *frame* the *field* period (or rather: frequency) is easily obtained by dividing twice the line frequency by 625 or 5^4. The line frequency itself is exactly 1/256 of the oscillator frequency so a simple eight bit binary counter can be used for this division ratio. The block diagram of figure 5 shows the general arrangement of the sync generator, and the figure numbers corresponding to each individual block are shown in brackets.

The heart of the generator is the 4 MHz clock oscillator with its associated divider train that generates all the required pulse lengths and timing intervals (figures 6 and 7). The blocks below this represent the logic circuitry that produces each portion of the complete sync waveform. Finally, all the 'bits' of the sync waveform are mixed in the sync and video mixer to give the complete sync waveform. Video signals from other circuits such as the pattern generator are also mixed in at this stage, together with the chroma subcarrier signal for colour signals. No colour generator circuits have been included in the present design, but the generator is fully equipped for colour modules to be added later, if and when IC-technology makes them feasible without undue circuit complexity.

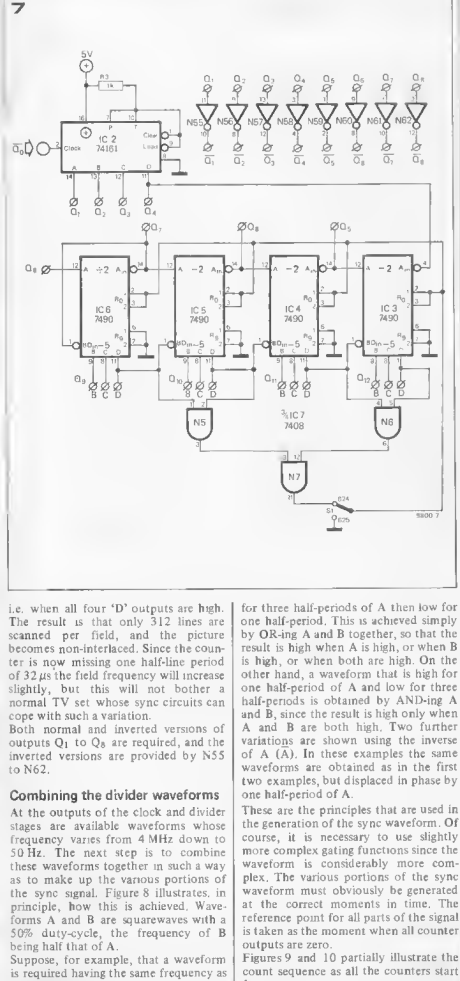
Clock generator

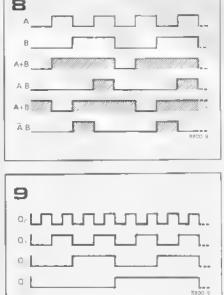
Figure 6 shows the circuit of the clock generator, which is a simple yet reliable crystal oscillator based on two NAND gates. Trimmer C2 provides fine adjustment of the oscillator frequency, and buffered antiphase clock signals are available at the outputs of N3 and N4.

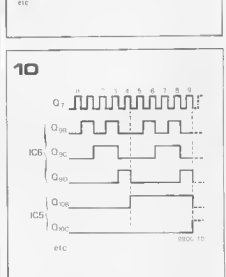
Timebase dividers

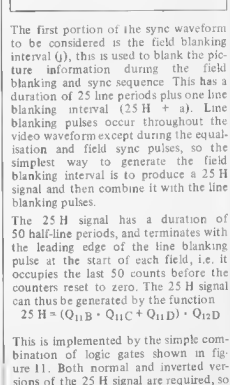
The 4 MHz clock signal must be divided down using digital counters to give all the longer timing intervals required in the generator, and the circuit of the timebase divider chain is given in figure 7. The Q_0 output of the clock generator is first divided by 16 using a 74161 4-bit synchronous counter. Output Q_4 is then fed into four cascaded 7490 counters. The 7490 is a decade counter, but comprises an independent divide-by-two counter and divide-by-five counter that can be utilised separately if desired. Here, the four divide-by-two sections are first cascaded to divide the Q_4 output of IC2 by a factor of 16. The clock frequency has now been divided by a factor of 256 altogether, so the Q_8 output of IC6 is at line frequency, i.e. 4,000,000/256 or 15625 Hz.

The divide-by-five sections of IC3 to IC6 are also cascaded to form a divide-by-625 counter, and the Q_7 output of IC5, which is at twice line frequency is fed into the B input of IC6. Twice line frequency divided by 625 is 50 Hz, which is field frequency, and this is the frequency obtained at the $Q_{12}D$ output of IC3. It is at this stage that the interlaced/non-interlaced option is made available. With S1 grounded, the 625 counter normally counts (naturally enough) up to 625. This corresponds to one field of a normal interlaced picture i.e. 625 half-line periods or 312½ lines. Setting S1 in the upper position causes the counter to reset at a count of 624,









i.e. when all four 'D' outputs are high. The result is that only 312 lines are scanned per field, and the picture becomes non-interlaced. Since the counter is now missing one half-line period of 32 µs the field frequency will increase slightly, but this will not bother a normal TV set whose sync circuits can cope with such a variation.

Both normal and inverted versions of outputs Q_1 to Q_8 are required, and the inverted versions are provided by N55 to N62.

Combining the divider waveforms

At the outputs of the clock and divider stages are available waveforms whose frequency varies from 4 MHz down to 50 Hz. The next step is to combine these waveforms together in such a way as to make up the various portions of the sync signal. Figure 8 illustrates, in principle, how this is achieved. Waveforms A and B are squarewaves with a 50% duty-cycle, the frequency of B being half that of A.

Suppose, for example, that a waveform is required having the same frequency as B but a different duty-cycle, say high for three half-periods of A then low for one half-period. This is achieved simply by OR-ing A and B together, so that the result is high when A is high, or when B is high, or when both are high. On the other hand, a waveform that is high for one half-period of A and low for three half-periods is obtained by AND-ing A and B, since the result is high only when A and B are both high. Two further variations are shown using the inverse of A ($\bar{A}$). In these examples the same waveforms are obtained as in the first two examples, but displaced in phase by one half-period of A.

These are the principles that are used in the generation of the sync waveform. Of course, it is necessary to use slightly more complex gating functions since the waveform is considerably more complex. The various portions of the sync waveform must obviously be generated at the correct moments in time. The reference point for all parts of the signal is taken as the moment when all counter outputs are zero.

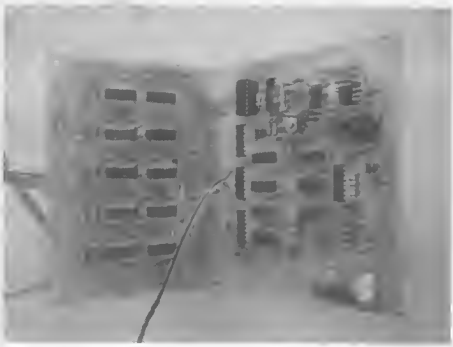
Figures 9 and 10 partially illustrate the count sequence as all the counters start from zero.

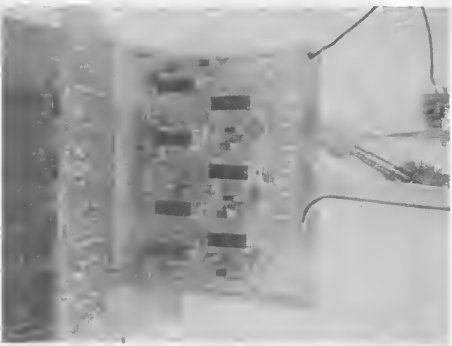
The first portion of the sync waveform to be considered is the field blanking interval (j), this is used to blank the picture information during the field blanking and sync sequence. This has a duration of 25 line periods plus one line blanking interval (25 H + a). Line blanking pulses occur throughout the video waveform except during the equalisation and field sync pulses, so the simplest way to generate the field blanking interval is to produce a 25 H signal and then combine it with the line blanking pulses.

The 25 H signal has a duration of 50 half-line periods, and terminates with the leading edge of the line blanking pulse at the start of each field, i.e. it occupies the last 50 counts before the counters reset to zero. The 25 H signal can thus be generated by the function

$$25\,H = (Q_{1B} \cdot Q_{1C} + Q_{1D}) \cdot Q_{2D}$$

This is implemented by the simple combination of logic gates shown in figure 11. Both normal and inverted versions of the 25 H signal are required, so an inverter is added to the output. The fact that an open collector inverter is





used is quite incidental, it just so happened that this allowed the use of one less IC and was convenient for the p.c.b. layout.

The next portion of the sync waveform to be considered is the interval during which the equalisation and field sync pulses occur (l, m and n). This has a duration of 7.5 H at the beginning of the field blanking interval. The 7.5 H signal is given by

$$7.5\,H = \overline{25\,H + Q_{10B} \cdot Q_{10C} + Q_{10D} + Q_{11D}}$$

The logic gating for this function is shown in figure 12. Here again, the inverted term is required.

The 2.5 H period when the field sync pulses occur, and the 2.5 H periods on either side of it when the equalisation pulses occur, can easily be derived from the 7.5 H signal by gating with output Q_{10B}.

$$2.5\,H = \overline{7.5\,H \cdot Q_{10B}}$$

The logic gating is shown in figure 13.

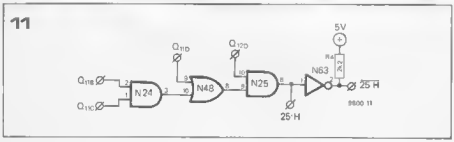
Having obtained these basic intervals it is now possible to see how they can be combined to generate the complete (sync-plus-video) waveform.

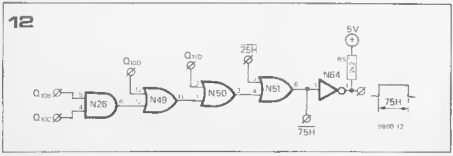
Firstly, line blanking pulses occur at 64 μs intervals throughout the video waveform, except during the 7.5 H period of equalisation and field sync pulses.

Line blanking pulses must therefore be AND-ed with 7.5 H to achieve this suppression.

Field sync pulses, on the other hand, must occur only during the 2.5 H period in the middle of the 7.5 H period, and equalisation pulses occur during the 7.5 H period on either side of the field blanking pulses, so these can easily be obtained by AND-ing with the 2.5 H and 7.5 H signals.

Gating of the picture information is very simple. The video signal is present except during the field blanking and line blanking intervals, so the video signal is simply AND-ed with 25 H and line blanking.





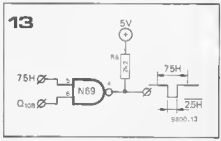


Figure 11. Geting to darive the 25 H signal.

Figure 12. Gating to derive tha 7.5 H signal.

Figure 13. Gating to obtain the 2.5 H signal.

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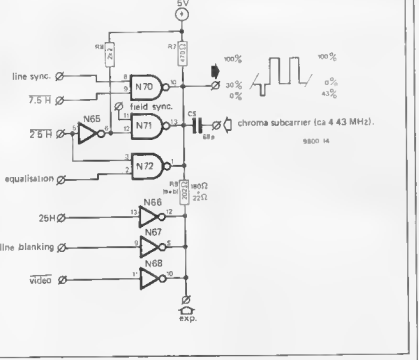

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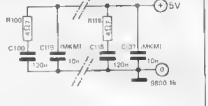

Figure 14. Complete circuit of the sync plus video mixer.

Figure 15. The power supply, which uses an IC regulator.

Figure 16. Extensive decoupling of the supply lines is required to avoid problems due to spurious pulses.

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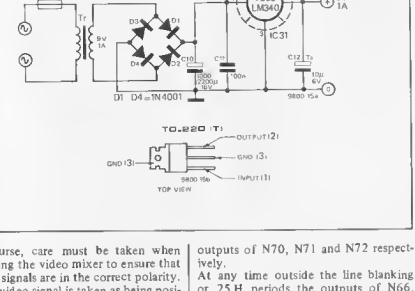

Of course, care must be taken when designing the video mixer to ensure that all the signals are in the correct polarity. If the video signal is taken as being positive (always above the 30% level) then the sync signals are negative (below the 30% level).

Sync plus video mixer circuit

Figure 14 shows the complete circuit of the mixer, which is based on open collector logic gates and mixing resistors, and its operation is fairly obvious. During the 2.5 H period or the line blanking interval the output of either N66 or N67 will be low, which will inhibit any video information on the output of N68 and will cause the junction of R7 and R9 (i.e. the output) to be held at the 30% level, except when it is pulled down to 0% by line sync, field sync or equalisation pulses at the outputs of N70, N71 and N72 respectively.

At any time outside the line blanking or 2.5 H periods the outputs of N66, N67 and N70 to N72 will be open-circuit, (the open-collector output transistors being turned off) so video information at the output of N68 can pass to the output. However, the video output can never fall below the 30% level (which would cause false sync pulses) since the output will be at 30% even for the minimum output (0 V) from N68.

It should be noted that the video signal is fed in an inverted form to N68, so that the output of N68 produces the normal video signal. Two other inputs are provided to the video mixer. The chroma subcarrier can be fed in via C8, and an experimental input (exp.) is provided to which other gates may be connected. This input also offers the possibility of selecting a grey level for the video signal rather than peak white level by connecting a resistor between this point and earth (typically 1 k). Generation of the line blanking, line sync, field sync and equalisation pulses will be considered in the next part of this article.

Power supply

The generator requires a power supply of 5 V at up to 1 A, depending on the number of modules used, and for compactness and simplicity a 7805 or LM 340 IC voltage regulator (TO-220 package) was chosen. Note that this IC should be provided with an adequate heatsink!

The power supply circuit is given in figure 15. To avoid any problems due to spurious pulses extensive decoupling of

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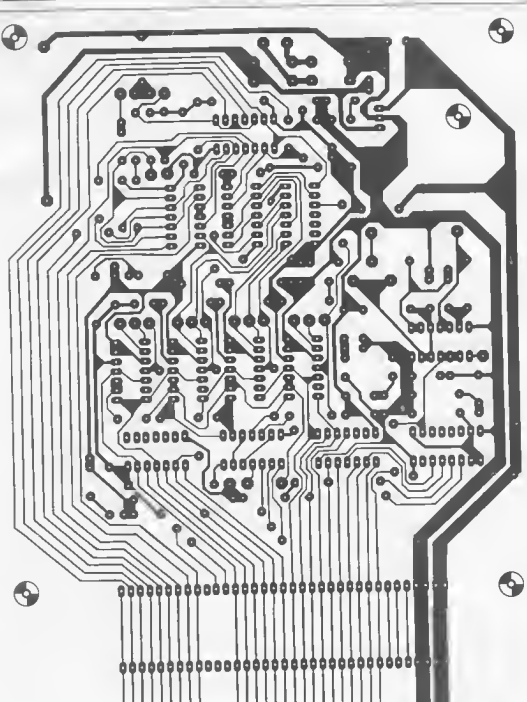

Parts list to figure 17.

Resistors:
R1,R2,R3 = 1 k
R4,R5,R6,R8 = 2k2
R7 = 470 Ω
R9a = 180 Ω
R9b = 22 Ω
R100 . . . R118 = 4Ω7

Capacitors:
C1,C101,C103,
C119 . . . C137 = 10 n
C2 = trimmer 10 . . . 60 p
C3 = 470 p
C4 . . . C7 = see part 2
C8 = 68 p
C9 = see part 2
C10 = 1000 . . . 2200 µ, 16 V
C11 = 100 n
C12 = 10 µ, 6 V tantalum
C100,C102,
C104 . . . C118 = 120 n

Semiconductors:
D1 . . . D4 = 1N4001
(min. 50 V, 1 A)
IC1 = 7400
IC2 = 74161
IC3 . . . IC6 = 7490
N5 . . . N7 = IC7 = 7408
N24 . . . N26 = IC13 = 7408
N48 . . . N51 = IC19 = 7432
N55 . . . N62 =
= IC20,IC21 = 7404
N63 . . . N68 =
= IC22 = 7405
N69 . . . N72 =
= IC23 = 7401
IC31 = 7805 or. LM340
The ICs not given here will be listed in part 2.

Sundries:
Tr = mains transformer, 8 V/1 A
fuse = 500 mA slo-blo
X-tal = 4 MHz series-resonance crystal
S1 = SPDT (single pole change-over)

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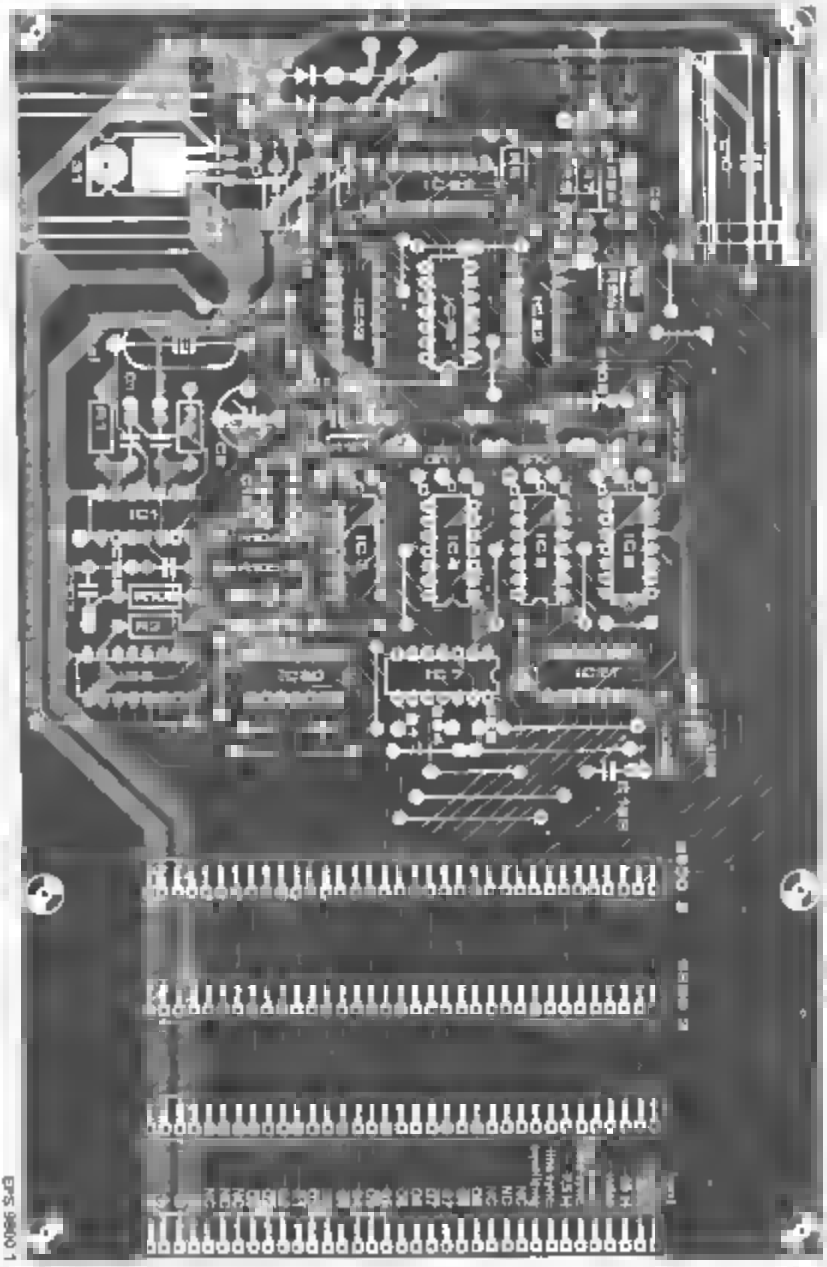


Figure 17. Printed circuit board and component layout for the circuits discussed in this article. This board also acts as a motherboard for the plug-in modules.

the supply lines is necessary, and this is shown in figure 16.

Printed circuit board

All the circuitry so far discussed is mounted on a printed circuit 'motherboard' to which the other modules are attached by wire links or by plug-in connectors, as will be discussed later. The p.c. board and component layout for the circuits so far mentioned, including the power supply, are given in figure 17.

Part 2 will give the 'missing parts' shown in the block diagram (figure 5): line blanking, line sync, field equalization, field sync, and burst enable. All these circuits will be mounted on one daughter board.

A second daughter board will be given in part 3. This contains all the necessary extension circuits for a pattern generator.

(to be continued)

C. Chapman

formant

the elektor music synthesiser (3)

Wiring to the keyboard contacts is largely eliminated by mounting the keyboard divider chain on p.c. boards directly behind the keyboard contacts, so that the 'tails' of the contacts can be soldered direct to the p.c. board. The wiring diagram of the keyboard divider boards is given in figure 1.

The p.c. board and component layout are given in figure 2. Each p.c. board covers one octave of the keyboard, so three p.c. boards are required. They are linked by butting together the ends and wiring across from one board to the next, terminal A to terminal A', B to B' and so on.

At the left-hand end of the keyboard points A to E are joined to the corresponding points on the interface p.c. board by short wire links. Since each keyboard divider p.c.b. has connections for only twelve sets of key contacts the extreme right-hand set of contacts (note 37) must be wired to the end of the p.c.b. as shown in figure 3. Note also the wire link between points B' and D'.

In order that the p.c. boards may be mounted directly behind the key contacts by glueing, the resistors and connections to the p.c.b.'s are on the copper side of the p.c.b.'s. This can clearly be seen in photo 1. All the resistors are, of course, 100 Ω 1% metal oxide types.

Selection of FET source resistors

As mentioned in the last article, the source resistors for FETs T1, T3 and T4 must be selected before the keyboard interface p.c.b. can be completed and tested. This is accomplished using the test circuit of figure 4a. With the gate grounded the gate-source voltage U_S is measured and a corresponding source resistor for each transistor is selected from table 1.

Table 1

U_S (V)	R_S (k Ω)
0.2	22
0.25	18
0.3 . . . 0.4	15
0.4 . . . 0.5	12
0.6 . . . 0.8	10
0.9 . . . 1.1	8.2
1.2 . . . 1.6	6.8

In the previous article the keyboard and keyboard interface circuits were described, together with the printed circuit board for the keyboard interface. In this article the p.c. board layout for the keyboard resistance divider is given, together with constructional details of the keyboard case. The description of the voltage-controlled module unit is then commenced, starting with the power supply and details of the module case.

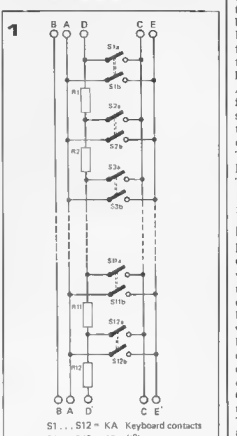


Figure 1. Circuit diagram of one keyboard divider p.c.b.

Table 1. Selection table for FET source resistors.

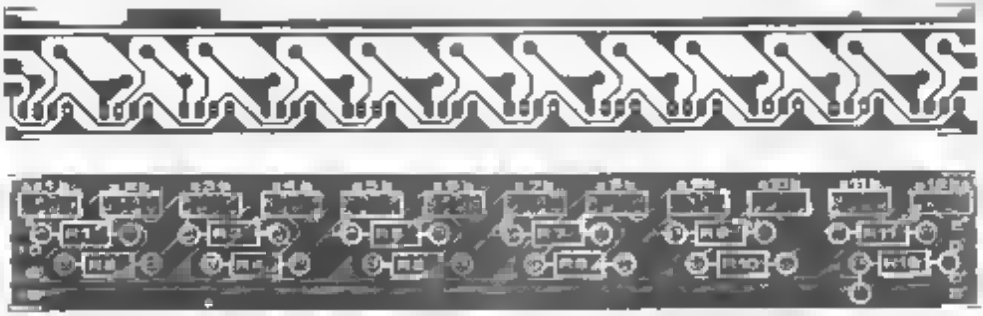
At the same time the gate leakage of each transistor should be checked to ensure that it is within acceptable limits. This is done by removing the grounding link across C_G (330 p). This capacitor will now charge through the gate leakage of the FET, and the source voltage will rise. The rate of change of voltage should be slower than one volt per second. Any FET which cannot meet this criterion should be rejected. This test should also be applied to T2, and when the tests are complete each FET, together with its selected source resistor, can be soldered into the circuit. Due to the possibility of leakage around the sample and hold area of the circuit (T1 to T3) great care should be taken to ensure that the back of the board is scrupulously clean, with no blobs of soldering flux or greasy thumbprints. After testing, the back of the board may be sprayed with insulating varnish.

Although the BF244 or BF245 is specified for T1 to T4, since practically all specimens of this device will function in the circuit, it is possible to use the cheaper and more popular 2N3819 for T2. It should be noted that the board is laid out for the pinning of the BF245. The pinning of the BF244 and most 2N3819's is different, as shown in figure 4b.

Interface receiver

In the early design stages the KOV and GATE outputs from the interface board were fed direct into the voltage controlled modules. However, it was soon discovered that the input currents taken by these modules caused significant voltage drops along the connecting cable between keyboard and module unit, especially if this was long. In particular, earth return currents along the common earth wire shared by the KOV and GATE outputs caused modulation of the keyboard voltage by the gate pulse. This problem was overcome by providing high impedance buffer stages at the receiving end of the connecting cable. The circuit for this 'interface receiver' is shown in figure 5. It consists simply of a 741 connected as a voltage follower for the KOV input, and a similar voltage follower with an input delay circuit for

2



the GATE input. The output of this circuit also drives an LED to indicate when a gate pulse is present.
A printed circuit board and component layout for the interface receiver are given in figure 6. The two outputs are taken from single screw terminal blocks cut from a "chocolate block" type of mains connector. This is so that connections to extra voltage controlled modules can be added if and when the system is extended.

Testing of the keyboard interface assembly

Once the keyboard interface (see part 1, figures 10 and 11) and interface receiver boards are complete they can be tested, provided a ±15 V supply is available; otherwise the testing must wait until the synthesiser power supply has been built. The final adjustment is not carried out until the keyboard assembly is mounted in its case, but these preliminary tests will show up any faults in the circuits and save a lot of frustration at a later stage. The test procedure is as follows:

1 Current consumption

Connect positive and negative supplies to the keyboard interface (part 2, figure 10) and measure the current flow in both the positive and negative supply leads. This should be between 18 and 25 mA.

2 Keyboard current source

a) Connect a multimeter between points B (positive) and D (negative) and monitor the current. This should be adjustable between 0.8 and 1 mA by means of P6.

b) Check the virtual earth point, pin 2 of IC2. The voltage between this point and the 0 V rail should be less than 5 mV with a 1 k resistor connected between points B and D.

3 Gate circuit

Connect point E on the interface board to point A via a switch and measure the voltage at point G with respect to 0 V. It should be −12 to −15 V with the switch open and +12 to +15 V with the switch closed.

Parts list to figure 2

Resistors:
R1 ... R12 = 100 Ω 1%

Miscellaneous:
S1 ... S12 = KA keyboard contacts

Note that a set board is required for each octave. For a three-octave synthesiser for instance three boards and 36 resistors are required. For further details see text, figures 1 and 3 and photos 1 and 2.

3

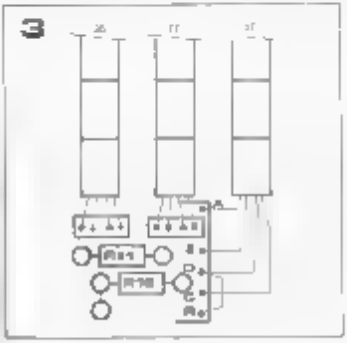


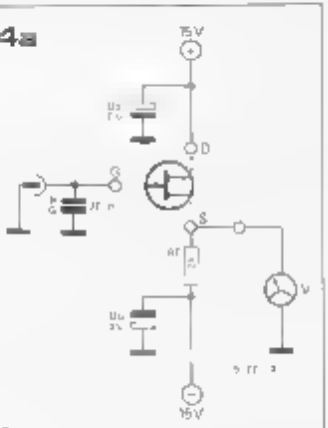
Figure 2. Printed circuit board and component layout for the keyboard (EPS 9721-4).

Figure 3. Showing the wiring to the 37th key contact block.

Figure 4. Test circuit for FET's and pinouts of BF244, BF245 and 2N3819.

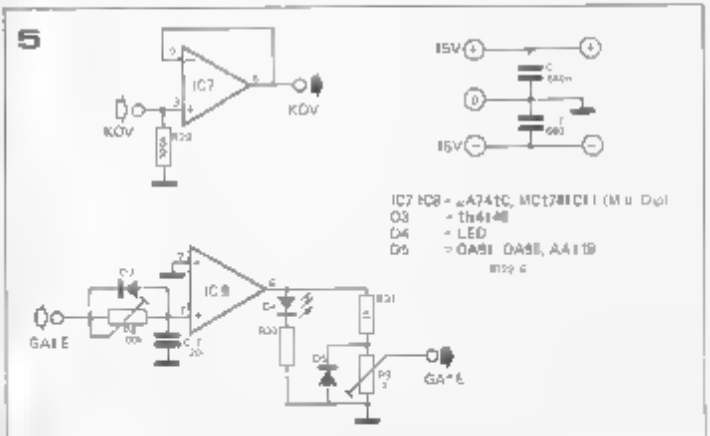
Figure 5. Circuit of the interface receiver.

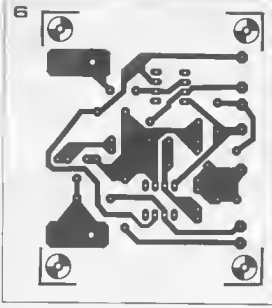
4a

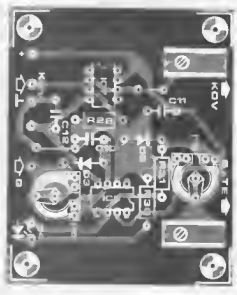


b

5







Parts List to figure 6

Resistors:
R29 = 100 k
R30,R31 = 1 k

Presets:
P8 = 100 k
P9 = 1 k

Capacitors:
C10 = 220 n
C11,C12 = 680 n

Semiconductors:
IC7,IC8 = µA741C,MC1741 CP1 (mini DIP)
D3 = 1N4148
D4 = LED e.g. TIL209
D5 = OA91,OA95,AA119

4. Sample and hold

a) Retain the switch from the previous test. Connect point C to an SPDT switch so that this point can be switched between point A and ground. With point C grounded, the gate switch closed and P1 set to minimum resistance the source voltage of T4 must be less than 4 V and should not change when the gate switch is opened.

b) Leave the gate switch open and ground point C using the SPDT switch. The source voltage of T4 must not change. Close the gate switch and the source voltage should now rise by between 3.6 and 4.6 V. Open the gate switch and this new voltage should be maintained.

Figure 6. Printed circuit board and component layout for the interface receiver (EPS 9721-2).

Figure 7. Mounting plate for the interface board.

Figure 8. a: Dimensions of the keyboard case. b: Exploded view of the keyboard case.

c) Set P1 to maximum resistance, changeover switch to ground point C and close the gate switch. The source voltage of T4 should now drop to its original value over two to three seconds.

5. Summing emplifier

a) Offset adjustment. Maintain the same switch positions as in test 4c. Using S1, switch P2 out of circuit and turn sliders of P3 and P5 to ground. Use P4 to set the KOV output to zero volts.

b) Coarse tuning. Switch P2 into circuit using S1 and turn P2 fully clockwise and then anticlockwise, when the KOV output should be +5 V and −5 V respectively.

c) Fine tuning. Switch P2 out of circuit and turn P5 fully clockwise, when the KOV output should be about 150 mV.

d) FM. Turn P5 fully anticlockwise. Link point FM to point A on the board. Using P3 it should be possible to vary the KOV output between zero volts and about 10 V.

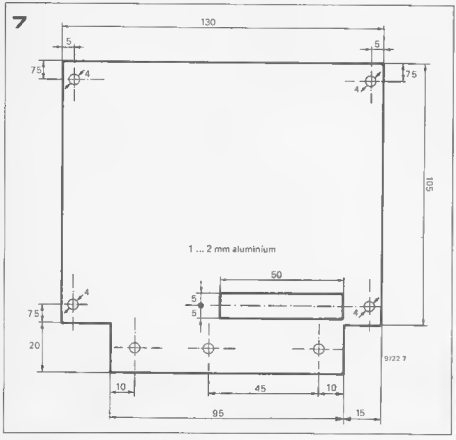
6. Interface receiver

Interconnect the interface and interface receiver boards (connections GATE, KOV, +15 V, −15 V and ground). Repeat tests 3 and 5b, but monitor the KOV and GATE outputs of the interface receiver. With the gate switch closed the indicator LED should glow. Finally, with the gate switch closed, use P9 to set the gate output voltage of the interface receiver to +5 V.

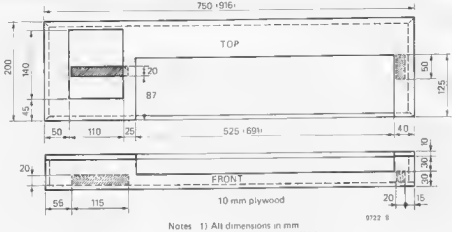
Keyboard unit assembly

Once the interface board has been tested, it and the keyboard can be joined to make an integrated keyboard unit.

This is accomplished by first making an aluminium mounting plate for the interface board, as shown in figure 7. The 'tongue' of this plate fits along the underside of the keyboard chassis (at the left-hand end) and is secured by three 4 mm nuts, bolts and lockwashers. A solder tag beneath one of the nuts

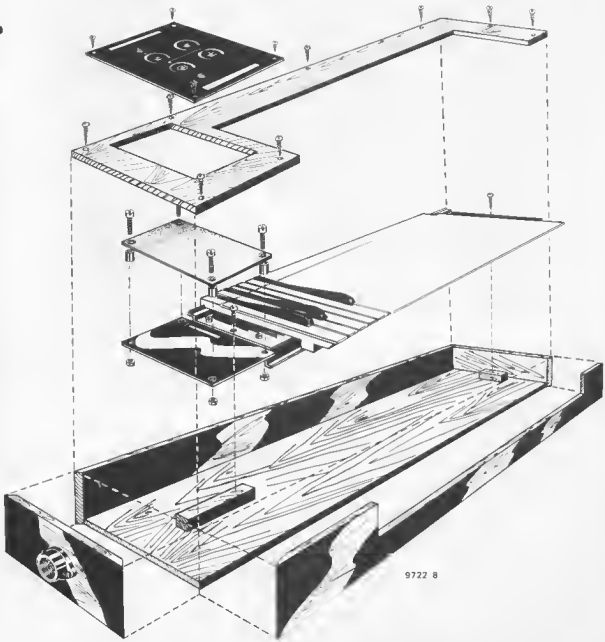


8a



Notes 1) All dimensions in mm
2) Normal dimensions valid for 3 octave Keyboard
3) Dimensions shown in brackets valid for 4 octave Keyboard

b



9

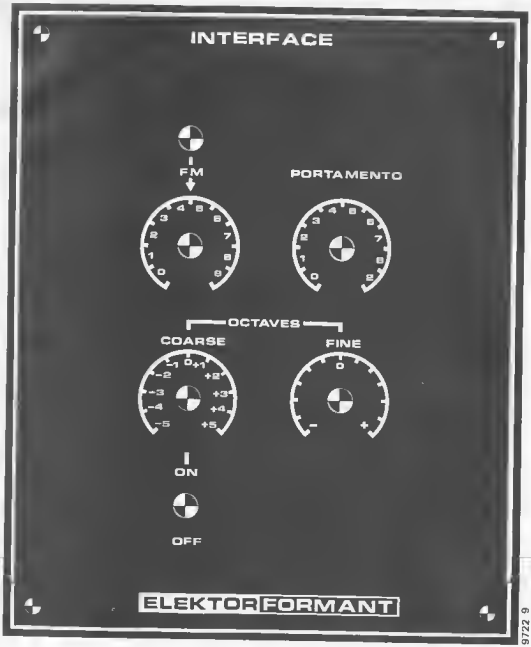


Figure 9. Interface board control panel.

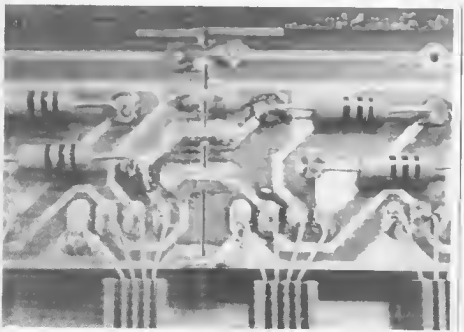
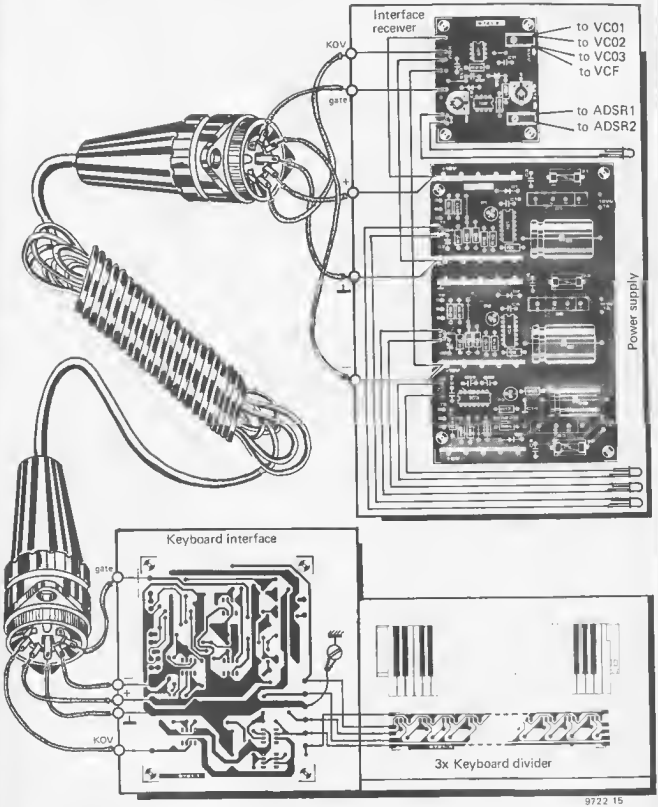
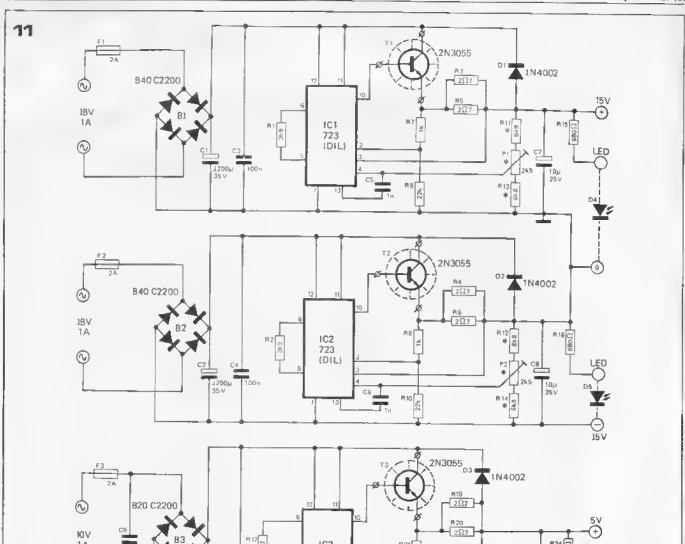


Figure 10. Showing the wiring between the keyboard unit, interface receiver and power supply.

Photo 1. Showing the wiring of the key contacts to the keyboard divider p.c.b.

10


Interface receiver
KOV
gate
to VC01
to VC02
to VC03
to VCF
to ADSR1
to ADSR2
Power supply
Keyboard interface
gate
KOV
3x Keyboard divider
9722 15



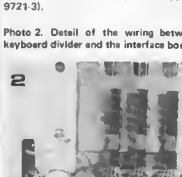
provides an earthing point for the keyboard. Note that the larger diameter hole in the tongue is not used yet; it will be required for mounting the keyboard in its case.

The next step is to mount the keyboard divider boards. As illustrated in photo 1, these boards should be interlinked in such a way that the ends of the boards actually touch at the junction, as otherwise the spacing of the contacts on the board with respect to the switch contact blocks will not be accurate. As described in part 2 (and illustrated in figure 2b), the contact blocks should be glued or bolted to a 3 mm thick plastic spacer (F). The keyboard divider boards can now also be mounted on this spacer, using either epoxy adhesive or double-sided self-adhesive tape ('Servotape', 'Tesatape' or similar). Note that the front of the divider boards should touch the contact blocks, as otherwise the wires from the blocks may be too short. The interface board can now be

Figure 11. Circuit of the Formant power supply.

Figure 12. Printed circuit board and component layout for the power supply (EPS 9721-3).

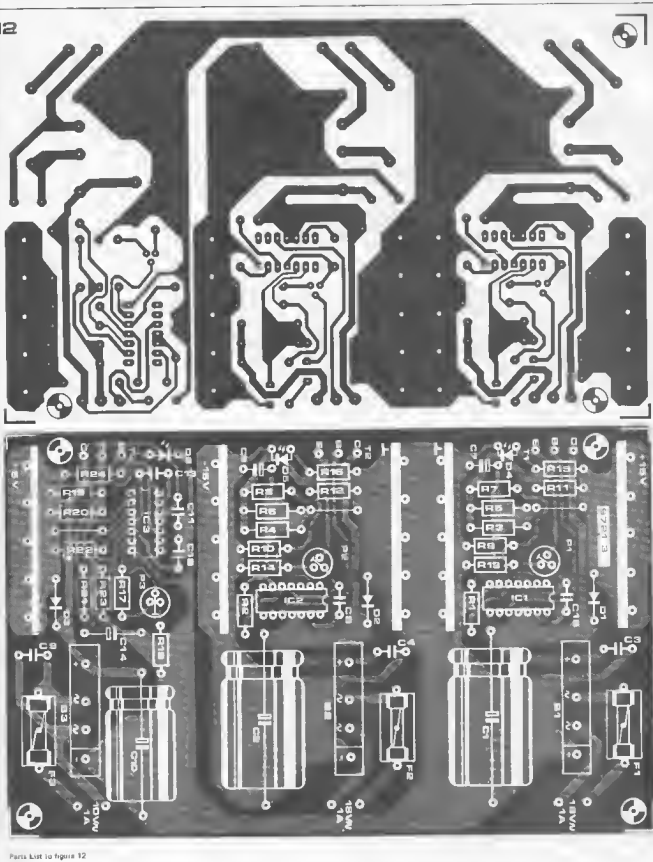
Photo 2. Detail of the wiring between the keyboard divider and the interface board.



mounted on top of its mounting plate using 4 mm nuts, bolts and spacers, and connections between the keyboard p.c.b.'s and the interface board are made by short wire links which pass through the rectangular slot in the mounting plate. The earthing point for the keyboard chassis is connected to point 'F' on the interface board. The complete assembly can be seen in photos 2 and 3.

Although the keyboard unit is now a single assembly it still requires a case to house it, and the dimensions of a suitable case are given in figure 8a. The materials should be chosen to suit the type of use (or abuse) to which the synthesiser will be subjected, and the choice is left to the individual constructor. However, the dimensions given in figure 8a are based on some assumptions, and if other materials are used the dimensions may have to be adjusted accordingly. The assumptions are that the baseboard is made of 10 mm ply-

12



Parts List to figure 12

Resistors
R1,R2 = 3k9
R3,R4,R5,R6,R19,R20 = 2k17/0.5 W
R7,R8 = 1 k
R9,R10 = 22 k
R11,R12,R13,R14 = 6k8
(2% metal oxide)
R15,R16 = 680 Ω
R17 = 2k7 (2% metal oxide)
R18 = 8k2 (2% metal oxide)
R21 = 2k2
R22 = 2k7
R23 = 15 k
R24 = 150 Ω

Presets:
P1,P2,P3 = 2k5 miniature (7 mm)
cermet

Capacitors.
C1,C2 = 2200 µ/35 V
C3,C4,C9,C11,C12 = 100 n
C5,C6,C13 = 1 n
C7,C8 = 10 µ/25 V tantalum
C10 = 2200 µ/16 V
C14 = 10 µ/16 V

Semiconductors:
D1,D2,D3 = 1N4002

D4,D5,D6 = LED (e.g. TIL 209)
T1,T2,T3 = 2N3055
IC1,IC2,IC3 = 723 (DIL)
B1,B2 = 40 V 2 2 A bridge rectifier
B40/C2200
B3 = 20 V 2 2 A bridge rectifier
B20/C2200

Miscellaneous.
F1,F2,F3 = 2 A slow blow fuse
Transformer(s) with 18 V, 18 V and 10 V
secondaries at 1 A
3 Heatsinks approx 100 mm x 50 mm
with 30 mm fins

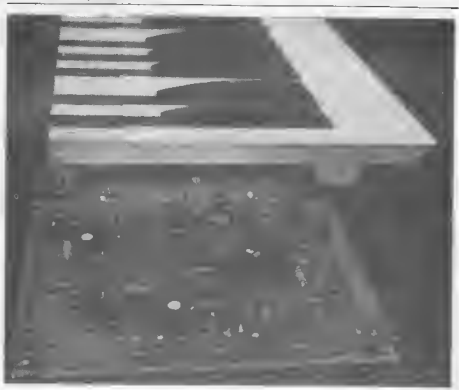


Photo 3. Showing the mounting of the interface board.

wood; that the top panel is also made of fairly thick plywood (10 . . . 15 mm) so as to leave room for the potentiometers above the interface board; that the side panels are made of plywood no thicker than 15 mm.

Particular note should be taken of the two wooden spacers glued to the bottom. These are required for mounting the finished keyboard assembly in the case.

Figure 8b is an 'exploded view' of the complete assembly, illustrating several of the points mentioned above. For screening purposes the inside of the case should be completely lined with thin aluminium or copper sheet or foil, which must be connected to ground.

A front panel layout for the interface controls is given in figure 9. This mounts directly over the interface board and is secured to the keyboard case by four chromium-plated woodscrews.

Potentiometers P1, P2, P3 and P5 (portamento, FM, coarse and fine tuning) are mounted on the front panel together with S1 and the FM input socket, which is a 4.5 mm jack. Connections between the front panel and the interface board should be made sufficiently long to enable the front panel to be removed without difficulty. If desired one edge of the front panel may be hinged for easy access to the interface board. The output and supply connections to the interface board are made by means of 5-pin DIN connectors, and a hole for the DIN socket should be cut in the side of the keyboard case adjacent to the interface board. The DIN-connectors should be high quality locking types, as the cheap plastic variety will quickly fail after repeated connecting and disconnecting.

Connections from the interface board to the DIN socket are shown in figure 10.

Power Supply

For final adjustment of the keyboard unit it is necessary to use the synthesiser's own power supply to ensure accurate setting of the volts/octave characteristic of the keyboard. For this reason the power supply circuit is now described.

Three output voltages are required for the synthesiser: +15 V, −15 V and +5 V. These must all be stable and easily adjustable, and for this reason all three supplies are based on the tried and trusted 723 precision voltage regulator IC. The circuit of the power supply unit is given in figure 11.

It will be noted that all three circuits are positive regulator circuits with an external power transistor to increase the output current. The −15 V supply is obtained simply by linking the positive output of this circuit to ground. This does have the slight disadvantage that separate transformer windings and rectifiers are required for each 15 V supply, but it does mean that both the positive and negative supplies are of identical design.

Each supply is equipped with foldback current limiting, and can comfortably supply over 800 mA, which should be adequate for any possible extension of the synthesiser. When limiting occurs (at about 1.2 A) the output voltage will fall and the current will fold back to about 500 mA with a short-circuited output. Current limiting of any of the outputs is indicated by the extinction of the LED indicator connected across that output.

A printed circuit board and component layout for the power supply unit are given in figure 12, and it should be noted that the output connections to T3 are different from those of T1 and T2, being arranged B-E-C instead of C-B-E. Good quality components should be used in the construction of the

Photo 4. The completed power supply board.

power supply and the power transistors should be mounted on generous heat-sinks, for example finned heatsinks of 100 mm x 50 mm with 30 mm high fins. The AC supplies to the stabilisers may be provided by a single transformer with multiple secondary windings (if available) or by a number of smaller transformers. In either case the transformer(s) should be generously rated, the one amp secondary current specified being the minimum acceptable.

Power supply connections to the voltage-controlled modules will be taken from the power supply by separate wires to each module. For this reason each power supply rail is equipped with a substantial connection 'busbar'. These are made from copper strip or pieces of copper laminate board, and are soldered to terminal pins pushed through the p.c. board. This arrangement can clearly be seen in photo 4.

Once the power supply unit has been built the output voltages can be set to their correct values. The −15 V supply should be adjusted to within 1% of its nominal value using a DVM, since the accuracy of this supply voltage has a direct bearing on the volts/octave characteristic of the keyboard. The +15 V and +5 V supplies need only be set to within 3% of their nominal values.

Keyboard calibration

Once the synthesiser's own power supply has been tested and adjusted the offset compensation and volts per octave characteristic of the keyboard can be adjusted. The keyboard interface, interface receiver and power supply are connected as shown in figure 10.

Offset compensation

The overall tuning is switched off (S1 'off', i.e. position b). Depress the lowest key of the keyboard and hold it down while adjusting P4 so that the KOV output of the interface receiver is zero.

Volts/octave characteristic

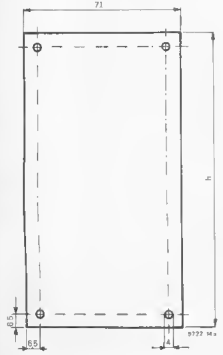
This should be adjusted to an accuracy

13

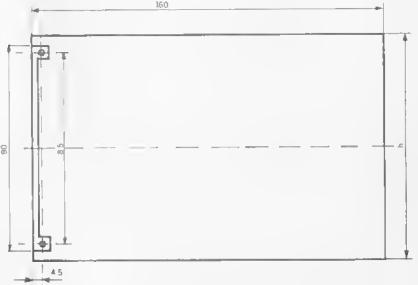
Figure 13. A suggested layout for a 'basic' synthesiser in a home-constructed module housing.

Figure 14. The dimensions of the Formant modules are compatible with the Eurocard rack system.

14a



b



all dimensions in mm

Panel	h mm
small	3 U = 132,6
large	6 U = 265,9

Board	h mm
small	100
large	200

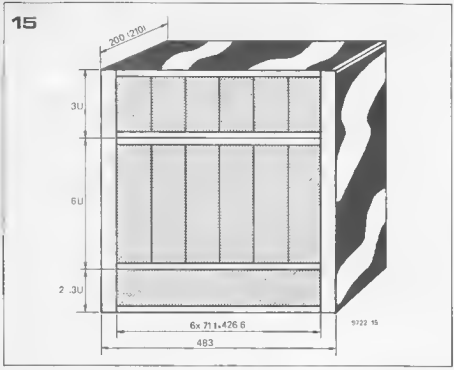


Figure 15. A case containing one 6U and one 3U rack will accommodate six large and six small Formant modules. (It can be useful to add a 2U or 3U bottom panel (using a larger case!), behind which amplifiers etc. can be mounted.

of at least 1% using a DVM. The overall tuning remains switched off. The KOV output is measured and P6 is adjusted so that alternately depressing keys one octave apart causes the KOV output to change by exactly one volt. The Formant keyboard is now compatible with any synthesiser that uses a standard 1 V/octave keyboard.

Finally, the offset compensation should again be checked and readjusted if necessary.

Gate delay

Accurate adjustment of the gate delay is not possible until the voltage controlled modules have been constructed, but an approximate adjustment will suffice until that time. P7 on the interface board should be set to about one quarter of its maximum resistance, and P8 on the receiver board should be set to minimum.

Modular construction

A modular method of construction was chosen because it allowed the greatest flexibilty in the final design. Each voltage-controlled circuit is constructed on its own p.c. board which plugs into a socket in the module housing that supplies power, control voltage and gate pulses. Interconnections between modules are made by means of patch cords.

The advantage of this system is that the synthesiser can be made as simple or as complex as is required. Provided sufficient space is left in the module housing for additional modules, it is possible to build a playable instrument with just a small number of modules, and to extend it as when desired. This also means that every instrument can be tailored to the individual constructor's taste and is not fixed within rigid limits set by the designer. However, for those who require a little more guidance as to the right 'mix' of modules that should be adopted, a suggestion for a 'middle-of-the-road' instrument is given in figure 13. This utilises three VCO modules, one VCF, one dual VCA module, two ADSR envelope shapers, one LFO module and one noise module.

The module printed circuit boards and front panels are compatible with the Eurocard rack system. Two module heights are employed in Formant. A double-height (6U) module is used for the voltage-controlled modules (VCO's, VCA's and VCF's) while a single-height (3U) module is used for the ancillary circuits (envelope, shapers, noise generator etc.).

The basic dimensions of the modules are given in figure 14. The Eurocard rack system operates on a card spacing of 5.08 mm (0.2") or multiples thereof. Each Formant module occupies a panel width of approx. 71 mm, so the 426.7 of panel width available will accommodate six modules. A 6U rack and a 3U rack stacked together will thus accommodate six large and six small modules, as shown in figure 15, so if the proposed instrument is built this will leave space for one large and one small module to be added later.

Of course some readers, especially those with previous experience of synthesisers, may already have a firm idea of the type of instrument they wish to build, and may like to construct a purpose-built case of wood or some other material. This is quite permissible, as the module housing does not require screening.

Coming soon

Electronics on the verge.....

Biofeedback

Para biometrics

Psycho phenomena

Relaxation generator

slotless model car track part 4

Having described the servo amplifier in the previous article, the motor speed controller is discussed. This is followed by a description of the 'prop tester', which can be used to test servo amplifiers and motor controllers.

Readers may be wondering why no p.c. board layout has been given for a receiver, a description of which was given in the first article of the series. The reason is that the prototype receiver left something to be desired in terms of sensitivity and ease of tuning, and in consequence has been slightly redesigned. While the new design was being perfected it was felt preferable to start with the 'business end' of the car electronics and work backwards to the receiver, rather than giving a p.c. board for an imperfect circuit.

Motor Speed Control

The speed of the car drive motor is varied by altering the motor current. As the circuits must be fairly miniaturised it is not possible to use a series regulator transistor to vary the supply voltage to the motor, since this would dissipate too much power and would require a large heatsink. Pulse width control of the motor is therefore employed, which means that the motor is switched on at full power for some of the time, and switched off for some of the time, the on/off ratio depending on the position of the speed control joystick. The average motor current and hence the motor speed also varies proportionally to the on/off duty-cycle.

The advantages of this system are that the motor switching transistor is either saturated or turned off, and thus dissipates little power, and that the motor is always driven at full power, so the maximum torque is available, for example, when starting.

The principle of the system is shown in figures 1A to 1C. The upper waveform in each case represents the motor speed control pulse for a particular car, picked out of the multiplex pulse train that controls all the cars. As has already been discussed with reference to the multiplex encoder and servo amplifiers, control is effected by varying the pulse width between one and two milliseconds. The motor speed controller converts this into a drive pulse to the motor that varies from no pulse (figure 1A) through a pulse with a 50% duty-cycle (motor at half speed, figure 1B) to full power applied to the motor all the time (figure 1C).

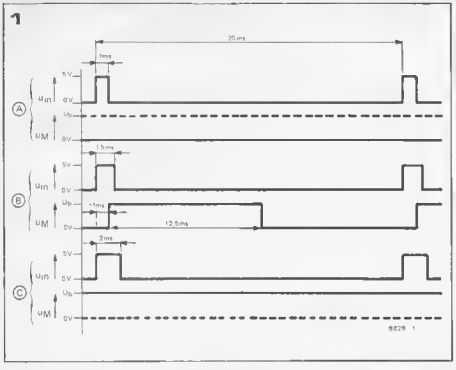
Block Diagram

A block diagram of the motor speed controller is shown in figure 2. Control pulses from the multiplex decoder are fed to an inverter, whose output is used to trigger a reference monostable (M1) that gives an output pulse of 1.1 ms duration. The inverted control pulses, together with the monostable output pulses, are fed to the two inputs of a NOR gate. This produces an output pulse whose length is the difference between the control and reference pulses as shown in figures 3A to 3C. In figure 3A the control pulse is shorter than the reference pulse, so the NOR gate output remains permanently low. In figure 3B the control pulse is longer than the reference pulse and the NOR gate output remains high for 400 μs, while in figure 3C the control pulse is at its maximum and the NOR gate output remains high for 900 μs.

The next stage of the circuit consists of two current sources I_L and I_E, and a voltage comparator. I_L provides a constant charging current for C3, but I_E, which discharges C3, is switched on when the NOR gate output is high, and off when it is low. I_E is approximately thirty times I_L, which is an important point to note.

When the NOR gate output is permanently low (control pulse less than 1.1 ms) I_E will be turned off and C3 will charge to a voltage greater than U_{ref}. The comparator output will thus be high and the motor drive amplifier (MDA) will be switched off. When the NOR gate output is high for its maximum period of 900 μs (control pulse length 2 ms), C3 will discharge to zero with a current I_E during this period, the comparator output will go low and the motor will be switched on. During the interval between control pulses (23 . . . 24 ms) C3 will be recharged at a current I_L. However, the voltage on C3 will never exceed U_{ref}, so the motor will remain switched on until the next control pulse arrives.

At intermediate settings of the speed control lever, C3 will not discharge quite so far during the high output period of the NOR gate. During the interval between control pulses there-



fore, the charging current I_L will charge C3 above U_{ref}, and the motor will switch off before the arrival of the next control pulse.

This effect is clearly illustrated in figures 4a to 4f. Figures 4a and 4b show the normal and inverted versions of the control pulse, varying between one and two milliseconds, while figure 4c shows the reference pulse. Figure 4d shows the NOR gate output pulse varying between zero and 900 µs. Figure 4e shows the corresponding discharge and charge times for C3, and the comparator output.

It is evident from this diagram that, as the length of the control pulse increases, C3 discharges to a lower potential and thus takes a correspondingly longer time to re-charge to the point at which the comparator output goes high and the motor turns off.

Figures 5 to 9 show some oscillograms taken from the prototype, which further illustrate the operation of the circuit and may prove useful should any faultfinding be necessary. The circled letters refer to the corresponding waveforms in figure 4. Figure 5 shows the control pulse and capacitor voltage with a control pulse length of 1 ms, while figures 6 and 7 show the capacitor waveforms as the control pulse length is increased. Figures 8 and 9 show the capacitor waveforms and the comparator outputs corresponding to figures 6 and 7.

Figure 1. The motor controller converts the 1·2 ms variation of the control pulse width into a motor drive pulse whose duty-cycle varies from 0 to 100%. The average motor current, and hence the motor speed, also varies from 0 to 100%.

Figure 2. Block diagram of the motor controller. After each reference pulse C3 is discharged for a time equal to the difference between the control pulse and the reference pulse at a current I_E · C3 then charges at a current I_L until the comparator threshold is exceeded, during which time the motor runs.

Figure 3. A NOR gate compares the inverted control pulse with a reference pulse and gives an output pulse equal to the difference between the two.

Figure 4. Showing how the discharge and charge times of C3, and hence the motor drive pulse width, vary with the control pulse width.

Figure 5 to 9. Oscillograms illustrating the operation of the motor controller. The circled letters refer to the same waveforms in figure 4.

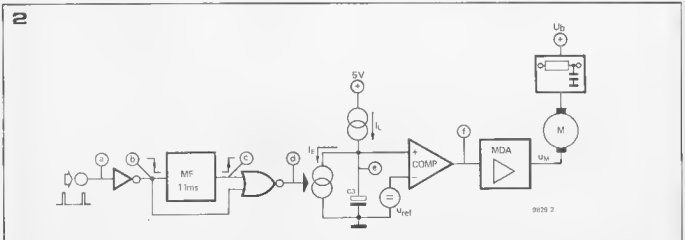
Suppression

One part of the block diagram remains to be explained, and this is the suppression circuit for the motor. Good suppression is essential, as any spikes occuring on the supply line could cause faulty operation of the receiver, multiplex decoder, servo amplifier, or the motor controller itself. The suppression circuits which will be described should be adequate for even the (electrically) noisiest motors.

Complete Circuit

Figure 10a shows the complete circuit of the motor speed controller. T1 is the input inverter, which also acts as a high impedance buffer for the multiplex decoder output, since this circuit can supply only a small output current. The output pulse from the collector of T1 is differentiated by C1 and R4 to give a series of spikes to trigger monostable T1/T3, D1 ensuring that triggering occurs only on the negative-going spikes. Outputs from the collectors of T1 and T3 are also taken to the inputs of the NOR gate comprising T4 and T5. T1 to T5 are contained in a CA3086 transistor array IC.

The I_E constant current source is constructed around T6, and is switched on only when the NOR gate output is high (T4 and T5 turned off) when current will flow through R12, R13, D2 and D3 to provide a positive base bias for T6. The I_L current source is built around T7 and provides a continuous constant current of around 600 µA. This current determines the slope of the charging ramp, i.e. angle φ in figures 8 and 9. Because of component tolerances it may be necessary to vary this current by experimenting with the value of R15.



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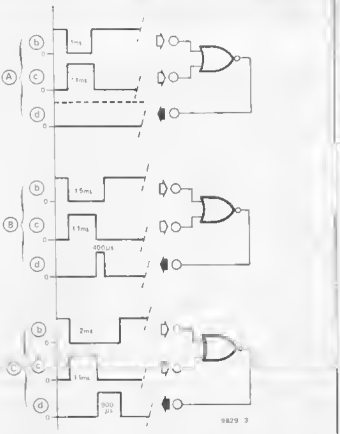

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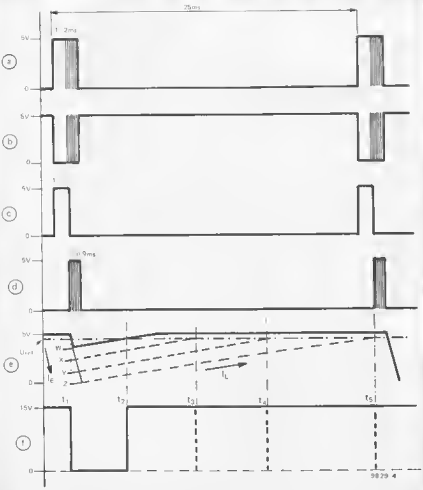

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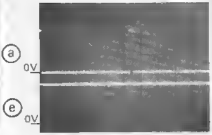

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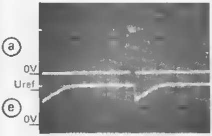

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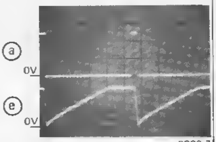

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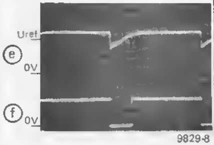

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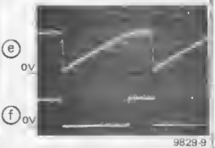

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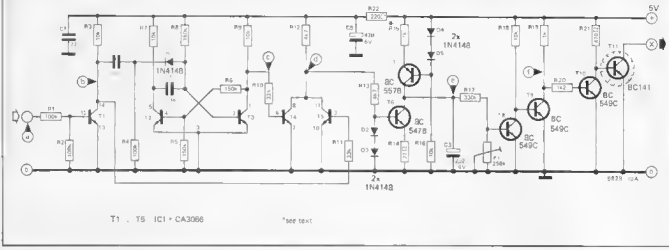
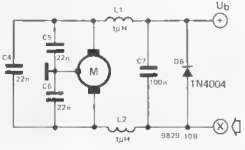
10a



10b



10c

The comparator comprises T8 and T9, the reference voltage being provided by the base-emitter 'knee' voltage of T8. The threshold voltage of the comparator may be adjusted by means of P1.

The motor drive amplifier comprises T10 and T11, T11 being the output transistor that carries the motor current. As this transistor has an open collector, i.e. it is not committed to the +5 V supply rail, the motor supply voltage connected to the racetrack can be chosen to suit any motor with which the cars are fitted.

Motor Suppression

Good motor suppression is vital, and no attempt should be made to skimp on this part of the circuit. The motor suppression components are shown in figure 10b. The chokes and capacitors provide r.f. suppression, while D6 short circuits the back e.m.f. of the motor, which performs the dual function of protecting T11 and providing motor braking.

The suppression components should be soldered as close as possible to the motor terminals, as shown in figure 10c. Note that the junction of C5 and C6 is connected to the motor case. This suppression circuit should be adequate for most motors which are of reasonable quality and in good condition, but if extra suppression is required L1 and L2 may be increased to 10 μH. Note that these chokes must be capable of handling the full motor current (which can be up to 1 A) and should have a low resistance so that no significant voltage is dropped across them, as this would reduce the motor power.

P.C. Board

Figure 11 shows a p.c. board and twice fullsize component layout for the motor speed controller. The p.c.b. is of miniature construction, like the servo amplifier, and the same comments apply as regards assembly. T11 requires only a small cooling clip, which can be made from any odd scrap of copper or brass shim.

Parts List to figure 11

Resistors.
R1,R2,R4 = 100 k
R3,R7,R9,R16,R18 = 10 k
R5,R6,R8 = 150 k
R10,R11 = 33 k
R12,R13 = 4k7
R14 = 27 Ω
R15,R19 = 1 k
R17 = 330 k
R20 = 1k2
R21 = 470 Ω
R22 = 220 Ω
P1 = 250 k, lin preset

Capacitors:
C1 = 1 n ceramic disc
C2 = 10 n MKM
C3 = 2µ2/6 V tantalum bead
C4,C5,C6,C8 = 22 n ceramic disc
C7 = 100 n MKM
C9 = 47 µ/6 V tantalum

Semiconductors:
IC1 = T1 . . . T5 = CA3086
T6 = BC547 B or equ.
T7 = BC 557 B or equ.
T8,T9,T10 = BC549 C or equ.
T11 = BC141
D1,D2,D3,D4,D5 = 1N4148
D6 = 1N4004

Miscellaneous:
L1,L2 = 1µH heavy-duty choke

Figure 10a. Complete circuit of the motor controller.

Figure 10b. The motor suppression circuit, which cuts down interference pulses from the motor, and also protects the controller output transistor.

Figure 10c. The motor suppression components must be soldered as close as possible to the motor terminals.

Figure 11. Printed circuit board and component layout for the motor speed controller.

Figure 12. Block diagram of the 'prop tester', which can be used to test many types of servo amplifiers and motor speed controllers.

Figures 13 and 14. Showing the waveforms at various points in the prop tester circuit.

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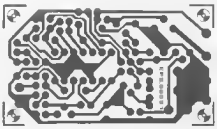

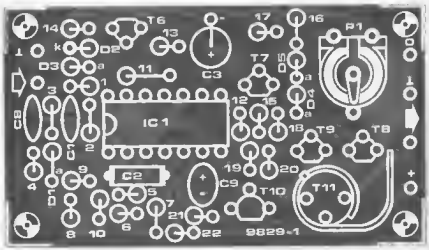

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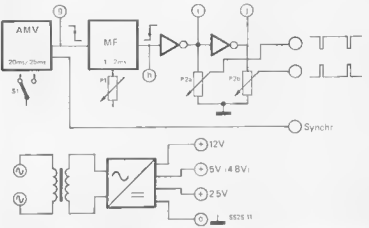

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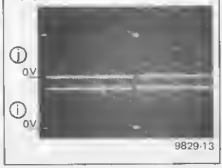

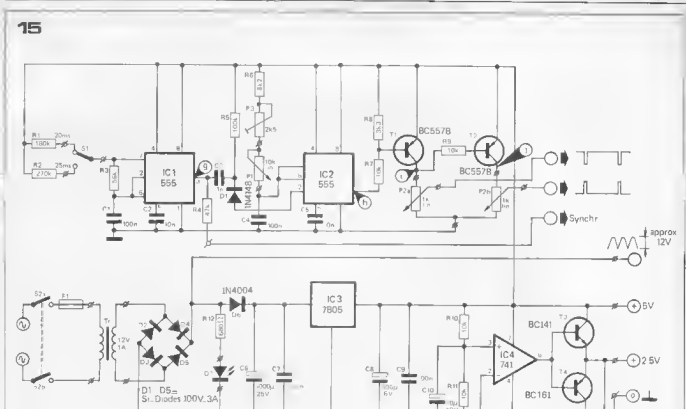

The Prop Tester

In order to test and adjust the servo amplifier and motor speed controller without the need to connect up the entire transmitter/receiver system, a simple proportional tester has been developed. In addition to testing the Elektor circuits this can be used with any commercial servo amplifiers and speed controllers that operate on the same principle.

A block diagram of the tester is given in figure 12. It consists of an astable multivibrator whose period can be switched between 20 ms and 25 ms. The negative-going edge of the output waveform triggers a monostable whose pulse width can be varied from one to two milliseconds by means of P1. Normal and inverted versions of the monostable pulse are provided for feeding to the circuits under test, and the output level of these can be adjusted to find the threshold level of the circuit. A sync output for an oscilloscope is also provided.

A centre-tapped, stabilised 5 V supply is provided to power the circuit under test, together with an unstabilised 12 V output to power the car drive motor. Figures 13 and 14 show the waveforms at various parts of the circuit.

The circuit of the prop tester is given in figure 15. The astable and monostable are built around two 555 timers, while the inverters are T1 and T2. A 7805 IC regulator provides the 5 V stabilised supply, and IC4, T3 and T4 provide the low impedance centre tap.

Adjustment of the Prop Tester

An oscilloscope is extremely useful for adjustment of the prop tester. If a 'scope' is available, then all that is necessary is to use P3 to adjust the output pulse width to 1.5 ms, with P1 set in its centre position.

If no oscilloscope is available then the prop tester can be calibrated with sufficient accuracy using a steering servomechanism in conjunction with the servo amplifier for the car race track. The servo and servo amplifier are connected up and the input of the servo amplifier is connected to the shder of P2b in the prop tester. Before applying power P1 and P3 of the prop tester are set to their centre positions and P2 is set to give maximum output. S1 is set to the 25 ms position. Power is then applied and the servo should move to a position proportional to the pulse width. By adjusting P3 the servo can be set to its centre position, when the control pulse width will be approximately 1.5 ms. P3 can now be scaled linearly 1 to 2 ms, while P2 can be scaled 0 to 5 V.

Testing the Servo Amplifier

Once the prop tester has been adjusted it can be used fully to test the servo amplifier and the motor speed controller. When testing the servo amplifier, first turn P1 in the prop tester to its extreme left- and right-hand positions. If it is found that the control horns of the servo hit the end stops before these settings are reached then it will be necessary to reduce the value of R8 and R16 in the servo amplifier from 5k6 to 4k7. Each servo amplifier must be matched to the particular type of servo with which it is to be used.

Figure 15. Complete circuit of the prop tester.

Figure 16. Printed circuit board and component layout for the prop tester (EPS 9829-2).

Response Threshold

The next step in the test procedure is to rotate P1 of the prop tester back and forth, at the same time reducing the control pulse amplitude by means of P2, until the servo ceases to respond. The servo amplifier should not fail to respond until the control pulse amplitude has fallen below 2.5 V.

Adjustment of the Motor Controller

The motor speed controller and motor are connected to the prop tester and P1 is set to 1 ms. Preset P1 of the motor speed controller is set to its centre position, and power is applied to the circuit. The motor should remain stationary. P1 is next set to 2 ms, when the motor should start. Preset P1 is now adjusted until the motor runs at the

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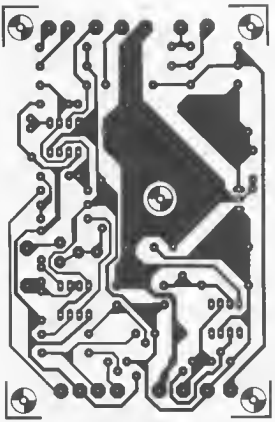

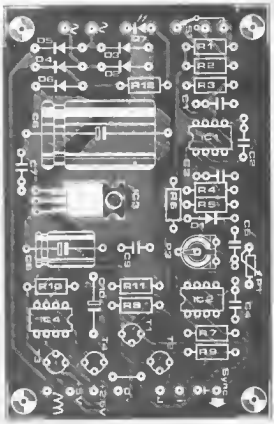

Parts List to figure 16

Resistors:
R1 = 180 k
R2 = 270 k
R3 = 56 k
R4 = 47 k
R5 = 100 k
R6 = 8k2
R7 R9,R10,R11 = 10 k
R8 = 3k3
R12 = 680 Ω
P1 = 10 k lin pot
P2 = 1 k lin stereo pot
P3 = 2k5 preset

Semiconductors:
IC1,IC2 = 555
IC3 = 7805 IC regulator
IC4 = 741
T1,T2 = BC557B or equ.
T3 = BC141
T4 = BC161
D1 = 1N4148
D2,D3,D4,D5 = Si-diode, 100 V/3 A
D6 = 1N4004
D7 = LED

Capacitors:
C1,C4,C7,C9 = 100 n MKM
C2,C5 = 10 n ceramic disc
C3 = 1 n ceramic disc
C6 = 1000 µ/25 V
C8 = 100 µ/6 V
C10 = 10 µ/10 V

Miscellaneous:
S1 = SPDT switch
S2 = DPST mains switch
Tr1 = transformer 12 V/2 A
F1 = 100 mA slow-blow fuse
Fuseholder

maximum desired speed. It should be noted that, if a 12 V motor is used, this will occur when the duty-cycle of the drive pulses approaches 100%. If a lower voltage motor is used then full speed will be achieved at a lower duty-cycle. With lower voltage motors care should be taken not to overload the motor while making this adjustment.

Potentiometer P1 is now returned to 1 ms and is then turned slowly clockwise. The motor should begin to run (under no load conditions) by the time P1 has reached the 1.3 ms mark.

Because of component tolerances it is possible that the motor may run erratically when set to maximum speed. This is due to the charging current of C3 being too low, and may be cured by reducing the value of R15 to 820 Ω. K

market

Portable direct-writing recorders

A new range of portable direct-writing recorders combining precision pen-motor techniques with thermal writing is available from Gould Advance Ltd.
The Gould Allco 8000 Series recorders use the high-contrast thermal writing technique and are suited to a broad range of industrial, scientific and bio-medical measurement applications. The recorders are ideal for unattended operation, and retain good trace quality at the lowest speeds.

The 8000 Series includes six basic models with one, two, three, four, six and eight channels, with a choice of eight pushbutton-selected chart speeds ranging from 5 mm/min to 100 mm/s. All models can be supplied with or without preamplifiers, in a portable case or in a rack-mounted configuration.
Interchangeable plug-in signal conditioners provide a wide measurement range, and include a true root-mean-square level convertor, a thermocouple amplifier with calibrated zero suppression, a basic pre-amplifier with full-scale ranges from 50 mV to 500 V, a frequency-deviation convertor with centre frequencies of 50, 60 and 400 Hz, and a DC bridge pre-amplifier which also functions as a microvolt amplifier.
All the signal-conditioning modules have fully floating input circuits for operation at up to 500 V off-ground at any sensitivity. High common-mode noise rejection allows operation in noisy environments with grounded, fully floating or off-ground signal sources.
The recorders without pre-amplifiers accept direct inputs from external signal sources in the 0 - 5 V DC range. The input circuits are still floating and operate to 500 V off-ground.
Full-scale pen position controls are standard. Channel width is 50 mm (40 mm for eight channels). A new servo-controlled penmotor is used to give a rectilinear trace of 99.5% linearity, with a frequency response of 50 Hz at 40 mm and 100 Hz at 10 mm.
The recorders will operate in any position and in moving vehicles. A 12 V battery option is available in addition to 50 or 60 Hz mains operation. The chart drive may be controlled from the front panel or remotely, and event and time markers are standard.

Gould Advance Limited, Raynham Road, Bishop's Stortford, Herts, CM 23 5 PF.

(510 M)

Triple-output modular power supply for microprocessors

A new, triple-output power supply from Hewlett-Packard is designed specifically to power OEM microprocessor systems that need independently adjustable and isolated voltages. The fully enclosed HP 62312D supply simultaneously provides three outputs with a wide latitude of voltage combinations for most commonly used microprocessors. The main output is rated at 4.75 V to 5.25 V at 3 A, while the other two each range from 4.75 V at 0.38 A to 12.6 V at 0.6 A. All outputs are isolated from each other and from the chassis, providing the user a wide selection of polarities. These output ratings are obtained at up to 40°C, but the supply may be operated up to 70°C with derating. Output effects for source and load are listed as 0.1 percent respectively. Periodic and random deviation is 1 mV rms, 3 mV p-p; 20 Hz to 20 MHz. The supply also features remote programming terminals to control the main 5 V output for margin testing.
Input voltage taps can be changed by the user to cover the range of 104 V AC to 127 V AC or 208 V AC to 250 V AC at 48 to 63 Hz. Protection features include an internal AC fuse, fixed fold-back current limit and standard overvoltage protection on the main 5 V output (optional on the other two outputs).
OEM price for the Hewlett-Packard 62312D triple-output power supply is £83 each in quantities of 100.

Hewlett Packard Ltd., King Street Lane, Winnersh, Wokingham, Berkshire, RG11 5AR.

(518 M)

Gas Detector

A range of instruments for the detection of accumulations of inflammable gas in the atmosphere, have been announced by ANACON Instruments Ltd. Based on new versions of the Taguchi semiconductor gas sensor, these instruments utilize modern circuit techniques which result in the reliable detection of gas concentrations which are well below explosive limits; that is, below 20% L.E.L. Further, the instruments can be preset to alarm at the extremely low levels demanded by safety in the presence of toxic inflammable gases such as carbon monoxide. The first instruments to be offered are the battery-operated hand-held versions, types 720 and 730. The smallest is the palm-sized 720, which has only an ON-OFF switch, and a push-button for testing the electronic alarm circuit. It contains a rechargeable Ni-Cd cell which powers the sensor for some 3 hours; and a 9-V battery which will run the electronics for up to a year of normal usage. This instrument is designed for the protection of those persons who must occasionally enter areas where gas might be present.
The model 730 is rather larger, though still hand-held, and incorporates a battery condition meter which indicates the state of charge of the (larger) Ni-Cd cell. It also has a two-position switch which makes it partially selective to either hydrocarbons such as North Sea gas (methane), or light gases such as carbon monoxide.
A third model type 750 is a mains-operated 'GASTEC' which can be permanently mounted in appropriate areas in industrial, commercial or domestic premises, and will audibly indicate the presence of an inflammable gas. Although an audible alarm is mounted on the instrument panel itself, one or more slave alarms can be positioned in other rooms of the building. The top-of-the range model 750 includes audible and visual indication of both sensor *and* mains failure; and will run off its own internal supply for over an hour in the event of such a mains failure. This model can also be used as a gas concentration alarm in plants where potentially hazardous mixtures of inflammable gases are used as part of the industrial process.

Anacon Instruments Ltd., St. Peters Road, Maidenhead, Berks. SL6 7QA

(477 M)