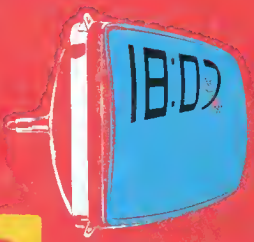
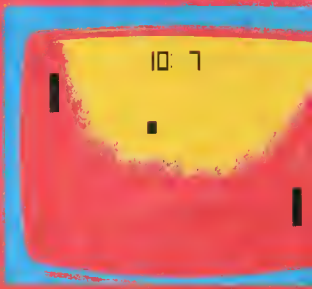
up-to-date electronics for lab and leisure

ELEKTOR 18

Time on TV
Score on TV
Loud mouth





October 1976 40p

elektor decoder

What is a TUN?
What is 10 n?
What is the EPS service?
What is the TQ service?
What is e missing link?

Semiconductor types

Very often, e large number of equivalent semiconductors exist with different type numbers. For this reason, 'abbreviated' type numbers are used in Elektor wherever possible:

- '741' stands for µA741, LM741, MC741, MIC741, RM741, SN72741, etc.
- 'TUP'or 'TUN' (Transistor, Universal, PNP or NPN respectively) stands for any low frequency silicon transistor that meets the specifications listed in Table 1. Some exemples are listed below.
- 'DUS' or 'DUG' (Diode, Unwersal, Silicon or Germanium respactively) stands for any diode that meets the specifications listed in Table 2.
- 'BC107B', 'BC237B', 'BC547B' all refer to the same 'family' of almost identical better-quality silicon transistors. In general, any other mamber of the same family can be used instead. (See below.)

For further information, see 'TUP, TUN, DUG, DUS', Elektor 17, p. 948.

Table 1. Minimum specifications for TUP (PNP) and TUN (NPN).

$V_{CEO,max}$	20V
$I_{C,max}$	100 mA
$h_{FE,min}$	100
$P_{tot,max}$	100 mW
$f_{T,min}$	100 MHz

Some 'TUN's are: BC107, BC108 and BC109 families; 2N3856A, 2N3859, 2N3860, 2N3904, 2N3947, 2N4124.
Some 'TUP's are: BC177 and BC178 families; BC179 family with the possible exception of BC159 and BC179; 2N2412, 2N3251, 2N3906, 2N4126, 2N4291.

Table 2. Minimum specifications for DUS (silicon) and DUG (germanium).

	DUS	DUG
$V_{R,max}$	25V	20V
$I_{F,max}$	100mA	35mA
$I_{R,max}$	1µA	100µA
$P_{tot,max}$	250mW	250mW
$C_{D,max}$	5pF	10pF

Some 'DUS's are: BA127, BA217, BA218, BA221, BA222, BA317, BA318, BAX13, BAY61, 1N914, 1N4148.
Some 'DUG's are: OA85, OA91, OA95, AA116.

BC107 (-8, -9) families:
BC107 (-8, -9), BC147 (-8, -9),
BC207 (-8, -9), BC237 (-8, -9),
BC317 (-8, -9), BC347 (-8, -9),
BC547 (-8, -9), BC171 (-2, -3),
BC182 (-3, -4), BC382 (-3, -4),
BC437 (-8, -9), BC414

BC177 (-8, -9) families:
BC177 (-8, -9), BC157 (-8, -9),
BC204 (-5, -6), BC307 (-8, -9),
BC320 (-1, -2), BC350 (-1, -2),
BC557 (-8, -9), BC251 (-2, -3),
BC212 (-3, -4), BC512 (-3, -4),
BC261 (-2, -3), BC416.

Resistor and capacitor values

When giving component values, decimal points and large numbers of zeros are avoided wherever possible. The decimal point is usually replaced by one of the following international abbreviations:

p	(pico-) =	10^{-12}
n	(nano-) =	10^{-9}
µ	(micro-) =	10^{-6}
m	(milli-) =	10^{-3}
k	(kilo-) =	10^{3}
M	(mega-) =	10^{6}
G	(giga-) =	10^{9}

A few examples:
Resistance value 2k7: this is 2,7 kΩ, or 2700 Ω.
Resistence value 470: this is 470 Ω.
Capacitance value 4p7: this is 4,7 pF, or 0,000 000 000 004 7 F .
Capacitance value 10 n: this is the international way of writing 10,000 pF or .01 µF, since 1 n is 10^{-9} farads or 1000 pF.

Mains voltages

No mains (power line) voltages are listed in Elektor circuits. It is assumed that our readers know what voltage is standard in their part of the world! Readers in countries that use 60 Hz should note that Elektor circuits are designed for 50 Hz operation. This will not normally be a problem; however, in cases where the mains frequency is used for synchronisation some modification may be required.

Technical services to readers

- **EPS service.** Many Elektor articles include a lay-out for a printed circuit board. Some — but not all — of these boards are available ready-etched and predrilled. The 'EPS print service list' in the current issue always gives a complete list of available boards.
- **Technical queries.** Members of the technical staff are available to answer technical queries (relating to articles published in Elektor) by telephone on Mondays from 14.00 to 16.30. Letters with technical queries should be addressed to: Dept. TQ. Please enclose a stamped, self addressed envelope; readers outside U.K. please enclose an IRC instead of stamps.
- **Missing link.** Any important modifications to, additions to, improvements on or corrections in Elektor circuits are generally listed under the heading 'Missing Link' at the earliest opportunity.

ELEKTOR

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Number 10

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contents

score on screen for TV games

Although the MM5841 IC, described elsewhere in this issue, is primarily intended to display time and TV channel number on a TV screen, it may of course be used to display any other numerical information that is fed into it. The IC is thus ideal for displaying the score in TV games (e.g. Elektor TV Tennis), as described in this article.

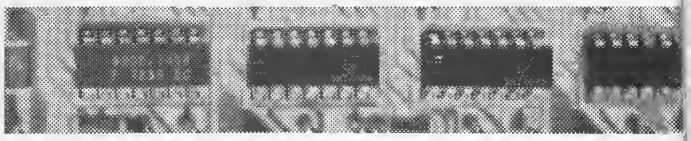
Before reading this article it is essential to read the article 'Time on TV', elsewhere is this issue, in order to understand the operation of the MM5841.

In the 'Time on TV' article it was explained how the MM5841 could accept up to eight digits in inverted BCD code (hours, minutes, seconds and TV channel number) and write them on the TV screen. To display the score of a TV game, the MM5841 is fed with information from score counters instead of from a digital clock. The other main difference is that no internal connections are required to the TV, as was the case with the time display. Since the picture is being generated by the TV game the output of the scoring unit can simply be fed into the video mixer along with the rest of the picture information and thence to the modulator.

Figure 1 shows a block diagram of the scoring unit.

The circuit contains two twin decade counters (block D) that register the score for each player. These counters receive clock pulses from the 'TV Tennis' extensions board described in Elektor No. 13. Which counter receives the clock pulse depends on which player has scored the point, and this is also determined by control signals from the extension board.

Altogether there are five inputs to the scoring unit from the extension board. Two of these are simply line and field sync pulses from points H and I, which control the timing sequence of the MM5841. The other three are concerned with the score counting. Referring back to issue 13, readers will no doubt remember that a score point is determined by the Q output of FF3 (figure 15) going high. This triggers the score sound effect circuit in figure 11.



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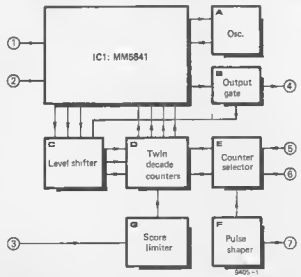


Table for figure 1.

1 = Hor. synch. ('H').
2 = Vert. synch. ('I').
3 = To ball generator ('8' and '9').
4 = Video out ('A').
5 = From ball direction flip-flop, Q of FF2 ('Q').
6 = From ball direction flip-flop, $\overline{Q}$ of FF2 ('J').
7 = From score output ('SCO').

The points referred to in brackets are connections to the extension board, except the points '8' and '9' that are to be found on the basic board.

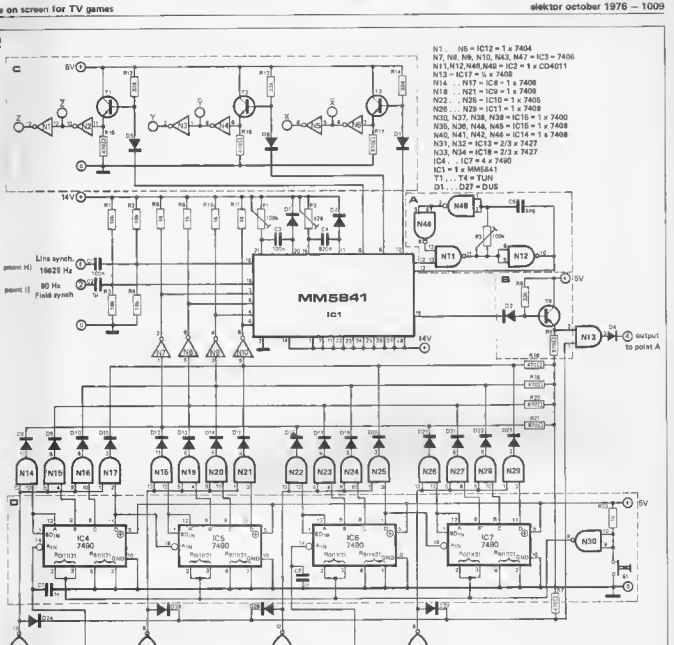


Figure 1. Block diagram of the scoring unit. The 'heart' of the circuit is the MM5841, which is discussed in greater detail in the article 'Time on TV'.

Figure 2. Complete circuit of the scoring unit. The boxes shown with dashed lines correspond to those in the block diagram.

Since this occurs only when a point is scored, this signal may be used to trigger the score counters. In actual fact use is made of the $\overline{Q}$ output of FF3 (which goes *low* when a point is scored). This is used to trigger a monostable in the scoring unit, which provides a short pulse to clock the score counter. The Q output of FF3 is available at point SCO on the extension board.

Of course a clock pulse occurs each time a point is scored, irrespective of which player scores it, so it is necessary to direct the clock pulse to the correct score counter. This is easily done since the direction in which the ball is travelling is known by the outputs of FF2 on the main TV tennis board. When a point

is scored then if the ball is travelling to the left the Q output of FF2 is high and the point is obviously scored by the right-hand player. On the other hand if the ball is travelling to the right the Q output of FF2 is high and the point is scored by the left-hand player. The Q and $\overline{Q}$ outputs of FF2 are used to gate the clock pulse into the right and left-hand score counters respectively (via counter selector block E). The Q and $\overline{Q}$ outputs of FF2 are available on the edge of the extension p.c. board at points O and J.

The outputs of the score counters must be multiplexed before they can be fed into the MM5841. This operation is controlled by the digit address' outputs of the MM5841, via a CMOS/TTL level shifter block C. There are two outputs from the scoring unit. One of these is the video signal that comprises the score, and the other is a 'score limit' output that prevents the ball from being served after one of the players has reached a preselected maximum score. This can be set to 10, 20, 30, 40, 50 or 60.

Pulse shaper, counter selector and counters

The complete circuit of the scoring unit is given in figure 2. The SCO input arrives at the input of N39 and triggers a monostable comprising N39 and N38. The output of this is buffered and inverted by N37. The clock pulse is routed either to the input of the right-hand score counter (IC4, IC5) via N36, or to the input of the left-hand score counter (IC6, IC7) via N35, depending on the state of FF2. The score counters

Parts list

Resistors.
R1,R2 = 10 k
R3,R4 = 18 k
R5,R12,R13,R14 = 33 k
R6,R7,R15 ... R21,R24 = 470 Ω
R8 ... R11,R22,R23 = 1 k

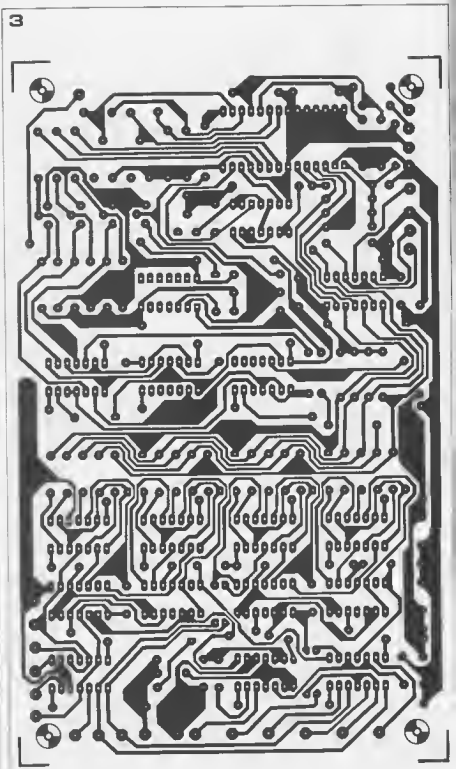
Capacitors:
C1,C3 = 100 n
C2 = 1 µ
C4 = 820 p
C5 = 5p6
C6 = 22 n
C7 ... C10 = 1 n

Decoupling:
C_X = 100 n
C_Y = 100 µ, 10 V

Semiconductors:
T1 ... T4 = TUN
D1 ... D27 = DUS

ICs:
IC1 = MM5841
IC2 = CD4011
IC3 = 7406
IC4 ... IC7 = 7490
IC8 ... IC11,IC14,IC15,IC17 = 7408
IC12 = 7404
IC13,IC18 = 7427
IC16 = 7400

Miscellaneous:
P1,P3 = preset potentiometer 100 k
P2 = preset potentiometer 47 k
S1 = push-button switch n.o. contact
S2 = six-way 2-pole switch



Figures 3 and 4. Printed circuit board and component layout for the complete circuit (EPS 9405).

may be reset to zero by S1.

Digit selection

On the four outputs of each counter stage are four AND gates wired as transfer gates. These allow one digit at a time to be selected and fed into four four-input OR gates comprising D8 to D23 and R18 to R21. The outputs of the OR gates are inverted to convert the data to the inverted BCD code required by the MM5841. The inverters N7 to N10 have high-voltage open-collector outputs, and the collector load resistors are taken to the +14 V rail so that the inverters also provide a TTL to CMOS logic level shift.

Selection of the counter output to be fed into the MM5841 is controlled by the digit address outputs of this IC. The digit address (X, Y and Z) outputs are connected to T3, T2 and T1 respectively, which perform a CMOS to TTL level shift. The outputs from the emitters of these transistors are buffered by inverters N1 to N6, and the X, Y and Z outputs and their complements are available. These are used to control three-input NOR gates N31 to N34, which perform the digit selection, e.g. N31 has inputs X, Y and Z. When the digit address is 000 (all three inputs low) then the output of N31 will be high and the outputs of IC4 will be selected. N32 has inputs X, Y and Z, so when X is high and Y and Z are low the inputs of N32 will be low and the output high, so the outputs of IC5 will be selected, and so on.

Video output and unused digit blanking

The MM5841 has facilities for displaying up to 8 digits when used in the normal time and TV channel mode, but of course only four digits are used in this application. For this reason it is used in the 'four-digit, time only' mode. However it will then still give a colon between the two pairs of digits, which must also be suppressed. This is accomplished by blanking the video output of the MM5841 except when one of the used digits is selected.

The video output appears at pin 15 of the IC and is CMOS to TTL level-shifted by T4 then fed to AND gate N13. The other input of N13 is connected to the output of a diode OR gate comprising D24 to D27, whose inputs are fed by the outputs of N31 to N34. Only when one of the outputs of N31 to N34 is high will the input (pin 1) of N13 be high and the video signal will be allowed through. At all other times the video signal will be inhibited. The video signal is fed via diode D4 to point A of the video mixer, where it is combined with the rest of the picture information.

4 MHz Clock

This differs slightly from the circuit used in the 'Time on TV' article. CMOS NAND gates are again used, but as CMOS gates are not used anywhere else in the circuit there are two spare gates available in a 4011 package, and these are incorporated into the clock oscillator (block A, figure 2). This introduces two propagation delays into the timing sequence, so the value of the timing capacitor is reduced. The frequency can be varied by P3 to alter the width of the digits in the display.

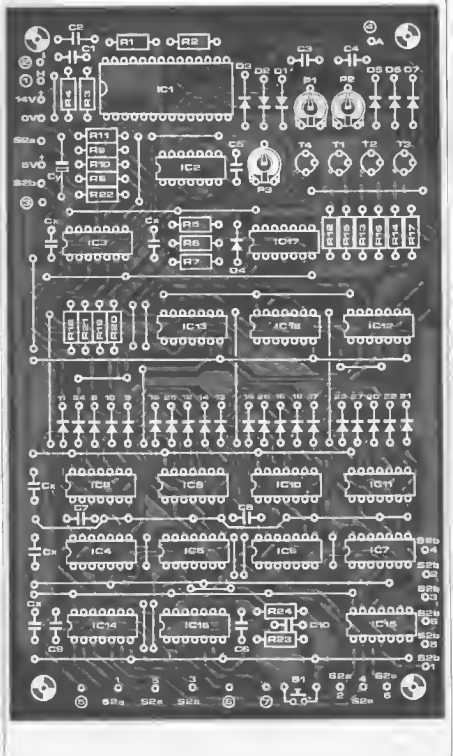
Vertical and horizontal position

As in the 'Time on TV' circuit, the vertical and horizontal position of the display may be altered by P1 and P2.

Sync inputs

As explained in the 'Time on TV' article, the logic levels for the sync inputs of the MM5841 are unusual, the logic 0 or low level being typically V_{DD} - 5 V (in this case 9 V) instead of the more usual V_{SS} (0 V). These inputs must be interfaced with the TTL outputs of the sync circuits of the TV Tennis. Fortunately this is easily accomplished by holding the sync inputs normally at +9 V by potential dividers R1/R3 and R2/R4. The sync pulses are then A.C. coupled through C1 and C2.

4



At this point it should be noted that the values of R1 . . . R4 are critical. If there are problems with the sync, try increasing the values of R3 and R4 to about 20 k.

Score limiter

When the preselected maximum score is reached the score limiter inhibits monostables IC1 and IC2 that produce the ball signal on the main TV Tennis board. Referring to issue 11 p 319 figure 1, the output of the score limiter is connected to points 8 and 9. The output of the score limiter is normally high, so the 'B' inputs of IC1 and IC2 are high and the monostables function normally. When the maximum score is reached the output of the score limiter will go low and the monostables can no longer be triggered.

The score limiter (block G) is connected to the outputs of the highest decade of the left and right score counters, and the maximum score is selected by S2. For example, with S2 in the first position the A output of IC7 is connected to the input of N43. When the left-hand player's score reaches 10 first this output will go high and the output of N43 will go low, inhibiting the ball signal. If the right hand player is the first to score 10 then the A output of IC5 will go high and the output of N47 will go low, inhibiting the ball signal. For a score of 20 the B outputs of the counters are used. For a score of 30 the A and B outputs are ANDed together and so on, up to a maximum score of 60.

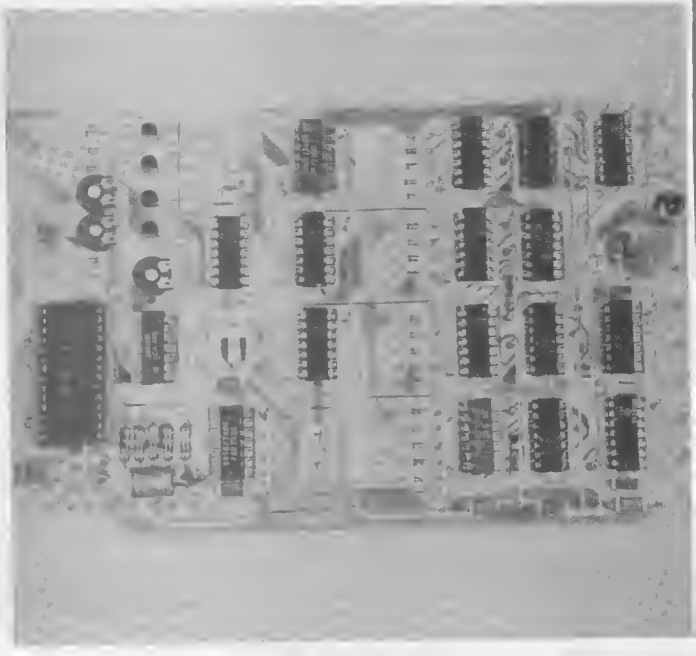
Construction

A p.c. board and component layout are given in figures 3 and 4. Construction is quite straightforward and no problems should be experienced provided the usual precautions are taken for handling CMOS. Apart from power supply connections and switches the only external connections are to the rest of the TV Tennis circuitry, and these connections are detailed in figure 1. All the connection points will be found along the edge of the extension printed circuit board, with the exception of points 8 and 9, which are on the main p.c. board.

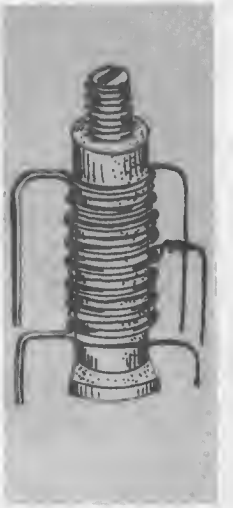
The power supplies for the scoring unit may be obtained from the supplies in the existing game. The +5 V may be obtained from the +5 V rail on the extension board. The +14 V rail may conveniently be obtained from the +18 V supply to the sound effects amplifier by using a simple series regulator. Make sure this voltage does not exceed 15 V, or the chips may be damaged. The current consumption is only about 15 mA.

Adjustments

The adjustments to the scoring unit are made by P3, which adjusts the character width, and P1 and P2, which adjust the position of the display on the TV screen.



FM on 11 meters



In earlier issues of Elektor (February and April 1975) it was explained why frequency modulation is one of the most efficient methods of modulating a carrier wave. To prove the point, not only by theoretical but also by experimental demonstration, this article describes the design and construction of a practical model intending to bear out the correctness of the abovementioned statement.

The transmitter circuit described is intended to be used in the 27 MHz citizen band but will also produce good results in the hands of a 28 . . . 30 MHz narrow band FM operator. Its frequency stability is sufficient for the purpose and the output power (250 mW) is enough to establish reliable communications over short distances. The receiver circuit shown in this article is of a quite unsophisticated design but nevertheless will give a good account of itself.

The entire system would lend itself admirably to such applications as wireless microphones, intercoms, baby alarms, and so on, if it were not for just one little snag: at the present time, regrettably, radio transmissions in this band are legally restricted.

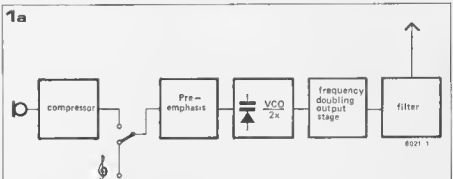
The experimenter is advised to operate in a closed circuit mode, via a suitable length of coaxial cable, to avoid getting into trouble with the law.

The 27 MHz citizens band

The original use of this band was to meet the need for inexpensive wireless telephone links for industrial purposes in the USA. As the interest in this band spread, the initial purpose became more obscure and the use of the band became more general. As more and more people came onto the citizens band, congestion and channel crowding became more the rule than the exception, forcing the industrial users to move out of the band.

Over the past 10 years the CB situation in the United States has become a free-for-all where the majority of users completely ignore the rules set down by the FCC. However, during the last year there seems to be a upswing of law abiding operators coming onto the band.

Fundamental differences exist between the fields of interest of the average citizen band operator and the fully licensed radio amateur. The amateur



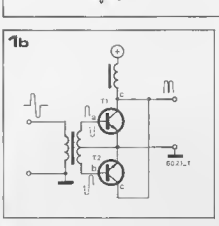


Figure 1a. Block diagram of the transmitter.

Figure 1b. Simplified diagram of the output stage showing phase relationships between input and output signals.

licensee has the technical know-how and ability needed to obtain a license, whereas some CBers may not know the difference between the mains connector and the microphone . . . Furthermore, the licensed radio amateur may be roughly divided into two groups: the 'software' category, or those who take the design of their equipment for granted and are intent mainly on the communications, and the 'hardware' category mainly interested in the electronic aspect of their gear.

The availability of so much off-the-shelf equipment may discourage the technically minded operator from keeping abreast of new developments in the field of electronics. The present article is intended to stimulate those who would like to be experimenting again, although we are well aware of the fact that the equipment described will probably not find immediate practical applications.

The transmitter

The block diagram is shown in figure 1a. The input stage is a speech compressor/amplifier. This reduces the effect of variations in the speaker-to-microphone distance and, at the same time, prevents overmodulation. A suitable compressor design was described in Elektor, April 1975, p. 440.

After pre-emphasis, the signal modulates the varicap oscillator. The second harmonic of the oscillator frequency is fed to a frequency-doubler output stage. This functions as follows (figure 1b).

Transistor T1 and T2 are driven in antiphase, each one being conductive only when the driving signal exceeds the base-to-emitter threshold. The signal appearing at the common collectors is similar to a full wave rectified AC signal. The advantage of all this frequency doubling is that the circuit becomes more stable. Feedback cannot occur, since the input and output frequencies of each stage are different.

The efficiency of the frequency doubling output stage is highly dependent upon the 'active' phase angle, that is, the phase angle over which the base current is flowing (see figure 2). With correct selection of parameters, setting the active phase angle to not more than 90°, the efficiency of the doubler stage equals the efficiency of class C amplifiers. Best results are obtained with high speed switching transistors such as the BSX 20, BSX 61 and 2N2219. This enables a continuous effective output of 0.5 W to be obtained with the BSX 20 and a 9 V power supply, and 4 W with a BSX 61 or 2N2219 at 15 V.

Under these conditions, the efficiency at 27 MHz amounts to 70%, and the same figure is obtained at 100 MHz.

However, it is not advisable to run the transmitter at such high power, since even minor deviations from the optimum parameters could then blow up the transistors. To be on the safe side, do not aim for more than 250 mW with the BSX 20 or 2 W with the other types.

The circuit of the complete transmitter, less the dynamic compressor, is shown in figure 3. T4 and T5 are a two-stage amplifier. The pre-emphasis is determined by the frequency dependent feedback network (C16, R13).

The varicap modulated and frequency

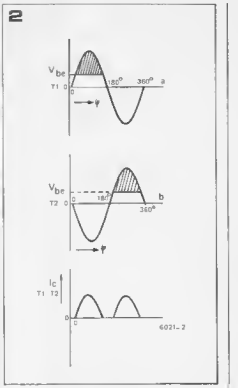
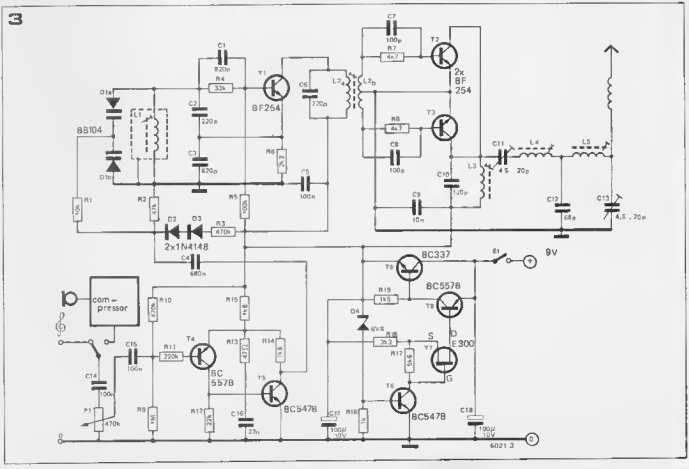


Figure 2. Detailed representation of the phase relationship between the input signals on the base of T1 and T2 (shaded area is where the transistors conduct) and the resultant output signal.

Figure 3. Circuit diagram of the transmitter.

Figure 4. Circuit diagram of the receiver.



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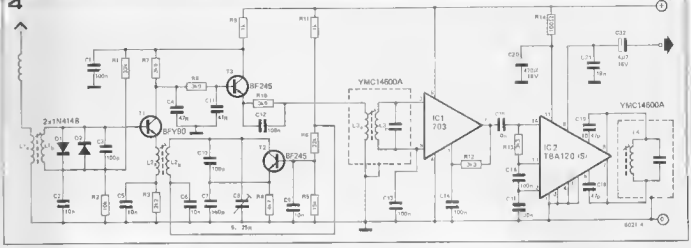
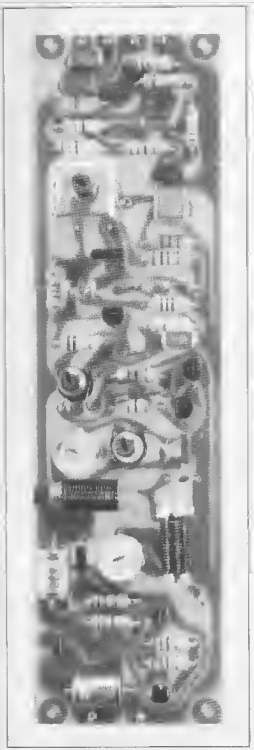
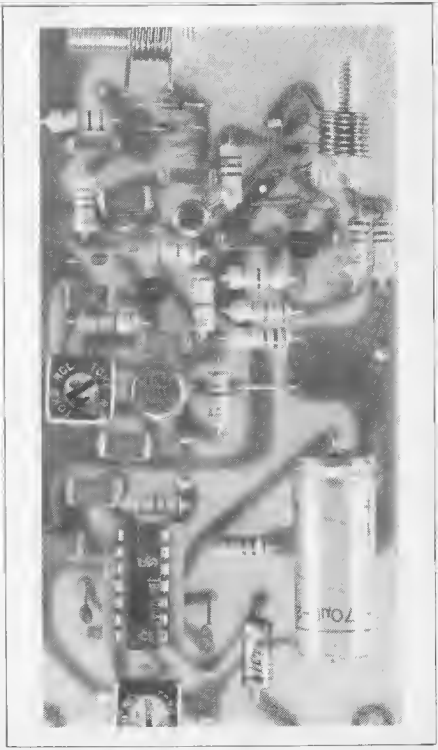
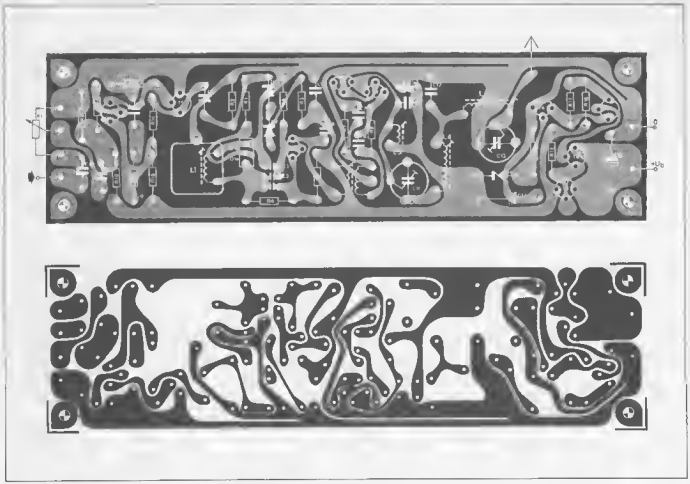

6 ... 15 V
2x1N4148
BFY90
BF245
BF245
YMC14600A
IC1
703
IC2
TBA120 (S)
YMC14600A
5 ... 25n
8021-4







doubling oscillator (T1) is temperature stabilised by D2 and D3. It drives the final class-C pushpull frequency doubler (T2, T3) that feeds into the aerial matching filter L3/C10, L4/C11, L5/C12/C13.
When properly built, the transmitter will comply with official requirements regarding frequency stability and spurious radiation, so that it is suitable for operation by licensed radio amateurs in the 10 meter band.

The receiver

The design target for this circuit (figure 4) was a straightforward receiver without any frills, and with moderate sensitivity and selectivity.
The intercoming 27 MHz signal is converted, by mixer T1 and local oscillator T2, into an I.F. signal of approximately 455 kHz. This is passed through a low-pass filter, to an amplifier/limiter/discriminator (IC1 and IC2).
The low IF frequency (455 kHz) was chosen for effective limiting action, high gain and low feedback. The inherent drawback of poor image rejection was considered acceptable since very few transmitters are operating on the image frequencies. When properly adjusted the receiver specifications are:
sensitivity:
4 μV for 26 dB S/N
10 μV for 50 dB S/N
bandwidth/input signal level:
200 kHz/ 4 μV
300 kHz/10 μV
image rejection:
3 dB
maximum signal deviation:
120 kHz.

Construction and alignment

It must be noted that capacitors of up to 10 nF should be of the ceramic type, and radio amateurs who intend to use the equipment with a 15 V power supply should remember that some ceramic types can stand only 12 V. Capacitors from 10 nF to 100 nF can be MKM types.
A shortwave receiver fitted with a signal strength meter, or a grid dipper, can be used to tune the oscillator to 6.75 MHz, after which L2 is adjusted to maximum meter deflection at 13.5 MHz. Apart from the shortwave receiver, the latter tuning operation can also be carried out with the help of a high impedance voltmeter connected to the base of T2 or T3. Rectification in the transistor will cause a negative potential with respect to ground to build up on the base. L2 tuning will be correct when this negative voltage is at its maximum.
Tune-up of the aerial matching filter can then be accomplished by using a receiver with an S-meter.
The transmitter must be housed in a metal case, and special care must be taken to ensure that the aerial output terminal is well grounded to the rest of the circuit. Otherwise, stray RF currents will have some nasty effects. Since the installation into a metal case will affect the tuning adjustments, the equipment must be encased in such a way as to allow re-adjustment.
Now is a good time to do the final alignment of the transmitter, by repeaking coils L2, L3, L4 and L5 along with C11 and C13. These controls should be adjusted for minimum noise in the audio output of the receiver.

Receiver alignment

For alignment of the receiver, assuming that no signal generator is available, the transmitter is used as a signal source. With the transmitter connected to a dummy load (50 Ω/1 W resistor), receiver capacitor C8 and coil L2 should be adjusted so the transmitter signal is heard in the receiver's audio output. There should be a drop in the noise level. Coils L1 and L3 can now be adjusted for a further noise reduction. The signal will be very strong due to the close proximity of the transmitter, so for final alignment of the receiver it should be moved some distance away from the transmitter. C8, L2, L1 and L3 can now be re-adjusted for maximum quieting. This procedure should be repeated until no further improvement in sensitivity is obtained.
Now apply an audio input to the transmitter and increase its level (deviation) until some distortion is noted in the audio output from the receiver. Adjust L4 for minimum distortion while continuing to increase the transmitter deviation. At some point no further improvement can be obtained. The receiver is now completely adjusted.

Conclusion

When these FM units are compared with

an AM system of similar output power, the difference in audio fidelity and range of the FM system should prove interesting.
Once again it should be pointed out that these units are for experimental use, and were not intended for chatting around town. If such operations were undertaken, interference to other services in the same frequency band could occur over a distance of several miles. Such interference would most certainly be frowned upon by the boys down at the post office.

Coil table

Transmitter:
L1 = 28 turns/30 SWG
L2 = 10 turns/20 SWG (collector winding)
8 turns/30 SWG centre-tapped
L3 = 7 turns/20 SWG
L4 = 19 turns/24 SWG
L5 = 19 turns/24 SWG

Receiver:
L1 = 7 turns/20 SWG (base winding)
2 turns/30 SWG (antenna winding)
L2 = 7 turns/20 SWG (collector winding)
2 turns/30 SWG (emitter winding)
L3,L4 = 455 kHz I.F. trans, YMC1-4600A

The coil forms should be 6 mm diameter with 4 mm core. Cores should have a green or white mark. There should be no spacing between the turns on single winding coils. The primary and secondary turns of coupling coils should be intermeshed.

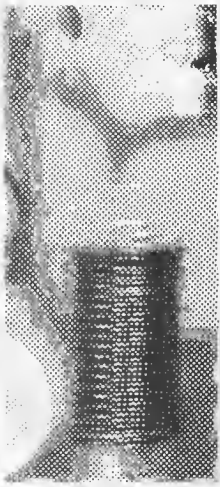
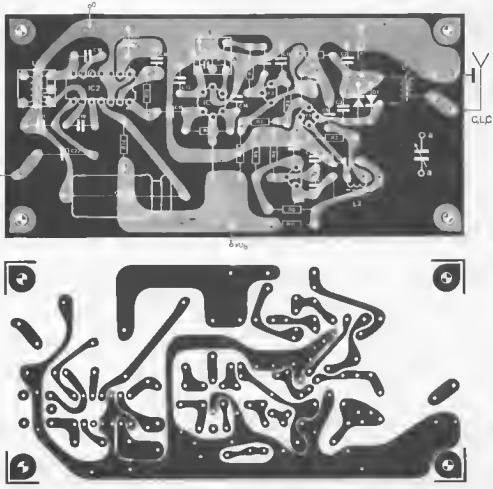


Figure 5. Board layouts for the transmitter and receiver.



autoranger for DFM

R. Decker

This circuit automatically selects the optimum gate period for a frequency measurement, positions the decimal point in the display and indicates the units of the measurement (Hz, kHz, MHz). The need for a manual range selection switch is thus eliminated, making possible more rapid measurements.

A block diagram of the autoranger is shown in figure 1. The counter gate pulses are derived, in the conventional manner, from a 1 MHz crystal oscillator followed by a seven decade frequency divider. However, unlike a conventional frequency counter the gate period is selected, not by a switch but by an 8-input digital multiplexer. One of the inputs (in this case the gate pulses) can be switched through to the output of the multiplexer depending on a three-bit binary address applied to the data select inputs of the multiplexer. The multiplexer address is obtained from the outputs of a four-bit up/down counter.

To obtain the maximum resolution from the frequency counter the gate period must be chosen so that the most significant (highest) decade of the display is greater than zero. On the other hand the counter must not overflow. This is achieved in the following manner:

At the end of each count period a pulse from the counter timing logic enables the latches that store the count before resetting the main counters. This pulse is also fed to one of the clock inputs of the up/down counter. If the highest decade of the frequency counter is zero (i.e. the selected gate period was too short) then this is detected by the zero detector logic and a 'count up' instruction is given to the up/down counter. The multiplexer address is changed and a longer gate period is selected for the next count.

If, on the other hand, the counter overflows then a flip-flop connected to the 'D' output of the highest decade latch is set. Once the counter has overflowed it is pointless to continue the count so a 'count down' instruction is given to the up/down counter and the timing logic is overridden. The main counters are reset and the up/down counter counts down so that the multiplexer selects a shorter gate period for the next count.

The up/down counter will count up (or down) at the end of each count cycle until the optimum gate period is found (i.e. until the highest decade displays a number from 1 to 9). The up/down counter will then be inhibited. Where it is not possible to achieve the optimum gate period (i.e. if the frequency is so low that the highest decade is zero even with the longest gate pulse, or the frequency is so high that the counter overflows with even the shortest gate pulse) then the up/down counter will count to its maximum or minimum count and stay there. It will not cycle continuously.

In addition to providing the multiplexer address the up/down counter also controls the positioning of the decimal point and the Hz, kHz and MHz indicator lamps.

Timing Logic

As the counter timing logic is perhaps the most complicated part of the whole set-up it is considered in more detail in figure 2, and a timing diagram is given in figure 3. Obviously, the count, latch, reset, display cycle is a continuous, closed-loop operation, so to investigate its operation we must break the loop at some point and consider this as the starting point.

In figures 2 and 3 the starting point is taken as the trailing edge of the gate pulse or a negative-going edge from the overflow flip-flop. Either of these will trigger monostable IC3b, which provides a short delay after the completion of the measuring period. When IC3b resets its $\overline{Q}$ output triggers monostable IC2b, which provides the latching pulse. IC2b has insufficient fanout to drive all the latches in a frequency counter, so its output is buffered by a power inverter N11. The output of N11 triggers monostable IC1a, which provides a delay to ensure that all the data have been safely stored in the latches before triggering monostable IC1b which resets the counters. The output of IC1b is also buffered by N10 to provide sufficient fanout to drive the counter reset inputs. The output of IC1b also triggers monostable IC3a, which provides a pulse to reset the overflow flip-flop.

Monostable IC2a provides a variable pulse length which determines the display time (i.e. the time for which the count is displayed before the next count cycle). The next count cycle is not initiated until IC2a resets.

The timing sequence is shown in detail in figure 3. The sequence is initiated by the negative-going (trailing) edge of the gate pulse, which triggers IC3b. This provides about a 1 μs delay before it resets, triggering IC2b which provides a 1 μs latch pulse. The trailing edge of the latch pulse triggers IC2a, which determines the display time, and IC1a, which provides a 1 μs delay to ensure that the data stored in the latches are valid before it resets and triggers IC1b, which provides a 1 μs counter reset pulse. Once the counters have been reset the overflow flip-flop can also safely be reset by a pulse from IC3a, without any danger of it being re-triggered.

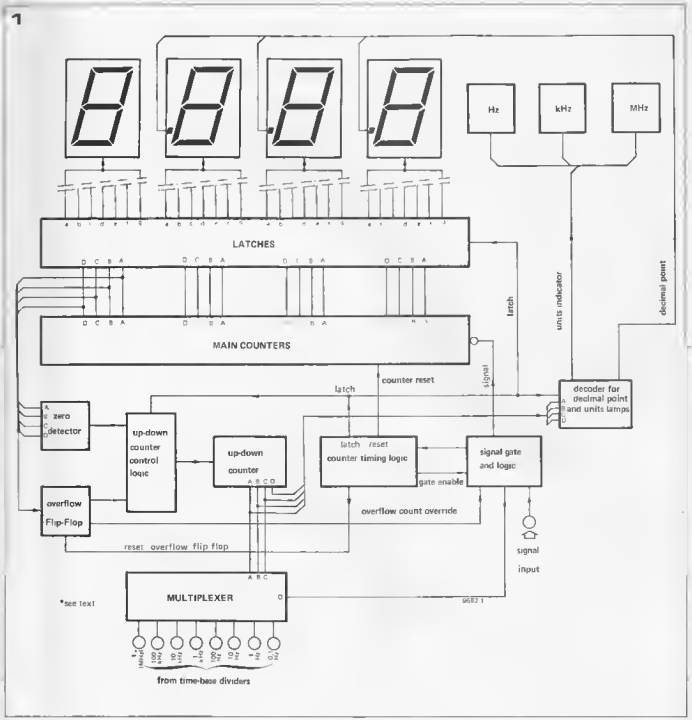
Complete Circuit

Figure 4 gives the complete circuit of the auto ranger. The heart of the circuit is the up/down counter IC6. Pulses may be fed from the output of N11 (latch output), either to the up count input via N15 or to the down count input via N13, under the control of the zero detector and overflow flip-flop.

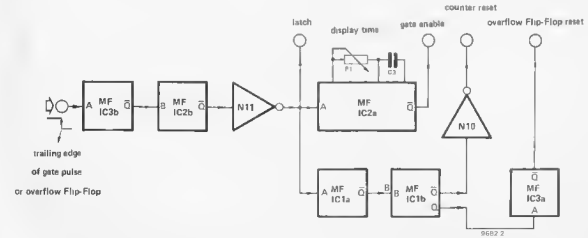
Figure 1. Block diagram of the autoranger.

Figure 2. Block diagram of the timing logic.

1


Hz
kHz
MHz
LATCHES
MAIN COUNTERS
latch
units indicator
decimal point
counter reset
signal
decoder for decimal point and units lamps
zero detector
up-down counter control logic
up-down counter
latch reset
counter timing logic
signal gate and logic
gate enable
overflow Flip-Flop
overflow count override
reset overflow flip flop
signal input
MULTIPLEXER
*see text
9682 1
from time-base divider

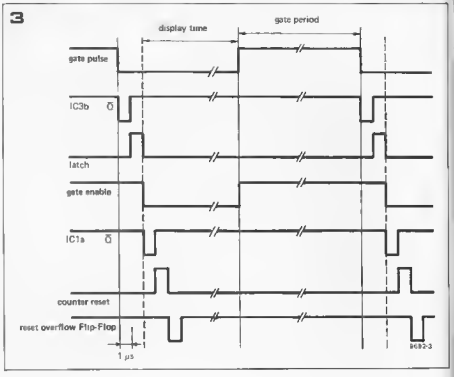
2

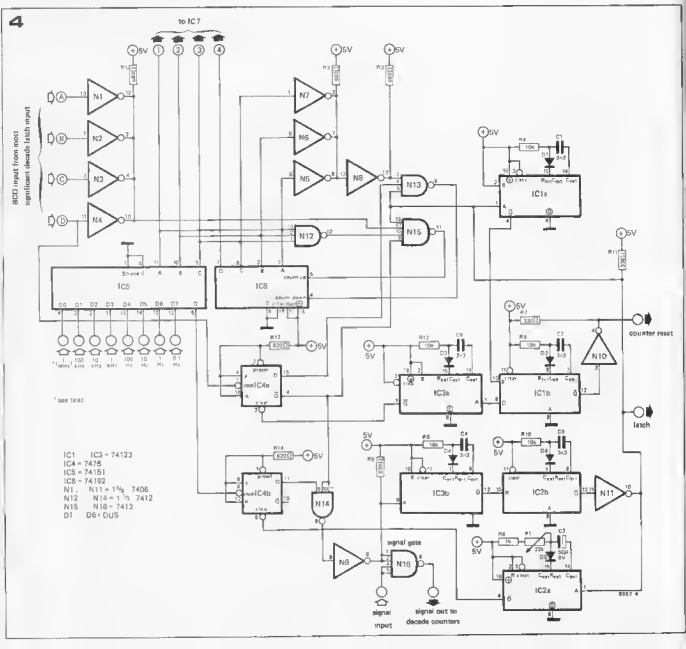

counter reset
latch
display time
gate enable
overflow Flip-Flop reset
MF IC3b
MF IC2b
N11
MF IC2a
N10
MF IC1a
MF IC1b
MF IC3a
trailing edge of gate pulse or overflow Flip-Flop
9682 2

Underflow

The zero detector comprises four open-collector inverters N1 to N4 connected as a four-input NOR gate. While the BCD outputs of the highest decade latch are not zero then the output of the gate will be low and the output of N15 will remain high. However, when inputs A, B, C and D are all zero the output of the NOR gate will be high and latch pulses can pass through N15 to make the counter count up. However, two other input conditions on the inputs of N15 can inhibit this:

1. If the highest decade overflows by a count of exactly 10 the highest digit will still be zero. However, the overflow flip-flop IC4a will have been clocked by the D output of the highest decade and its $\bar{Q}$ output will be low, thus holding the output of N15 high and inhibiting the up count.
2. When IC6 has reached a count of 7 the A, B and C outputs will all be high so the output of N12 will be low. The output of N15 will be high, thus inhibiting any further up count.





Overflow

When the counter overflows the D output of the highest decade will clock flip-flop IC4a, which will perform several functions:

1. as mentioned earlier, the up count will be inhibited.
2. During normal counting the $\overline{Q}$ output of IC4a will be high and the counter gate pulse from IC4b will pass through N14. However, if the overflow flip-flop is clocked the $\overline{Q}$ output will go low and the gate pulse will be blocked, thus terminating the count early.
3. When IC4a is clocked the Q output will go high, thus allowing a latch pulse through N13 to the down input of the up/down counter. If the counter is already at zero this function is inhibited by N5, N6 and N7, connected as a NOR gate. When the A, B and C outputs of IC6 are all zero the output of this NOR gate will be high, the output of N8 will be low and the output of N13 will be held high regardless of any other input conditions.

Counter Timing Logic

The only parts of the timing logic not discussed earlier are the gate pulse flip-flop IC4b and the signal gate N16. IC4b is held in the 'clear' state during the display time by the $\overline{Q}$ output of IC2a. When IC2a resets then IC4a will be clocked on the trailing edge of the next clock pulse received from the multiplexer IC5. The signal gate N16 will then be held open. On the next clock pulse trailing edge IC4b will again be clocked and will return to the initial state, so the signal gate will close. The gate period is thus equal to one complete cycle of the clock input from the multiplexer. Completion of the gate period initiates the latch, display and reset cycle as described earlier (IC3b is triggered by the negative going output of N9).

Decimal point and range indication

The final part of the circuit is the decimal point and range indication decoder, figure 5. The outputs of IC5 are stored in a latch (IC7) and the outputs of the latch are fed to a BCD-to-decimal decoder-driver, IC8. The outputs of IC8 are then fed to diode AND gates to drive the decimal points of the display and the range indication LEDs (See Table 1).

Editorial notes

1. The 1 MHz input to IC5 (figure 4) is rather pointless: a measuring range of 1-10 GHz is not likely to be required! The circuit will work just as well if 100 kHz is fed in here instead (in other words, connect D0 and D1 of IC5 to the same 100 kHz signal).
2. For measuring at high frequencies (over 18 MHz), gate N16 will have to be replaced by a faster type.
3. The simplest way to use the circuit with a six-digit counter is to consider the four digits shown as the least significant digits of the total display. The extra two digits will then extend the maximum frequency count in each range. The inputs to N1 . . . N4 should still be taken from the most significant digit (not the third!). Inputs D0 . . . D3 of IC5 can all be connected to the 1 kHz input in this case.
4. The 'autoranger' will always set the counter for maximum accuracy, even if this means a 10 s gate time. A manual override may be desirable . . .

Figure 3. Timing diagram of the counter timing logic.

Figure 4. Circuit diagram of the autoranger.

Figure 5. Circuit diagram of the display decoder.

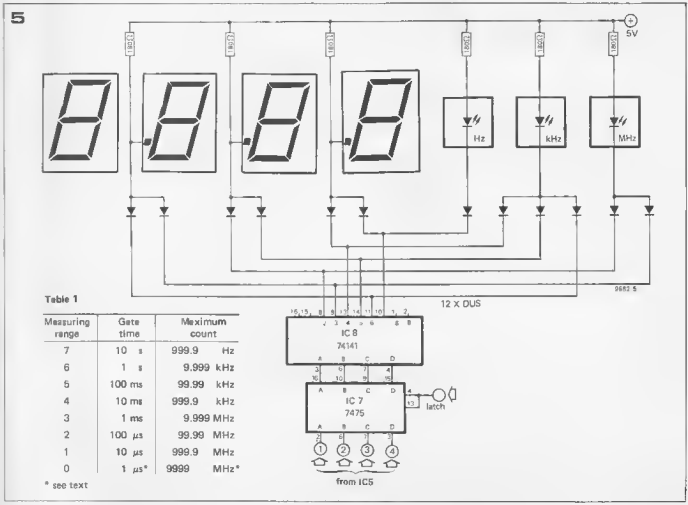


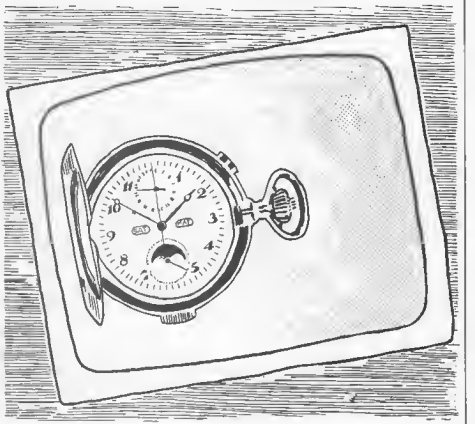
Table 1

Measuring range	Gate time	Maximum count
7	10 s	999.9 Hz
6	1 s	9.999 kHz
5	100 ms	99.99 kHz
4	10 ms	999.9 kHz
3	1 ms	9.999 MHz
2	100 µs	99.99 MHz
1	10 µs	999.9 MHz
0	1 µs*	9999 MHz*

* see text

time on TV

The current trend in the TV industry seems to be the proliferation of 'gadgets' for use with the TV set, and the use of the TV screen to display information other than pictures. Typical examples of this trend are the sophisticated ultrasonic remote control units currently available, Teletext, and of course TV games. This article takes a look at two IC's that can be used to display the time on a TV screen.



Using two IC's from National Semiconductor, the MM5841 and MM5318, it is possible to display, on a TV screen, the time and TV channel number. For the home constructor the second possibility is less attractive since it involves modifications to the channel selector, which can be quite complicated. The time display, on the other hand, requires only connections to the TV timebase and video stages.

At this point it must be stressed that it is impossible to provided a design that is universally applicable to all TV sets. Interfacing of the clock to the TV set must therefore be left to the ingenuity of the individual constructor, although some generalised suggestions are given. This should, of course, be attempted only by those familiar with the 'innards' of TV sets.

Figure 1. Block diagram of Time on TV system using MM5841 and MM5318.

Figure 2. Internal block diagram of the MM5841.

The circuit

Although the complete circuit requires only the MM5841, MM5318 and a handful of other components the internal organisation of these IC's is fairly complex. Figure 1 shows a block diagram of the system, which shows the basic functional arrangement without going into too much detail.

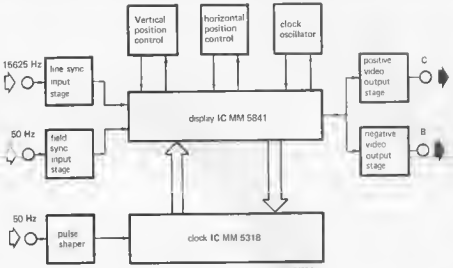
The clock part of the circuit is the MM5318. This is much like any other digital clock IC. It accepts a 50 or 60 Hz timing signal, and provides multiplexed digit outputs. There are however, one or two unusual features which make it suitable for this application. In addition to the usual seven-segment outputs, the MM5318 provides outputs in inverted BCD (BCD) code. Secondly, the multiplexing is not controlled by an internal oscillator, as in a normal clock, but is controlled by a 3-bit binary address provided by the MM5841.

The MM5841 is synchronised to the TV picture scan by field and line sync pulses. These may be delayed by monostables built into the IC so that the vertical and horizontal position of the time display can be altered to suit individual taste. An external clock oscillator controls the operation of the MM5841 during each line scan. The frequency of this oscillator may be varied between 4 and 6 MHz to alter the character width. The circuit is provided with two output stages that provide positive and negative video signals so that black or white characters may be selected.

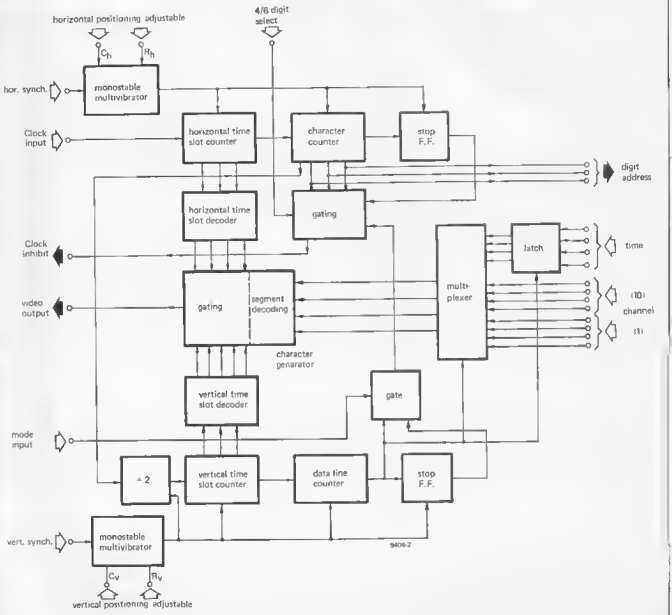
MM5841

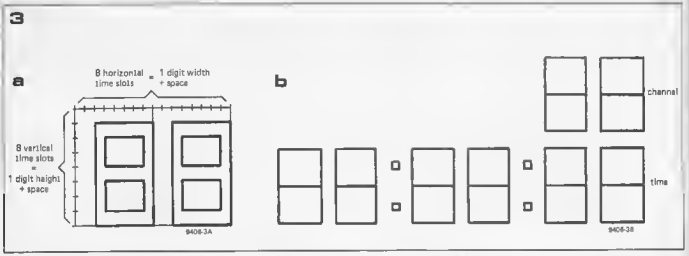
Figure 2 shows the internal organisation of the MM5841, whilst figures 3a and 3b show how each character is built up, and the format of the display. Each digit is built up from a matrix of 8 x 8 'timeslots'. A horizontal timeslot has a duration equal to the period of the clock oscillator, which can be varied

1


Vertical position control
horizontal position control
clock oscillator
15625 Hz
line sync input stage
display IC MM 5841
positive video output stage
C
50 Hz
field sync input stage
negative video output stage
B
50 Hz
pulse shaper
clock IC MM 5318
9406-1

2


horizontal positioning adjustable
4/6 digit select
Ch
Rh
hor. synch.
monostable multivibrator
Clock input
horizontal time slot counter
character counter
stop F.F.
digit address
horizontal time slot decoder
gating
Clock inhibit
latch
time
multi-plexer
video output
gating
segment decoding
(10)
channel
(1)
character genarator
vertical time slot decoder
gate
mode input
÷ 2
vertical time slot counter
data line counter
stop F.F.
vert. synch.
monostable multivibrator
9406-2
Cv
Rv
vertical positioning adjustable



between 250 ns and 170 ns approximately to alter the character width. A vertical timeslot comprises 4 lines of a complete TV frame, i.e. two lines per field. To provide horizontal and vertical spacing between characters the first two horizontal slots and the first vertical slot are always blank. Figure 3b shows the format of the complete time and channel display. The channel display is of course blanked in this application.

Writing of the characters on the TV screen is controlled by the TV field and line sync pulses. To understand the operation of the circuit it is first necessary to identify and explain some of the blocks in figure 2.

Character generator

This accepts an input in BCD from the multiplexer and decodes it to seven-segment form. The gating selects a point in the 8 x 8 character matrix depending on the horizontal and vertical timeslot inputs at that time. When the character has an element at that point in the matrix then a video pulse appears at the output.

Multiplexer

This selects which digit is fed to the character generator at a particular time. Channel 10's, channel 1's or time. The time input is already multiplexed under the control of the digit address output.

Horizontal counters

The horizontal timeslot counter counts clock pulses from the 4 MHz clock. Its outputs are decoded (in the timeslot decoder) and fed to the character gating. On each 8th pulse the character counter is advanced by one. This changes the digit address fed to the MM5318 so that the next digit is multiplexed into the character generator.

Vertical counters

The vertical timeslot counter is preceded by a flip-flop that accepts an input from the character counter so that every two lines the vertical timeslot counter advances by one. After sixteen lines a pulse is fed to the data line counter, which determines whether the display is on the first row of digits (the channel number) or the second row (time). After 32 lines the data line counter feeds a pulse to the stop flip-flop, which inhibits the 4 MHz clock until the next field.

Horizontal and vertical monostables

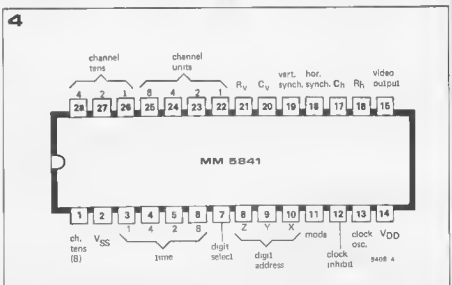
These are triggered by the line and field sync pulses and introduce delays before the counters are allowed to start, thus determining the horizontal and vertical position of the display.

Having discussed some of the blocks within the IC the operation of the entire circuit during one picture field can be examined.

The starting point in the sequence can be taken as sometime during the preceding field after completion of display writing. The data line counter is at its maximum count, the vertical stop flip-flop is set and the 4 MHz clock is inhibited, so all the counting functions within the IC are stopped.

At the beginning of the next field the vertical monostable is triggered by the field sync pulse, resetting the ÷ 2 stage, vertical counter, data line counter and vertical stop flip-flop. This enables the 4 MHz clock. At the beginning of each line scan the horizontal monostable is triggered by the line sync pulse. This holds the horizontal counters reset for the period of the monostable, after which the horizontal timeslot counter starts to count clock pulses. This delay determines the position of the display relative to the left-hand edge of the screen. However, while the vertical monostable is triggered the vertical counters are held in the reset state, so no display appears. This delay determines the position of the display relative to the top edge of the screen. When the vertical monostable resets the vertical timeslot counter begins to count pulses from the character counter.

The display is thus built up line by line. At the beginning of each line there is a delay. Then the horizontal timeslot counter begins to count clock pulses and writes the first line of the first digit. On the 8th clock pulse the character counter advances, changing the digit address so that the second digit is multiplexed into the character generator. The first 8 elements of the second character are then written by the horizontal timeslot counter, followed by the fourth, fifth and sixth digits (unless only four digits have been selected). At the end of the sixth character the divide-by-two flip-flop preceding the vertical timeslot counter receives a pulse, and the horizontal stop flip-flop is set. This inhibits the clock generator until the next line, preventing the horizontal counters from



starting their cycle over again, as otherwise the display would occur more than once across the screen (of course, the first row of characters uses only the fifth and sixth digits for the channel display).

This cycle is repeated, with the vertical timeslot counter advancing every two lines. The height of a vertical element is thus two lines per field, but since a complete frame takes two fields this means a vertical element occupies a total of four lines, the odd numbered lines being written during one field, and the even-numbered lines being interlaced between them on the next field. When the vertical timeslot counter reaches a count of eight a pulse advances the data line counter for the start of the second row of digits (time). When the vertical timeslot counter reaches a count of 16 the data line counter again advances, setting the vertical stop flip-flop which inhibits the 4 MHz clock. The circuit now remains quiescent until the start of the next field.

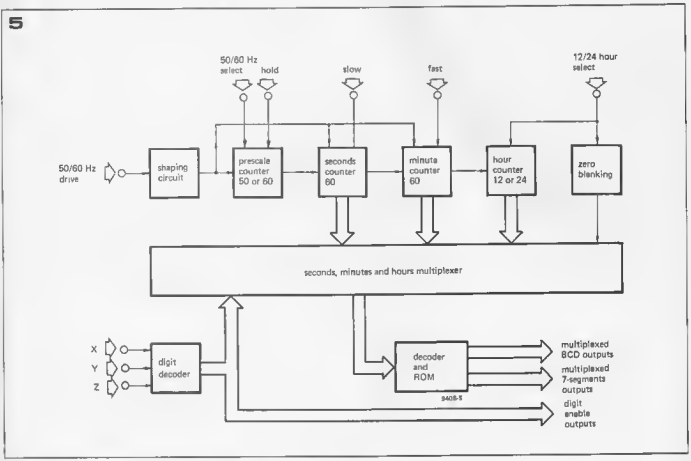
The IC has facilities for inhibiting the time display and displaying the channel number only. This is accomplished by the mode control. A '1' on the mode control input gives time and channel number, a '0' gives channel number only. When channel only is selected the output of the data line counter is used to inhibit the clock after the first character row.

MM5318

This is a fairly conventional single-chip clock with one or two variations to make it suitable for interfacing with the MM5841.

The block diagram of figure 5 shows that it has the usual facilities for 50 or 60 Hz timing input, 12 or 24 hour display, slow, fast and hold controls for time setting, and multiplexed seven-segment outputs. However, in addition to seven-segment outputs it also has outputs in inverted BCD code to interface with the MM5841. Unlike a conventional clock, the multiplexer is controlled, not by a free-running internal clock, but by a three-bit address generated by the MM5841.

5



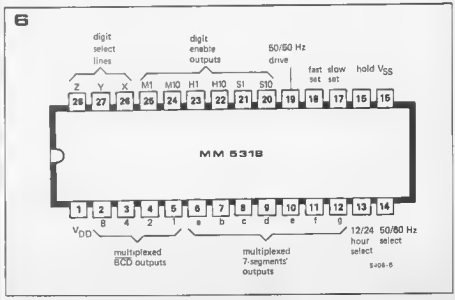
Figures 3a and 3b. Showing breakdown of digits into 8 x 5 matrix and format of display on TV screen.

Figure 4. Pinout of MM5841.

Figure 5. Internal block diagram of MM5318.

Figure 6. Pinout of MM5315.

6



Complete system using MM5841 and MM5318

Apart from the interfacing with the TV video stages (which will be dealt with later) the external circuitry required is fairly straightforward and problem-free.

Line sync input stage

The first requirement is for circuits to pick up line and field sync pulses from the TV. These circuits are basically identical, as shown in figure 7.

The line sync can be obtained either from the sync separator or from the line flyback blanking circuit in the TV set. The latter is usually easier. The pulses are amplified and fed to pin 18 of IC1. If pulses of the correct polarity cannot be found in the TV set, a COSMOS inverter can be included between the collector of the transistor and the corresponding pin of IC1.

The field synchronising signal can also be derived from either the field flyback blanking signal or from the sync separator. As in the previous case, it may be necessary to add an inverter in series with the output. A Schmitt trigger could be used, but in practice an ordinary CMOS NAND gate is quite adequate.

With large input voltages from the field or line oscillator (i.e. much greater than supply voltage) it will be found that the input waveform will be clipped. This will mean that the display cannot be positioned near the top or left of the screen but will appear in the middle. Instability of the display position may also result.

This effect can be cured by attenuating the input level so that the waveform does not clip. The best value of the input resistors (R1 and R4 in the main circuit) can be anywhere between 10 k and 100 k.

Horizontal and vertical position shift

The monostables that produce the horizontal and vertical delays are integrated into the IC, but they require external timing components. The internal circuit of one monostable is shown in figure 8, together with the external timing components. The various circuit waveforms are shown in figure 9. Due to the RC network the rectangular pulse V1 is differentiated and a positive pulse in excess of V_{DD} is produced. To avoid damage to the IC this must be limited to V_{DD} + 0.3 V by an external germanium diode connected to V_{DD}.

Clock pulse generator

This is simply an astable multivibrator constructed around two CMOS NAND gates (figure 10). The frequency may be varied by means of P4 to alter the character width. The oscillator is gated by the MM5841, it operates when a '1' appears on pin 12 of the IC. The display may be suppressed altogether by opening switch S2, which disables the clock generator.

50 Hz timing input to MM5318

This circuit, shown in figure 11, will accept an input from one of the low-

Figure 7. Circuit to pick up line and field sync from TV set.

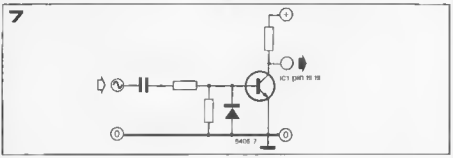
Figure 8. Internal circuit of the line and field delay monostables.

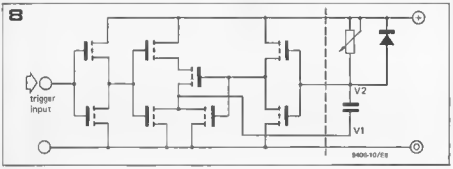
Figure 9. Input and output waveforms of the monostable, showing the need for clipping of the positive spike.

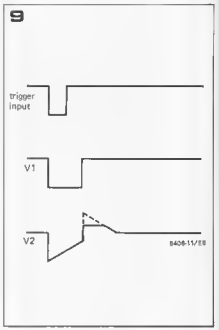
Figure 10. 4 - 6 MHz clock generator.

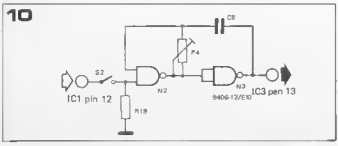
Figure 11. 50 Hz timing pulse input sheper.

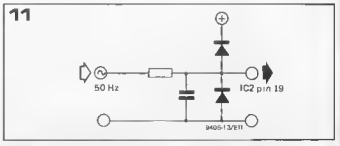
Figure 12. Complete circuit of Time on TV unit.











voltage A.C. supplies in the TV set (from 16 - 24 V). This is clamped to V_{DD} and V_{SS} by the diodes.

Complete circuit

A complete practical circuit is given in figure 12 incorporating all these ancillary circuits. Additionally the video output (pin 15) is provided with two buffer stages. T4 provides a positive video output and T3 provides a negative video output.

Since only the time is being displayed in this application it is necessary to suppress the channel inputs. The IC does not have any control input for the selection of time only. Fortunately, if an input greater than 9 is presented to each channel input there will be no channel display since only digits 0 - 9 can be displayed and all other input codes are invalid. Grounding all the channel inputs corresponds to input codes of 15 in inverted BCD, so grounding all channel inputs will suppress the channel display.

Interfacing with TV

The simplest method of interfacing the video output of the MM5841 with the TV is by direct injection into the TV video stages. This is best done at the base of the video output transistor or the control grid of the output valve (luminance output transistor or valve in a colour TV).

The circuit of figure 13a may be connected to the positive video output stage of figure 12, or the circuit of figure 13b may be connected to the negative video output stage. One will give white characters while the other gives black, but which gives which is dependent on the type of video output stage in the TV. Figures 14a and 14b show positive and negative video waveforms.

The diodes serve to isolate T3 and T4 from the TV video stage when there is no signal from the MM5841, as otherwise the TV video output stage might be loaded, thus affecting the picture. When there is no time signal the diodes are reverse-biased. The extent to which the diodes are reverse-biased is important, and is controlled by the adjustable potential divider. If the reverse-bias voltage is too great then the diodes will never be forward-biased, even when the time signal is present, and no display will appear on the screen. On the other hand, if the bias is insufficient the peak signal level during a time signal may exceed peak white level, resulting in overmodulation and saturation of the TV tube (figure 15a). It is thus essential to adjust the bias so that the peak level of the time signal is equal to or slightly less than the normal peak white video signal (figures 15b to 15c).

If black characters are chosen overmodulation of the tube is not a problem. However, it is possible for the signal to go more negative than black level (i.e. into the 'blacker-than-black' region) in which case false sync pulses may be produced. This would only be a problem in TV's where sync separation is performed after the video output stage. Correct adjustment of the bias potential will find the correct compromise.

A far greater problem with the direct injection method is the risk of signal reflection and ringing. This is visible as the appearance of the characters 'in relief' on the screen. It can be reduced by careful matching of input and output impedances.

Interfacing by parallel video stage

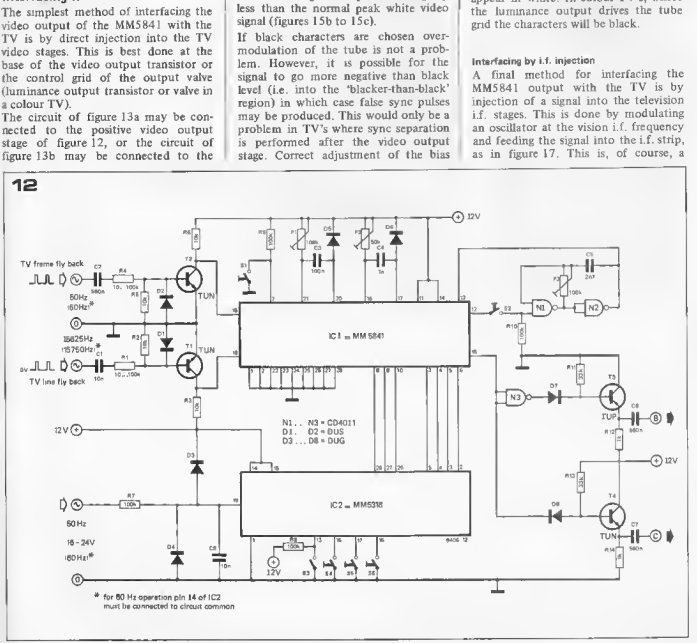
An alternative method of interfacing is to connect an extra video stage in parallel with the TV video output stage, as shown in figures 16a and 16b. The extra transistor or valve must be turned off when there is no time signal output, which means that it must be fed from the positive video output (if it were normally on it would short out the original video output stage).

In this case the colour of the characters cannot be chosen but depends on the type of video output drive to the tube. With grid controlled tubes the characters will appear in black, with cathode controlled tubes the characters will appear in white. In colour TV's, where the luminance output drives the tube grid the characters will be black.

Interfacing by i.f. injection

A final method for interfacing the MM5841 output with the TV is by injection of a signal into the television i.f. stages. This is done by modulating an oscillator at the vision i.f. frequency and feeding the signal into the i.f. strip, as in figure 17. This is, of course, a

12



much more complicated method and problems arise with screening etc.

Practical construction

In any practical construction involving modifications to a TV set great attention must be paid to safety since the 0 V rail of the circuit is connected to the TV chassis which is not isolated from the mains. All of the circuitry must be mounted in the TV cabinet and none of it must accessible from the outside without removing the back cover of the TV. The only externally accessible controls should be the three timesetting pushbuttons, which should have bodies constructed of an insulating material and plastic pushbuttons adequately insulated from the contacts.

In transistor and hybrid TV's there will probably be a low voltage DC power supply which can provide the 14 V required by the circuit. It will, of course, be necessary to measure the current drawn by the circuit to ensure that the TV can adequately supply it.

In valve TV's it may be necessary to provide a separate mains power supply from a small transformer. This should be carefully positioned to avoid any interference with the TV set from the field of the transformer.

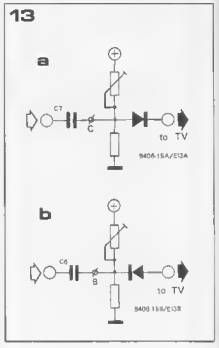
Figure 13a and 13b. Circuits for direct injection of time signal into TV video output stage.

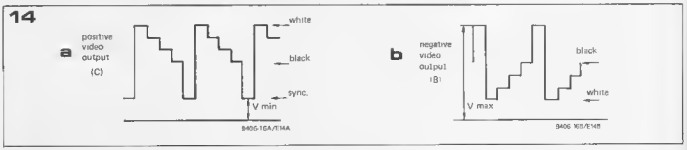
Figures 14a and 14b. Positive and negative video waveforms.

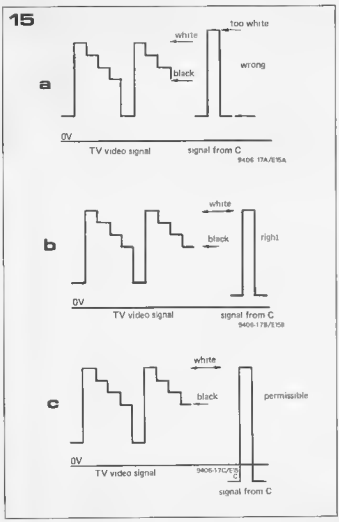
Figure 15. Showing correct and incorrect adjustment of bias potential in figure 13.

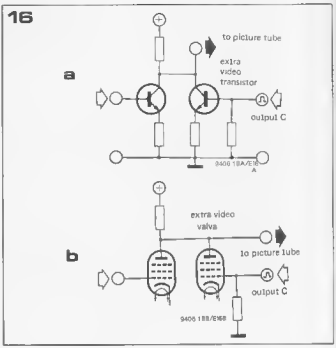
Figures 15a and 16b. Interfacing by means of parallel video output transistor or valve.

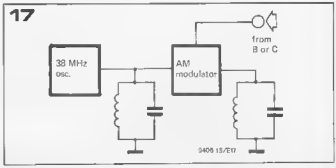
Figure 17. Interfacing by injection of modulated signal into the vision i.f.









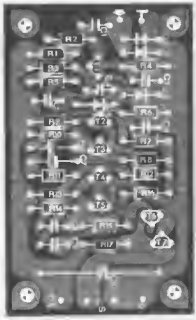


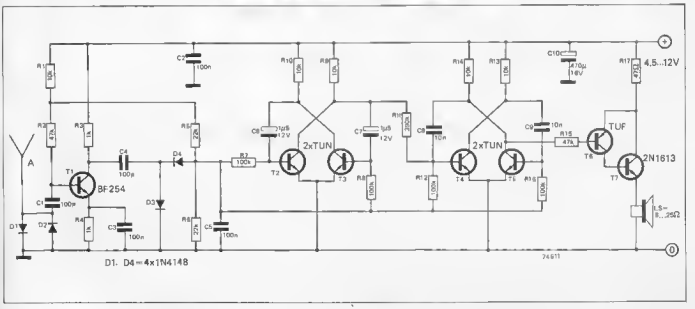
alignment squeaker

or an 'audible signal-strength indicator'

The alignment squeaker's main use is for the adjustment and alignment of transmitters and antennas. To ensure a true indication of the field strength, the measurement should be carried out at some distance from the transmitting antenna. Since meters are somewhat difficult to read at any distance over a few feet some alternate solution had to be found. An audio indicator, which could be heard over a distance of say 100 feet, seemed to be a logical solution to the problem and since the human ear is much more sensitive to changes in frequency than to amplitude changes, this unit was designed to change pitch as the field strength varies.

The RF signal received by the rod antenna 'A' in the squeaker is amplified by T1 and the signal is then detected (rectified) by diodes D3 and D4. This detected signal drives two multivibrators in such a way that their frequencies increase with the antenna signal. Furthermore, to improve the perception of field changes, the multivibrator consisting of T2 and T3 modulates the multivibrator comprised of T4 and T5. The interaction between these two multivibrators makes the slightest RF field change noticeable. The circuit can be used for frequencies between 100 kHz and 200 MHz, although it is less sensitive above 30 MHz. A difference in field strength of 1 or 2 dB is clearly noticeable; and the unit can be used with transmitters with an output power as low as 10 mW.





SQ decoder

part 2

Last month we published the circuit of the SQL-200 SQ decoder, with a printed circuit board design as supplied by CBS. Since our circuit board design staff felt they could do a better job (!), they were given the go-ahead. The new design, as published here, will now be made available through the EPS service.

The main reason for designing a new board was the fact that the transistors and potentiometers used by CBS have rather unusual pinning. The new board design will accept both the original suggested transistor types and the more common European equivalents. To clarify matters, the collector, base and emitter connections are marked on the board.

Furthermore, the board will accept both the DIL and the metal can version of the μA723 (IC6).

During lab tests of the new board, one or two problems arose. These have led to one or two minor modifications of the circuit.

Capacitors C32 and C26 have been turned round, since the voltage at the IC3 end proved to be the more positive.

Transistors T7 . . . T10 would have to have a very high current gain indeed for this to be otherwise.

C42 and C43 are now shown as electrolytics, since any other type would take up too much room. Tantalum electrolytics should be used here.

One of the four emitter followers (T7 . . . T10) proved to be unstable. This was quite obvious, since the output sounded very distorted and an FM receiver started to howl. The solution was simple: an extra resistor R_X was included close to the offending transistors base. Should this problem arise, the extra resistor can easily be included on the board: there are two additional holes connected by a narrow track in series with each base connection. These holes are marked with an asterisk. If the additional resistor is required, break the track between the holes and mount the resistor instead.

In the stereo position, the two unused emitter followers (T8 and T10) caused problems. This is solved by connecting their inputs to ground through S1b and S1d.

The position 'Rxy' on the board is for an alternative option. To get a slightly more 'forward facing' reproduction, the CF sounds can be raised by 1.2 dB. This is accomplished by changing the values of R42 and R57 to 3k3 and adding an 18 k resistor in the Rxy position.

The 'brass shield' does not necessarily have to be brass. A piece of printed circuit board with two wires soldered on it will do just as well.

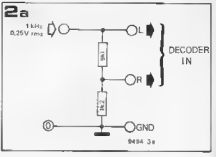
Adjustments

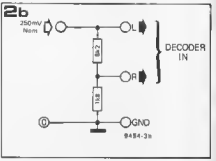
The power supply voltage is set at 20 V with R105.

The only other adjustment is the variable blend setting.

Connect a voltmeter ($\geq 20\,k\Omega/V$) between the positive lead of C29 and supply common. Connect the appropriate resistive network shown in figure 2 to L_T and R_T. Drive a constant music signal, or a 1 kHz sinewave into the network. While the audio is applied, note that if R73 is rotated from one end to the other end, the voltage of C29 varies from a high level (8 volts or more) down to almost 0 volts. This indicates the correct performance. Now, set the potentiometer so that C29's voltage just reaches the lowest value. You will find this setting to be very sensitive . . . this is because you are setting the threshold at which the FET *switches* (when T12 drops to near 0 volts) and the gain of T12 is very high.

For further checkout and operating suggestions, see the previous article in Elektor 17.





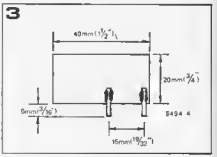


Figure 1. Complete circuit of the SQ logic decoder.

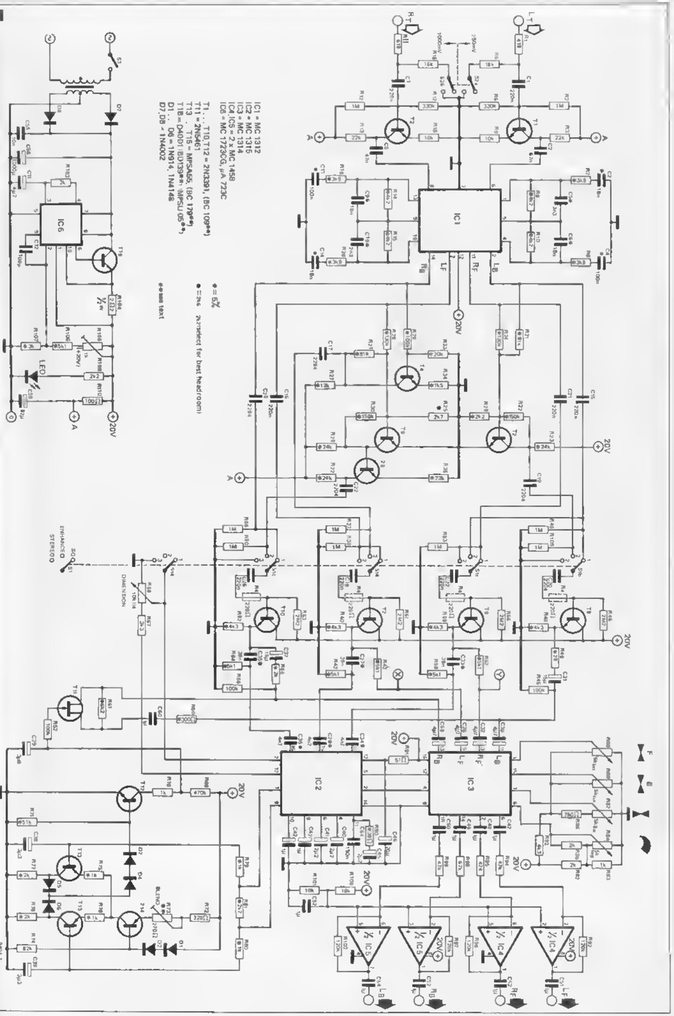
Figure 2a. Network for variable-blend adjustment when using a 1 kHz sine-wave. The outputs from this network are fed to the L_T and R_T inputs of the decoder.

Figure 2b. Network for variable-blend adjustment when using a music source.

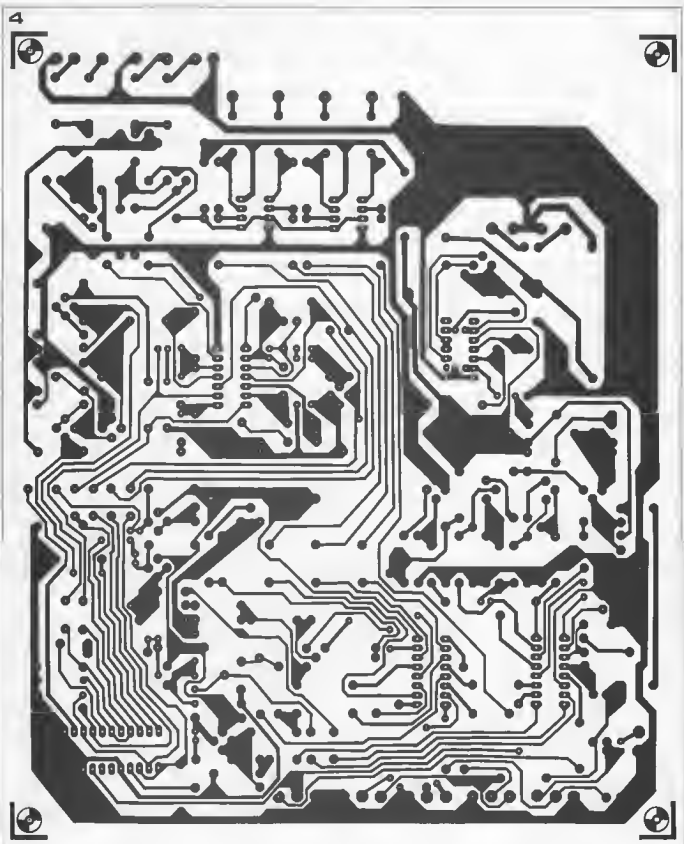
Figure 3. This brass shield should be mounted on the p.c. board between the mains transformer and the output amplifiers. A small piece of printed circuit board can also be used.

Figure 4. Component layout and p.c. board for the decoder.

1


IC1 = MC 1312
IC2 = MC 1315
IC3 = MC 1314
IC4, IC5 = 2 x MC 1458
IC6 = MC 1723CG, µA 723C
T1 ... T10, T12 = 2N3391, (BC 109**)
T11 = 2N5461
T13 ... T15 = MPSA55, (BC 179**)
T16 = D40D1 (BD139**: MPSU 05**)
D1 ... D6 = 1N914, 1N4148
D7, D8 = 1N4002
* = 5%
• = 2k6 2k2 (select for best headroom)
** see text
ENHANCED STEREO
SQ
DIMENSION
BLEND
LED
20V

4

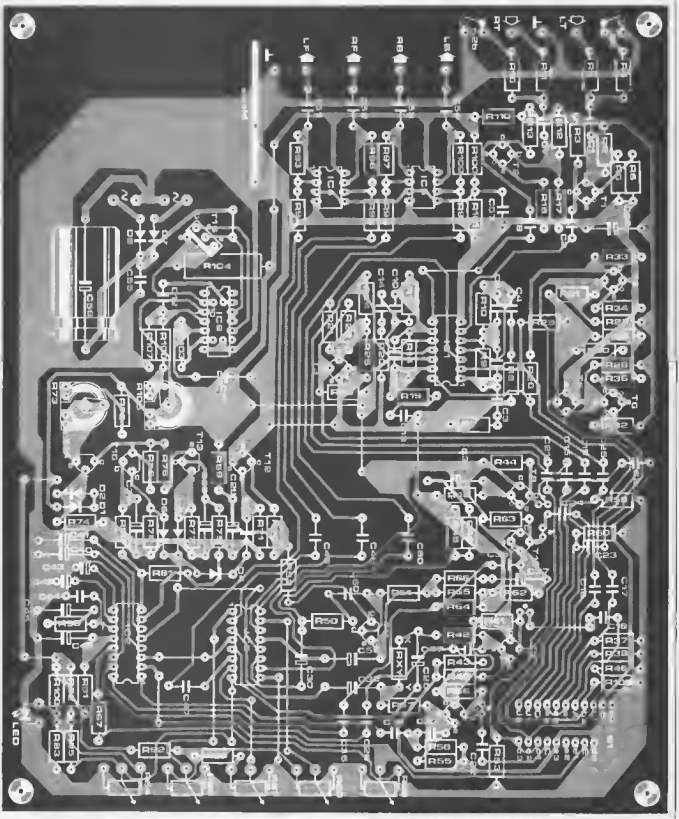


Parts list

Resistors
R1,R11 = 47 k
R2,R12,R37,R38,R48,R53,R59,R60, R109 = 1 M
R3,R13 = 22 k
R4,R15 = 15 k
R5,R17 = 330 k
R6,R16,R100,R101 = 10 k
R7,R8,R19,R20 = 3k9 (5%)
R9,R10,R14,R15 = 4k7 (5%)
R21,R31 = 91 k (5%)
R22,R30 = 150 k (5%)
R23,R29,R32 = 24 k (5%)
R24,R25 = 130 k (5%)
R25 = 2k2 (5%)
R26 = 100 k (5%)
R27 = 12 k (5%)
R33 = 20 k (5%)
R34 = 1k5 (5%)
R35 = 2k7
R36 = 22 k (5%)
R40,R48,R55,R62 = 4k3 (5%)
R41,R44,R68,R83 = 2M2
R42,R43,R57,R58,R64,R106 = 5k1 (5%)
R45,R52,R65 = 100 k
R49,R66,R77,R78 = 2 k (5%)
R50 = 30Ω (5%)
R51 = 5k2 (5%)
R67 = 2k2
R69 = 470 k
R70,R83 = 1 k
R71 = 51 k (5%)
R72 = 220 Ω
R74 = 82 k
R75,R76,R79,R80 = 1 k (5%)
R81 = 2k7 (5%)
R82,R85,R103 = 2 k
R86 = 750 Ω
R90 = 30 Ω (5%)
R91 = 51 Ω
R92 = 4k3
R93,R96,R97,R102 = 120 k
R104 = 20Ω/¼ W (5%)
R107 = 3 k (5%)
R108 = 2k2
R110 = 100 Ω
R68 = 10 k lin potentiometer
R73 = 270 Ω preset
R84 = 5 k log potentiometer
R87,R88,R89 = 5 k lin potentiometer
R105 = 1 k preset

Capacitors
C1,C7,C15 . . C25 = 220 n
C2,C5 = 47 n
C3,C6,C9,C14 = 18 n (5%)
C4,C13 = 100 n (5%)
C8,C10 = 3n3 (5%)
C11,C26,C30,C32,C33 = 4µ7/25 V

4



C12 = 100 p
C27,C33,C35 = 39 n (5%)
C28,C34,C36 = 4n7 (5%)
C29 = 3u9/25 V (tantalum)
C31,C37 = 15 µ/25 V
C38,C39 = 3u3/25 V
C40,C41,C45 = 2u2/25 V
C42,C43,C47 . . C54,C57,C60 = 1 µ (not electrolytic)
C44 = 150 n
C46 = 20 . . 22 µ/25 V
C55 = 10 n
C56 = 1000 µ/35 V
C59 = 47 µ/25 V

Semiconductors
T1 . . T10,T12 = 2N3391,MPS6520, 9C109
T11 = 2N5461
T13 . . T15 = MPSA55, BC179
T16 = D40D1, MPSU05, BD139
IC1 = MC1312P
IC2 = MC1315P
IC3 = MC1314P
IC4,IC5 = MC1458CP, MC5558CP
IC6 = MC1723CG, µA723C
D1 . . D6 = 1N914
D7,D8 = 1N4002
D9 = LED

Sundries
Mains transformer, secondary 2 x 18 . . 24 V, 125 mA.
Selector switch, SPST (five pole, three way), preferably make before break
Mains fuse and fuseholder, if required, 250 mA fast blow for 220-245 V mains; 500 mA fast blow for 110-145 V mains.

To raise CF sounds by 1.2 dB, change the values of R42 and R57 to 3k3 and add resistor Rxy = 18 k.
NOTE THAT THE SUPPLY VOLTAGE MUST BE SET AT 20V WITH R105 BEFORE IC1 . . . IC5 ARE MOUNTED ON THE BOARD.

digits on TV

W. Frenken

This circuit can be used to display a row of up to eight digits on a TV screen. It gives a video output consisting of horizontal and vertical synchronisation pulses and the black/white pattern corresponding to the digits in seven segment format.
It will accept an eight-digit parallel input and, as an example, the circuit of an eight-decade frequency counter is also given.
Leading-zero blanking is included in the design.

There are numerous applications for a circuit that will display digits on a TV screen. The maximum number of digits that will fit on the screen depends, of course, on the size chosen. For most applications the size chosen here should be suitable: eight digits over the full width of the screen. In principle, the system can be used to give up to five rows, or a total of 40 digits. However, in this circuit the display is limited to one row.

The digits are 'written' on the screen as a pattern of white dashes, stacked vertically on top of each other. The European TV system has 625 lines for each complete picture, and each picture is built up in 40 ms (two 'fields' of 20 ms each). This means that each line takes 64 μs. The line sync pulse takes 12 μs, leaving 52 μs for the visible portion of each line.

It so happens, as we will see later on, that it simplifies matters to use multiples of 1 μs for all the time-slots. Since we want eight digits in a row, with gaps between them, an obvious 'binary' choice is 2 μs per digit with 2 μs gaps. This will give digits that are nearly one inch wide (2 cm) on a large screen.

The seven-segment digits are built up as shown in figure 1. Letters A to G indicate the seven segments, and each digit consists of two or more of these segments. Since the digit width is 2 μs, the shortest time-slots (t1 and t3) are only ½ μs – but this will not present any problems.

The next point is to choose the correct height. The height of one vertical unit (L1, for instance) should be the same as one horizontal unit. The horizontal unit is ½ μs, which is $\frac{1}{104}$ times the length of one line – the duration of one (visible) line is 52 μs. Since the width-to-height relationship of a TV picture is 4:3, the 'vertical unit' must be

$$\frac{4}{3} \times \frac{(312.5 - 20)}{104} = 3.75 \text{ lines}$$

in each field (the duration of each visible field is $\frac{625}{2} - 20$ lines). This is not easy to obtain, so 4 lines are used instead – a nice round binary number ... The digit height is then 24 lines per field (48 lines per picture), or just over one inch (3 cm).

Timebase generator

The first requirement for a stable picture is that it is built up at a speed that is 'TV compatible'. Furthermore, the digit generator and the television set must run in synchronism. Both requirements can be met by using a sync generator that runs at normal TV speed, and using this to generate the digit pattern.

The basic timebase is shown in figure 2. The clock generator consists of N1 and N2 with the 1 MHz crystal. This drives a divide-by-eight counter (FF1 to FF3) which, in turn, drives a second divide-by-eight counter (FF4 to FF6). The total division ratio is therefore 64, so that the output period time is 64 μs – the line frequency. The simplicity of this division is one of the main reasons for choosing 1 μs as the basic time unit! At this stage, it is interesting to mention the so-called octal way of counting. Since binary systems work in powers of 2, basic counts are 2, 4, 8, 16, 32, etc, corresponding to the basic counts in 'normal' decimal counting of 9, 99, 999, etc. 'Octal' counting groups three basic binary counts together, and uses decimal numbers. The basic counts are then 7, 77, 777, etc. To give a few examples: binary 1 is octal 1; binary 11 is octal 3; binary 101.110 is octal 56. To distinguish octal numbers from decimal numbers, an extra 8 is added, thus: 56_8 (octal) = 46 (decimal). The two divide-by-eight (= octal) counters therefore count from 00_8 to 77_8.

The total picture consists of 625 lines and two fields. This means that the field synchronisation is required every 312.5 lines, or, to put it differently, every 625 half-lines. The output of FF5 corresponds to half-lines. This output is connected to four divide-by-five counters in cascade (IC4 ... IC7). The output of FF7 can now be used for field sync.

Sync generator

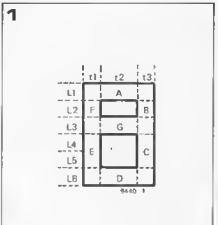
The actual sync signals required are rather more complicated. The outputs of the counters FF1 to FF6 and IC4 to IC7 are connected to the video generator shown in figure 3.

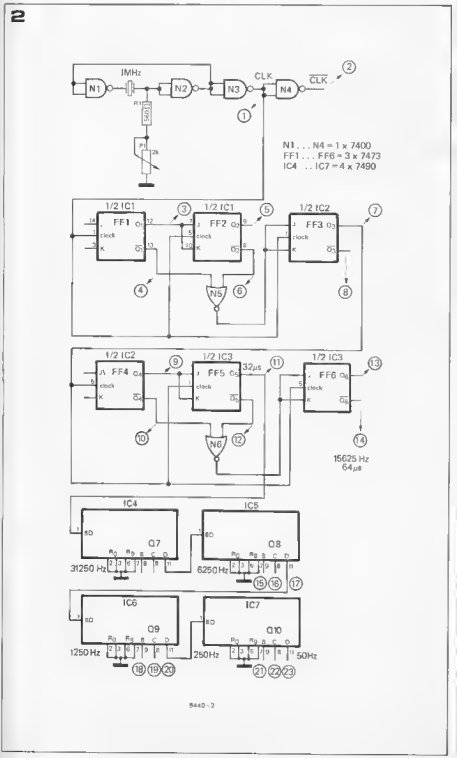
The line sync pulse $\overline{LSY}$ (output from N27) is derived from Q3 to Q6, so it lasts from 111 100 to 111 111, or $74_8 \ldots 77_8$, which is 4 μs (see table 1 and figure 4). The 'blacker-than-black' signal, or line blanking ($\overline{LBL}$, output of N12), lasts from 72_8 (through 77_8 and 00_8) to 05_8. This corresponds to 58 μs in one line through to 5 μs in the next line. The total duration is therefore 12 μs, with the 4 μs sync pulse 'off-centre' in the middle.

Something similar is required for the field sync. The field sync pulse itself, $\overline{FSY}$, lasts from half-lines 590 ... 594; the equalizing pulses $\overline{FSE}$ from 585 ... 589 and from 594 ... 599; and the field blanking $\overline{FBL}$ (blacker-than-black) from 585 ... 624. To be slightly more specific, the sequence is as follows. During the first five half-lines, 585 ... 589, the output of N19 ($\overline{FSG}$) is low. This allows the equalizing pulses $\overline{EQP}$ from N20 to pass gate N22, and from there through N26 to the output. During the next five half-lines, 590 ... 594, the output from N18 (field sync, FSY) is high. This field sync pulse is mixed with the equalizing pulses $\overline{EQP}$ in gate N25, giving the output $\overline{FSY}$. Finally, during the third five half-lines, 595 ... 599, the second set of equalizing pulses are passed through gates

Figure 1. Seven-segment display format on the TV screen. The digits are 2 μs wide (t1 + t2 + t3) and 6 'vertical units' high. Each vertical unit is a total of 8 lines on the screen.

Figure 2. The timebase generator, comprising a 1 MHz clock generator, a 1 . . . 64 μs divider and a half-line counter.





N22 and N26. During this whole period (585 . . . 599) the output of N24 is low, providing the first part of the frame blanking $\overline{FBL}$; during the following period (600 . . . 624) gate N13 takes over this frame blanking function.

The normal line sync (LSN) is blocked by gate N23 during the field sync sequence.

The function $\overline{END}$ corresponds to the end of each field (half-lines 575 . . . 599), and it can be useful for synchronising external circuits.

The video input is connected to N28. Resistors R3, R4 and R5 are a simple digital-to-analog converter which produces the correct video output levels for the various signals:

'white' = 100%;
'black' = 35% ($\overline{BLA}$);
'blanking' = 30% ($\overline{LBL}$ and $\overline{FBL}$);
'sync' = 0% ($\overline{SYP}$).

Character generator

The circuits described so far produce basic timebase outputs (from ½ μs to field sync) and all necessary sync pulses. There is also an input for digital video signals. The next step is to produce digits in the desired video format.

The height of the characters is determined by the 'vertical unit': 4 lines. In figure 5, the input is at line frequency. Two flip-flops (FF7 and FF8) are used as a divide-by-four counter; output Q13 is the 'vertical unit'. The following three flip-flops (FF9 to FF11) form a vertical unit counter, and the six vertical units required (L1 . . . L6) can be derived from their outputs.

Gates N35 and N36 form a flip-flop. When this is set, output Q11 holds FF7 . . . FF11 in the reset condition, so that no digits can be generated. Gate N34 produces the signal DST (display start), resetting flip-flop N35/N36. This enables the other flip-flops, but it takes a further four lines for Q13 to change state for the first time, starting the character generation. If the inputs to N34 are connected as shown, the digits will be written at the bottom of the screen.

The vertical unit counter counts from L0 to L6. When it switches to L7, flip-flop N35/N36 is set by gate N33. This, in turn, resets and blocks FF7 . . . FF11. End of digit.

The width of the digits is determined by the horizontal units: ½ μs, 1 μs and ½ μs for t1, t2 and t3 respectively. These units are derived from the timebase generator by part of the circuit shown in figure 6.

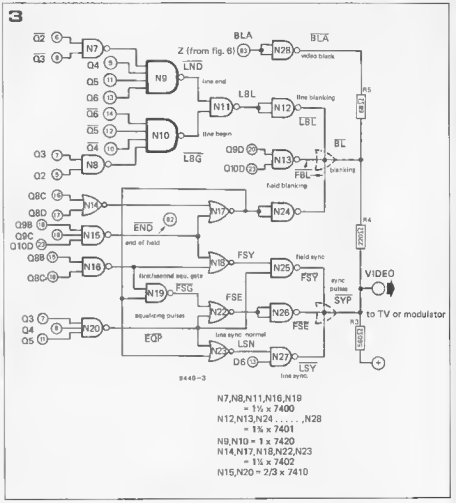
N56 derives t1 from Q1, $\overline{Q2}$ and CLK, so t1 corresponds to the first ½ μs out of every 4 μs. N57 produces t2, the following 1 μs; finally, N58 produces t3, the final ½ μs. After a further 2 μs (the gap between digits), the cycle is repeated. This total cycle, corresponding to digit-plus-gap, is repeated 16 times for each line, or 13 times for the visible portion of each line.

These horizontal units t1 . . . t3 are now combined with the vertical units L1 . . . L6 from figure 5 and the seven-

segment signals a . . . g to produce the total video output BLA. As an example, segment A is formed as follows.
Horizontal units t1 . . . t3 are combined in N62, giving a signal over the full width of the digit. Vertical unit L1 and seven-segment signal 'a' are combined in N59. The outputs from N62 and N59 are then combined in N63 to produce the video output Ā, corresponding to segment A in the display.
Gates N52 and N54, wired into the 'segment A' circuit, give a certain 'finesse' to the unit . . . The seven-segment decoder used gives a basic '6', that is, the top bar (segment A) is missing. However, a clearer display is obtained when this segment is added. If the A segment is driven whenever the D and G segments are 'on', the only difference is that this top bar is added to the '6'.
Gates N53 and N55 perform a similar function to improve the display of the '9'.
The digital video output BLA can be connected to the video input in figure 3 (N28) to give white digits on a black background. If black digits on a white background are required, an inverter will have to be connected in series. If both options are required, an exclusive-or gate can be connected in series, with a switch between the other input of this EXOR and ground.
In the discussion so far we have simply assumed that seven-segment signals a . . . g are available. Happily, they are not difficult to obtain. The BCD to seven-segment decoder is shown in figure 7.
The decoder is a 7447 (IC8). Under normal conditions it converts a binary code to a seven segment output. Its output is only enabled during the time that digits are being displayed (DPT = display time) and the time that the digits are not changing (PLG = parallel load gate). These functions will be explained further on.
The 'lamp-test' input is connected to S1 — after all, if an input is available, why not use it? This simply produces an '8' at the output, i.e. all seven segments, so that it gives a quick check of the logic circuits. The display should be 88888888 when this switch is closed.

Display generator

The eight-digit display is derived from a frequency counter. The circuit (figure 8) is not very sophisticated, since the main purpose is simply to derive eight digits to drive the display. It is simply one example of how to drive the rest of the circuit.
The frequency counter consists of eight decade counters (IC14 . . . IC21). The input count pulse (CTP) comes from the input gate N67. The input frequency is applied to the input (INP), as one would expect . . . The 50 Hz output from the main timebase (Q10D in figure 2) is divided by 50 in IC12 and IC13 to produce a 1 second output which drives the input gate.
During the time that Q18A is low



N7,N8,N11,N16,N18 = 1½ x 7400
N12,N13,N24 . . . . . ,N28 = 1½ x 7401
N9,N10 = 1 x 7420
N14,N17, N18,N22,N23 = 1½ x 7402
N15,N20 = 2/3 x 7410

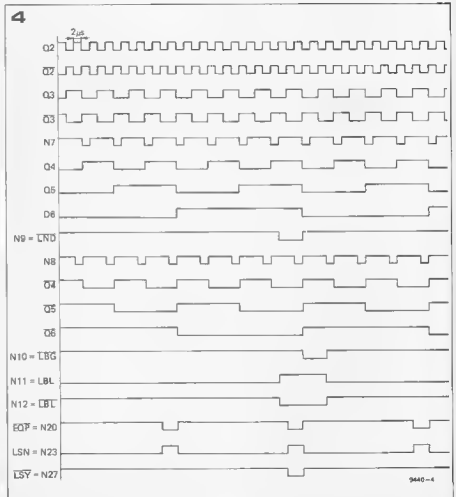


Figure 3. The sync generator. This produces the line and field sync pulses, line and field blanking, and includes a video input.

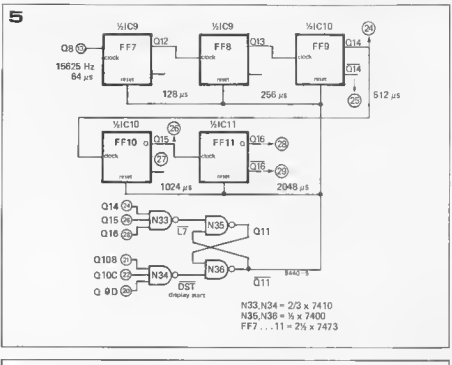
Figure 4. Pulse diagram showing the derivation of the line sync (LSY) and line blanking (LBL) pulses.

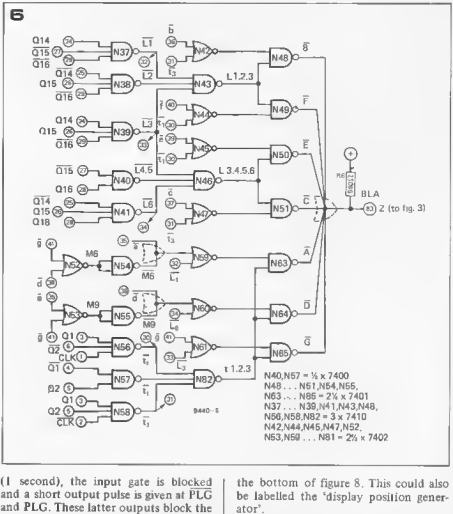
Figure 5. The vertical unit counter. This also produces the 'display start' signal corresponding to the top of the display.

Figure 6. The horizontal unit counter and seven-segment to video encoder.

Table I. Part of the counting sequence of the two divide-by-eight counters (FF1 . . . FF6).

n_{10} decimal count	'8's Q6	Q5	Q4	'1's Q3	Q2	Q1	n_8 octal count
0	0	0	0	0	0	0	00
1	0	0	0	0	0	1	01
2	0	0	0	0	1	0	02
3	0	0	0	0	1	1	03
4	0	0	0	1	0	0	04
5	0	0	0	1	0	1	05
6	0	0	0	1	1	0	06
7	0	0	0	1	1	1	07
8	0	0	1	0	0	0	10
9	0	0	1	0	0	1	11
10	0	0	1	0	1	0	12
11	0	0	1	0	1	1	13
⋮							
26	0	1	1	0	1	0	32
27	0	1	1	0	1	1	33
28	0	1	1	1	0	0	34
29	0	1	1	1	0	1	35
30	0	1	1	1	1	0	36
31	0	1	1	1	1	1	37
32	1	0	0	0	0	0	40
33	1	0	0	0	0	1	41
⋮							
59	1	1	1	0	1	1	73
60	1	1	1	1	0	0	74
61	1	1	1	1	0	1	75
62	1	1	1	1	1	0	76
63	1	1	1	1	1	1	77
64	0	0	0	0	0	0	00





(1 second), the input gate is blocked and a short output pulse is given at PLG and PLG. These latter outputs block the seven-segment decoder (figure 7) and load the shift register (figure 9), as will be explained further on. Towards the end of the PLG pulse, the END pulse also appears (from figure 3) at the input of N66, producing a reset pulse (RES) for the eight decade counters IC 14 . . . IC21.

A completely separate unit within the display generator is the section shown at the bottom of figure 8. This could also be labelled the 'display position generator'.

The character generator (figure 5) determines the vertical position of the digits: the half-line counter is enabled by the DST signal. However, the horizontal position is still undetermined.

The unit is designed to produce a row of 8 digits. Each digit takes 4 µs, so the total display width (including the gaps between the digits!) is 8 x 4 = 32 µs. An exclusive-or gate (N72) is used to derive the 'display time' signal (DPT) from the

main timebase. This signal lasts 32 μs and it is positioned in the centre of each line.

Gate N71 derives a signal from the vertical time unit counter in the character generator (figure 5). This signal corresponds to the total vertical height of the digits. The combination of the horizontal display position DPT with the vertical display position signal from N71 results in a signal which corresponds to the exact position of the display: DSG. During this display period, pulse t3 from figure 6 is passed by gate N74. The result is a sequence of pulses which coincide with the end of each digit. This signal is used as 'clock' (SRC) for the shift register. This is the next part of the circuit to be discussed.

Display memory

During the 'count' period, the result of the preceding count must be stored somewhere. Furthermore, since there is only one character generator, the eight digits in the total display must be presented to this character generator one at a time and at the correct moments. Both of these requirements can be fulfilled by using a shift register as a memory.

This shift register (figure 9) uses eight ICs. It actually consists of four separate shift registers running in parallel, one for each binary 'bit'. The top shift register (IC22 and IC23) is used for storing the eight 'least significant bits' (Bit A) of the eight digits in the displays, so its output is connected to the 'A' input of the decoder (figure 7). The remaining three registers are used for bits 'B', 'C' and 'D' respectively.

At the end of each count period, the outputs of the eight decade counters in figure 8 correspond to the eight digits required for the display. The Most Significant Digit (i.e. the left-hand one) corresponds to the output of IC21, and so on down the row to the Least Significant Digit which corresponds to the output of IC14. The display on the TV screen is written from left to right, so the first digit will be the Most Significant Digit. The correct order to store the digits in the shift register is therefore: output from IC21 at the extreme right-hand end (the output), and all other outputs in order down the register from right to left.

The actual storing of the information into the shift register is controlled by the 'parallel load gate' signal PLG (from figure 8). This signal appears just before the start of each new count.

If no further action is taken, the Most Significant Digit will remain at the output of the shift registers. This digit will then appear eight times on the screen during the display period. Since this is not the intention, the shift registers must now be set into motion. This is what the 'shift register clock' signal is needed for.

As discussed in the previous section, the SRC signal consists of a sequence of pulses which coincide with the end of each digit. They are only present during the display period. The shift registers move their information up one position on the trailing edge of each clock pulse. This corresponds to the end of each digit.

The results are now as follows. At the beginning of each line of the display period, the Most Significant Digit is present (in binary code) at the output of the shift registers. After the corresponding pattern has been displayed, the shift registers move up one position so that the second digit is present at the output. After the pattern for this digit has been displayed, the shift registers advance again, and so on. As the information for the digits is shifted out at the right-hand end it is fed back in at the left, so that it is not lost.

Display blanking

The only part of the circuit not yet discussed is the lower part of figure 7: the display blanking.

The output of gate N29 is '1' outside the display time (DPT) and during the time that new information is being loaded into the shift registers (PLG). This 'DBL' signal is inverted by N30 and drives one of the display blanking inputs of the decoder. The result is that all outputs go to '1' and none of the seven segments can be displayed.

Furthermore, flip-flop N31/N32 is reset and the output of N31 drives the other display blanking input. Since the DST signal corresponds to the true display time, including the horizontal boundaries, this flip-flop is reset during each line after the pattern for the last digit has been displayed. The display blanking now remains operative until the flip-flop is set.

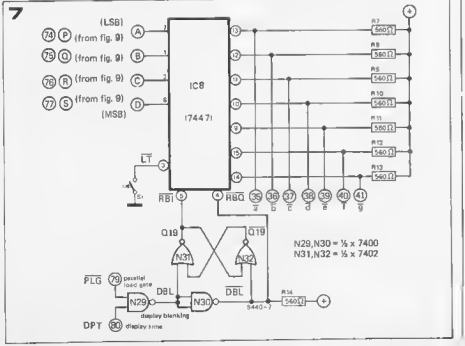
As soon as the display time is reached during the next line, this overriding reset is removed. However, this does not mean that the flip-flop is automatically set. For this to happen, the RB0 output of the decoder must become logic '1' (note that 'RB0' can be used both as input and as output!). This output remains '0' as long as a zero is present at the decoder input, however. The result is that any 'leading zeroes' are suppressed: the display blanking remains operative.

As soon as a digit is presented to the decoder that is not zero, RB0 becomes '1'. This sets the flip-flop, and all further digits (including any zeroes) are displayed until the DPT signal again resets the flip-flop. ■

Figure 7. The binary to seven-segment decoder. The circuit includes display blanking and leading zero blanking.

Figure 8. The frequency counter end shift register clock pulse generator.

Figure 9. The shift register.



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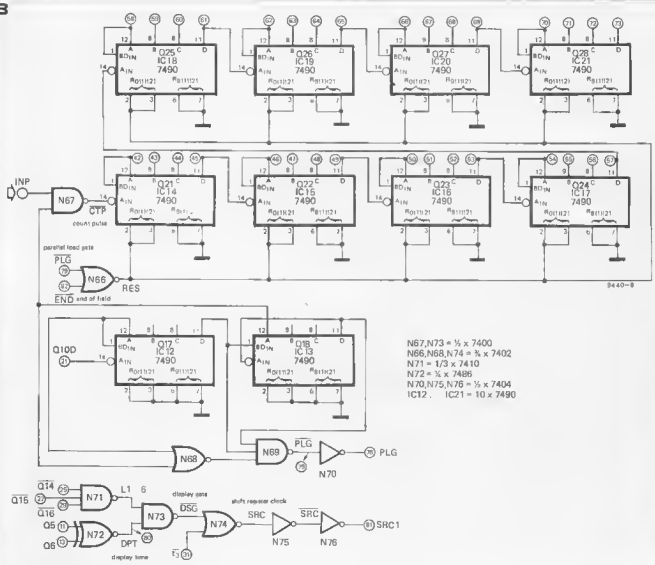
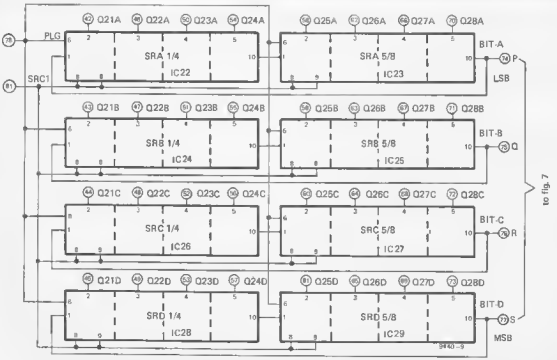

IC18 7490
IC19 7490
IC20 7490
IC21 7490
IC14 7490
IC15 7490
IC16 7490
IC17 7490
IC12 7490
IC13 7490
INP
N67
CTP
count pulse
parallel load gate
PLG
N66
RES
END end of field
Q10D
N68
N69
PLG
N70
PLG
Q14
Q15
Q16
Q5
Q6
N71
N72
DPT
display time
L1 6
display gate
DSC
N73
N74
shift register clock
SRC
N75
SRC
N76
SRC1
N67,N73 = ¼ x 7400
N66,N68,N74 = ¾ x 7402
N71 = 1/3 x 7410
N72 = ¼ x 7486
N70,N75,N76 = ½ x 7404
IC12 . IC21 = 10 x 7490
9440—8

9


PLG
SRC1
SRA 1/4 IC22
SRA 5/8 IC23
SRB 1/4 IC24
SRB 5/8 IC25
SRC 1/4 IC26
SRC 5/8 IC27
SRD 1/4 IC28
SRD 5/8 IC29
BIT-A LSB
BIT-B
BIT-C
BIT-D MSB
to Fig. 7
9440—9
SRA . . .SRD = B x 7495

dual voltage regulators

In the article 'Integrated Voltage Regulators' (Elektor 11 and 12) positive and negative IC voltage regulators of both fixed and variable voltage types were discussed. This article is intended as a follow-up and looks at dual regulator ICs (i.e. those that provide both a positive and a negative output). Practical designs are presented for laboratory power supplies providing up to ±30 V at 2 A.

Since the vast majority of electronic circuits are designed for a positive supply rail the first IC voltage regulators were, quite naturally, designed to provide a positive voltage.
In particular ICs were designed to provide 'on-card' stabilizing for logic circuits. Since the demand for negative voltage regulators was less, these were developed later and fewer types are available (see tables 1 and 2 p. 437 Elektor 12).
With the proliferation of operational amplifiers, audio amplifiers using op-amp techniques, analogue comparators and other ICs requiring a positive and negative supply, dual regulator ICs have been introduced.

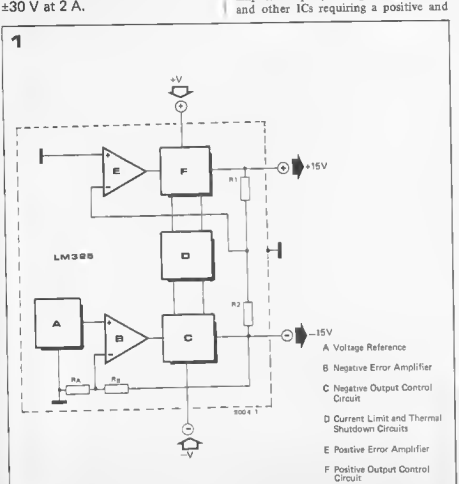
Tracking regulators

Most manufacturers of dual regulators use the 'tracking regulator' principle. Basically this means that both the positive and negative halves of the regulator use a common reference voltage, and the circuit is so designed that any voltage variations in one of the outputs will be followed by the other output. For example, if the positive supply of a dual regulator is designed to track the negative supply then, should the negative supply go more negative due to temperature drift or load variations, the positive supply will go more positive. This is particularly important in operational amplifier circuits, where the DC conditions in the circuit may be affected by the symmetry of the supply voltages.
An example of a dual tracking regulator, the National Semiconductors LM325, is given in figure 1, which shows the internal block diagram of the IC. The negative output voltage is obtained in the usual manner. A negative reference voltage (A) is fed into the non-inverting input of an amplifier (B). This drives the regulator output stage (C) and a voltage is fed back to the inverting input via the potential divider R_A/R_B. The amplifier drives the output stage until the output voltage (−15 V in this case) is such that the voltages on the inverting and non-inverting amplifier inputs are almost equal (within the limits determined by the loop gain). The output voltage is thus

$$V_{out} = V_{ref} \cdot \frac{R_A + R_B}{R_A}$$

The positive half of the regulator also has an amplifier and output stage, but in this case the non-inverting input is connected to the 0 V rail while the feedback is derived from the junction of the two resistors R1 and R2. The amplifier will adjust the positive output voltage until the voltage on its inverting input equals the voltage on its non-inverting input, which means that the voltage at

1



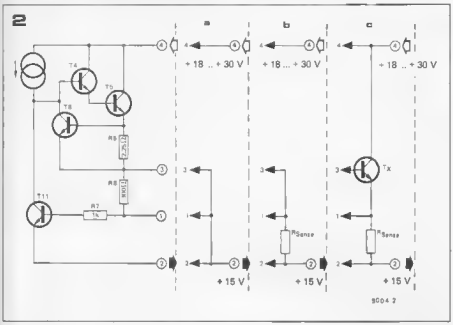


Figure 1. Block diagram of the LM326 dual regulator IC.

Figures 2 and 3. Positive and negative output stages of the LM325 showing the possibilities for external connections.

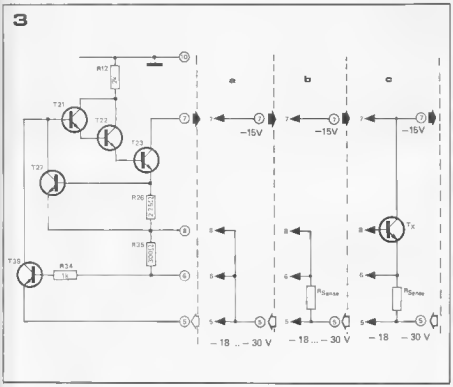
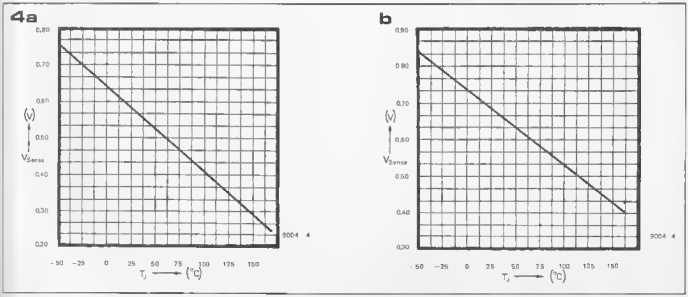


Figure 4. a. Graph showing temperature dependence of negative sense voltage.
b. Graph showing temperature dependence of positive sense voltage.



the junction of R1 and R2 must be zero. This means, for instance, that if R1 = R2 then the positive output voltage must always equal the negative output voltage.

If the positive and negative voltage are to be different then R1 and R2 are different. This is the case with the LM327 which provides a +5, −12 V supply. In this case R1 and R2 would be in the ratio 1:2.4.

Block D contains protection circuits that

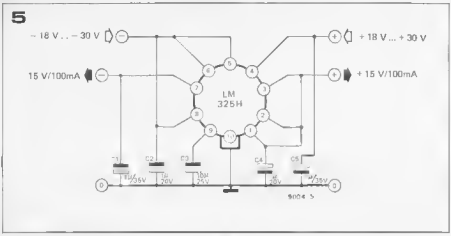
a. limit the output current
b. switch off the output if the IC becomes too hot (thermal overload).

The protection circuits operate on both the negative and positive outputs, so both supplies are well protected against thermal overload and short-circuited outputs.

Applications

The range of applications for the ICs in the National dual regulator series (LM325 − ±15 V, LM326 − ±12 V, LM327 − +5 V −12 V) become more obvious on studying the internal circuit of the IC, or at any rate the sections that are of interest. Figures 2 and 3 show partial circuits of the positive and negative output stages respectively, together with some possibilities for external circuitry to extend the range of applications. The ringed numbers correspond to the pin connections of the IC.

5



Internal current limit

Resistor R5 in the emitter lead of T5 is the internal current sensing resistor for the positive regulator. With pins 1, 2 and 3 of the IC connected together as shown in figure 2a, T8 will start to conduct as soon as the voltage drop across R5 reaches the base-emitter voltage of T8. This limits the base current into T4 and hence limits the output current. The output current limit is given by:

$$I_{lim}\ (amps) = \frac{V_{sense}}{2.25}$$

Where V_{sense} is the base-emitter voltage of T8 in volts and 2.25 is the value of R5 in ohms. The current limiting function for the negative supply is performed by R26 and T27 in figure 3a. The value of V_{sense} decreases with increasing temperature, so at high temperatures the current limit will operate at a lower current. Graphs of V_{sense} versus temperature are given for the negative regulator in figure 4a, and for the positive regulator in figure 4b. Figures 6a and 6b show how the onset of current limiting varies with temperature.

External current limit

If the short between pins 1 and 2 of the IC is replaced by a resistor as in figure 2b then the current limit can be controlled externally. When the voltage drop across Rsense reaches Vsense then T11 will turn on, limiting the base drive to T4. It is, of course, impossible to obtain an output current greater than that determined by the internal current limit, since this is still operative. R_{sense} must therefore always be greater than R5. The output limit current in this case is given by:

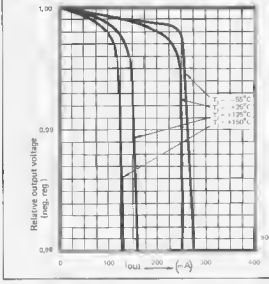
$$I_{lim} = \frac{V_{sense}}{R_{sense}}$$

The external current limit function for the negative regulator is performed by T39. The values for V_{sense} may again be obtained from figures 4a and 4b.

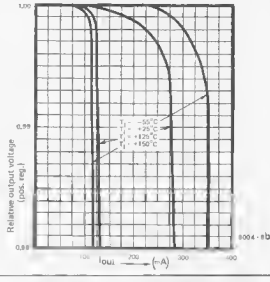
Increased output current

Like many other IC regulators, the output current of the LM325 series can be increased by adding an external power transistor. This is shown in figures 2c and 3c. Since the external transistor is not protected by the internal current limit it is essential to use an external current limit resistor. This is calculated in the same manner as for the current limit resistors in figures 2b and 3b, but there are now no restrictions on its value due to the internal current limit. Since the IC is now supplying only the base current for the external transistor then (if the external transistor has sufficient gain) several amps can be drawn

6a



b



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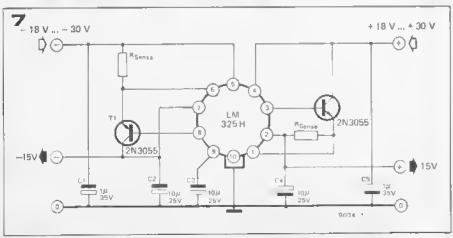


Figure 6. The most basic application of the LM325.

Figure 6. a. Graph showing onset of negative output current limiting at different temperatures.
b. Graph showing onset of positive output current limiting at different temperatures.

Figure 7. LM325 with external power transistors to increase the output current capability.

Figure 8. Functional block diagram of the Elektor PSU 76.

Figure 9. Prestabilizer section of the PSU 76.

before the internal current limit operates.

Practical circuits

The simplest circuit for a ±15 V regulator using the LM325 is given in figure 5. Pins 1, 2, 3 and 5, 6, 8 are joined as in figures 2a and 3a, so only the internal current limit is operative. The decoupling capacitors C1, C2, C4, and C5 improve ripple rejection and suppress any tendency to RF instability. They should be tantalum types. C3 suppresses noise generated by the internal voltage reference, and is only necessary if a very low noise level is required at the output.

±15 V 2 A regulator

The complete circuit of a ±15 V regulator with 2 A output current capability is given in figure 7. The sensing resistors can be chosen to give a current limit anywhere between 0 and 2 A. The popular 2N3055 power transistors are used as the output devices. It should be noted that 2N3055s are manufactured by two different processes, the planar process and the diffusion process. Those made by the planar method have a higher cutoff frequency (f_T) due to lower internal capacitances. These are preferable in this application as they introduce less phase shift into the circuit, and the danger of RF instability is consequently less. If 2N3055s with an f_T of less than 1 MHz are used then additional phase compensation may be required. C2 and C4 should be increased to 50 μ or greater and a 100 p capacitor may be connected between pins 8 and 9.

Elektor PSU 76

The LM325, 326 and 327 can supply only fixed voltages, but for laboratory use a variable supply is much more versatile. The Elektor PSU 76 is intended for use in laboratory or workshop and can supply independently variable positive and negative voltages from 0 to 15 V at currents of up to 1.2 A.

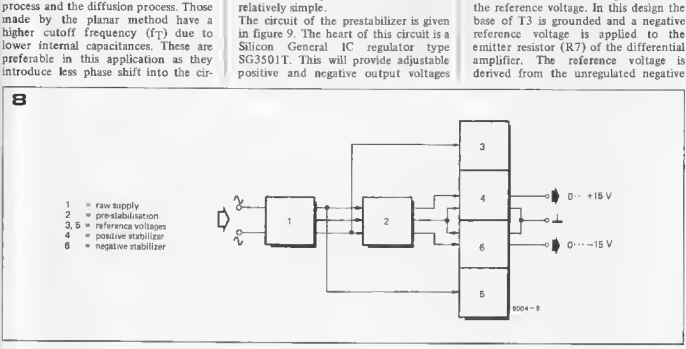
A block diagram of the PSU 76 is given in figure 8. The circuit is slightly unusual in that it incorporates, between the unregulated supply and the regulator, a prestabilizer stage. This takes the unregulated ±24 volt input and provides a prestabilized ±19 V output to the stabilizer. This means that the stabilizer does not have to cope with large line voltage variations and can be relatively simple.

The circuit of the prestabilizer is given in figure 9. The heart of this circuit is a Silicon General IC regulator type SG3501T. This will provide adjustable positive and negative output voltages that can be varied by P1. The outputs track so they are not (unfortunately) independently adjustable. The output current of the IC is increased by T1 and T2 while R4 and R5 set the current limit to about 1.2 A. There is thus no need for current limiting in the output stabilizer. Capacitors C3 and C4 suppress any tendency to HF oscillation, and they should be tantalum types. This also applies to C7 and C8.

Output Stabilizer

Figures 10 and 11 give the circuits of the positive and negative output stabilizers respectively. These are constructed entirely from discrete components and are of fairly conventional design, consisting of a differential amplifier, driver and series pass transistors. The only slightly unusual points in the circuits are the arrangements made to allow the output to be adjusted down to zero. In a more conventional design a positive reference would be applied to the base of T3, which would be balanced by a feedback voltage from the output to the base of T4. With such a design it is not possible to obtain an output less than the reference voltage. In this design the base of T3 is grounded and a negative reference voltage is applied to the emitter resistor (R7) of the differential amplifier. The reference voltage is derived from the unregulated negative

8



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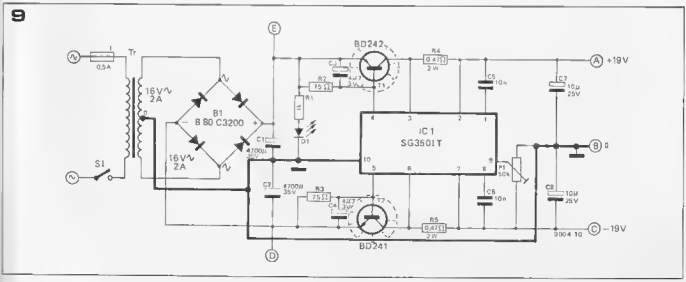
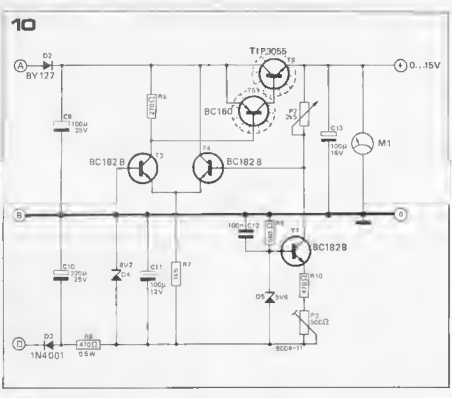
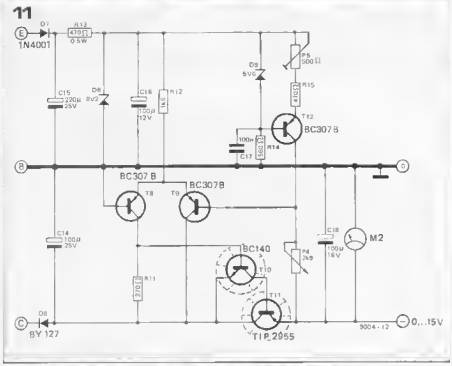






Parts list for figures 9, 10, 11, 12 and 13

Resistors.
R1 = 1 k
R2,R3 = 75 Ω
R4,R5 = 0,47 Ω, 2 W
R6,R11 = 270 Ω
R7,R12 = 1k5
R8,R13 = 470 Ω, 0,5 W
R9,R14 = 560 Ω
R10,R15 = 470 Ω
P1 = 50 k trimpot
P2,P4 = 2k5 lin.
P3,P5 = 500 Ω trimpot

Capacitors:
C1,C2 = 4700 µ, 35 V
C3,C4 = 4µ7, 3 V, tantalum
C5,C8 = 10 n
C7,C8 = 10 µ, 25 V, tantalum
C9,C14 = 100 µ, 25 V
C10,C15 = 220 µ, 25 V
C11,C16 = 100 µ, 12 V
C12,C17 = 100 n
C13,C18 = 100 µ, 16 V

Semiconductors:
IC1 = SG3501T (Silicon General)
T1 = BD 242, 2N4919
T2 = BD 241, 2N4922
T3,T4,T7 = MPS A18, BC 182 B
T5 = BC 160, 2N2561
T6 = TIP 3055
T8,T9,T12 = BC 307 B, MPS A70
T10 = BC 140, 2N1711
T11 = TIP 2955
D1 = LED
D2,D6 = BY 127 (50 V/5 A)
D3,D4 = 1N4001 or 1N4002 or 1N4003
B1 = B80C3200
D4,D8 = zener 8V2, 400 mW
D5,D9 = zener 5V6, 250 mW

Various items:
T_r = transformer 2 x 16 V, 2 A
M1,M2 = panel meters, 15 V f.s.d.
f = 0,5 A fuse, slow blow
S1 = mains switch

supply (point D in figure 9) and is stabilized by D4. Instead of the usual potentiometer to vary the feedback voltage and hence the output, the PSU 76 uses a potentiometer connected as a variable resistor in series with a constant current source T7. The current supplied by T7 is adjusted by P3 to about 7 or 8 mA, so that with P2 at maximum resistance the voltage on the base of T4 is slightly negative.

The negative output regulator (figure 11) is simply a mirror image of the positive regulator, so the foregoing remarks apply to this also, except that negative becomes positive and vice versa. A printed circuit board and component layout for this power supply are given in figures 12 and 13.

±30 V 2 A regulator

If the facility for independent adjustment of the positive and negative output voltages is not required then a much simpler circuit may be designed. Figure 14 shows the circuit of a ±30 V 2 A regulator based on the Raytheon RC4149. This IC will supply output voltages continuously variable between ±50 mV and ±30 V. The maximum output current of the IC is 150 mA for the DIL package and 200 mA for the TK package (metal can similar to TO-66). The IC has thermal protection that shuts down the outputs at a chip temperature of +175°C.

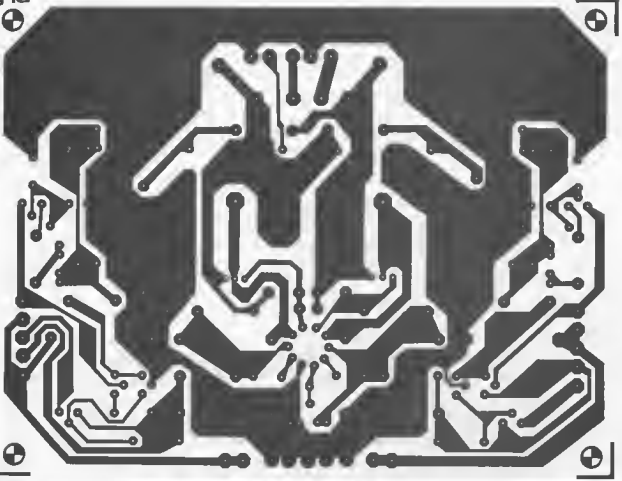
In the circuit of figure 14 the output current capability of the IC is increased by T1 and T2, and external current limiting is provided by T3 and T4 in conjunction with current sensing resistors R3 and R4. The output voltage is adjusted by P1. R5 determines the reference current fed into P1 and hence the output voltage range (scale factor) over which P1 is effective. 71k5 is the correct value for the output voltage

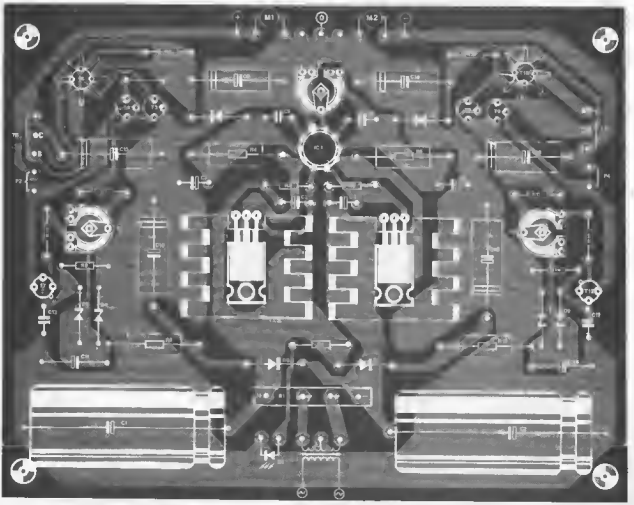
Figure 10. Positive output regulator of the PSU 76.

Figure 11. Negative output regulator of the PSU 76.

Figures 12 and 13. Component layout and p.c. board for PSU 76 (EPS 9004).

12,13





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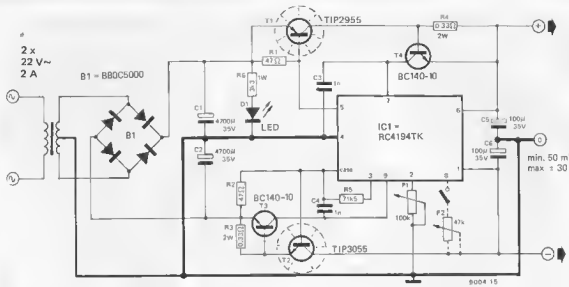
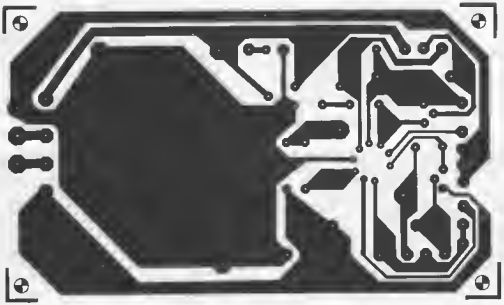

2 x
22 V~
2 A
B1 = B80C5000
B1
C1
4700µ
35V
D1
LED
C2
4700µ
35V
R1
470Ω
R6
1W
C3
1n
T1
TIP2955
R4
0.33Ω
2W
T4
BC140-10
IC1 =
RC4194TK
C5
100µ
35V
C6
100µ
35V
min. 50 mV
max. + 30 V
R2
470Ω
T2
BC140-10
C4
1n
R5
7k5
P1
100k
P2
47k
R3
0.33Ω
2W
T3
TIP3055
9004 15

15,16



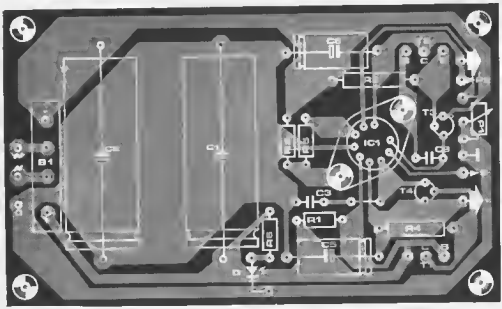

B1
C1
C2
IC1
T3
T4
R1
R2
R3
R4
C3
C4
C5
C6

Figure 14. ±30 V 2 A regulator. Outputs are not independently adjustable in this circuit.

Figures 15 and 16. Component layout and p.c. board for ± 30 V 2 A regulator (EPS 9005).

Figure 17. Pinouts of the ICs described in this article.

Parts list for figures 14 and 16

Resistors:
R1,R2 = 47 Ω
R3,R4 = 0.33 Ω/2 W
R5 = 71k5
R6 = 3k3, 1 W
P1 = 100 k lin.
P2 = 47 k lin.

Capacitors:
C1,C2 = 4700 μ, 35 V
C3,C4 = 1 n
C5,C6 = 100 μ, 35 V

Semiconductors:
IC1 = RC4194 (Raytheon)
T1 = TIP2955
T2 = TIP3055
T3,T4 = BC140-10, 2N1711
D1 = LED
B1 = B80C5000 (80 V, 5 A)

Various items:
T_r = mains transformer, 2 x 22 V/2 A

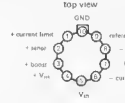
range 50 mV-30 V. If this is difficult to obtain then a 68 k may be used instead, but the output voltage with P1 at max will then not be exactly 30 V.
Some adjustment of the output voltages relative to one another is possible with the balance control P2, but its inclusion is not really recommended unless different positive and negative output voltages are really necessary. A switch is fitted since P2 must not be left in circuit when the positive and negative outputs are to be equal, as it will affect the balance even in its maximum position. With the value given P2 is effective only in the lower voltage ranges (up to about 15 V). For use above 15 V its value must be increased considerably, and this introduces further complications since additional decoupling is then necessary. A printed circuit board and component layout for the ±30 V 2 A regulator are given in figures 15 and 16. Note that the board is designed for the TK package version of the IC. Figure 17 gives the pinouts of all the ICs described in this article.

Constructional points

The most important constructional point is that all the power transistors must be adequately cooled. Remember that a stabilized supply is effectively a class A amplifier. Each of the devices in the 30 V regulator may have to dissipate over 70 W when the output is short-circuited, so the heatsinks should have a thermal resistance of less than 1°C/W if the temperature is not to rise more than 70° or so above ambient. In the PSU 76 design the dissipation is split between the power transistors in the prestabilizer and those in the output stage. The worst case dissipation in the output transistors occurs when the unit is supplying low voltages at 1.2 A, and is about 22 W. The worst case dissipation in the prestabilizer transistors occurs when the output is shorted with the output voltage set to maximum. The dissipation in each transistor is then about 28 W. Heatsinks with a 3°C/W thermal resistance would be adequate in this power supply.
Use caution when selecting the power transformer. The output voltage should not exceed 2 x 22 V (2 x 22 V is a good value). It is advisable to measure the voltage between the IC case connection and pin 5, before the IC is installed on the p.c. board. This voltage must not be more than 35 V DC, if it is, the IC will be damaged. A good safety margin is a good idea.

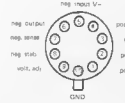
17

LM325H LM326H LM327H
top view

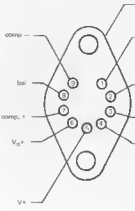


Caution,
pin 5 is connected
to the case

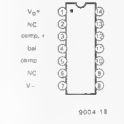
SG 3501
top view



RC 4194 TK
Bottom view



RC 4194 D
top view



9004 18

Literature:
National Semiconductor, Raytheon and Silicon General data sheets and application notes.

the LOUD mouth

Loud hailers are used wherever people need to make themselves heard over a large distance. The design described here is meant for use in cars and thus derives its power from the car battery. This means that the maximum voltage available is only 12 Volts, so some unconventional circuits are required to produce sufficient audio output power. A symmetrical output stage using a transformer is used to feed a 4 ohm loudspeaker, which results in a 16 to 1 power step-up when compared with a conventional push-pull arrangement. The amplifier operates in class C, which is a bit unusual for audio use. To reduce the effects of (class C) crossover distortion a high frequency bias is superimposed on the input audio signal. The effect of these somewhat unusual features are described in the following paragraphs.

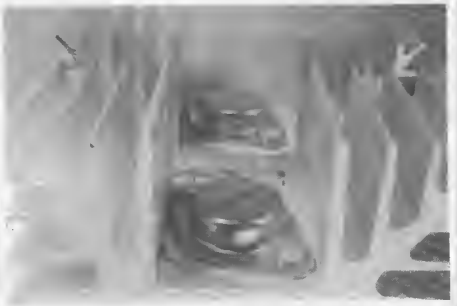
The primary power supply is limited to the 12 volts derived from the car battery. It would, theoretically, be possible to have this voltage stepped up by some sort of converter device which would enable a higher power output level to be obtained with a given loudspeaker impedance, but in practice this leads to poor efficiency and great expense. A more practical approach is required.

First, let us consider the problem in greater detail. The maximum power supplied by a single ended pushpull stage is roughly calculated from the following rule-of-thumb equation:

$$P_{max} = V^2/8R_L$$

in which V stand for the power supply voltage and R_L for the load impedance. This formula completely disregards all losses in the output stage. The actual maximum output power will be even lower. This means that for a 12 volt power supply and a 4 ohm loudspeaker the theoretical maximum output power (not including losses) would be approximately 4.5 W, obviously on the low side for a 'loud' hailing system.

Much more power for a given supply voltage can be delivered by a bridge-type output stage. This consists of two identical output stages driven in anti-phase. In this way the voltage swing is doubled, which results in a 4 fold power increase (P_{max} approximating $V^2/2\,R_L$). Under the same given conditions this arrangement will yield us a maximum output power of about 18 W. In the final design, the power available from the output stage is stepped up by a further factor of 4 by using a 2 to 1 load matching transformer. P_{max} is now approximately $V^2/\frac{1}{2}R_L$, which (theoretically) would give 72 W into a 4 ohm load at 12 V. Allowing for unavoidable losses, the actual output will be about 40 W. The signal delivered by this final stage will not be exactly 'hi-fi'. The main objective with this design was to help a 'soft' speaker to become a 'loud' speaker. High fidelity is of secondary importance. In spite of the relatively poor audio quality, however, good intelligibility is maintained.



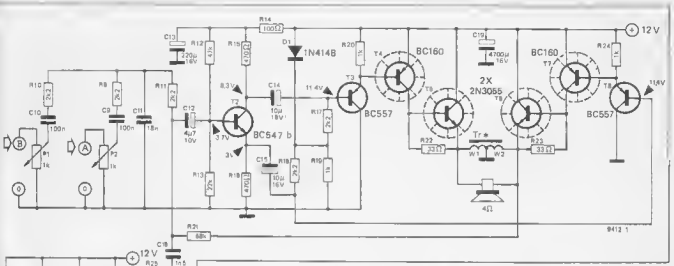
Main amplifier

The main amplifier circuit is shown in figure 1. There are two inputs, one for speech, one for music, with mixing controls P1 and P2. The input signal is passed on to a phase splitter that produces the in-phase signal (at the splitter emitter) and the anti-phase signal (at the collector) required for the symmetrical pushpull stage.

To increase the output power even further, an output transformer is used.

The function of this output transformer can be explained as follows. If the amplifier is fully driven, at one 'end' of the output swing T5 will be fully conductive and T6 will be cut off. At that instant, the current flowing through

1



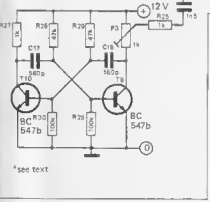


Figure 1. The loud mouth. The maximum output power is sixteen times greater than for a 'normal' amplifier operating at the same supply voltage.

Figure 2. Crossover characteristics. They demonstrate the affect of a square wave HF bias superimposed upon an audio signal.

transformer winding W1 will set up a voltage across this winding of 12 V. The emf induced in the opposite transformer winding will also be 12 V, which results in 24 volts across the entire transformer and, therefore, across the loudspeaker terminals. This is the peak swing for a half-period of the output signal. The r.m.s. value is 0.7 × 24 V, which is approximately 17 V. The corresponding maximum output power will then be approximately $P_{max} = \frac{U^2}{R_L} = \frac{17^2}{4} \approx 72$ W. As stated earlier, the inevitable losses will reduce the maximum output power in practice to about 40 W.

To cut down distortion, resistor R21 provides some degree of negative feedback.

The HF bias

The output stage operates in class C, so the drive signal must reach a certain level before the output responds. The advantage of class C operation is the relative immunity to temperature fluctuations. However, class C also has a major drawback: if no special precautions are taken, the 'dead zone'

2

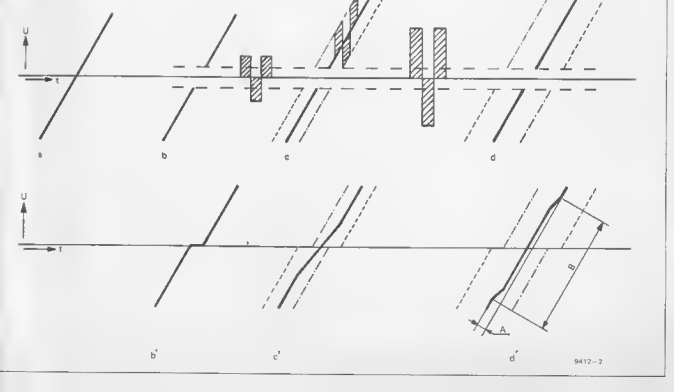
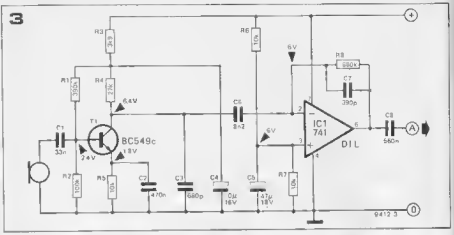
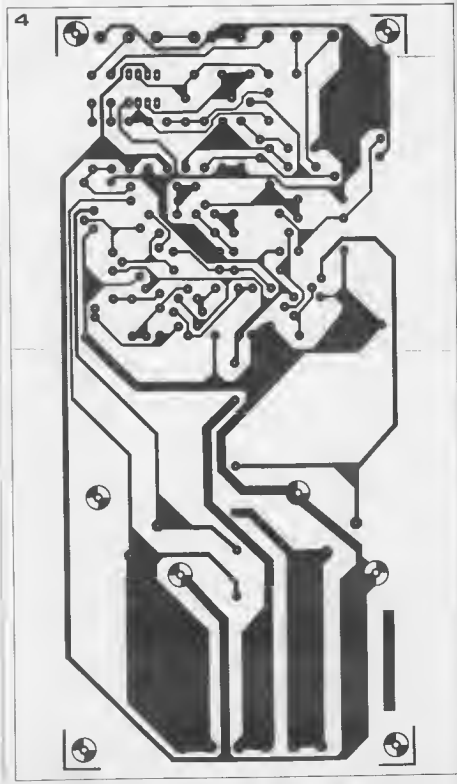


Figure 3. Microphone preamplifier. The value of R8 can be modified if higher or lower input sensitivity is required.

Figure 4. Printed circuit board and component layout (EPS 9412).





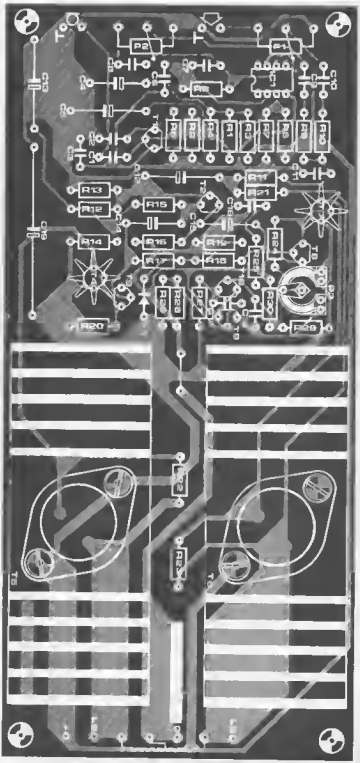
Complete parts list

Resistors:
R1 = 390 k
R2,R28,R30 = 100 k
R3 = 3k9
R4 = 27 k
R5,R6,R7 = 10 k
R8 = 680 k (see text)
R9,R10,R11,R17,R18 = 2k2
R12,R26,R29 = 47 k
R13 = 22 k
R14 = 100 Ω
R15,R16 = 470 Ω
R19,R20,R24,R25,R27 = 1 k
R21 = 68 k
R22,R23 = 33 Ω
P1,P2 = 1 k log. pot.
P3 = 1 k preset pot.

Capacitors:
C1 = 33 n
C2 = 470 n
C3 = 680 p
C4,C14,C15 = 10 µ/16 V
C5 = 47 µ/16 V
C6 = 8n2
C7 = 390 p
C8 = 560 n
C9,C10 = 100 n
C11 = 18 n
C12 = 4µ7/10 V
C13 = 220 µ/16 V
C18 = 1n5
C17,C16 = 560 p
C19 = 4700 µ/16 V

Semiconductors:
IC1 = 741
T1 = BC 549c, BC 109
T2,T9,T10 = BC 547b, BC 107
T3,T8 = BC 557, BC 177
T4,T7 = BC 160
T5,T6 = 2N3055
D1 = DUS

Miscellaneous:
Tr = transformer 2 x 12 V/3 A



inherent to this type of operation will cause objectionable crossover distortion. In this design the distortion was reduced by superimposing an HF bias signal onto the input audio. This HF bias consists of nothing more than a 30 kHz square wave signal. It is generated by an astable (T9, T10). The effects of this HF bias can be better explained from the graphs shown in figure 2.

Figure 2a shows a given input audio signal. The central dead zone in which there is no output response is shown in figure 2b, the resultant output according to 2b' clearly indicating severe crossover distortion. Figure 2c shows the effect of a square wave superimposed upon the original input signal. The output signal, which also has this square wave superimposed on it, would fill the area between the dashed lines in figure c'. However, after filtering, the output signal becomes equal to the average value, which is shown as a bold line in figure c'. This curve demonstrates a more continuous transition over the dead zone, resulting in a much lower distortion.

When the HF bias amplitude is increased, as shown in figure 2d, the smoothed output signal will be as indicated by the bold line in 2d'. Evidently, crossover conditions are determined by the HF bias amplitude and the offset 'A' which in turn depends on the width of the dead zone. This width may be affected by temperature changes, but this bas little effect on the audible distortion. The transition zone 'B' depends directly on the HF bias amplitude, which in turn depends on the power supply voltage. However, 2d' indicates that fluctuations in the supply voltage and, consequently, fluctuations in the width of zone 'B' will not audibly affect the distortion in the output signal. P3 is used to set the HF bias amplitude.

The microphone preamplifier

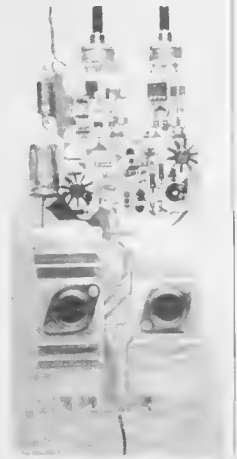
The sensitivity (gain) of the main amplifier, shown in figure 1, is not very high. For this reason a preamplifier stage must be added if a dynamic microphone is to be used. The circuit for a suitable preamp is shown in figure 3. It is included on the printed circuit board.

The discrete transistor stage (T1) acts both as an impedance matching device and a low noise amplifier. Since the noise characteristics of the preamplifier output stage, a 741 opamp, are not all too favorable, a satisfactory signal-to-noise figure could not be obtained without the help of this additional transistor. The overall gain now becomes so high that it will readily lead to clipping of the preamplifier output signal. In practice, this is usually not so serious for speech: the intelligibility of spoken messages is still quite good, and it has the advantage that the average output power of the system is greatly increased. However, if the distortion is too objectionable the value of R8 can be decreased, reducing the sensitivity to a suitable level. On the other hand, if the gain is too low then R8 can be increased

to a suitable value.
The preamplifier is meant for 50 kΩ microphones, but also works quite well with 500 ohm mikes.

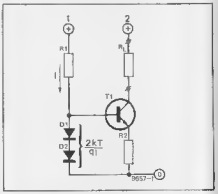
Some practical advice

Figure 4 shows the printed circuit board and component layout. The HF bias is set with P3. Connect an ammeter in the power supply line and adjust P3 so that under no-signal conditions the current is about 300 to 400 mA.
To prevent any mishaps when the equipment is being connected to the car battery it is recommended to insert a fuse of approximately 5 A in the power supply line.
The power transistors T5, T6 and the drivers T4, T7 require heat sinks. Cooling fins will suffice for T4 and T7; T5 and T6 must be mounted on a heat sink with a thermal resistance of 3°C/W or less. There is sufficient room on the p.c.b. for all of these sinks.
T_T can be a standard mains transformer with two 12 V, 3 A secondaries. The primary is not used, but since it will develop an uncomfortably high voltage its terminals should be well insulated.
The circuit is designed for 4 ohm loudspeakers. However, if 40411 transistors are used for T5 and T6, a 2 ohm load is permissable. In that case the maximum output power will increase to some 80 W.



improved current source

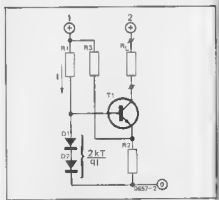
The basic circuit of a current source is shown in figure 1. The base-to-emitter potential for the source transistor T1 is derived from the '+1' power supply terminal through the



potential divider R1, D1, D2. The T1 collector current is approximately

$$\frac{600 \ldots 700}{R_3} \text{ milliamps}$$

where R2 is in ohms.
Minor fluctuations in the '+1' voltages affect the T1 collector current via the differential resistance of D1 and D2. This can, of course, be prevented by using a zener diode to stabilise the '+1' voltage.
An alternative method is to add a resistor R3 from the '+1' terminal to the



T1 emitter, as shown in figure 2. If R3 is chosen so that

$$\frac{R_3}{R_2} = 20 \times V$$

where V is the voltage '+1', the T1 collector current will remain constant in spite of supply voltage fluctuations.

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