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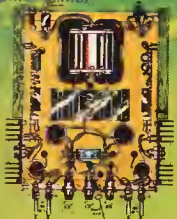

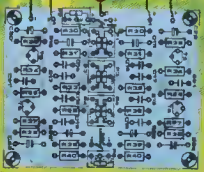

April
1976 40p

contents

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CMOS + afterburner = LOCMOS

This article takes a look at the latest developments in logic circuit technology and explains the advantages of LOCMOS.

Today's problems in logic design

Not long ago, the designer had a relatively simple choice between available logic families to determine what speeds were available, and at what cost in power. In the last two or three years many new logic families have appeared, with overlapping specifications, making it much harder to decide which family comes closest to satisfying a given set of requirements.

In the past, for high speed applications the choice was emitter-coupled logic (ECL) with gate propagation delays of one to three nanoseconds; the power dissipation was about 30 mW per gate. For industrial control systems and for peripherals of small computers, standard 7400 transistor-transistor logic (TTL) was the best; 10 ns delays were tolerable and 10 mW per gate power dissipation presented no problems. There was a great deal of flexibility and both small- and medium-scale ICs were readily available.

For low power, where speed was not important, the designer normally chose 74L, a low-power family that dissipated around one milliwatt per gate but could seldom be pushed faster than about 30 ns. With the knowledge that 74H was always there, for faster designs that would tolerate more power the designer settled for 5 ns and 20 mW per gate. Many new logic families have since appeared. Not only do their specifications overlap, but there is the difficulty of non-compatibility between families, so it is quite impossible to mix, for example, the low power capability of complementary-metal-oxide-semiconductor (CMOS) with the nanosecond capability of emitter-coupled-logic on the same board. Power supply requirements vary, too, drive capabilities are never the same, and so on.

And now LOCMOS has arrived . . . . Before we look at the latest developments in greater depth, let's define precisely what we mean by the terms we use.

Two basic technologies

In semiconductor technology, the transistor, that tiny chip of crystalline material which amplifies or switches electrical current, is now a 25-year-old invention that began the solid-state revolution. Although still widely used as a discrete component, it is giving way to the integrated circuit in which many transistors, as well as diodes and other circuit elements are batch-fabricated on a single silicon chip in a series of photolithographic and diffusion steps.

There are two fundamental processes for fabricating ICs. These are:

- bipolar
- metal-oxide-semiconductor (MOS).

Bipolar processes

Currently the most popular, the bipolar process is one of two fundamental processes for making integrated circuits. A bipolar IC is made up of layers of silicon with differing electrical characteristics. Current flows between the

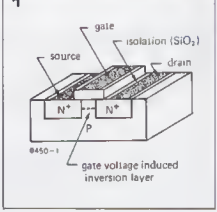


Figure 1. Cross-sectional view of a MOS field-effect transistor.

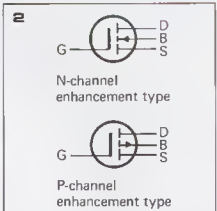


Figure 2. Schematic symbols for MOS transistors. G = gate, D = drain, B = bulk (substrate), S = source.

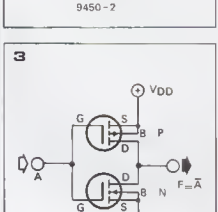


Figure 3. Complementary-symmetry inverter circuit using MOS transistors.

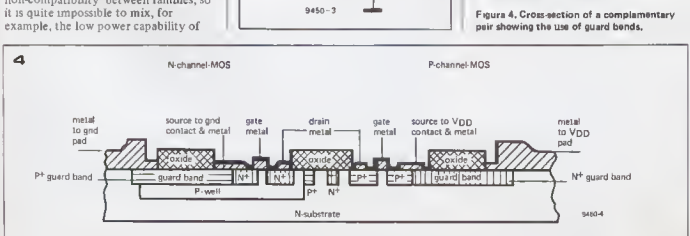


Figure 4. Cross-section of a complementary pair showing the use of guard bands.

layers when a voltage is applied to the junction or boundary between the layers.

- *Transistor-transistor logic (TTL)*
  By far the most successful bipolar IC logic is transistor-transistor logic, which gets its name, as do other digital IC product families from the way that the components are combined to form the logic elements. Digital ICs solve problems by manipulating electrical signals that represent bits of information. Basic TTL is a mature product, but faster and lower-power versions are expected to extend the life of TTL into the 1980s.

- *Emitter-coupled logic (ECL)*
  Emitter-coupled logic is a 10-year-old bipolar digital IC family that uses a more complex design than TTL to speed up IC operations. Emitter-coupled logic is costly, power hungry, and difficult to use, but it could become important in the next generation of large computers because it is four times faster than TTL.

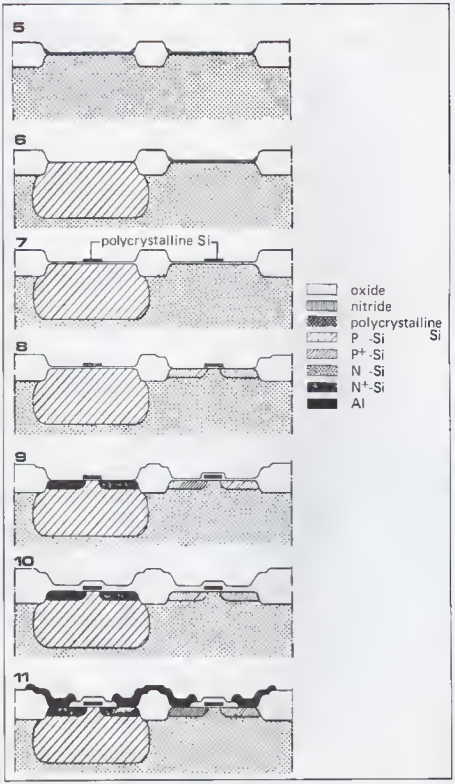
- *Integrated-injection logic (I^2L)*
  Integrated-injection logic is the latest bipolar logic design. Although a number of successful circuits have been produced, it is still early days. For large scale integration (LSI), I^2L enables over 1000 gate functions to be integrated on a single chip. I^2L technology also allows analogue and digital functions to be combined on the same chip.

Metal-oxide-semiconductor (MOS) processes

The second fundamental process for fabricating ICs is metal-oxide semiconductor. The active area of a MOS chip is at its surface, where a gate electrode applies a voltage to a thin layer under it to create a temporary channel through which current can flow.

- *PMOS*
  The oldest MOS circuit technology uses a channel of P-type material, where the flow of current is made up of positive changes. PMOS now accounts for most MOS volume. Because the action in a MOS circuit is near the surface, contamination that would be minor in a bipolar device caused serious problems in the early days of MOS.

- *NMOS*
  N-channel MOS, where the flow of current is made up of negative charges, is just now moving into production. It is two to three times



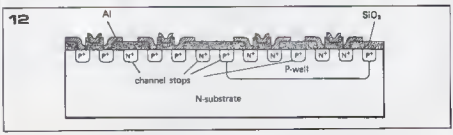


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Figure 6 . . . 11. LOCMOS manufacturing process.

Figure 12. Conventional metal gate CMOS.

Figure 13. Silicon gate CMOS increases performance.

Figure 14. Cross-section and top view of an inverter in LOCMOS technology. Silicon gate with local oxidation reduces chip area.

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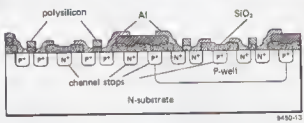

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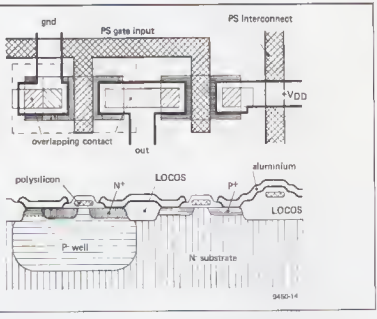

faster than PMOS circuits, but manufacturing is harder to control than PMOS. These problems have now been overcome.

- *Complementary MOS (CMOS)*
  In monolithic ICs using bipolar transistors, it has not been possible to exploit the numerous advantages of complementary-symmetry circuits because conflicting technological factors currently mitigate against the fabrication of optimized NPN and PNP bipolar transistors on the same substrate. However, the complementary-symmetry circuit advantages can be harnessed in ICs by integrating compatible P-channel and N-channel enhancement-type MOS field-effect transistors on a monolithic substrate to create an IC that is as fast as an NMOS circuit but consumes very little power.

CMOS circuits, in configurations which encompass both logic and memory, are excellently suited to use in digital circuit applications and are characterized by their micropower quiescent operation, moderately fast propagation delay, excellent noise immunity, large fanout capability, and operation from a single power supply over a wide voltage range (see Table 1). The characteristics of CMOS logic and memory circuits are comparatively immune to variations in temperature.

Table 1

	Standard TTL	CMOS 5 V Supply	CMOS 10 V Supply
Propagation Delay	10 ns	35 ns	25 ns
Flip-Flop Toggle Frequency	35 MHz	5 MHz	10 MHz
Quiescent Power	10 mW	10 nW	10 nW
Noise Immunity	1 V	2 V	4 V
Fanout	10	>50	>50

Basic principles of MOSFETs

The basic building block of CMOS logic circuits is the complementary pair MOS inverter consisting of a pair of N-channel and P-channel enhancement mode, insulated gate field-effect transistors (FETs) utilizing metal gate electrodes.
Field-effect transistors combine the inherent advantages of solid-state devices (small size, low power consumption, and mechanical ruggedness) with a very high input impedance.

Unlike bipolar devices in which performance depends on the interaction of two types of charge carriers, holes and electrons, field-effect transistors are unipolar devices, i.e., operation is basically a function of only one type of charge carrier, holes in P-channel devices and electrons in N-channel devices.
Early models of field-effect transistors used a reverse-biased semiconductor junction for the control electrode. In MOS field-effect transistors, a metal control gate is separated from the semiconductor channel by an insulating oxide layer. One of the major features of the metal-oxide-semiconductor structure is that the very high input resistance of MOS transistors (unlike that of junction-gate-type field-effect transistors) is not affected by the polarity of the bias on the control (gate) electrode. In addition, the leakage currents associated with the insulated control electrode are relatively unaffected by changes in ambient temperature. Because of their unique properties, MOS field-effect transistors are particularly well suited for use in digital switching applications, as well as in linear voltage amplifiers and voltage-controlled attenuators.
The operation of field-effect devices can be explained in terms of a charge-control concept. The metal control

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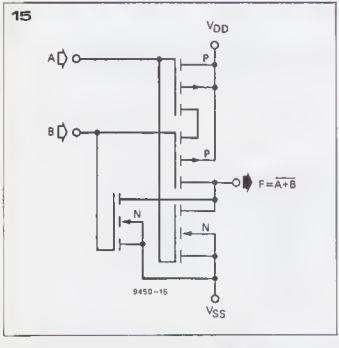

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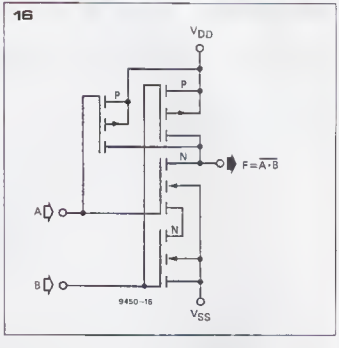


electrode, which is called a gate, acts like a plate of a capacitor. A charge placed on the gate induces an equal but opposite charge in the semiconductor layer, or channel, located beneath the gate. The charge induced in the channel can then be used to control the conduction between two ohmic contacts, called the source and the drain, made to opposite ends of the channel.

The MOS type of field-effect transistor uses a metal gate electrode separated from the semiconductor material by an insulator. Like the P-N junction, this insulated-gate electrode can *deplete* the source-to-drain channel of active carriers when suitable bias voltages are applied. However, the insulated-gate electrode can also increase the conductivity of the channel *(enhancement)* without increasing steady-state input current or reducing power gain.

The two basic types of MOS field-effect transistors are the depletion type and the enhancement type. All CMOS circuits are of the enhancement type. In this type, the gate must be forward-biased to produce active carriers and permit conduction through the channel. No useful channel conductivity exists at either zero or reverse gate bias.

Because MOS transistors can be made to utilize either electron conduction (N-channel) or hole conduction (P-channel), two distinct enhancement-type MOS field-effect transistors are possible.

An N-channel enhancement-type MOS transistor (reversal of N-type and P-type regions would produce a P-channel enhancement-type transistor) is normally non-conducting until a sufficient voltage of the correct polarity is applied to the gate electrode. When a positive bias voltage is applied to the gate of an N-channel enhancement transistor, electrons are drawn into the channel region beneath the gate. If sufficient voltage is applied, this channel region changes from P-type to N-type and provides a conduction path between the N-type source and the N-type drain regions. (In a P-channel enhancement transistor, the application of negative bias voltage draws holes into the region below the gate so that this channel region changes from N-type to P-type and again provides a source-to-drain conduction path.)

The CMOS inverter

The CMOS inverter, shown in figure 3 works like this. With a positive supply voltage V_{DD}, if a positive voltage V_I is applied to the input (logic state '1'), then the N-channel transistor becomes conducting while the P-channel transistor does not conduct. The output voltage is then zero (logic state '0'). If the input voltage is now made zero ('0'), the P-channel transistor becomes conducting and the N-channel transistor is switched off. The output voltage is now V_{DD} ('1'). The two MOS transistors therefore behave as switches, and the current in the circuit is determined by the very small leakage current of the switched-off MOS transistor. The current has a larger value only momentarily, during switching when both transistors are on for a short period.

Advantages of CMOS circuits

The advantage of a CMOS circuit is that the channel resistance values can be small and hence the switching speeds high, and the quiescent current and therefore the stand-by power is practically zero. Other advantages of CMOS circuits compared with ordinary MOS circuits are the immunity to fluctuations in the supply voltage or in the input voltage. The sensitivity to input voltage fluctuations is low because the input voltage at which the circuit changes over from one logic state to the other is equal to about half the supply voltage, while the actual transition takes place over a very small range of input voltage. It is also easy to make a CMOS circuit compatible with other logic circuits such as TTL.

Standard CMOS

All these advantages would make CMOS transistors very suitable for use in integrated circuits, were it not for the fact that with the same tolerances the packing density is smaller than for ordinary MOS transistors.

Protective guard bands surround separate MOS devices, tunnels, wells, and diodes or combinations of MOS devices which are interconnected through common diffused regions for the purpose of preventing leakage. All P-channel devices, tunnels, and diodes must be surrounded by a continuous N^+ guard band which also serves as a tunnel to help conduct current from the external supply voltage V_{DD} across the N-type substrate to every P-channel device tied to the external supply. Similar heavily doped P^+ guard bands surround all N-channel devices, tunnels, and diodes to help conduct current from the external ground supply V_{SS} across the P-well to every N-channel device tied to ground. Contact to the N-type substrate may be made through the N^+ guard band and

returned to the V_{DD} pad; contact to the P-well substrate may be made through the P^+ guard band and returned to the ground pad. Guard bands may be narrow strips or, where space permits, large diffused areas that minimize resistance in the V_{DD} and V_{SS} supply lines. Guard bands are also used to prevent parasitic channels thereby assuring complete device cutoff; this cutoff is accomplished by having the gate metal, as it leaves the end of the channel, cross a guard band prior to stepping up over the thick oxide.

Summary of CMOS features

- *Low Power*
  The net quiescent current, which is determined by the leakage current of the 'off' device, is in the barely perceptible nanoampere region. Even when switching, little power is required since both transistors are only partially on. CMOS consumes less power than standard TTL by a factor of at least 10^6 under static conditions, when power dissipation per gate is of the order of only 10 nW.
- *High noise immunity*
  CMOS has a near ideal transfer characteristic and an extremely sharp cutoff between a logic '0' and a logic '1'. About four times better than TTL. CMOS logic circuits are finding their way into automobile applications, and industrial process control where they can operate undisturbed by high electrical factory noise.
- *Wide supply voltage range*
  Single power supply voltages from 3 to 15 V can be used with CMOS circuits. In industrial use, this means that the expensive, close-tolerance power supplies can be eliminated in favour of a cheap unstabilized supply.

As a replacement for TTL, CMOS is well known to be extremely cost-effective. But what is less known about CMOS is its ability to operate at fairly high speeds at increased but still moderate power consumption. In fact, CMOS has a lower propagation delay-power product than any other logic family. By operating just below TTL speeds, medium- and large-scale integrated CMOS packages can perform the same logic functions as TTL but with the added advantages of lower power-supply requirements, high noise immunity, and lower costs.
However, being composed of complementary structures, CMOS circuits require an additional device per gate input over other MOS structures as well as an additional isolation region. Consequently, they are only about a third as dense as other MOS devices, even though they are smaller than most

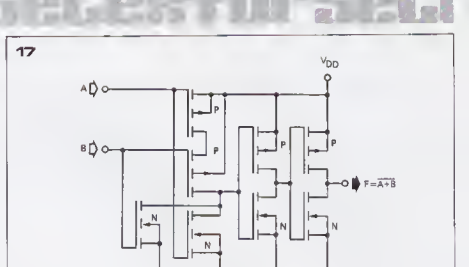


Figure 15. Conventional, unbuffered two-input NOR gate.

Figure 16. Conventional, unbuffered two-input NAND gate.

Figure 17. Two-input NOR gate with buffered output in LOCMOS.

equivalent bipolar structures. This tends to place CMOS in applications where low power is extremely desirable, where medium-scale integration can be used, and where high speeds are not essential – in other words, in the industrial and communications sector.

CMOS + LSI + LOCOS = LOCMOS

It has now been found that marked reduction in surface area can be obtained by using a local oxidation technique known as LOCOS (LOCal Oxidation of Silicon) developed at Philips Research Laboratories, combined with a special technique for applying P-type wells. This process can be controlled in such a way that LSI circuits can be made.
In the LOCOS technique, a silicon substrate is coated with a layer of silicon nitride, which is used as a mask in a later oxidation of the silicon when a silicon-dioxide layer is formed at the places where the nitride has been removed. Most of this 'LOCOS' oxide sinks into the silicon and gives good separation between regions of different doping. It takes up far less space than the conventional isolation diffusion.
We shall now describe the process used for making CMOS circuits by the LOCOS technique – the 'LOCMOS technology'. The starting material is a wafer of N-type silicon whose surface has the <100> orientation. A surface with this orientation generally has very few surface states, and little charge appears in the oxide grown upon it, this gives a low and reproducible threshold voltage. The wafer is first coated with a thin layer of silicon nitride, which is next removed at the places where the isolation oxide is formed, and the silicon is then oxidized until the oxide layer is 1.8 μm thick (figure 5).
The next step is to remove the nitride at the places where the P-islands for the N-channel transistors have to appear – this is done by standard photo-etching techniques. After this P-type regions are produced at these places by a special technique (figure 6).

In this technique the silicon is doped with boron in such a way that the boron concentration at the surface has the value necessary for good operation of the MOS transistor, while the maximum of the concentration profile is located about 1.5 μm beneath the surface. This approach prevents parasitic N-type channels from forming along the LOCOS oxide. With this method there is no need to use guard bands.

After the P-diffusion the rest of the nitride is removed, and a thin oxide layer is formed thermally. A poly-crystalline layer of silicon is then applied. Next the polycrystalline layer is doped with phosphorus to make it an N-type conductor, and a pattern is etched in it for the electrodes and a part of the interconnection pattern (figure 7); the doping is necessary to give a low series resistance to the conductors and hence a high switching speed.

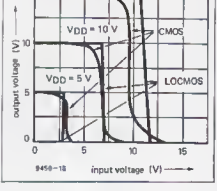
The next step in the process is to produce P-type sources and drains by boron diffusion at previously etched openings in the oxide layer (figure 8). The gates and the LOCOS oxide serve as self-aligning masks. Since these electrodes are small the stray capacitances are small, which also helps to give a high switching speed.
After the boron diffusion a thin oxide is again formed on these regions. The N-type sources and drains are next produced in a similar treatment, with a phosphorus diffusion (figure 9).
A silicon-dioxide layer is then deposited pyrolitically, and openings are etched in this to allow contact between the electrodes and the interconnection pattern (figure 10).
Finally, a layer of aluminium is applied by vacuum evaporation and the interconnection pattern is formed in this by etching (figure 11).

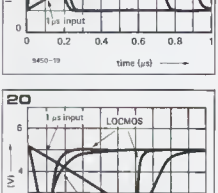
Improved packing density with LOCMOS

Conventional metal gate CMOS is shown in figure 12. Here, the N^+ and P^+ guard bands surround the P- and N-channels respectively.
In figure 13, silicon gate CMOS increases the performance due to gate self-alignment and reduced capacitance, but the required guard bands limit the savings in area.
The result is a highly improved packing density and a higher internal speed. An additional advantage of silicon gate processes is the inherent facility of having two isolated layers (polysilicon and aluminium) for interconnection. It can be seen that the LOCMOS process is a very attractive one for large-scale integration.
LOCMOS technology combines a silicon gate with local oxidation to reduce the chip area, as shown in figure 14, silicon dioxide replacing the guard bands. Because the LOCOS grows into the bulk of the silicon, the contact holes can overlap the LOCOS without fear that there will be a short circuit to the underlying substrate. This reduces the necessary diffusion area, thereby reducing the drain capacitance. The self-alignment of the diffusions also makes any special clearance between the N- and P-transistors unnecessary and the special diffusion profile built into the P-well makes any channel stopper diffusions superfluous.

Disedvantages of older gate designs

Figure 15 illustrates a conventional, unbuffered two-input NOR gate. One N-channel transistor, connected to the supply voltage, V_{SS}, will conduct when either input is high, causing the output





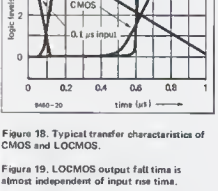


Figure 18. Typical transfer characteristics of CMOS and LOCMOS.

Figure 19. LOCMOS output fall time is almost independent of input rise time.

Figure 20. LOCMOS output rise time is almost independant of input fall time.

Figure 21. Comparison of transfer characteristics of TTL and LOCMOS.

to go low through the on resistance of the device. If both inputs are high, both N-channel devices go on, in effect halving the on resistance and making the output impedance (and hence propagation delay) a function of input variables. Similarly, the P-channel devices are switched on by low signals; i.e., when both inputs are low, conduction from the supply voltage, V_{DD}, to the output will occur.
Now, since the P-channel devices are in series, their chip area must be enlarged so that their on resistance will decrease and hold the high impedance of the output within specification. And, as the number of gate inputs increases, even larger P-channel devices are required, causing severe variations of the output impedance with input patterns to V_{SS}. For example, in unbuffered CMOS, the two-input NAND gate as shown in figure 16 interchanges parallel and serial transistor gating to achieve the dual logic function. The change in output resistance moves to the P-channel transistors connected to V_{DD}, while the N-channel devices, being serially connected, must be increased in size.
Needless to say, this sensitivity of propagation delay to input pattern can cause all sorts of mysterious system problems – for example, errors may occur only with certain data patterns. Older designs, therefore, have several disadvantages:

- Since logic transistors are also output devices, they must be large enough to supply full output drive current.
- Output impedance (and hence propagation delay) is a function of input logic conditions (speed is pattern sensitive).
- Output transition time is a function of input transition time.
- Noise immunity is not as good as theoretically possible.

LOCMOS uses low impedanca buffers

To minimize any pattern sensitivity of propagation delay and to standardize delay and output drive, the new oxide-isolated design concept adds an output buffer stage to the gate configuration (figure 17). This technique actually reduces chip size, since now only two large output transistors are required, and it also improves noise immunity because the increased voltage gain results in nearly ideal transfer characteristics. The high voltage gain of greater than 10,000 also provides significant pulse shaping, since output transitions are independent of input rise and fall times.
Buffering provides the following advantages:

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- standardized low impedance outputs
- propagation delay is less dependent on input logic pattern or transition times
- propagation delay less sensitive to capacitive loading
- better noise immunity
- only two large output transistors are required
- decreased input capacitance

Characteristics of buffered design

Typical transfer characteristics shown in figure 18 clearly indicate that a buffered gate is almost ideal.
Figure 19 shows that with a buffered gate, the output fall time is almost independent of the input rise time.
Figure 20 shows that the buffered gate output rise time is almost independent of the input fall time.

LOCMOS system considerations

- propagation delay
- noise immunity
- power supply requirements
- power dissipation
- input characteristics
- interface to TTL

Propagation delay
LOCMOS d.c. fanout is almost unlimited. Fanout is therefore limited by propagation delay effects.
Propagation delay depends on load capacitance; it is strongly influenced by supply voltage; and it is affected by ambient temperature, but less so than TTL.
To determine the propagation delay:

- Start from basic data sheet numbers.
- Derate for capacitance load over 15 pF.
- Derate for minimum power supply voltage including regulation and ripple effects.
- Derate for maximum ambient temperature.

Noise immunity
The superior noise immunity of LOCMOS comes from its almost perfect transfer characteristic, as shown in figure 21.
Good noise immunity is typically 45% of the supply voltage. Noise immunity is expressed by:

$$V_{NL} = V_{IL\,max} - V_{OL\,max}$$

$$V_{NH} = V_{OH\,min} \quad V_{IH\,min}$$

LOCMOS has higher noise immunity than any other logic family. One limitation of LOCMOS noise immunity comes from coupling from external noise sources. The amount of noise current required to switch a LOCMOS device is actually quite low, because the input impedance is high (Table II).

Table II

	TTL (high)	TTL (low)	LOCMOS V_{DD} = 5 V	LOCMOS V_{DD} = 10 V
Typical output impedance	100 Ω	10 Ω	400 Ω	200 Ω
Typical noise immunity	1.5 V	1 V	2.5 V	5 V
Noise current required to induce noise	15 mA	100 mA	6.25 mA	25 mA

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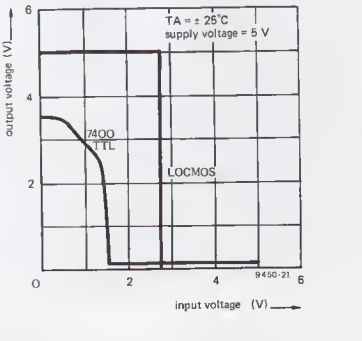

Power supply requirements
LOCMOS is specified over an operating V_{DD} range of 3 to 15 V. This introduces cost saving possibilities unavailable with other logic forms. LOCMOS can operate from batteries, unregulated power supplies, and available non-logic power supplies. The minimum V_{DD} is 3 V, or higher as required for noise immunity or propagation delay. The maximum V_{DD} is 15 V, or lower as determined by power dissipation. Both minimum and maximum values of V_{DD} depend on the interface to other logic forms.

Power dissipation
The total power dissipation may be determined from:

total power = quiescent power + transient power

AC power is made up of 3 components

1. Charging and discharging of internal capacitance.
2. Current which flows during switching when both N and P transistors are conducting.
3. Charging and discharging of load capacitance.

The transient power dissipation effects of internal capacitance and current spiking may be lumped and are given in data sheets. Figure 22 shows the power dissipation per gate against input frequency for different supply voltages. The effects of additional load capacitance, beyond that shown in the data sheets may be calculated by:

load power = $C_L(V_{DD})^2 f$,

where C_L = external load capacitance and f = frequency of operation.
The total power, therefore, will be:

total power = $I_{DD} \cdot V_{DD}$ + internal transient dissipation (from data sheet) + $C_L(V_{DD})^2 f$.

Interface to TTL
Two constraints must be satisfied when interfacing to another family.

1. Input voltage levels to LOCMOS should be as close as possible to V_{SS} for logic '0' and V_{DD} for logic '1'.
2. The LOCMOS outputs must be capable of driving the necessary current and voltage requirements of the interfacing circuit.

SELEKTOR

For standard TTL driving LOCMOS,
- $V_{IH(MIN)}$ for LOCMOS must be 3.5 V
- $V_{OH(MIN)}$ for standard TTL is 3.5 V typical at $V_{CC} = 5$ V.

Therefore standard TTL will typically drive LOCMOS directly.
For CMOS driving TTL, all LOCMOS outputs drive 400 µA at 0.4 V over the full temperature range.
All inputs are protected against static discharge, as shown in figure 23.
Due to the resistor being in series with the input protection diodes, an input signal from a low impedance source can be applied in the absence of supply voltage without damaging the diodes.

Summary of LOCMOS

Advantages of CMOS
- very low power
- wide supply voltage range
- high noise immunity.

Philips' LOCMOS offers in addition:
- LOCOS techniques – reproducible high performance
- buffered, standardised outputs simplify design
- best noise immunity
- decreased sensitivity to capacitive loading
- a gate packing density twice as great as conventional CMOS
- higher speeds

Standard range

The Philips standard range of LOCMOS devices already consists of some 60 types. Motorola are also starting production, with 5 types available so far.

N.V. Philips Gloeilampenfabrieken
Elcoma Division
P.O. Box 523, Eindhoven – the Netherlands.

23

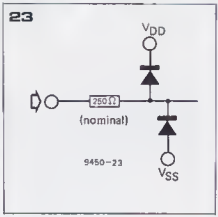

Figure 22. Variation of power dissipation for a typical gate with input frequency for different supply voltages.

Figure 23. All inputs are protected against static discharge.

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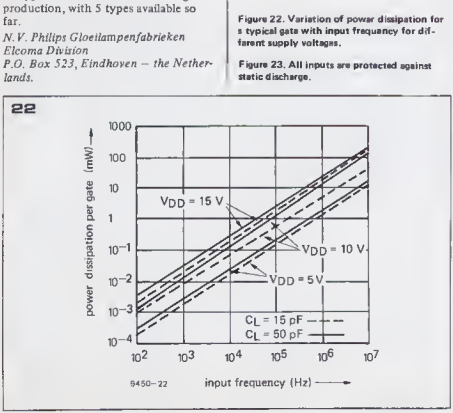


27-Channel ultrasonic remote control unit

Motorola have just announced a CMOS 27-channel ultrasonic transmitter and a companion NMOS receiver which together form a complete remote control system for television and other applications. The system is used in conjunction with a 22-button keyboard to give a viewer remote control of all the user-variable functions of a television receiver.
When used in conjunction with a television receiver, the ICs allow remote selection of up to 12 channels, three 60-step analogue channels, automatic switch-on when channel is selected, automatic muting of sound during channel change and switch-on, two auxiliary outputs, dual switching outputs (PAL or SECAM) and a strobe output for use with on-screen displays.
Used with a 22-button keyboard, an external amplifier and transducer together with a battery and about a dozen discrete components, the CMOS MC14422 transmitter forms a complete ultrasonic transmitter for the remote control of television receivers. When none of the push-buttons is actually pressed, the IC automatically reverts to a shut-down state in which power consumption is reduced to such a low level it was unnecessary to provide an on/off switch.
The MC14422 generates up to five output frequencies which are transmitted in an output sequence which lasts for four time periods. Dunng the final slot or period, one of two frequencies may or may not be transmitted.
A non-integral variable frequency divider is used to derive the output frequencies from an on-chip LC reference oscillator.
These lie in the range 34,688 to 42,755 Hz. An RC oscillator, running at a much lower frequency, determines the speed at which the keyboard is scanned and the length of the output sequence.
The NMOS receiver (MC6525) is based on the superheterodyne principle and has multiple repetitive verification of the received code to further increase system security. With a sensitivity of 250 mV r.m.s. the MC6525 can be driven from a relatively low gain preamplifier. Reset of the receiver logic is performed automatically when the MC6525 is re-powered.

Motorola Ltd.
Semiconductor Products Division.
York House
Empire Way
Wembley, Middlesex.

microprofessor

That's life.
Valves or tubes are distinctly passé – except where they are used for controlling the flow of fluids or gasses. Schools and technical colleges have switched over to transistors. A brave step, but by now the price of TTL ICs has dropped to an all-time low (a 7400 costs the same as a BC107), COSMOS prices are still falling rapidly, and both TTL and COSMOS may well be laid by the heels in the near future by one or more of the other new technologies (Low Power Schottky TTL, LOCMOS, I^2L, etc.).
And now, over the horizon looms the microprocessor . . . .
Nearly all self-respecting manufacturers of semiconductors have designed a system, improved it, and are now trying to force it down the throat of the poor consumer.
System prices have dropped within the last year from over £ 150 to nearer £ 20 (one manufacturer is offering the MPU itself at £ 5–10,000 up), and they will probably go down even further in the near future.
This would be very nice, if only the prospective buyer knew what to do with the things. They are available in quantity and diversity, they are relatively cheap, and they will do the job for him – if only he knew what job that was.
There's plenty of hardware, but very little software. Or, to put it differently: we are being presented with a solution, and now we have got to start looking for a problem.
Of course, we have some idea of what kind of problem to look for, because we know that a microprocessor can be programmed to perform quite complex functions.
In the more 'domestic-consumer-oriented' field one could consider an on-board controller for fuel-injection, anti-skid braking etc. in cars; electronic games; musical instruments; a program selector cum commercials rejector for radio and TV.
However, none of these ideas seems to come anywhere near the true capabilities of the system, although everyone feels that some really worth-while applications must exist.
A (welcome!) avalanche of applications is to be expected within the next year or two – certainly if the present-day blizzard of data sheets is anything to go by.
We are waiting for the person who can show us how to use the things properly: the microprofessor.
And we are waiting – with a mixture of fear and anticipation – to see what new technology lies in store for us next year.

(Cartoon reproduced with permission from radio-tv-elektronic 1975, Nr. 11).

The preamplifier and control amplifier described in this article offer high performance at low cost. Furthermore, the control amplifier (with volume, treble, bass, balance and stereo 'width' controls) can be used as a small hand-held 'remote control' unit. The connection to the main equipment can be almost any length of four-core screened cable.

T. Meyrick

part 1

Table 1.

Features

- low cost
- remote control capability for volume, tone and stereo balance and 'width'
- optimal matching to any signal source
- high performance
- standard components

Figures

- distortion: 0.03% typical, 0.07% max.
- S/N ratio:
  linear inputs > 100 dB
  disc input > 95 dB
- sensitivity:
  can be preset for each input separately
  from 1.25 mV up to 1500 mV
- input impedance:
  disc input: 47 kΩ
  other inputs, depending on selected sensitivity: 50 . . . 150 kΩ
- output level:
  nominal: 400 mV (0.03% distortion);
  max. : 1 V (0.1% distortion)
- tone controls:
  bass : ± 12,5 dB at 63 Hz;
  treble: ± 10 dB at 12.5 kHz

Remote control is becoming the done thing.

For toy cars, television sets, model aeroplanes or gantry cranes, remote control is either essential or useful or simply has 'gimmick' value. Depending on the application and on the amount of money available, the remote control link can be wireless (i.e. without wires) or it can be a sufficient length of wire, cable or string.

For domestic Hi-Fi equipment, remote control comes in the 'useful' category: for instance, setting the stereo balance no longer entails five or six trips between the listening position and the main equipment. On the other hand, for most people it will not be worth a disproportionate sum of money. For this reason, a relatively cheap type of link was chosen for the system described here: four-core screened cable. This in turn has led to a somewhat unconventional layout of the various units, as illustrated in the block diagram (figure 2).

In conventional circuits (figure 1), the input selector switch is usually at the input to the control amplifier (B). In that case, one of the inputs that it can select is a disc preamplifier (A) that raises the output level of a magnetic cartridge to that of the other input sources and provides the IEC (RIAA) equalisation. The input selector switch is followed by a volume control and a buffer stage driving the tone controls.

In the design described here, the power

supply arrangements for the control amplifier are complicated enough – it would be even more inconvenient if a buffer stage had to be included between the volume and tone controls. The solution chosen is to use a low-value volume control potentiometer, suitable for direct connection to the tone control circuit, and put the buffer stage at the input side of the volume control. The buffer stage can now be combined with the preamplifier and powered in the normal way. A further advantage of this system is that the long cable is now driven from a low-impedance source.

However, the system is now beginning to depart quite drastically from standard practice. Referring back to the block diagram, figure 2: the fact that the buffer stage and preamplifier have been combined (A) means that all input signals must be fed to this combination. The input selector switch must precede the preamplifier, so the latter must be capable of coping with both high and low level signals. To do this, it will need additional switching inside the feedback loop. This complication can be turned into a further advantage: the circuit can be optimally matched to any normal input source, by selection of fixed resistors and/or equalisation networks. In this way, an extremely good signal-to-noise ratio and a very large overload margin can be achieved.

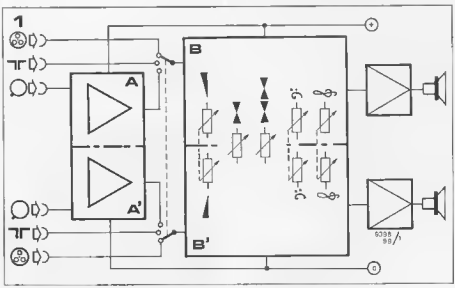
The next point to be considered is the actual link to the remote control unit (B). Since the complete control amplifier is to be included in this hand-held unit, one would normally require two screened cores for the input, two screened cores for the output, and two wires for supply positive and common. If a little care is taken in the design, the screen of the cable can be used for supply common. This means that five-core screened cable would be required. However, four-core screened cable is more readily obtainable – it is used for the connection from a tape recorder to a main amplifier system – so some way must be found for eliminating one more of the connections. The solution chosen is to use a 'phantom' power supply.

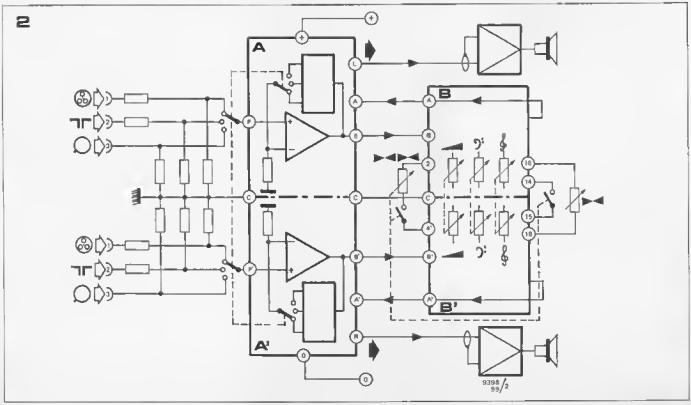
To put it simply – a more detailed description will follow later – the collector resistors and output coupling capacitors of the final stage of the control amplifier are mounted on the pre-amplifier board. This means, in effect, that the positive supply and the output of the control amplifier can both run down the same core; a separate connection for the positive supply is no longer required.

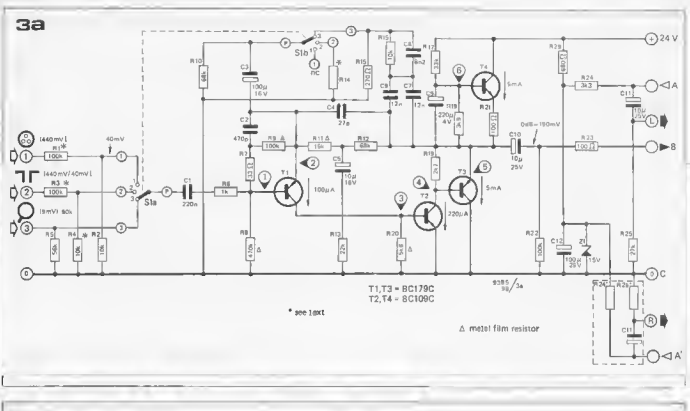
The description of the system given so far may give the impression that the circuits are quite complex and sophisticated – which should in turn mean that

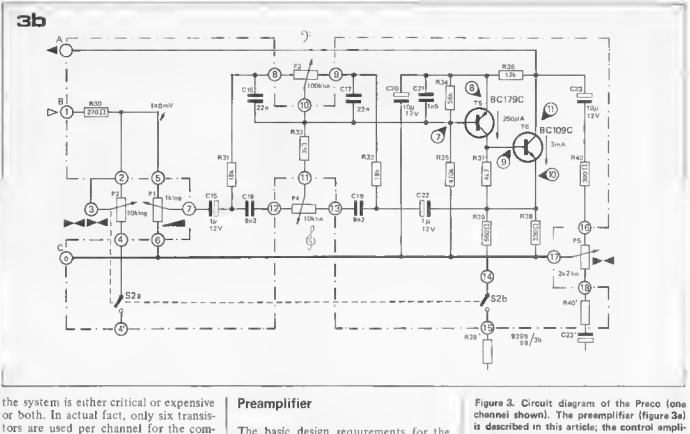
Figure 1. Block diagram of a conventional preamplifier / control amplifier system. The preamplifier is only used for magnetic cartridges.

Figure 2. Block diagram of the Preco. All inputs are fed via attenuators to the pre-amplifier (A); the control amplifier (B) is connected to the preamplifier via four-core screened cable.









the system is either critical or expensive or both. In actual fact, only six transistors are used per channel for the complete system (preamplifier and control amplifier), see figure 3.

When so few components are used for a fairly complicated system, it is to be expected that several compromises are incorporated in the circuit. Performance will normally suffer. In actual fact, the specifications of this system are so good (table 1) that it is definitely a good choice even for those who are not looking for remote control facilities: there is no reason why both units should not be mounted in one box for use as a conventional system.

Preamplifier

The basic design requirements for the preamplifier have been outlined above. To recap briefly: all input signals are to be fed to this unit, and it is to be matched to the input sources by using fixed attenuators at the input and further switching in the feedback loop; furthermore, it must have a low-impedance output to drive the long cable and the tone control circuits.

The amplifier used will need something more than two transistors! The requirements are: plenty of open-loop gain, even when looking into a low-impedance load, and the ability to supply enough

Figure 3. Circuit diagram of the Preco (one channel shown). The preamplifier (figure 3a) is described in this article; the control amplifier (figure 3b) will be discussed in part 2.

current into that load. A fairly heavy-duty output stage is required.

Figure 3a shows the circuit. R1 to R5 are the input attenuators, followed by the input selector switch (S1a). This will be discussed in detail further on. The input transistor (T1) is a PNP type, and it is set at a fairly low collector current (100 μA). In this way, excessive low-frequency ($\frac{1}{f}$) noise is avoided and an extremely high signal-to-noise ratio is attainable.

The voltage across R7 and R9 is the base-emitter voltage of T1, i.e. approximately 550 mV. Since the current through these resistors is practically identical to the current flowing through R8, the total voltage drop across R9, R7 and R8 is also fixed: approximately 3 V. The collector current of this transistor is set by the value chosen for R20, since the voltage drop across this resistor must also be approximately 550 mV. The value given (R20 = 5k6) sets the collector current at 100 μA. This current flows through the DC feedback path (R11 and R12) and gives a voltage drop across these resistors of approximately 8.5 V. This means that the DC voltage at the output (emitter of T3) is fixed at approximately 3 + 8.5 = 11.5 V. This setting is relatively independent of supply voltage variations.

The 'heavy-duty' output stage consists of transistors T2, T3 and T4. T2 and T3 can be considered as one 'super-transistor' and T4 is a gyrator-choke which supplies the DC collector current, so that the AC collector current is all available for driving the load and the feedback loop.

The 'super-transistor' has one or two little quirks. Its effective transconductance (this is the ratio between output current and input voltage) is enormous, so that with any reasonable load it will give an extremely high voltage gain (thousands). This means that the internal feedback cannot be neglected: the input impedance is drastically reduced and Miller effect due to the collector-base capacitance of T2 will cause an early open-loop roll-off. Neither of these quirks have any serious consequences – provided one is aware of them!

A current source could have been used as collector load for the super-transistor. In the circuit actually used, T4, R17, R18 and R21 do behave like a current source set at approximately 5 mA. However, adding C9 gives the circuit a more choke-like behaviour, so that the pre-amplifier is relatively insensitive to ripple on the power supply. Furthermore, when power is first applied the circuit 'starts up slowly' without producing a sudden transient.

The components R22 ... R26, C12 and Z1 are really part of the control amplifier, so they will be discussed later.

The remaining components (R10 ... R16, C3 ... C7 and S1b) constitute the feedback loop.

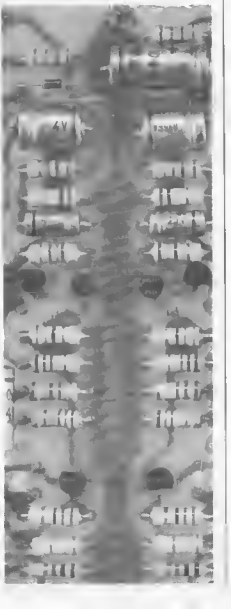
Matching to the signal source

As mentioned previously, the preamplifier is matched to any given signal source by means of the input attenuator and a switch in the feedback loop. It is now time to study exactly how this is done.

In position 1 of the input selector switch, only the basic feedback network is in circuit. This consists of two sections: R11, R12, R13, C4 and C5 on the one hand, and R10 with C3 on the other.

Basic star-delta transformation of the first section shows that this is equivalent to a 130 k resistor between the emitters of T1 and T3, loaded at T3 emitter by an extra 42 k resistor to supply common. The influence of the capacitors is neglected for the moment. Neglecting C3, R10 (68 k) is connected in parallel with the simulated 42 k resistor, giving a total resistance of 68 k/42 k ≈ 26 k. This means that the basic gain is approximately 6.

This basic gain is sufficient to prevent common-mode overloading of the first transistor: the nominal input sensitivity is approximately 30 ... 40 mV. High level input sources are switched via suitable input attenuators; the values shown (R1 = 100 k, R2 = 10 k) will give a sensitivity of approximately 400 mV. Capacitor C2, in conjunction with R7 and R9, provides an HF bypass and a step roll-off in the open-loop gain. C4 gives a further roll-off.



A high-sensitivity 'flat' input (e.g. microphone) is obtained by omitting the input attenuator and increasing the closed-loop gain. As an example, consider the situation with the input selector switch in position 2. R3 is replaced by a wire link, and R4 could be, say, 3k3 for a low input impedance. Simultaneously, R14 will be switched into circuit via S1b. If a value of 3k3 is chosen for R14, the gain will be set by the simulated 130 k resistor and the simulated 42 k parallel with R10 and R14 – i.e. approximately 2k9. The gain becomes approximately 45, giving a sensitivity of 4 ... 5 mV.

Very low values for R14 (below about 330 Ω) will provide very high sensitivities – and audible noise. A better solution in this case would be to use a microphone transformer.

Position 3 of the input selector switch is for use with magnetic cartridges. R5 is used to set the correct input impedance. The feedback network now includes R15, R16, C6, C7 and C8. These components give two of the equalisation time constants; the third is determined by this network in conjunction with R11, R12, R13.

R15 sets the sensitivity of this input; the value given (270 Ω) gives a nominal input sensitivity of 5 mV, suitable for most 'high-output' cartridges. A lower value for R15 (down to 68 Ω) gives a higher sensitivity (to 1.25 mV), and a higher value (up to 470 Ω) gives a lower sensitivity (to 9 mV).

By applying the same principles, it would be possible to provide equalisation for tape reproduction. No provision for this will be made on the p.c. board, however. One must draw the line somewhere!

The second part of this article will give a description of the control amplifier, p.c. boards, construction and interconnection details.

ic rhythm generator

In the Summer Circuits Issue (July/August 1975) a brief description was given of the SGS IC rhythm generators type M252 and M253. This article deals with the applications of these IC's in greater detail, including their connection to simple instrument generator circuits suggested in the SGS application notes, and also interfacing with the 'Minidrum' described in Elektor Nos. 2 and 3. A more sophisticated rhythm generator, constructed from standard logic IC's, is planned for a future issue.

The rhythm generator of an electronic percussion unit is that section of the unit which generates control pulses to trigger the various instrument sound generators, in predetermined sequences appropriate to the preselected rhythm. It does not, of itself, generate the instrument sounds, so a complete percussion unit must contain a rhythm generator plus instrument generators to produce the required noises.

The rhythm generator must be capable of producing pulses at various points in the bar, to trigger the tone generators in the appropriate sequence. It follows, therefore, that the rhythm generator must contain a clock pulse generator and counter capable of dividing the bar down into basic time elements. Each beat in the bar will consist of a whole number of these basic time elements. Obviously, the more time elements there are to each beat then the more complex are the rhythms that can be produced. For example, in a rhythm with a 4/4 time signature there are four beats to the bar. If the beat was divided into only one basic time element one crotchet in length, then the rhythm instruments could be triggered at only four points in the bar, and the number of rhythm patterns available would be very limited. With a basic time element of one quaver the bar could be divided into 8 elements, with a semiquaver 16 elements, with a demisemiquaver 32 elements. The smaller the basic time element, the more subtle are the rhythms that can be produced.

Table 1

Division of bar into basic time elements.

Example 1. a. time: 4/4
b. basic time elements per beat: 8
c. beats per bar: 4
d. time elements per bar:
8 x 4 = 32.

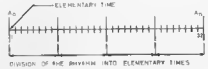
Example 2. a. time: 3/4
b. basic time elements per beat: 8
c. beats per bar: 3
d. time elements per bar:
8 x 3 = 24.

Example 3. a. time: 5/4
b. basic time elements per beat: 4
c. beats per bar: 5
d. time elements per bar:
4 x 5 = 20.

The total number of time elements in a bar depends on the number of elements per beat, and the number of beats per bar. Thus in 4/4 time, with 8 elements per beat there would be 32 per bar, but in 3/4 time there would be only 24. The counter in the rhythm generator must be capable of being programmed to count up to the appropriate number that the time signature demands before resetting to commence the next bar. The division of a bar in 4/4 time into time elements is shown in figure 1. Table 1 gives 3 examples of rhythms being divided up into basic time elements.

The basic block diagram of a rhythm generator is given in figure 2. It consists of a counter, count logic and a read only memory. The count logic is programmed by the rhythm selection input code, and determines the number that the counter reaches before resetting to zero. The ROM is addressed by the rhythm selection input code and the output of the counter. Thus as the counter counts through its sequence the contents of all the addresses through which it counts are read out in sequence. If the content of a particular address is a logic '1' then when the counter reaches that address a '1' will appear on the appropriate instrument output line, and the instrument will be triggered at that point in the rhythm sequence. The positive-going edge of the output from the memory determines the instant at which the instrument is triggered. If two successive outputs of the memory were '1' (i.e. the instrument was triggered twice in quick succession) then normally the output would initially go to '1' and stay there for two time elements, so the second triggering edge would not occur and the instrument would be triggered only

1



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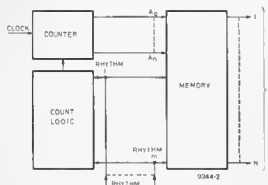

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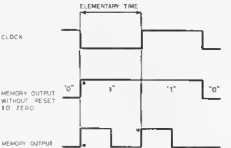

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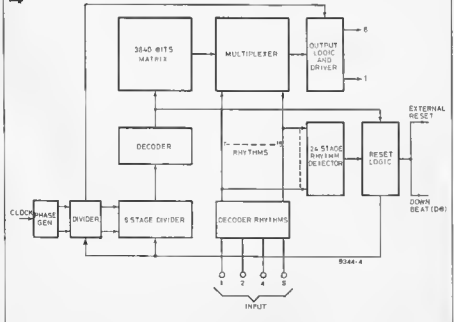

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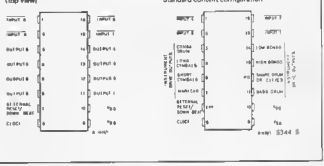

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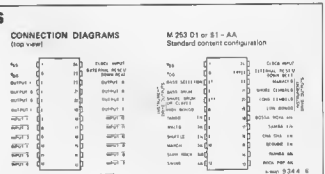

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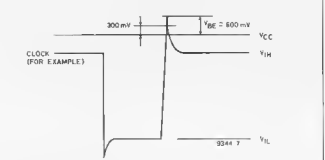


Figure 1. Sub-division of a bar into basic time elements.

Figure 2. Block diagram of a rhythm generator. The rhythm selection determines which instrument is activated at which time.

Figure 3. After each read-out, the memory outputs are reset to zero.

Figure 4. Block diagram of the rhythm generator IC type M252. The construction of the M253 differs from this insofar as the storage capacity of the matrix is somewhat smaller and the rhythm decoder is absent, since the rhythm selection is by 12 independent switches, one for each rhythm.

Figure 5. Pinout of the M252.

Figure 6. Pinout of the M253.

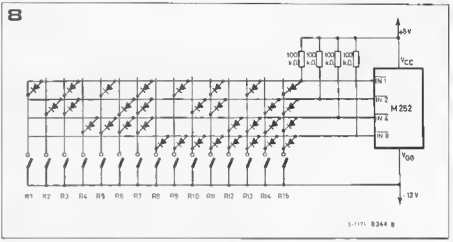
Figure 7. Positive voltage peaks should be limited to the value V_{CC} + 0.3 V. If this is exceeded, damage to the IC may occur.

Figure 8. Rhythm selection encoding for the M252 with diode matrix and selection switches for 15 rhythms (R1 . . . R15).

Figure 9. Encoding circuit for the M252 with TTL-IC's and 15 rhythm selection switches.

Figure 10. Similar circuit to that of figure 9, but using CMOS-IC's.

Figure 11. The SPDT switches of figure 10 can be replaced by single-pole normally open switches and 100 k resistors.



once (see second waveform in figure 3). To avoid this the output of the memory is reset to zero after the instrument has been triggered, and should the next output from the memory be '1' there will be a second positive-going edge to re-trigger the instrument (see third waveform of figure 3).

IC Rhythm Generators

Figure 4 shows the internal block diagram of the M252 rhythm IC, the pin configuration of which is given in figure 5. Pulses from the clock pulse generator are fed into a phase generator that produces two out-of-phase, non-overlapping pulse trains, which are required to control the following divider stage. This divider produces the reset pulses that reset the memory outputs back to zero after each readout. The width of the reset pulse is dependent on the mark-space ratio of the clock signal. The output of the first divider is used to clock a further 5 stage counter (divider) consisting of master slave flip-flops. This can count up to the maximum of 32 required to divide a bar of 4/4 time into 32 elements. The outputs of the divider are decoded and used to address the ROM, which in this case is simply a matrix. The inputs (rows) of the matrix are connected to the 32 outputs of the decoder, while the outputs (columns) are arranged in 15 groups of 8 outputs each. The 15 groups correspond to the 15 rhythms that the IC will produce, and the 8 outputs correspond to the 8 instrument outputs that the IC can drive. Which of these 15 groups is actually connected to the instrument outputs is dependent on the rhythm selected. The number of the rhythm selected is fed into the rhythm select inputs in binary, is decoded and used to control the multiplexer that routes the appropriate group to the output logic and drivers.

The counter reset logic is controlled by a rhythm detector, so that where the rhythm is in 3/4 time (or 6/8) the counter is reset after 24 clock pulses. For rhythms in 4/4 or 2/4 time the counter is allowed to achieve its maximum count of 32.

Pin 7 of the IC is a combined input/output connection. As an input it functions as an external reset to return the counter to zero from any point in the bar. As an output it provides a downbeat signal to indicate the first on-beat in the bar. The input and output functions may be isolated by means of a

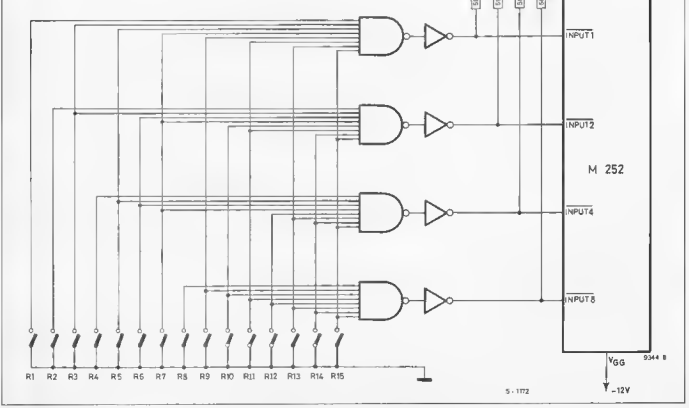


Table II

Instrument		IC-connection M252	M253
BD	Bass drum	11	4
SD/CL	Snare Drum/ Claves (woodblocks)	12	5
HB	High Bongo	13	6
LB	Low Bongo	14	19
MR	Maraccas	6	22
SC	Short Cymbals	5	21
LC	Long Cymbals	4	20
CD	Conga Drum	3	–
BA	Altern. Bass	–	3

	Rhythm		Input Code M252 8421	IC-connection M253
1.	Waltz	3/4	1110	8
2.	Jazz Waltz	3/4	1101	–
3.	Tango	2/4	1100	7
4.	March	2/4	1011	10
5.	Swing	4/4	1010	12
6.	Foxtrot	4/4	1001	–
7.	Slow Rock	6/8	1000	11
8.	Rock Pop	4/4	0111	13
9.	Shuffle	2/4	0110	9
10.	Mambo	4/4	0101	–
11.	Beguine	4/4	0100	15
12.	Cha Cha Cha	4/4	0011	16
13.	Bajon	4/4	0010	–
14.	Samba	4/4	0001	17
15.	Bossanova	4/4	0000	18
16.	Rumba	4/4	–	14

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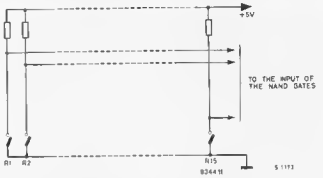

diode in the external reset line. In the case of time signatures other than 3/4 or 4/4, the downbeat output can be used to trigger a monostable, the output of which then provides the actual downbeat signal.

The rhythm selection is made by feeding a four bit binary-coded signal into pins 1, 2, 5 and 16. Table 2 gives the codes for each of the 15 rhythms that the IC can produce. When the input code is 1111 no rhythm is produced and the instrument outputs are inhibited. The counter still counts to 32 however and the downbeat signal is present.

The M253 functions in a similar manner to the M252, but, whereas the rhythm selection for the M252 is made in binary, the rhythm selection for the M253 is made by applying a logic '0' to one of 12 rhythm selection inputs. The storage matrix of the M253 has a capacity of 32 x 8 x 12 = 3072 bits, as opposed to the 32 x 8 x 15 = 3840 bits of the M252. The M253 is capable of producing only 12 basic rhythms, as opposed to the 15 produced by the M252, although by applying a '0' to more than one input simultaneously various mixed rhythms may be produced, which is not the case with the M252.

Electrical Characteristics

The static and dynamic electrical characteristics and absolute maximum ratings of the M252 and M253 are given in tables 3, 4 and 5 respectively. All voltages given in these tables are referenced to V_{SS}, which may be any convenient value with respect to ground. The actual value of V_{SS} is unimportant,

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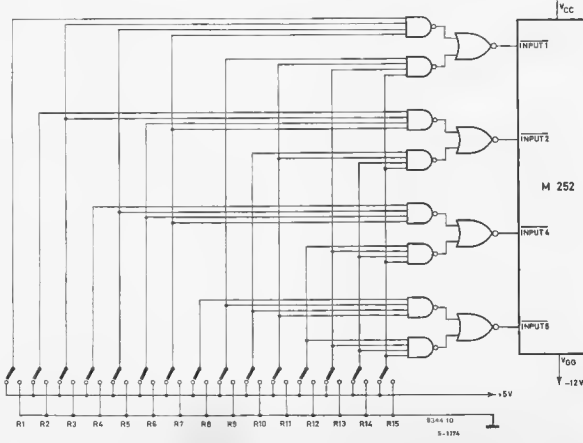

Table III

Static characteristics (positive logic, $V_{GG} = -11.4\ V \ldots -12.6\ V$, $V_{SS} = +4.75\ V \ldots +5.25\ V$, $T_{amb.} = 0 \ldots +70°C$, if not otherwise stated).

Parameter	Test conditions	min.	typ.	max.	Units
CLOCK INPUT					
V_{IH} Clock 1-level		$V_{SS} - 1.5$		V_{SS}	V
V_{IL} Clock 0-level		V_{GG}		$V_{SS} - 4.1$	V
DATA INPUTS					
V_{IH} Input 1-level		$V_{SS} - 1.5$		V_{SS}	V
V_{IL} Input 0-level		V_{GG}		$V_{SS} - 4.1$	V
I_{LI} Input current	$V_I = V_{SS} - 10\ V$, $T_{amb.} = +25°C$			10	µA
EXT. RESET					
V_{IH} Input 1-level		$V_{SS} - 1.5$		V_{SS}	V
V_{IL} Input 0-level		V_{GG}		$V_{SS} - 4.1$	V
DATA OUTPUTS					
R_O output impedance	$V_{SS} - 1\ V \leqslant V_O \leqslant V_{SS}$		250	500	k
V_{OH} Output 1-level	$I_L = 1\ mA$	$V_{SS} - 0.5$		V_{SS}	V
I_{LO} Output leakage current	$V_I = V_{IH}$, $V_O = V_{SS} - 10\ V$, $T_{amb.} = +25°C$			10	µA
POWER REQUIREMENTS					
PC Power dissipation	$T_{amb.} = +25°C$		120	250	mW

Table IV

Dynamic characteristics (positive logic, $V_{GG} = -11.4\ V \ldots -12.6\ V$, $V_{SS} = +4.75 \ldots 5.25\ V$, $T_{amb.} = 0 \ldots +70°C$, if not otherwise stated.

Parameter	min.	max.	Units
CLOCK INPUT			
f Clock frequency	0	100	kHz
t_p Pulse width[1]	5		µs
t_r Rise time[2]		100	µs
t_a Decay time[2]		100	µs
EXT. RESET			
t_p Pulse width	5		µs

[1] at 50% of the maximum amplitude.
[2] between 10% and 90% of the maximum amplitude

Table V

Absolute Limit Values

V_{GG} Supply voltage[3]	−20 V . . . +0.3 V
V_I Input voltage[3]	−20 V . . . +0.3 V
I_O Output current (per output)	3 mA
T_S Storage temperature	−55°C . . . +150°C
$T_{amb.}$ Operating temperature	0 . . . +70°C

[3] related to voltage V_{SS}

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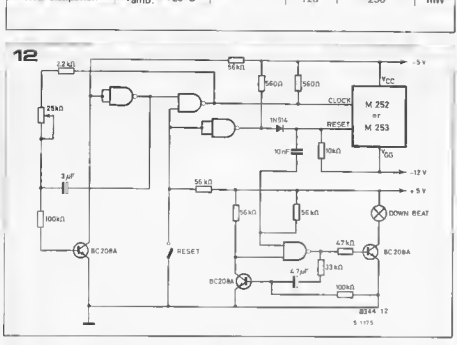


but it is important that the value of V_{GG} with respect to V_{SS} does not lie outside the range specified in table 5.

For example, if V_{SS} is +20 V then V_{GG} must not be below 0 V. If V_{SS} is 0 V then V_{GG} must not be below −20 V.

Where the rhythm IC is to be combined with other logic circuits requiring a positive supply voltage it is common practice to set $V_{SS} (= V_{CC}) = +5$ V and $V_{DD} = -12$ V.

None of the absolute maximum ratings given in table 5 must ever be exceeded, even for short periods. This applies equally in both the positive and negative sense. Taking the clock input (figure 7) as an example (the same consideration applies to all other pins), while it is essential that the input voltage should never become more negative than 20 V below V_{SS}, it is equally important that it should never become more positive than V_{SS}, even by a small amount, as otherwise the surrounding negative areas on the chip will be discharged and the circuit will not function reliably. Should the voltage exceed V_{SS} by more than 300 mV then the IC will almost certainly suffer permanent damage.

Interfacing

This section is intended to show various possibilities for practical applications of the rhythm IC, including interfacing with various types of instrument tone generator circuit.

Rhythm Selection

Selection of the desired rhythm in the case of the M252 can be carried out in several ways:

1. programming in straight binary using 4 single pole on-off switches. This is the simplest method in terms of circuitry, but the codes for each rhythm must be remembered or noted down.
2. diode-matrix encoder from 1-of-15 to binary (figure 8). The rhythm is selected by a single pole 16-way switch (can be rotary or 15-way dependent latch pushbutton bank). This is encoded into binary by the diode matrix. Using a rotary switch the 16th position would not be connected, so all inputs would be held high by the 100 k resistors and no rhythm would be selected. Using a 15-way pushbutton bank, the same would be achieved with no push-button depressed.
   The diodes used are type 1N914 (1N4148). Any other type with reverse breakdown voltage greater than 20 V and reverse leakage current less than 1 µA at 18 V would also be suitable.
3. 1-of-15 encoder using logic IC's (figure 9). This is the circuit of a decoder using TTL logic IC's. With no switches depressed the inputs of all the 8-input NAND-gates are high, the outputs are low, so the outputs of the inverters are high and no rhythm is selected. When a switch is depressed the inverter outputs assume the appropriate binary input code. An open collector inverter IC such as the 7405 should be used in this circuit, as the high output state voltage is not then limited by the saturation voltage of the output transistor and diode as it is with a 'totem-pole' output stage. For the 8-input NAND-gates four 7430 IC's would be suitable.

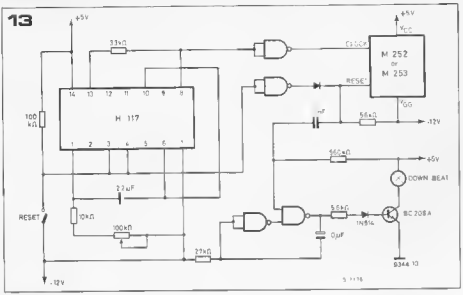


Figure 12. Clock generator and down-beat-indicator, using discrete components and one TTL-IC.

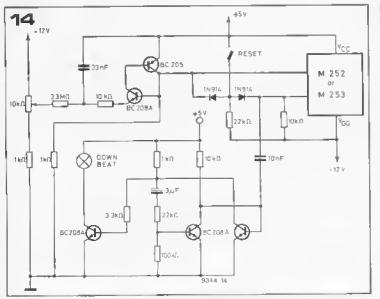
Figure 13. Clock generator using the HLL-IC H 117. This IC provides a very stable clock signal.

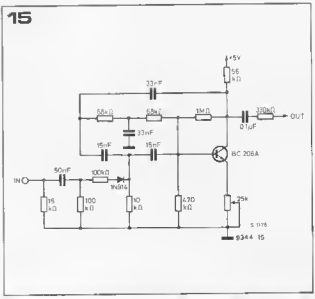
Figure 14. Circuit of a clock generator and down-beat-indicator consisting entirely of discrete components.

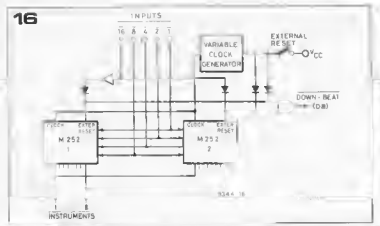
Figure 15. Instrument generator comprising a transistor and parallel-T-filter.

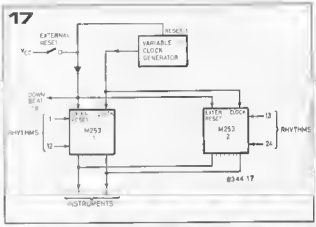
Figures 16 and 17. Using custom-programmed versions of the M252 or M253 twice the number of rhythms are available.

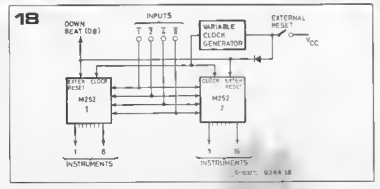
Figures 18 and 19. Again using custom versions of the IC's, the number of instruments may be doubled.

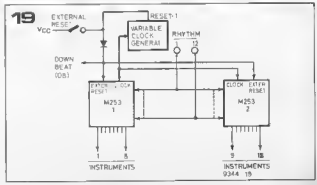


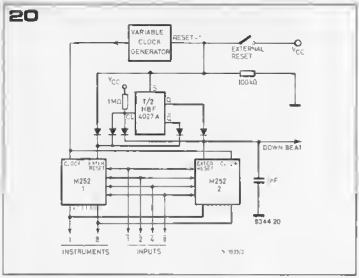


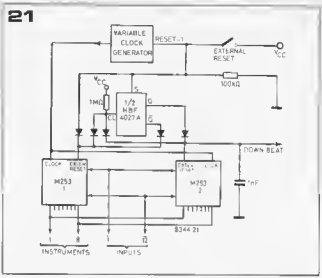












Another encoder circuit is shown in figure 10. This makes use of MOS IC's. In this case changeover switches are used to switch the inputs between the '0' and '1' states (single-pole switches and 100 k pullup resistors could also be used [figure 11]). Pullup resistors are not required at the outputs of the NOR-gates, however, as the high output voltage of CMOS is practically equal to supply voltage. IC's type 4012 would be suitable for the 4 input NAND gates (four IC's required), and for the NOR gates one IC type 4001 would be suitable.

Clock Generator

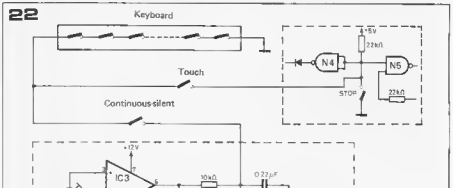
Figure 12 shows the circuit of a clock generator and downbeat indicator using TTL IC's and discrete components. An IC type 7400 can be used for the four 2-input NAND-gates. The frequency of the clock generator can be adjusted between about 3 and 30 Hz by means of the 25 k potentiometer. The downbeat indicator is a monostable consisting of a NAND-gate and transistor, and a second transistor that drives the indicator lamp or LED. The downbeat indicator lamp lights for about 350 ms on the first beat of each bar. The reset switch grounds the inputs of two NAND-gates, which inhibits the clock output and puts a '1' on the clock and reset inputs. The TTL IC's receive their supply voltage from V_{CC} (+5 V) and ground (0 V).

A second approach to the design of a clock generator and downbeat indicator is shown in figure 13. Here the clock generator is constructed around a high level logic (HLL) monostable IC type H117. The clock frequency can be varied between about 5 and 30 Hz by means of the 100 k potentiometer. For the NAND-gates an HLL IC type H102 can be used. The HLL IC's derive their supply voltage from the +5 V and −12 V supplies. The downbeat indicator lights for about 350 ms at the start of each bar.

Finally, figure 14 shows the circuit of a clock generator and downbeat indicator constructed entirely from discrete components. The clock frequency of this circuit can be adjusted from about 5 to 30 Hz by means of the 10 k potentiometer. In this circuit also the downbeat indicator lights for about 350 ms at the beginning of each bar.

Instruments

A simple circuit for the simulation of percussion instruments is given in figure 15. It consists, essentially, of a twin-T oscillator whose loop gain is adjusted by means of the 25 k potentiometer so that it just fails to oscillate. It then becomes effectively a high-Q resonant circuit that can be excited by a pulse from the rhythm generator fed into the input. Since the potentiometer adjusts the Q of the circuit it affects the time for which the circuit will ring after the input pulse has been applied, and hence the duration of the instrument sound.



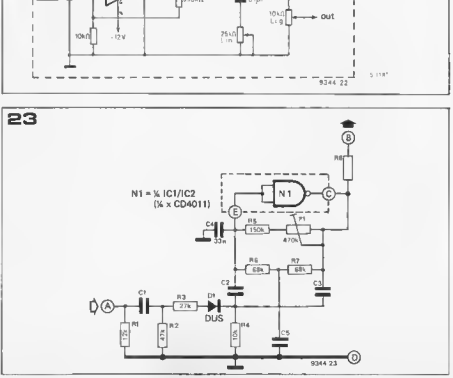


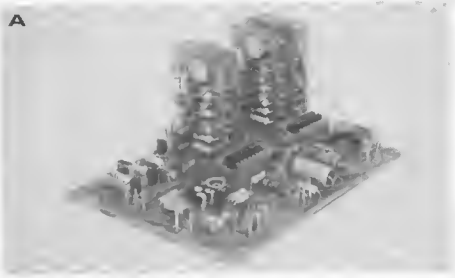
Figure 20 and 21. Using two custom IC's, in this circuit the first IC plays the first half of the bar, and the second IC the second half, thus doubling the number of time elements per bar.

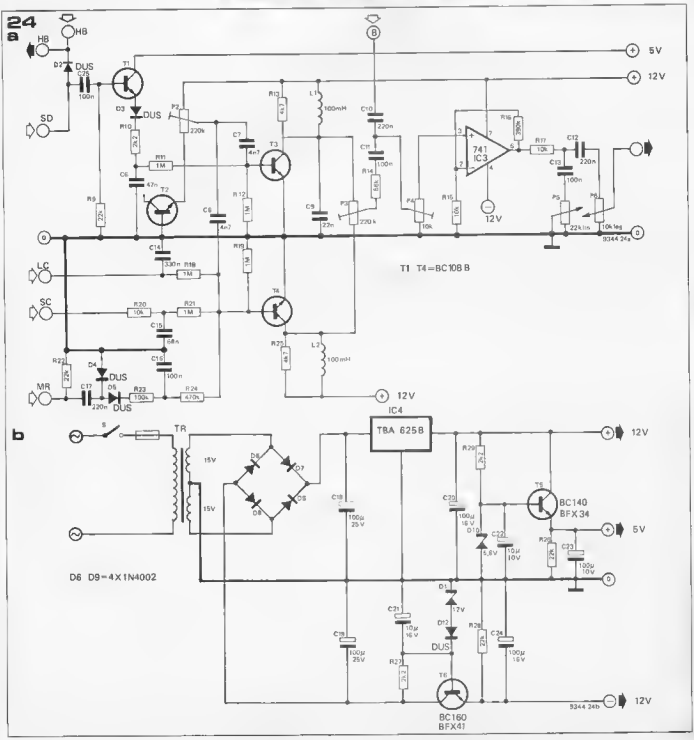
Figure 22. Automatic control of the rhythm generator by en organ keyboard or pedel-board.

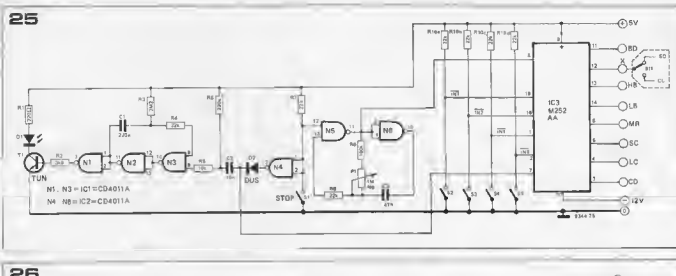
Figure 23. Circuit of the tone generator for percussion instruments, using a CMOS-gate as the active element instead of a transistor.

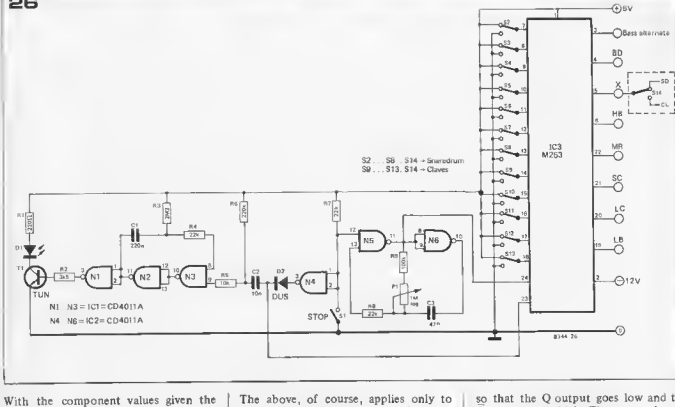
Figure 24. Circuit of the noise generators, pre-amplifier and power supply of a complete percussion unit.

Photo A. The five smaller instrument printed circuit boards are mounted on the base printed circuit board. Only four instruments are required for the M253, as this IC has no conga drum output.









With the component values given the circuit simulates the sound of a bongo. By changing the capacitance values the circuit can be made to simulate many other instruments such as bass drum, conga, woodblocks etc. Instruments that make use of filtered noise, such as cymbals and maraccas will be described later.

Extensions

In principle the number of rhythms can be doubled by connecting in parallel the instrument outputs of two rhythm IC's. This is shown for the M252 in figure 16 and for the M253 in figure 17. The rhythm selection for the M252's is made by means of a 5-bit binary input instead of the four-bit input required for one IC. The most significant bit is used to select one IC or the other by controlling the external reset input, and the other four bits select the rhythms in the normal way. For the M253's rhythm selection is simply a question of providing a programming switch with 24 positions instead of 12.

The above, of course, applies only to custom programmed versions of the IC, since the two IC's must have different rhythm patterns programmed into them. The standard versions of the IC obtainable on the retail market are available only with the standard programming shown in table 2.

In a similar manner, using custom programmed IC's the number of instruments can be extended to 16 by using two IC's programmed with the same rhythms but with different instrument outputs. This is shown in figures 18 and 19. In this case the rhythm select inputs of the two IC's are connected in parallel.

A third possibility is to use two custom programmed IC's to increase the maximum number of time elements per bar to 64, as shown in figures 20 and 21. In these two circuits the first half of the bar is played by the first IC, the second IC being inhibited by the Q output of the flip-flop, which holds the external reset input high. The downbeat output of the first IC then clocks the flip-flop so that the Q output goes low and the Q output goes high. The external reset input of the first IC is thus held high, inhibiting it, while the second IC plays the second half of the bar. At the end of the bar the downbeat output of the second IC clocks the flip-flop back to its original state.

Rhythm Generator and organ

An electronic percussion section is frequently built into an electronic organ, and it is useful in such a case to have the percussion unit controlled by the organ. Figure 22 shows a common method of achieving this. The parts of the circuit enclosed in dotted boxes are portions of figures 24, 25 and 26. The 741 op amp is the instrument output amplifier of figure 24 (IC3), while the two NAND-gates form part of the clock generator and reset circuit in figures 25 and 26 (N4 and N5).

The rhythm generator is usually controlled by series connected contacts on the pedalboard of the organ, and the

control can operate in several modes:

i with the stop switch closed the rhythm generator is reset and the clock is stopped.

ii with the stop, touch, and continuous/silent switches open the rhythm generator runs continuously.

iii with the continuous/silent switch open and the touch switch closed the rhythm generator will be reset until a pedal is depressed, when it will start. Obviously, as soon as the pedal is released it will be reset again, so the pedal note must be sounded for the whole of a bar in order to obtain the complete rhythm.

iv with the continuous/silent switch closed and the touch switch open the rhythm generator runs continuously but the instruments are heard only when a pedal is depressed, as at other times the output of the 741 is shorted to ground. In this case the downbeat indication must be used to synchronise the organ with the rhythm generator.

Note that the continuous/silent and touch switches should not be depressed simultaneously, as otherwise the output of the 741 will interfere with the clock.

Complete Percussion Section

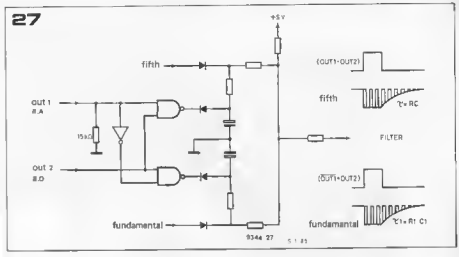
Having discussed the various possibilities, the circuit of a complete percussion section is given in figures 23 to 26. The unit contains percussion instruments of three kinds:

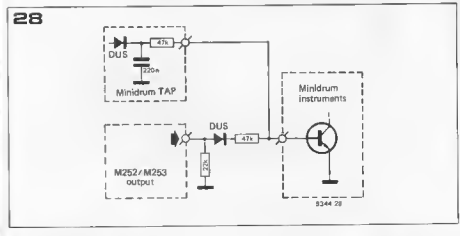
1. Those whose sound is a damped oscillation of a particular frequency i.e. high bongos (HB), low bongos (LB), bassdrum (BD), conga (CD) and claves or woodblocks (CL).
2. Those whose sound is derived by filtering white noise to achieve a particular spectrum i.e. long cymbal (LC), short cymbal (SC) and maraccas (MR).
3. Those whose sound contains both a damped oscillation and filtered noise, i.e. snaredrum (SD).

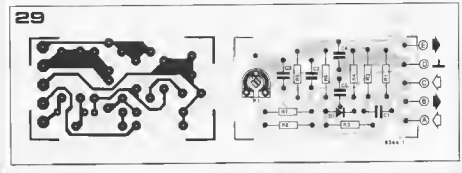
As mentioned earlier the first class of instruments is simulated using a twin-T oscillator circuit with insufficient gain to maintain oscillation. When this is excited by a control pulse from the rhythm generator it produces a damped oscillation that decays at a rate dependent on the loop gain of the oscillator. In the final circuit of the percussion unit a CMOS gate is used as the active element in the oscillator instead of a transistor. This circuit is shown in figure 23.

The control pulse from the rhythm IC is fed in at point A. R1 acts as a pull-down resistor for the 'open-drain' outputs of the rhythm IC. The control pulse is differentiated by C1 and R2 and is then fed into the twin-T oscillator via R3 and D1. D1 ensures that the oscillator circuit is affected only by the positive-going edge of the pulse, as during the negative-going edge D1 is reverse-biased. If D1 were not present then the oscillator would be severely damped by the negative-going edge of the pulse.

To produce the different instrument







Parts list for figures 23 and 29 components, common to all instrument oscillators.

Resistors.
R1 = 12 k
R2 = 47 k
R3 = 27 k
R4 = 10 k
R5 = 150 k
R6,R7 = 68 k
P1 = 470 k

Capacitors:
C4 = 33 n

Semiconductors:
D1 = DUS

Frequency determining components

Resistors:	Instruments				
	HB	LB	BD	CD	CL
R8 =	390 k	390 k	100 k	390 k	1 M

Capacitors:

C1 =	33 n	39 n	150 n	56 n	4n7
C2,C3 =	10 n	12 n	47 n	18 n	1n5
C5 =	33 n	39 n	150 n	56 n	4n7

Figure 25. Circuit of the complete rhythm generator section using the M252, including down-beat indicator.

Figure 26. The same circuit as figure 25, but with the M253.

Figure 27. Circuit for controlling the alternating bass of an organ.

Figure 28. Interfacing the rhythm generator described here with the 'Minidrum'.

Figure 29. Printed circuit board and component layout for the circuit of figure 23. The NAND-gate is on the main p.c.b. (EPS 9344-1).

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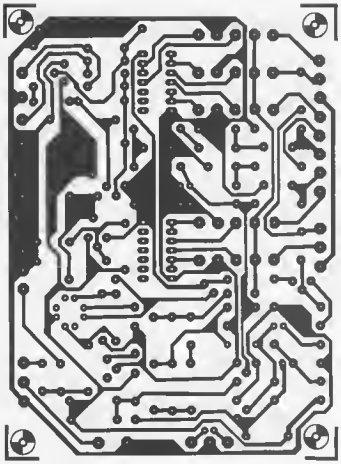


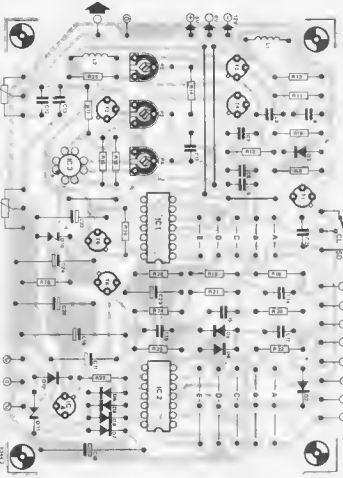


Figure 30. Printed circuit board and component layout for the circuit of figure 24. (EPS 9344-2).

Photo 8. A 16 position binery coded switch for rhythm selection with the M252.

Parts list for figures 24 and 30

Resistors:
R9,R22,R26,R28 = 22 k
R10,R27,R29 = 2k2
R11,R12,R18,R19,R21 = 1 M
R13,R25 = 4k7
R14 = 56 k
R15,R16,R20 = 10 k
R16 = 390 k
R23 = 100 k
R24 = 470 k
P2,P3 = 220 k
P4 = 10 k
P5 = 25 k lin.
P6 = 10 k log.

Capacitors.
C8 = 47 n
C7,C8 = 4n7
C9 = 22 n
C10,C12,C17 = 220 n
C11,C13,C16,C25 = 100 n
C14 = 330 n
C15 = 68 n
C18,C19 = 100 µ/25 V
C20,C24 = 100 µ/16 V
C21 = 10 µ/16 V
C22 = 10 µ/10 V
C23 = 100 µ/10 V

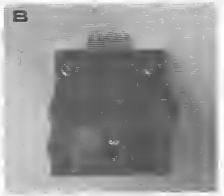
Semiconductors.
D2,D3,D4,D5,D12 = DUS
D6,D7,D8,D9 = 1N4002
D10 = 5.6 V Zener
D11 = 12 V Zener
T1,T2,T3,T4 = BC108B
T5 = BC140/BFX34
T6 = BC160/BFX41
IC1,IC2 = CD4011 (see figure 23)
IC3 = 741
IC4 = T8A625B

Miscellaneous:
L1,L2 = Coil 100 mH
Transformer = 2 x 15 V, 500 mA secondary, 220-240 V primary

sounds only C2, C3 and C5 need to be varied to alter the frequency of oscillation. The values of these components for the different instruments are given in the parts list. P1 varies the damping of the oscillator and hence the rate at which the instrument sound decays. The outputs of the instrument generators are fed out through mixing resistors (R8) to the output amplifier IC3 in figure 24 (point B). The values of R8 are different for the various instruments to obtain the correct relative amplitude for each instrument.

The white noise for the second class of instruments is derived from the reverse-biased base-emitter junction of an NPN transistor (T2 in figure 24). This junction exhibits avalanche breakdown (like a zener diode) at between 5 and 9 volts in most cases, and, like a zener diode, it generates noise.

The manner in which the noise signal is switched depends on the particular instrument to be simulated. In the case of the long cymbal the control pulse charges up C14 and turns on T4. The noise signal from the slider of P2 is applied to the base of T4 via C8. Filtering of the noise is achieved by the inductor L2 in parallel with R25. The impedance of this increases at high

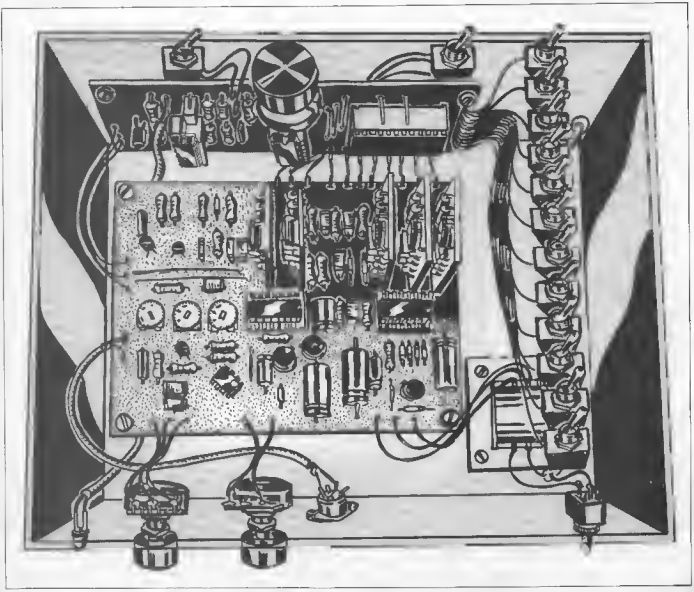


frequencies, so the gain of this stage increases with frequency, which means that the high frequency components of the noise signal are amplified more than the low frequencies. When the control pulse finishes, the voltage on C14 decays exponentially – so T4 gradually turns off. The short cymbal operates in more or less the same manner, but C15 is smaller than C14, so the decay and turn-off is more rapid.

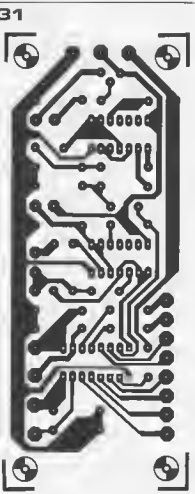
The characteristic of the cymbal sound is thus a fairly rapid attack followed by a more or less gradual decay.

The amplitude of the maraccas sound builds up relatively slowly and then decays. The reason for this is that C16 is charged up fairly slowly via D5 and R23, so T4 turns on gradually. When the control pulse ends C16 discharges through R24 into the base of T4, and T4 gradually turns off as the voltage on C16 falls.

The snaredrum makes use of both an instrument oscillator and a noise signal. The snaredrum control pulse is fed to the base of T1 via C25, and is also fed to the oscillator via D2. The same oscillator is also used for the high bongos, so D2 provides isolation to prevent the high bongo control signal from triggering the snaredrum noise circuit. When the control pulse turns on T1, C6 is charged via D3 and R10; T3 is then turned on by the voltage on C6, allowing the noise signal on C7 to be amplified by T3. The collector resistor R13, L1 and C9 form a filter to modify the spectrum of the snaredrum noise. The noise amplitude is controlled by P2, and the relative amplitudes of the snaredrum noise and the other noise instruments are set by P3. The noise signals are fed, together with the other instrument inputs at point B, into the output amplifier IC3.



31



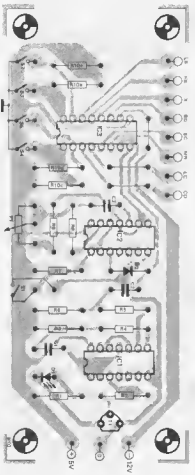


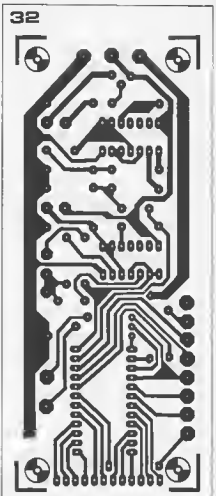
Figure 31. Printed circuit board and component layout for the circuit of figure 25. This printed circuit board (EPS 9110) has already been published in the 'Summer Circuits' issue July/August '75.

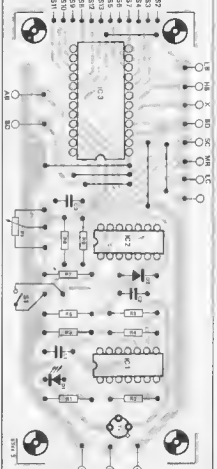
Figure 32. Printed circuit board and component layout for the circuit of figure 26. (EPS 9344-3).

Parts list for figures 25, 26, 31 and 32

Resistors:	figures 25,31	figures 26,32
R1 =	220 Ω	220 Ω
R2 =	3k9	3k9
R3 =	2M2	2M2
R4,R7,R8 =	22 k	22 k
R5 =	10 k	10 k
R6 =	220 k	220 k
R9 =	100 k	100 k
R10 =	22 k (4x)	—
P1 =	1 M	1 M
Capacitors:		
C1 =	220 n	220 n
C2 =	10 n	10 n
C3 =	47 n	47 n
Semiconductors:		
D1 =	LED	LED
D2 =	DUS	DUS
IC1,IC2 =	CD4011	CD4011
IC3 =	M252AA	M253AA
Miscellaneous		
S1 =	Single pole normally open (SPST)	Single pole normally open (SPST)
S2 . . . S5 =	Single pole normally open (SPST)	—
S2 . . . S13 =	—	Single pole, changeover (SPDT)
S14 =	Single pole, changeover (SPDT)	Single pole, changeover (SPDT)

32





The output amplitude can be controlled by P6, and P5 functions as a treble cut control to modify the tone of the instruments.
The lower section of figure 24 is the power supply for the percussion section. It makes use of an IC voltage regulator and two simple series stabilizers, and requires little explanation.

Clock generator and rhythm IC

Figure 25 shows the circuit of the clock generator and downbeat indicator as used with the M252, while figure 26 shows a similar circuit for the M253, the only difference between the two being the rhythm selection switching. The clock generator and downbeat monostable in these circuits make use of CMOS NAND-gates. P1 adjusts the clock frequency.
The stop switch S1 is arranged so that the first beat of the bar occurs immediately the switch is opened. If the switch is closed than the reset input is held high by N4 and the output of the clock (N5) is also high. When the stop switch is released the reset condition is removed and the clock generator immediately gives a negative-going pulse, starting the rhythm sequence.
The downbeat indicator consists of a monostable (N2 and N3) to lengthen the short downbeat pulse available from the downbeat output of the IC so that it can be seen, together with a driver stage (N1 and T1) to switch the LED 1.
S14 is provided to give a choice between snaredrum and woodblocks. Normally the snaredrum would be used for rhythms 1-9 of the M252, and those rhythms selected by inputs 7-13 of the M253, while the woodblocks would be switched in for the remaining rhythms. This is a question of personal taste, however.

Alternating Bass

A facility found on the M253 but not on the M252 is the output BA (pin 3) for control of the alternating bass of an electronic organ. A circuit for this purpose is shown in figure 27. The organ bass note and a note a fifth higher are fed into the circuit. Whenever a BD control pulse appears, but no BA control pulse then the fundamental is allowed through to the output. When both the BD and BA control pulses occur simultaneously then the fifth is allowed through to the output. The result is alternating fundamentals and fifths on each beat of the bass drum.

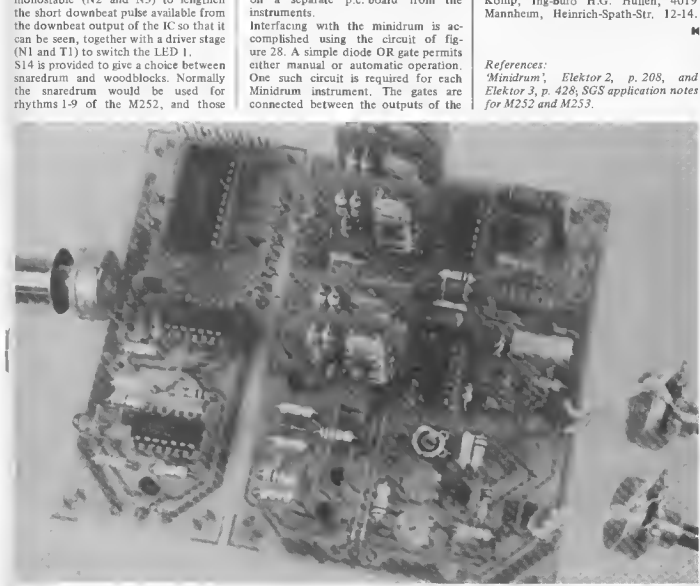
Interfacing with minidrum

Although the foregoing circuits may be assembled as a complete automatic percussion section, some readers may wish to interface the rhythm section of this system with the 'Minidrum' described in Elektor Nos. 2 and 3, rather than using the instruments described here. This can easily be done as the rhythm section is on a separate p.c. board from the instruments.
Interfacing with the minidrum is accomplished using the circuit of figure 28. A simple diode OR gate permits either manual or automatic operation. One such circuit is required for each Minidrum instrument. The gates are connected between the outputs of the manual TAP and the trigger inputs of the instruments.

Construction of complete percussion section

The p.c. board layouts for the rhythm generator section of the percussion unit are given in figures 31 (M252) and 32 (M253). The instrument section board layout is given in figure 30. Although the CMOS gates for the instrument oscillators are mounted on this board the frequency-determining components are mounted on small 'daughter-boards' (see figure 29 and photograph A) so that they can easily be changed for experimentation with different instrument sounds. The connection points A to E on the daughter-boards correspond to similar connection points on the mother-board. Similarly, the instrument outputs of the rhythm section board line up exactly with the corresponding inputs on the mother-board, so these two boards may be mounted side-by-side and joined by short links.
As a final note, a special 16-position switch with binary coded outputs is available for rhythm selection using the M252. This is not, so far as we are aware, available in the U.K. but it may be obtained from a German firm — Komp, Ing-Büro H.G. Hullen, 4019 Mannheim, Heinrich-Spath-Str. 12-14.

References:
'Minidrum', Elektor 2, p. 208, and Elektor 3, p. 428; SGS application notes for M252 and M253.



Polaroid timer

The development of Polaroid films is temperature dependent. For monochrome film the development time varies, whereas for colour film the exposure varies and a 'cold-clip' may have to be used. The timer described here has a temperature sensor, so that it will indicate how and for how long films should be developed.

As owners of Polaroid cameras will know, Polaroid film is temperature sensitive. Monochrome film must be developed for varying times depending on the temperature. The new colour film ('Polacolor 2') has improved development time latitude and may be developed for 60 seconds at ambient temperatures between 18 and 32°C (65-90°F). At temperatures above 32°C the exposure control on the camera must be turned one mark towards 'darken'. At temperatures below 18°C the exposure control must be turned one mark towards 'lighten' and the 'cold-clip' provided with the camera must be used. At temperatures below 13°C the exposure control must be turned two marks towards 'lighten' and the cold-clip must be used. Development time is 60 seconds in all these cases.

The more expensive versions of Polaroid cameras have built-in development timers, but not a thermometer!

The timer described in this article performs several functions.

1. it provides a temperature dependent development time for monochrome prints.
2. It provides a 60 seconds development time for colour prints and indicates the required setting of the exposure control, and if the cold-clip is required.

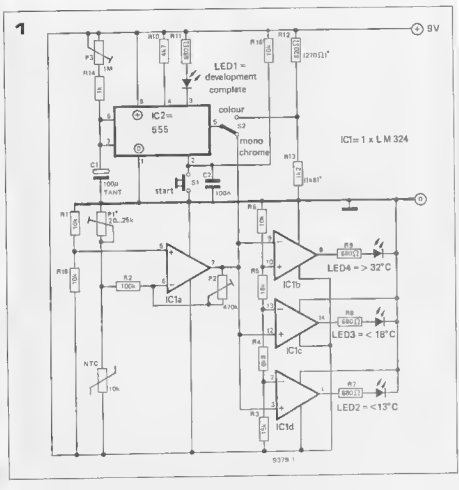
Operation of the timer is quite simple. The basic timer is a 555 in the monostable mode. With S2 in the colour position it provides a 60 second interval.

Temperature control is provided by a NTC thermistor which forms part of a bridge circuit. The bridge is balanced by P1 at 21°C. Any increase or decrease in temperature will cause an imbalance which is amplified by op-amp IC1a. The imbalance voltage is applied to the control voltage input of the 555 to increase or decrease the development time. The voltage is also applied to three op-amps connected as comparators. When the temperature is above 32°C the voltage on the inverting input of IC1b will be less than the reference voltage on the non-inverting input, so LED 4 will light, indicating 'exposure control 1 mark darken'. Between 18 and 32°C no LEDs will be lit, below 18°C the voltage on the +input of IC1c will exceed the voltage on the −input, so LED 3 will light, and below 13°C LED 2 and LED 3 will be lit.

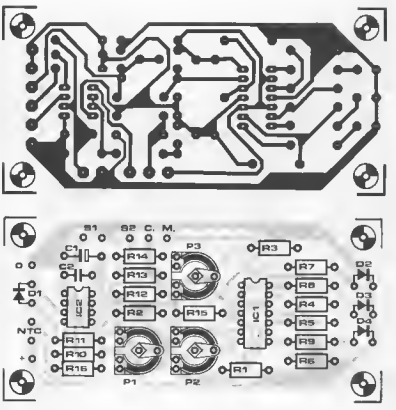
For monochrome film, the development time depends on the ambient temperature – and on the type of film. When S2 is set in position 'monochrome', the setting of the timer is controlled by the output of IC1a.

Construction and adjustment

Various options are offered as far as the



2



Parts list

Resistors:
R1,R6,R15 = 10 k
R2 = 100 k
R3 = 15 k
R4 = 6k8
R5 = 18 k
R7,R8,R9,R11 = 680 Ω
R10 = 4k7
R12 = 820 Ω (or 270 Ω, see text)
R13 = 1k2 (or 1k5, see text)
R14 = 1 k
P1 = 12 k (fixed) or 22 k (presat), see text
P2 = 470 k (preset)
P3 = 1 M (preset)

Capacitors:
C1 = 100 µ/10 V
C2 = 100 n

Semiconductors:
IC1 = LM324
IC2 = 555
D1 . . . D4 = LED

construction is concerned – the choice will depend on how much of a perfectionist the constructor is!

First the values of R12 and R13 must be chosen. These depend on the type of *monochrome* film chosen:

– for type 87, R12 is 820 Ω and R13 is 1k2;
– for type 107, R12 is 270 Ω and R13 is 1k5.

Adjustment now proceeds as follows: First set the correct development time for colour:

– set S2 in position 'colour';
– adjust P3 so that the development time is 60 seconds.

Now set the monochrome timing. For this there are two possibilities, an easy way (A) that should be accurate enough for all normal use, and a more difficult procedure (B) for the perfectionist. We advise procedure 'A' . . . .

A. the easy way:

– use a fixed 12 k resistor instead of P1;
– temporarily, replace the NTC by a fixed 18 k resistor;
– set S2 in position 'monochrome';
– adjust P2 to give a development time of 90 seconds (for film type 87) or 45 seconds (for film type 107);
– replace the NTC resistor.

B. for perfectionists only:

– heat the NTC to 21°C (70°F);
– set S2 in position 'monochrome' and adjust P1 until the correct development time is achieved (45 seconds for film type 87 or 22.5 seconds for film type 107), the output of IC1a should be almost exactly half the supply voltage – the NTC bridge is in balance;
– cool the NTC to 10°C (50°F);
– adjust P2 until the correct development time is achieved: 90 seconds for film type 87 or 45 seconds for film type 107.

The advantage of method B is that it compensates for any tolerance in the nominal value of the NTC (this is why P1 was added in the first place!). However, a brief calculation shows that a 10% error in NTC value will give approximately 18% error in the development times, which is within the latitude allowed by the film. Even 20% spread in NTC value gives 'only' 36% spread in the times, corresponding to an error of some 2°C (4°F) in the temperature measurement. A final word on the construction: the NTC must be at ambient temperature, of course, so it should not be mounted inside the (closed) box. The power supply can be very simple: the circuit draws relatively little current, and any supply voltage from 9 to 15 V can be used – without need to readjust the trimmers. ◀

Figure 1. The complete circuit diagram of the timer.

Figure 2. The p.c. board and component layout (EPS 9379).

Temperature is important. The temperature of the film and the film holder **at the time of processing** has an important affect on the picture, although the film may be exposed successfully at any temperature. When the temperature is below 70°F (21°C), process for longer than the standard time, as indicated in the chart, below. Processing below 35°F (2°C) is not recommended.

TEMP. C.	TEMP. F.	TIME (sec.) Type 87	TIME (sec.) Type 107
24°	75°	30	15
21°	70°	45	22.5
18°	65°	60	30
10°	50°	90	45
7°	45°	120	60

integrated voltage regulators

The first part of this article dealt with universal, variable voltage regulators, and in particular the 723. The second part discusses the three-pin, fixed voltage IC regulators. These were first introduced as 'on-card' stabilizing for TTL circuits, and thus the first generation of these IC's were 5 V regulators. Now whole families of three-pin regulator IC's have been introduced with a wide choice of preset output voltages. This article deals with applications of these regulators, and also with ways of extending their voltage and current capability.

part 2

Fixed Voltage Regulators

These regulators IC's are intended to provide a stabilised supply capability with the minimum of external components. Consequently there are no connections for frequency compensation, current limit or voltage adjustment, all these functions being performed on the chip. The number of pins required is therefore reduced to three, input, output and common.

The regulators operate on the principles already outlined in the discussion of the 723. They almost invariably incorporate foldback current limiting. The newer types also incorporate thermal shutdown, which turns off the output transistor if the chip temperature becomes excessive (usually +165°C). The most recent types have so-called 'safe area limiting', which prevents the output stage from going outside its safe power dissipation.

The range of devices available is now quite large, and the output voltages commonly available range from +5 to +24 and −5 to −24 volts at currents from 100 mA to 3 A. Tables I and II give some idea of the range of types available, although they are necessarily incomplete and will probably be out of date by the time this article is in print, since new developments are taking place continuously.

Basic circuits using 3-pin regulators

The use of three-pin regulators is simplicity itself, and the two circuits for positive and negative regulators are given in figures 1 and 2. The only additional components required are a transformer, fuse, bridge rectifier and reservoir capacitor. To reduce output noise and ripple, and to eliminate any tendency to r.f. instability tantalum capacitors C_A and C_E may also be included. Having chosen the appropriate IC for the intended application, calculation of the other component values is relatively simple using a little arithmetic and guesstimation.

Component Values

As an example let us consider the case of an audio preamplifier requiring a power supply of +24 V at 60 mA. From Table I the LM 78L24 appears to be suitable, as this will provide +24 V at up to 100 mA. The TO-5 package is the most suitable as this can easily be fitted with a cooling clip. The pinout of this device is given in figure 9 (1). It is worth noting at this point that manufacturers have not agreed on a pin connection standard for the use of packages in voltage regulator applications, as can be seen from the different pin connections to the TO-5, TO-3 and TO-220 packages in figure 9, so beware!

Referring to Table I it can be seen that the input voltage range of the IC lies between 27.5 and 38 V. The choice of an input voltage too close to the lower limit should be avoided, as a drop in the mains voltage could easily cause the IC to come out of regulation. On the other hand, working too close to the upper limit will mean that the voltage dropped across the IC, and hence the power dissipation, will be high. A reasonable compromise is to choose the mean of the two voltages, which in this case is

Figure 1. Basic circuit using fixed positive voltage regulator.

Figure 2. Basic circuit using fixed negative voltage regulator.

Figure 3. Increasing the output voltage of a fixed voltage regulator by raising the potential of the common pin.

Table 1. A representative range of fixed positive voltage regulators.

Table 2. A representative range of fixed negative voltage regulators.

around 33 V. Transformer secondary voltages are specified as RMS (root mean square) values, so the required transformer secondary voltage for a D.C. voltage of around 33 V is:

$$V_{sec} = \frac{33}{\sqrt{2}} \text{ volts} = 23.3 \text{ V}$$

Of course, to be absolutely correct one should allow for the voltage drop across the bridge rectifier, which is about 1.4 V. In the event, the nearest commonly available secondary voltage is 24 V, so the D.C. output voltage will be:

$$V_{D.C.} = 24\sqrt{2} - 1.4$$
$$= 24 \times 1.414 - 1.4$$
$$= 33.6 - 1.4$$
$$= 32.2 \text{ which is a little on the low side.}$$

In practice, of course, due to tolerances in the transformer and differences in nominal mains voltage up and down the country the figures after the decimal point are meaningless anyway, and 32 V is quite a good enough approximation to the required value.

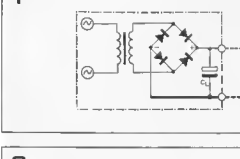
For calculation of the reservoir capacitance the rule of thumb 2200 μ per ampere of output current is useful, so in this case (allowing for the maximum

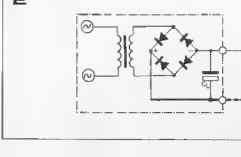
1 X = YES — = NO

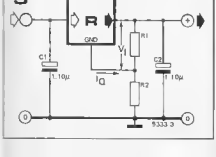
Type	V_{out} stab. (V)	I_{out} max. (A)	V_{in} min. (V)	V_{in} max. (V)	Internal current limit	Thermal protection	Safe area limit	Package	Pinout (figure 9)
LM78L05	5	0,1	7	20	X	X	X	TO-5, TO-92	1, 2
TBA 625 A	5	0,13	8	20	X	–	–	TO-5	3
LM342-05	5	0,2	7,5	20	X	X	X	TO 202 P	4
µA 78M05	5	0,2	7	20	X	X	X	TO-5	1
LM 341-5,0	5	0,5	7,5	20	X	X	X	TO 202 P	4
L 129	5	0,85	7,5	20	X	–	–	TO-125	5
LM 309 K	5	≈ 1	7	35	X	X	–	TO-3	6
LM 340-05	5	1,5	7	35	X	X	X	TO-220	7
LM 323 K	5	3	7,5	20	X	X	X	TO-3	6
LM 5000	5	3	9	20	X	X	–	TO 3	8
LM 342-8	8	0,2	8	25	X	X	X	TO-202 P	4
LM 341-6,0	6	0,5	7,2	25	X	X	X	TO-202 P	4
µA 78M06	6	0,5	9	21	X	X	X	TO-5	1
LM 340-6	8	1,5	8	25	X	X	X	TO-220, TO-3	7, 6
µA 7806	5	1,5	8	25	X	X	–	TO-3, TO-220	6, 7
LM 78L08	8	0,1	10,5	23	X	X	X	TO-5, TO-92	1; 2
LM 342-8	8	0,2	11	23	X	X	X	TO-202	4
µA 78M06	8	0,5	11,5	23	X	X	X	TO-5	1
LM 341-8,0	8	0,5	10,5	25	X	X	X	TO-202	4
µA 7808	8	1,5	10,5	25	X	X	–	TO-3, TO-220	6, 7
LM 340-8	8	1,5	10,5	25	X	X	X	TO-3, TO-220	6, 7
TBA 435	8,5	0,14	11,5	20	X	–	–	TO-5	3
LM 342-10	10	0,2	13	25	X	X	X	TO-202	4
TBA 825 B	12	0,1	15	27	X	–	–	TO-5	3
LM 78L12	12	0,1	14,5	27	X	X	X	TO-5; TO-92	1, 2
LM 342-12	12	0,2	15	30	X	X	X	TO-202	4
LM 341-12	12	0,5	14,5	30	X	X	X	TO-202	4
µA 78M12	12	0,5	14,5	30	X	X	X	TO-5	1
L 130	12	0,72	14,5	27	X	–	–	TO-126	5
LM 340-12	12	1,5	17,5	30	X	X	X	TO-3, TO-220	6, 7
µA 7812	12	1,5	14,5	30	X	X	–	TO-3, TO 220	6, 7
TBA 625 C	15	0,1	18	27	X	–	–	TO-5	3
LM 78L15	15	0,1	17,5	30	X	X	X	TO-5, TO-92	1; 2
LM 342-15	15	0,2	18	30	X	X	X	TO 202	4
µA 78M15	15	0,2	17,5	30	X	X	X	TO-5	1
LM 341-15	15	0,5	17,6	30	X	X	X	TO 202	4
L 131	15	0,6	17,5	27	X	–	–	TO-126	5
LM 340-15	15	1,5	17,5	30	X	X	X	TO 3, TO 220	6, 7
µA 7815 C	15	1,5	17,5	30	X	–	–	TO-3, TO-220	6, 7
LM 78L18	18	0,1	21,4	33	X	X	X	TO 5, TO 92	1, 2
LM 342 18	18	0,2	21	33	X	X	X	TO-202	4
LM 341-18	18	0,5	20,7	30	X	X	X	TO-202	4
LM 340-18	18	1	21	33	X	X	–	TO 3, TO-220	6, 7
µA 7818	18	1,5	21	33	X	X	–	TO-3, TO 220	6, 7
µA 78M20	20	0,5	23	36	X	X	X	TO 5	1
LM 78L24	24	0,1	27,5	38	X	X	X	TO 5; TO 92	1; 2
LM 342-24	24	0,2	27,2	38	X	X	X	TO 202	4
LM 341-24	24	0,5	27	38	X	X	X	TO 202	4
LM 340-24	24	1	27	38	X	X	X	TO-3, TO-220	8, 7
µA 7824	24	1,5	27	38	X	X	–	TO-3, TO-220	6, 7

2 X = YES — = NO

Type	V_{out} stab. (V)	I_{out} max. (A)	V_{in} min. (V)	V_{in} max. (V)	Internal current limit	Thermal protection	Safe area limit	Package	Pinout (figure 9)
LM320T5,0	–5	1,5	–7,5	–25	X	X	–	TO-220	9
LM345	–5	3,0	–7,8	–20	X	X	X	TO-3	8
LM320T6,0	–6	1,5	–8,5	–25	X	X	–	TO-220	9
LM320T8,0	–8	1,5	–10,5	–25	X	X	–	TO-220	9
LM320T12	–12	1,5	–14,5	–32	X	X	–	TO-220	9
LM320T15	–15	1,5	–17,5	–35	X	X	–	TO-220	9
LM320T18	–18	1,5	–21	–35	X	X	–	TO-220	9
LM320T24	–24	1,5	–27	–36	X	X	–	TO-220	9







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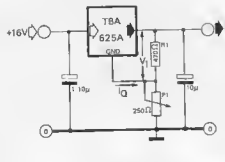

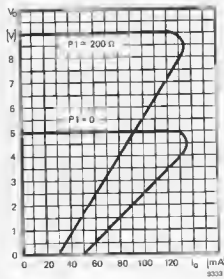

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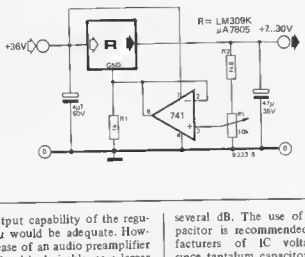


100 mA output capability of the regulator) 220 μ would be adequate. However, in the case of an audio preamplifier a low hum level is desirable, so a larger value, say 1000 μ 40 V, would be chosen to reduce the ripple level.

The ripple rejection of the LM 78L24 is quoted as 30 dB min., 43 dB typical at 120 Hz (USA line frequency = 60 Hz), but these figures apply equally well to UK conditions (line frequency = 50 Hz, ripple frequency = 100 Hz).

Ripple rejection can further be improved by inclusion of a tantalum capacitor across the output, as mentioned earlier. This may have a value between 1 μ and 10 μ and will give an improvement of several dB. The use of a tantalum capacitor is recommended by all manufacturers of IC voltage regulators, since tantalum capacitors have a lower inductance than aluminium types.

The input capacitor C_E is only necessary if the IC is some distance (in terms of lead lengths) away from the reservoir capacitor. This is particularly the case with 'on card' stabilizing, where a single transformer may supply several racks of logic p.c.b.'s, each with its own regulator IC.

The above gives a brief idea of the considerations involved when designing with regulator IC's, but in particular cases the manufacturers data sheet should always be consulted, as this gives much more information than can possibly be given in Tables I and II.

Variation of Output Voltage

Although the choice of output voltages available should prove adequate for most applications, there will be some cases where the required voltage is not found in the standard range. In such cases a regulator with a lower output voltage may be used, and the voltage may be increased by taking the common connection to a higher potential than ground. The total output voltage will then be the normal output voltage (which is maintained between output and common connection) plus the offset voltage.

The required effect can be obtained by connecting a potential divider between the output and ground, with the common pin of the IC connected to the junction of the divider resistors (figure 3). When the output of the IC is unloaded the IC itself draws a quiescent current, which flows out of the common pin. This will flow through R2. There is also a contribution to the current through R2 from the output via R1. If the quiescent current of the IC is known it is thus a relatively simple matter to calculate the required values of R1 and R2 for a particular output voltage.

The total output voltage $V_0 = V_1 + V_2$ where V_1 is the nominal output voltage of the IC and V_2 is the voltage drop across R2.

Now $V_2 = (I_Q + I_1)R_2$ where I_Q is the quiescent current and I_1 is the current through R1.

But $I_1 = \frac{V_1}{R_1}$

Therefore, substituting in the first equation:

$$V_0 = V_1 + (I_Q + \frac{V_1}{R_1})R_2$$

$$= V_1 (1 + \frac{R_2}{R_1}) + I_Q R_2$$

The disadvantage of this method is that the quiescent current of the IC must be known, and it can vary between different specimens of the same IC. For instance the quiescent current of the TBA 625A is quoted as being between 5 mA and 16 mA. There are two approaches to overcome this difficulty. One can measure the quiescent current by inserting a milliammeter in series with the common pin, then calculate the values of R1 and R2. This method is clearly only suitable for 'one-off's'. Alternatively one can calculate the values of R1 and R2 for a typical value of quiescent current, then allow some adjustment with a potentiometer, as in figure 4.

Of course a drawback of either method is that one of the main advantages of the fixed voltage regulator i.e. the known, preset output voltage, is thrown away as soon as any adjustment has to be made. For the best results R1 should be chosen so that the current through it is at least equal to the quiescent current of the IC.

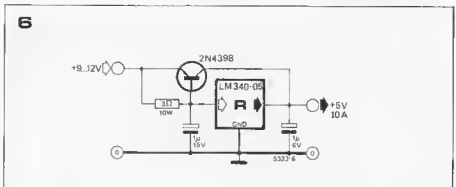
Figure 4. Substitution of a preset for R2 permits adjustment of the output voltage and allows compensation for variations in IC quiescent current. The foldback current limit still operates satisfactorily when using this circuit.

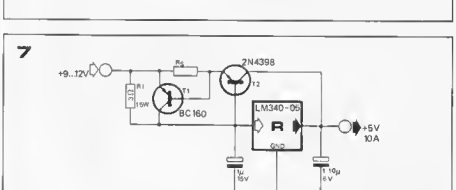
Figure 5. If an op amp connected as a voltage follower is used to increase the output voltage the operation of the circuit is independent of the IC quiescent current.

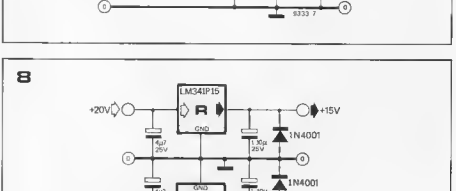
Figure 6. Increasing the output current of a fixed voltage regulator by an external 'current dumping' power transistor.

Figure 7. Current limit protection for the external power transistor.

Figure 8. An example of a dual voltage regulator using fixed positive and negative regulators. The diodes protect the regulators in the event of shorts between the supply lines.







In the circuit of figure 4, for example, a particular specimen of the TBA 625A was used which had a quiescent current of 10 mA. Thus to give 10 mA through R1, R1 is 500 Ω, so 470 Ω was chosen as the nearest preferred value. With P1 set at minimum the output voltage is the nominal 5 V output of the IC. With P1 at maximum resistance 20 mA flows through it so 5 V is dropped across P1. The total output voltage is thus +10 V, so the adjustment range is from +5 to +10 V.

Using this circuit the foldback current limiting is still operative, as the graph in figure 4 shows. The foldback characteristic is shown for normal 5 V operation of the IC (R2 = 0), and for R2 = 200 Ω. It can be seen that at the higher output voltage the current folds back to a slightly lower value. The maximum output current of around 130 mA is unaffected, although 10 mA of this is, of course, lost through R1.

Another method of increasing the output voltage of fixed voltage regulators, which does not require knowledge of the quiescent current of the IC is shown in figure 5. This makes use of an op amp connected as a voltage follower. The output voltage of a follower is, of course, equal to the input voltage, so the voltage at the slider of P1 is the same as the voltage at the ground pin of the regulator. This voltage is 5 V below the output voltage of the regulator, so the voltage at the slider of P1 is also 5 V below the output voltage. With P1 at minimum the output voltage of the op amp is zero, so the stabilised output voltage is simply the nominal output voltage of the regulator. With P1 at maximum 5 V is dropped across R2. The maximum output voltage is thus:

$$V_{max} = \frac{5 \cdot (P_1 + R_2)}{R_2}$$

R1 is included to sink a portion of the quiescent current from the ground pin of the regulator, since the source or sink current of the 741 is 10 mA maximum.

Note that to achieve zero volts at the ground pin of the regulator the op amp must be able to sink the total quiescent current of the regulator IC. This may not always be the case, depending on the quiescent current of the IC used. Hence, in figure 5 the minimum output voltage is shown as 7 V. The maximum input voltage, and hence the maximum output voltage, is limited by the supply voltage which may safely be applied to the op amp, in this case 36 V.

Although the examples given in figures 3, 4 and 5 used 5 V regulator IC's, there is no reason why other types should not be used.

Increased output current

The output current capability of fixed voltage regulators can be increased by the use of external power transistors, though the principle of operation is different from that used with the universal type of regulator. Figure 6 gives an example of how this is achieved. At low output currents the total output current flows through the 3 Ω resistor and through the regulator IC (neglecting quiescent current). When the current reaches about 200 mA the voltage drop across the resistor is about 0.6 V, so the external power transistor

starts to turn on, and a portion of the output current is 'dumped' through it.
The external power transistor in figure 6 has no current limit protection, and a short circuit on the output will almost certainly destroy it. Current limiting can fortunately be included by the addition of a single transistor and current sensing resistor, as shown in figure 7. For an output of 10 A R_S should be chosen as about 0.06 Ω. At this current 0.6 volts will be dropped across R_S, so T1 will start to turn on and short out the base drive to T2, thus limiting the output current.
When designing such circuits using external power transistors it is essential to ensure that the external power transistor starts to turn on at a fairly small proportion of the maximum output current rating of the regulator IC. The reason for this is fairly obvious. If the external transistor does not turn on until the IC is fairly near its maximum output current then it will limit at only a slightly higher output current. As a typical example, the base emitter resistor for the external power transistor might be chosen so that the IC supplied 20% and the power transistor 80% of the total output current.

Dual Voltage Regulators

Dual voltage regulators to provide positive and negative power supplies for such things as op amps can easily be assembled using positive and negative fixed voltage regulators, as in figure 8. This is an example of a power supply suitable for op amps, but other voltages may of course be used, and the positive and negative voltages may be different.
Where the positive and negative supply are supplying the same circuit e.g. an op amp, then the two protection diodes must be included across the output. These will safeguard the supplies in the event of a fault condition such as a positive to negative short circuit. In that case the positive output cannot be pulled more than about 0.6 V negative, nor can the negative supply be pulled more than 0.6 V positive. This prevents the regulators and output capacitors from being damaged by reverse voltages.
Dual power supplies in a single IC are now available, though the output current capability is somewhat less than that of the circuit of figure 8.

Practical Suggestions

When using IC voltage regulators there are a few constructional points that must be noted.

1. All conductors carrying substantial currents (input, output, earth return) must be as thick and as short as possible (this applies to p.c. board tracks).
2. Earth loops must be avoided.
3. All common (ground) connections must be taken to the reservoir capacitor.
4. Input and output decoupling capacitors must be mounted as close as possible to the IC input and output pins.

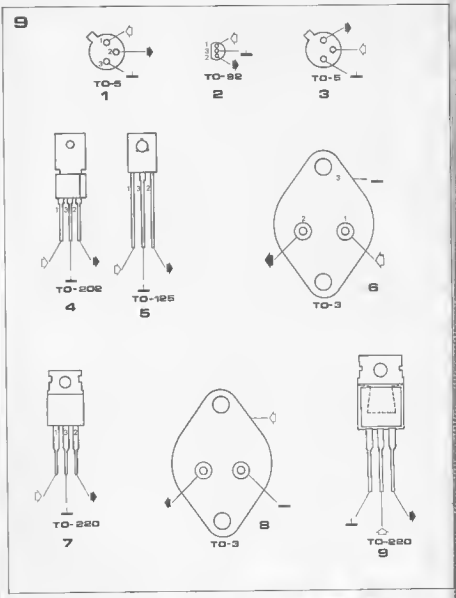
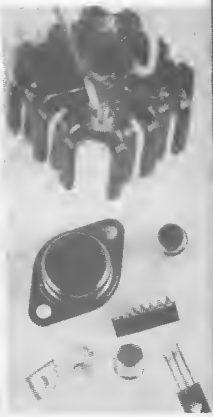
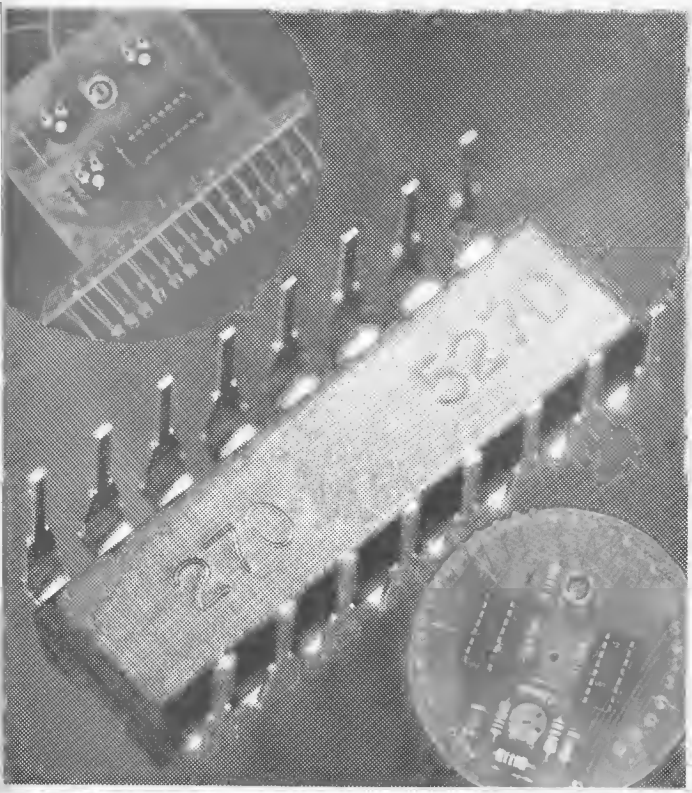


Figure 9. Pinouts of various packages used for IC voltage regulators.



5. Adequate cooling must be provided.

Finally, figure 9 gives pinouts of the more common packages used for IC voltage regulators. Different manufacturers use different pinouts for the same package and tables I and II show the correct pinout for each IC listed. ■



P.C.M. Verhoosel

LED meters

Analogue indicators that make use of columns of LED's to measure voltage or other parameters provide a robust alternative to the conventional moving coil meter in many applications. Using one of the special IC's currently available for this purpose, such as the Siemens UAA 170, such indicators can easily be constructed.

For some time Siemens has been marketing two IC's suitable for driving analogue LED displays. One of these is the UAA 170, a 16-pin IC with 8 encoded outputs capable of driving a column of 16 LED's. Only one of these LED's is lit at any time, which one is lit being dependent on the input voltage in such a way that as the voltage is increased a point of light will move up the column. A companion IC, the UAA 180, provides a 'thermometer' type of indication, i.e. as the input voltage increases, successive LED's light and stay lit, producing a column of light whose length is proportional to the input voltage.

The choice of IC depends on the taste of the individual user, but it must be remembered that the thermometer type of indicator consumes more current than the moving dot type, as more than one LED is lit.

Figure 1 clearly shows the difference between the two types of display.

The possible applications for LED meters are numerous, but they are particularly useful in two types of application. The first is where the response time of the meter must have special characteristics such as audio modulation meters. The attack and decay time can be tailored electrically, and are not dependent on the mechanical inertia of a conventional meter movement. The second is in applications requiring mechanical robustness, such as use in the presence of mechanical vibrations, which could damage moving coil instruments. Here the absence of moving parts gives the LED indicator almost unlimited life.

Of course it might be argued that in some of these applications instruments with a digital readout could be used, since they possess the same advantages of fast response and mechanical robustness, and additionally have greater resolution. However, an additional advantage of the analogue LED indicator lies in its ability to show trends. It is much easier to tell if a rapidly changing quantity is increasing or decreasing when using an analogue indicator than from the blur of figures on a digital display.

Principle of operation

Figure 2 shows a simplified internal circuit of the UAA 170. The input circuitry consists of a series of high-gain differential amplifiers. One input of each of these is commoned and connected to the input terminal via an emitter-follower buffer stage T1. The other input of each differential amplifier is connected to a point in a potential divider chain consisting of equal resistors R, which is fed from a reference voltage applied to T2. The differential amplifiers thus operate as analogue voltage comparators. Whenever the input voltage exceeds the reference voltage on a particular comparator the output of the comparator will change state. The UAA 170 contains 16 such comparators, so the input range from zero to full-scale is divided into 16 steps.

To avoid the necessity for 16 output pins the 16 LED's in the display are not driven individually but are arranged in a 4 x 4 matrix controlled by row and column outputs A to D and E to H. By enabling the appropriate row and column output one LED at a time can be lit. This is controlled by logic circuits represented by the box in the centre of the diagram. The logic circuitry is not shown in detail as it is rather complicated, and anyway it has little bearing

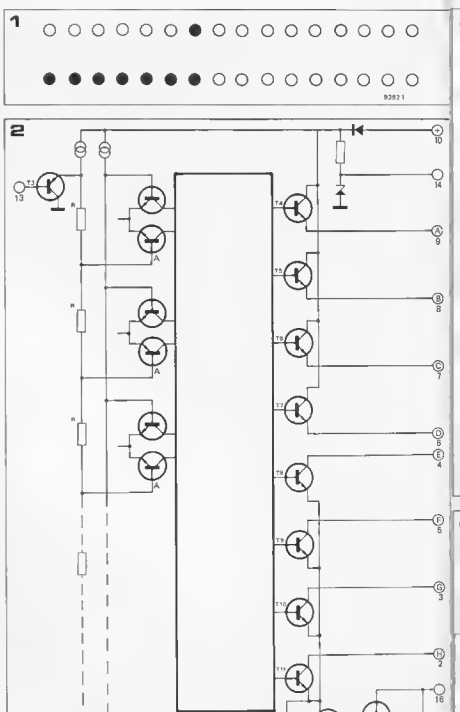
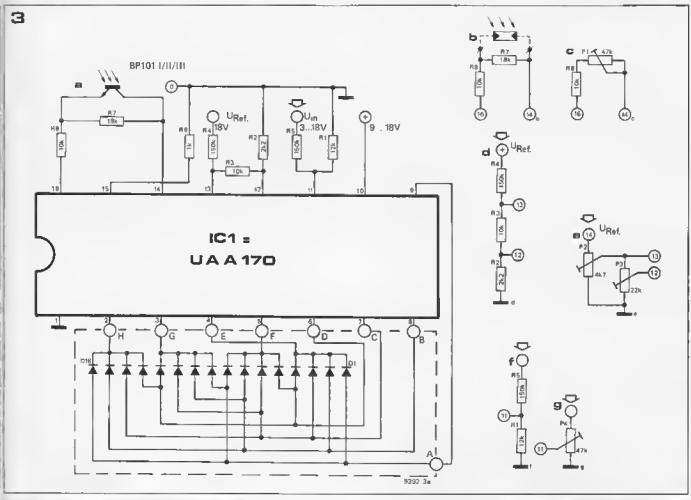
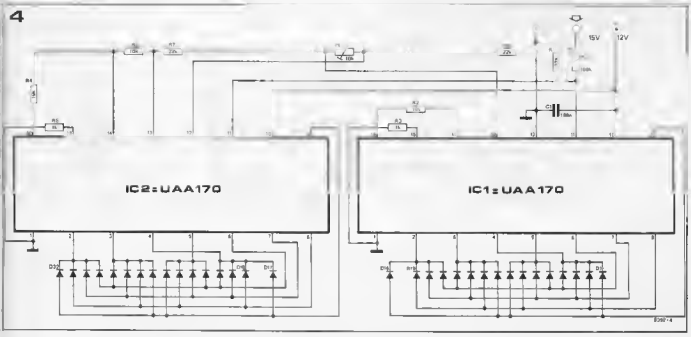


Figure 1. Showing the difference between single point and thermometer type indication.

Figure 2. Simplified internal circuit of the UAA170, showing the input circuitry and output drive circuitry.





on ion the input and output parameters of ion the IC.

th ant

Reference voltage inputs

To establish the input voltage range over which the circuit operates a reference voltage must be applied between pins 12 and 13 of the IC, with pin 13 being the more positive of the two. The input voltage range is set by the voltage difference between these two points. The voltage at pin 13 sets the full-scale reading of the meter. For input voltages in excess of the voltage at this point the last LED in the column will light and stay lit.

The voltage at pin 12 establishes the lowest reading of the meter. While the input voltage is below the voltage at pin 12 the first LED in the column will always be lit, and will not extinguish until the input voltage exceeds the voltage at pin 12, when the second LED will light. This feature is particularly useful in situations where the voltage

Figure 3. Practical circuit of a LED voltmeter using one UAA170 IC.

Figure 4. The scale length can be extended to 30 LED's using two IC's each covering a different portion of the input voltage range. D16 and D17 must be included in the circuit, although they can not be used as part of the scale.

to be measured is above a particular value, and voltages below that value are of no interest. A typical example is a 'suppressed zero' voltmeter for use in cars. Here only voltages between about 11 and 18 volts are of interest, since the battery voltage normally never falls below 11 V, and the generator cuts out above about 17 V. If voltages below 11 V were included on the voltmeter scale then more than half the scale would never be used. This can be avoided by making the UAA 170 operate from 11 to 18 volts. Below 11 volts the first LED would remain alight, which could be used as a low battery voltage indication.

Different reference voltages produce unusual effects on the display. With reference voltages above 4 V the changeover from one LED to another is instantaneous, i.e. as one LED extinguishes the next one lights up to maximum brightness immediately. As the reference voltage is reduced the changeover becomes more gradual, and with a reference voltage of about 1.2 V it is possible to have two LED's alight simultaneously at reduced brightness. The emitter followers T1-T3 provide a high input impedance, input current being of the order of 2 µA, so for many applications the UAA 170 and 180 can be connected direct to the voltage to be measured without any intermediate buffering.

For use in situations where a stable reference voltage is not available, the IC is provided with a reference voltage output (pin 14). A 5 V reference is available at this point, with an output current capability of up to 3 mA. If voltages in excess of 6 V are to be measured then an input attenuator must be used to scale down the input voltage at pin 11.

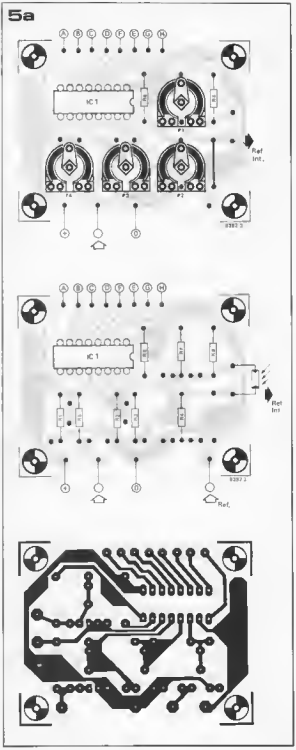
Brightness Control

The output current delivered to the LED display, and hence the brightness, can be altered by a brightness control connected between pins 14 and 16 of the IC. This may take the form of an LDR or phototransistor to adjust the display brightness to suit ambient lighting conditions, or it may be a manual control such as a potentiometer. A fixed resistor between pin 15 and ground adjusts the control characteristics of the brightness control.

Practical Applications

The complete circuit of a LED voltmeter is given in figure 3. This has phototransistor brightness control and, with the component values shown is intended for an input voltage range of 3 - 18 V.

Various alternative possibilities are shown accompanying the main figure. b) and c) show brightness control using LDR and manual brightness control with a potentiometer respectively. d) and e) show a fixed voltage divider for the reference voltage and an adjustable one using presets respectively. f) shows a fixed input attenuator, while g) shows a preset input attenuator.



For correct operation of the display all four LED's connected to one of the pins 2, 3, 4 or 5 should have the same electrical characteristics.

If the UAA 180 with its thermometer-type scale is used then the LED's should also be chosen for similar brightness, as otherwise the appearance of the display will be degraded.

Extension to 30 LED's

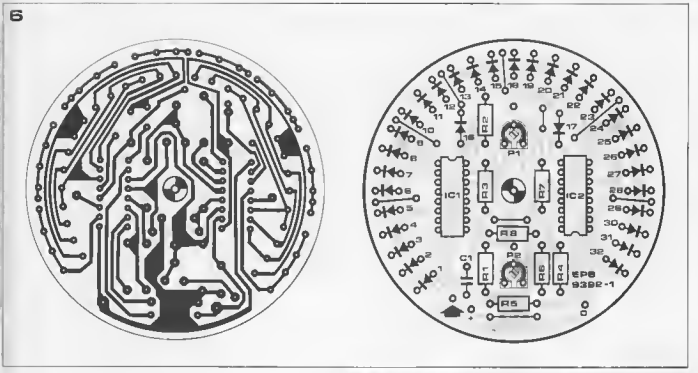
For applications requiring greater resolution than can be provided by 16 LED's the circuit may be extended using two IC's as shown in figure 4. Both IC's receive the same input voltage at pin 11, but the reference voltages are arranged so that the first IC operates over the input voltage range of say 0 - V/2, and

Figure 5a. Board layout for figure 3, with provision for automatic or manual brightness control and fixed or variable input and reference voltage attenuators (EPS 9392-3).

Figure 5b. p.c. board layout for LED display of figure 3 (EPS 9392-4).

Figure 6. p.c. board and component layout for a '270° meter' suitable for use with a reversible counter circuit (EPS 9392-1).

Note that the UAA170 and the UAA180 are not pin-compatible! The circuits and p.c.boards given here are only suitable for the UAA170.



Parts list for figure 3.

Resistors, figure 3a:
R1 = 12k
R2 = 2k2
R3,R8 = 10k
R4,R5 = 150k
R6 = 1k
R7 = 18k

Resistors, figures 3c, 3e, 3g:
R6 = 1k
R8 = 10k
P1,P4 = 47k preset
P2 = 4k7 preset
P3 = 22k preset

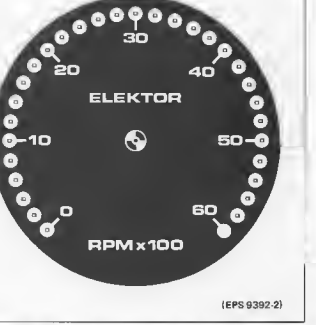
Semiconductors:
IC1 = UAA170
D1 . . . D16 = LED
Phototransistor (e.g. BP101) or LDR

Parts list for figure 4.

Resistors:
R1 = 22k
R2,R4,R6 = 10k
R3,R5 = 1k
R7,R8 = 22k
P1 = 10k preset
P2 = 100k preset

Capacitors
C1 = 100n

Semiconductors:
IC1,IC2 = UAA170
D1 . . . D32 = LED



the second IC over the range V/2 - V, where V is the full-scale input voltage.

It is necessary to omit the last LED from the display of the first IC and the first LED from the display of the second IC, otherwise for voltages below V/2 the first LED of the second IC would always be lit, and for voltages above V/2 the last LED of the first IC would always be lit. For this reason only 30 LED's may be used, not 32. This means that D16 and D17 should not be part of the scale, although they must be included in the circuit.

So that the omission of these two LED's does not cause a 'blind spot' in the middle of the display it is necessary to arrange that the second LED of the second IC lights as the 15th LED of the first IC extinguishes. This is accomplished by having the reference voltage on pin 12 of the second IC lower than the voltage on pin 13 of the first IC.

The voltage difference between these two points can be adjusted by P1. P1 should be adjusted so that D18 begins to light as D15 extinguishes. There should be no blind-spot where both LED's are extinguished, nor should two or more LED's be fully lit at the same time.

Practical construction

The construction employed depends upon the intended application of the LED meter. Two board layouts are given here, a linear scale suitable for use as an FM tuning scale (see Elektor 9 page 134) and a scale in a 270° arc, intended specifically for use as part of a car rev counter. *(Note that this circuit is not a complete rev counter! It is merely a replacement for the original analogue pointer instrument – Ed).*

The printed circuit boards and component layouts for the linear scale meter are given in figures 5a and 5b. The IC and its associated passive components are mounted on a separate board from the LED display. The output terminals of this board match up with the input terminals on the display board, so the display board may be mounted on the main board at right angles to it, or the two may be linked by ribbon cable.

Provision is made on the main board

for either LDR or manual brightness control (P1) fixed or adjustable reference voltage (R2, R3, R4 or P2, P3) and fixed or adjustable input attenuator (R1, R5 or P4).

The board layout of the rev counter scale is given in figure 6. This is provided only with adjustable reference voltage at pin 13 by means of P1. Reference voltage at pin 12 is zero. Input attenuation is adjustable by means of P2, and display brightness is fixed by R2 and R4.

Assembly

The scale of the instrument will probably consist of a faceplate marked with the actual scale values and pierced with holes through which the LED's can protrude. An example is given accompanying figure 6. To ensure proper alignment of the LED's with the holes in the faceplate the LED's should first be mounted on the p.c. board and secured by soldering one lead only, ensuring that all LED's are the same height above the board. The faceplate can then be placed over the LED's and having positioned each LED in its hole the second lead of each LED can be soldered.

Practical hints

The principle electrical parameters of the UAA 170 are given in table 1. It will be seen that the voltage on the signal and reference inputs, pins 11, 12 and 13, must never exceed 6 V. When measuring input voltages greater than 6 V an input attenuator must therefore be used, as in figures 3f and 3g. This may take the form of a fixed attenuator or a preset potentiometer. The same applies to the reference voltage inputs. It is evident that the input voltage to pin 11 at full-scale reading must be the same as the reference voltage at pin 13, thus:

$$V_{ref.} \cdot \frac{R_2 + R_3}{R_2 + R_3 + R_4} =$$

$$= V_{in\ max} \frac{R_1}{R_1 + R_5}$$

If V_{ref} and the maximum input voltage are known then the ratios of the resistors can easily be calculated. If V_{ref} can be the same as V_{max} then the resistors can be chosen such that R4 = R5 and R2 + R3 = R1. The ratio of R2:R3 is chosen such that the voltage at pin 12 is equal to the minimum input voltage at pin 11, so:

$$V_{ref} \cdot \frac{R_2}{R_2 + R_3 + R_4} =$$

$$= V_{in\ min} \cdot \frac{R_1}{R_1 + R_5}$$

but with R4 = R5 and R1 = R2 + R3 then

$$V_{ref} \cdot R_2 = V_{in\ min} \cdot R_1$$

therefore

$$R_2 = \frac{R_1\ V_{in\ min}}{V_{ref}}$$

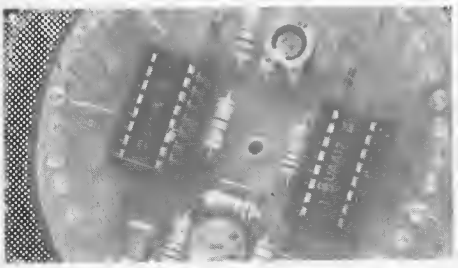
When choosing the actual resistor values the input current of the IC should be taken into account. If the total resistance is chosen so that the current through the potential divider chain is about 100 µA then the 2 µA input current of the IC can be neglected.

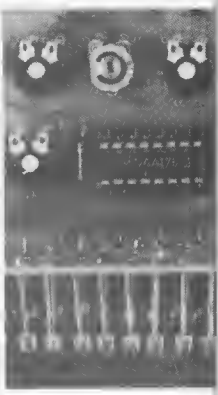
As mentioned earlier the current through the LED's, and hence the brightness, is controlled by what is connected between pins 14 and 16, and between pin 15 and ground. For example, with R6 in figure 3a chosen as 1 k, the with a resistance of 10 k between pins 14 and 16 the current through the display will be 50 mA. This corresponds to the phototransistor or LDR being fully illuminated and having minimum resistance. If the resistance between pins 14 and 16 is increased to 40 k then the display current falls to zero. The 18 k resistor across the phototransistor ensures that this can never occur in practice, even in total darkness, as the resistance is still only 28 k total.

Table 1

	absolute maximum	typical
Supply voltage	+ 18 V	–
Input voltage at pins 11, 12 and 13	+ 6 V	–
Output voltage pin 14	–	5 V
Output current pin 14	3 mA	–
Current consumption without LEDs	–	4 mA
LED drive current	50 mA	–
Input current at pins 11, 12 and 13	–	1·2 µA
Reference voltage between pins 12 and 13 for gradual display transition	–	1.2 V
Reference voltage between pins 12 and 13 for abrupt display transition	–	4 V

Table 1. Principle electrical specifications of the UAA170.





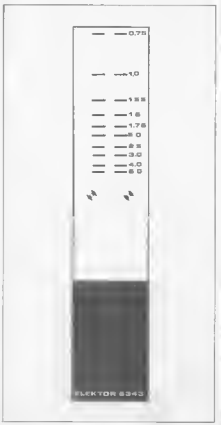
Stylus balance

Correct setting of stylus tracking force is of utmost importance – certainly for modern 'feather-weight' cartridges. The gauge that is built in to many modern record players is not always reliable, so a double-check by means of a separate balance is often advisable.

The 'ideal' tracking force for most modern cartridges is somewhere in the 0.75 . . . 3 gram range. Some ceramic or crystal cartridges do require a higher setting, but they are intended primarily for record players without any tracking force adjustment in the first place. On the other hand, some very high compliance cartridges can be used at a tracking force of less than 0.75 g, but this is usually only a nuisance: the slightest vibration of the record player or the smallest speck of dust can cause the needle to become airborne.
Most manufacturers specify the minimum and maximum permissable tracking force for their cartridges. In practice, the best value usually proves to be just under the specified maximum. It is perhaps worthy of note that the danger of damage to the record is greater if the tracking force is too low than if it is too high – within moderation, of course! As a rule of thumb, the maximum for dynamic cartridges with an elliptical stylus is about 1.5 g, whereas the maximum with a spherical stylus will be about 3 g. From the above it will be obvious that a useful measuring range for a stylus balance would be 0.75 . . . 4 grams.

The p.s.b.

The simplest type of measuring instrument for tracking force is a balance – and it can also be one of the most accurate types
An easy way of making such a balance is to use epoxy printed circuit board material. Computer aided design has resulted in the end product shown in figure 1: the printed stylus balance or p.s.b.
Round-headed furniture tacks, rivets or the like can be used as pivots. These are pushed through the holes until the heads lie flush against the back of the board. Due care should be taken at this stage: the calibration accuracy depends on the position of the pivots, and any sharp edges (such as deep scratches) can affect the freedom of movement.
The calibration depends on the mass per unit area of the material, of course; the scale shown is accurate for the boards supplied by the Elektor p.c. board service (EPS 9343).



How to use it

The balance is placed on the turntable so that it pivots on the round heads of the tacks (see photo). The stylus is now gently lowered onto the balance, and by sliding it up or down along the open track between the calibration marks (rotate the turntable a fraction) the position can be found where the whole set-up is in equilibrium. The tracking force can now be read off.
For the highest degree of accuracy it is advisable to set the anti-skating compensation at '0', and to level the record-player. The latter is always a good idea, anyway, in the interest of minimum wow.

EQUIN

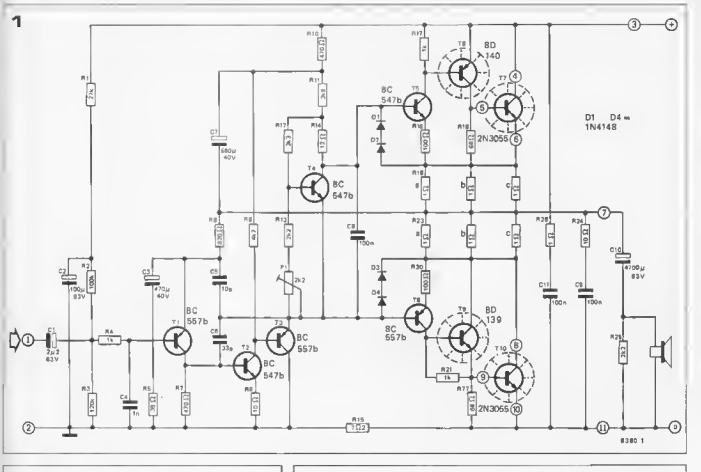
Of the many amplifier designs published in Elektor, the best known are perhaps the Equa and the Edwin.
The Edwin amplifier enjoys great popularity because of its simplicity and the certainty that it will work first time. Anybody who can hold a soldering iron steady can build a satisfactory Edwin.
The Equa amplifier is a more sophisticated design, more 'critical' if you like. It requires more care and a degree of insight from those who would build it. The final result is however a power amplifier of exceedingly high quality.
The obvious following design target was a power amplifier that would perform as well as the Equa — but was as uncritical to build as the Edwin.
The first part of this two-part article presents the theoretical background to the Equin amplifier, the second part will cover the practical aspects.

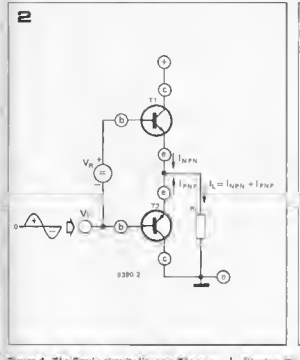
part 1

Any good amplifier should reproduce music, be it Beethoven or Bacherach, as it was recorded — without adding any of its 'own interpretations'.
This means that the designer must pay attention not only to the readily audible 'crossover' distortion, but also to the 'impulse response' (i.e. the stability) and to the related problem of 'transient intermodulation' (TIM).
The design must minimise the total audible effect of all these distortions at once. It is not too difficult to 'clobber' crossover distortion with a combination of suitable quiescent current and heavy negative feedback (60 dB or so). Such a degree of feedback can only be achieved without instability, however, by such an early 'open-loop rolloff' that serious TIM cannot be avoided.
This is the great objection to using internally 'compensated' op-amps, such as the 741!
On the other hand, an RMS total distortion of 0.1% is quite inaudible — provided only that it consists of low-order harmonics, without any trace of 'crossover spikes'. (Why do valve amplifiers sound so clean?)
The attempt to achieve optimal sound quality does not have to mean the use of large numbers of components. A handful of 'strategically' placed 'extra' parts in an otherwise standard design will often do the job better (and cheaper) than a radically new circuit. The standard design can indeed often already be improved by slight readjustment of component values, after one has taken a hard look at 'what affects the musical quality'.
Note that this design is not intended for people addicted to head-splitting SPL's. Massive amounts of distortion will not be unacceptable in such applications. This is an amplifier for clean reproduction at subjectively-realistic levels, in a domestic listening room.

Output stage

In a class B output stage there are two separate transistor-groups that deliver current in turn, depending on the instantaneous polarity of the drive signal.
Figure 2 shows the most usual stage configuration in simplified form. The NPN transistor T1 has its base linked, via a source of direct 'bias' voltage V_R, to the base of PNP device T2. In any practical amplifier T1 and T2 will each consists of two or three individual transistors, arranged to give high-performance NPN and PNP overall behaviour. When V_R is made zero, in other words when T1 and T2 have no 'quiescent' or 'standing' current, it can be seen from figure 3 that the load-current will be zero throughout a range of drive-voltages on each side of the actual axis-crossing. This 'dead zone' is the cause of crossover distortion.
The culprits are the NPN and PNP devices themselves, or rather their collector-current/base-emitter-voltage characteristics. At high current levels these curves can be made as linear as one would wish, by using current-dependent negative feedback obtained with emitter-resistors. At low current levels however these characteristics are sharply curved. The reason is that the 'transconductance' of T1 and T2 collapses at low current levels, so that no amount of feedback will help significantly.





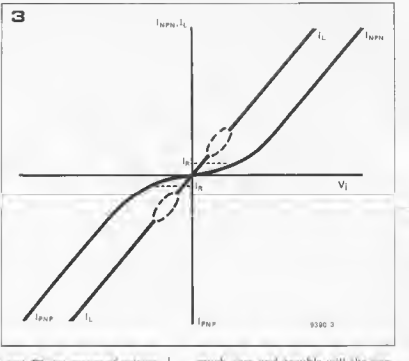


Figure 1. The Equin circuit diagram. The p.c. board layout and the supply arrangements will follow in part 2.

Figure 2. The principle of 'usual' class B output stages. T1 and T2 are 'compound' NPN and PNP transistors, built up as pairs or triples (or as single transistors).

Figure 3. The characteristics of the figure 2 circuit. The 'quiescent' current I_R serves to 'linearise' the crossover-region.

Biasing T1 and T2, by means of voltage V_R, will greatly improve matters. At the axis-crossing of the drive signal there will now be a steady current (the 'quiescent' current) in both devices – so that they both still have significant transconductance. In the ideal case the overlap of the NPN and PNP characteristics will be so arranged that the load-current follows the drive voltage linearly through the zero-axis-crossing (the 'crossover'). The extent to which this can be achieved depends on several points:

– Assuming that the ideal value of quiescent current does exist, how much care and trouble will the constructor take to set it?
– The ideal value is in fact that for which the ultimate 'slope' of the NPN curve lies in the same line as the PNP ultimate slope; the slope of each stage-half at crossover is then half the ultimate value. Irregularities in the curved part of the characteristics can prevent this state of affairs being maintained right through the crossover region.
– Complete regularity means that the curves should be each other's mirror image. This is the meaning of the

term 'complementary symmetry'. If a certain device within 'T1' is NPN, then the corresponding device inside 'T2' should be PNP, vice versa.
Thus would imply that the power devices within T1 and T2 also must be complementary types. This is where the rot sets in: not only are high-power complementary pairs difficult (i.e. very expensive) to produce – it is almost impossible to produce such a pair with really complementary high-frequency (switching) performance.
The usual approach is therefore to apply 'quasi-complementary' arrangements, where the two power devices have the same polarity (NPN). This will work *provided* precautions are taken to eliminate the inevitable asymmetry in the near-crossover parts of the overall transfer characteristic. This can be done well.

– The next point is that the value of the quiescent current may not drift with temperature. If the base-emitter junction of a steamed-up power device gets its oar between the 'base' and 'emitter' of T1 or T2, it will be necessary to regulate V_R by about -2 mV/°C, to hold the quiescent current steady. That can be quite a party: NTC resistors, sensing-diodes on the heat sink – plus the guesswork about the actual junction temperature, when all one has to go by is the (considerably lower) heat-sink temperature.

Assuming that such a compensation could be made dependable – would it be fast enough? Would the heating due to a loud passage of music not cause the immediately following quiet passage to be beset by cross-over distortion, due to the power device junction cooling off faster than the heat sink from which its temperature was being estimated?
To be short: no alteration of quiescent-current-setting V_R should be required to compensate for hot power-device junctions.

– When the power supply is unregulated one must furthermore take care that V_R does not depend to any extent on the instantaneous DC voltage on the power line. In the circuit of figure 1 the bias-voltage V_R (of figure 2) is obtained by means of the components T4, P1, R12, R13 and R14. Variations in supply voltage cause a varying drop across R14 that can be made to compensate for the error in the base-emitter voltage of T4 due to those same supply variations. The bias voltage is therefore held relatively constant.

Output stage circuits

Figure 4 shows several possible combinations of devices for making up T1 and T2 of figure 2. These two-transistor groups (driver plus power-transistor) are to be found in very many designs. The resistor R is typically 50 . . . 100 ohm; R_E is usually 0.2 . . . 0.5 ohm. The pairs a, b, c (identical to a) and g show NPN behaviour; d, e, f and h behave as PNP. The combinations a-d, b-e and g-h show true 'complementary symmetry'.
The combination a-e is the well-known 'quasicomplementary' output stage. Adding a diode and a resistor (as originally suggested by Baxandall) converts 'e' into 'f'; the asymmetry of a-f can be very small indeed, since the diode simulates the 'missing' base-emitter junction.
The 'darlingtons' a, c, g, d, f and h(=f) have an $I_E - V_{BE}$ characteristic with a long 'tail'. The stability of the quiescent current is relatively poor, but the input impedance (base to emitter) near cross-over varies smoothly.
The 'tail' in the characteristics of the 'compound' pairs b and e is short. These pairs have a good stability of quiescent current, but the input impedance shows discontinuities in the crossover region. Adding 'Baxandall diodes' to both b and e will give them darlington-like characteristics, but it will eliminate the 'hot' junction – giving improved quiescent current stability together with the smooth impedance-curve. See g and h in figure 4. This arrangement was used in the Equa-amplifier.
The objection to the figure 4 pairs is that they all have a fairly low current gain. This means that they require considerable amounts of drive-current. The obvious solution is to build up 'T1' and 'T2' as triples. Of the various possible configurations the so-called 'Quad-

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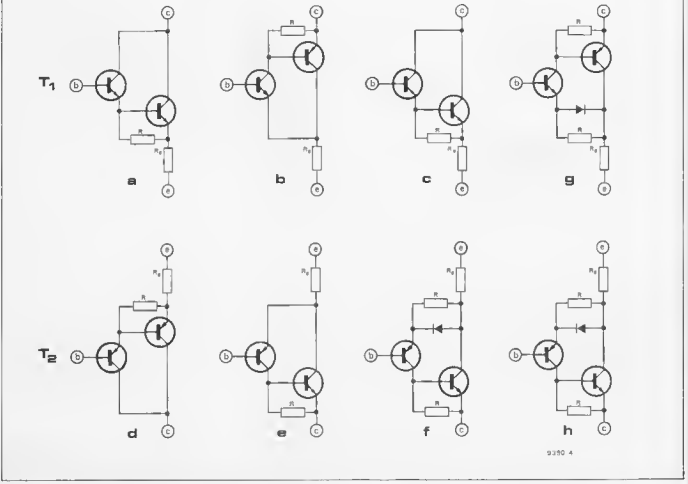


Figure 4. Well-known two-transistor configuration for T1 and T2. The vertical pairs (e with d, b with e, etc) can be combined to form an output stage with more-or-less complementery symmetry.

Figure 5. The 'Quad-triples' used for T1 and T2 in the 303 amptifier.

Figure 6. Modified triples used in the Equin amptifier.

Figure 7. 'Bootstrap-drive' to the output stage. The penultimate stage (T2 in figure 1) is shown as a current-source.

Figure 8. Equivalent of figure 7 when R1 and R2 are much greater then R_L and the impedances of C1 and C2 are negligibly small.

triples' are the best known (see figure 5). The quiescent current stability of the Quad triples is extremely good; the 2N3055's cannot get their oars into that part of the circuit! The I_E – V_{BE} characteristics have a short tail and the current gain is high. The misbehaviour of the input impedances near crossover is smoothed by the 100-ohm resistors.

The symmetry of the complete Quad output stage is however not quite what it could be. The voltage drop across the 1 kΩ resistor in the NPN triple is unequal to (in fact about half) that occurring in the PNP triple. This means unequal currents in the pre-drivers' – and mismatched 'crossover tails'.

This asymmetry has been practically eliminated in the Equin circuit by the figure 6 expedient of moving one resistor 'end'. The voltages across R17 and R21 are now equal, so that T5 and T8 are symmetrically biassed.

The optimal value of quiescent current for this output stage is low, so that it has interesting possibilities for very-high-power designs ('horsepower amplifiers'). (Quad themselves have meantime come up with a quite different approach to high-power design, see Quadi-complimentary'; Elektor 8, p. 1220).

Driving the output stage

The discussion up to now has implied that the output stage would be voltage-driven (i.e. from a zero source impedance). The alternative is current-drive.

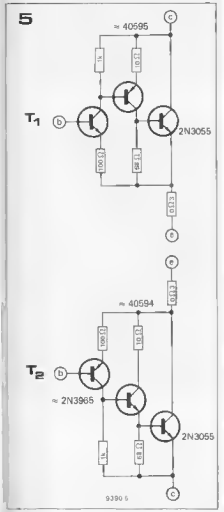
With voltage-drive the output current is related to the drive voltage by the 'slope' (transconductance) of the I_E – V_{BE} characteristic (figure 3). With current drive I_L is related to the drive current by the current gain of the compound transistors T1 and T2. However, the current gain is frequency-dependent to a greater extent than the slope, mainly because the latter can be improved by local feedback.

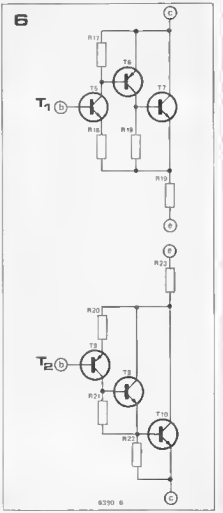
Current drive could in principle be equally successful – if there was a convenient way of applying suitable local feedback. It would however be hard to beat the convenience of the 'voltage-drive feedback' obtained with the emitter resistors of figures 4, 5 or 6.

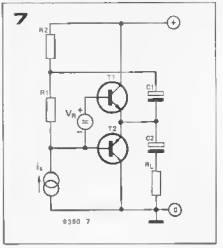
Another aspect is that a voltage-driven stage does not require (at least in principle) the use of current-gain-matched pairs. (A wild mismatch will not of course be any help. ..)

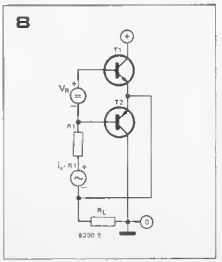
In most practical designs the drive is neither purely 'voltage' nor purely 'current'. Look at the circuit of figure 7. If C1 and C2 are sufficiently 'thickended' there is a link between the junction R1-R2, the emitters of T1 and T2, and R_L. The voltage across R1 is the output stage drive. The lower end of R1 carries the drive voltage plus the output voltage. It is driven from the collector of the last 'front-end' transistor, which, on its own, is a current-source.

P.J. Baxandall has shown (letter 'Sym-





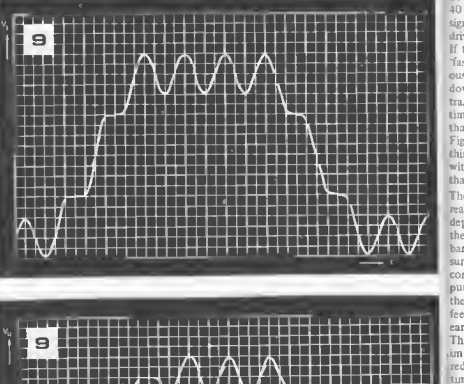


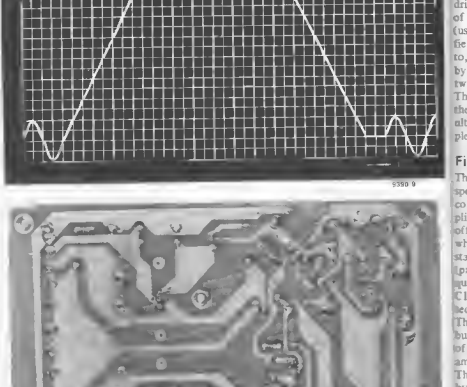


metry of a class B', Wireless World, September 1969, p. 416 etc.) that the figure 7 circuit is directly equivalent to that of figure 8, provided that R1 has a much higher value than R2; a calculation of the output voltage as function of the current i_S leads in each case to the same formula. Conclusion: the output stage is driven from a source-impedance R1 and operates in the common-emitter mode. It therefore does not behave as an emitter-follower, as some people would have one believe.
The gain obtained depends on the ratio of R1 to the input-impedance of the output stage. This impedance, as already noted, can show crossover effects. It is also frequency-dependent.
Crossover misbehaviour can therefore occur by two mechanisms: during the conversion of the current from the penultimate stage into drive voltage for the output stage, and in the conversion of this drive voltage into the output current I_L. Reduction in value of R1 will reduce the influence of the first mechanism. It will unfortunately also reduce the open-loop gain.
In the Equin amplifier, bootstrapping has been applied just as in figure 7. The figure 7 circuit reappears in the figure 1 circuit diagram as T2 (penultimate stage; current source i_S), R9, R10, C7 and C10. The difference is that the junction of T2 collector with R9 (R1 in figure 7) is connected indirectly to the base circuit of T5 and T8, via emitter-follower T3. T3 (with emitter load R11) presents a very low source impedance to the output stage – giving near-ideal voltage-drive conditions – simultaneously preventing the output stage from loading R1 (mechanism 1). The open-loop bandwidth is also improved by this tactic; T3 also provides the current required for the 'Miller' capacitor (C6 in this case) that has to be inserted to maintain stability under negative feedback. That capacitor would otherwise shunt the current source T2, causing extra phase-shift just where it can least be tolerated, in the middle of the 'danger area'.

Transient intermodulation distortion

Along with 'crossover', 'TIM' can be blamed for the 'gravelly' quality of sound from many transistorised power amplifiers. TIM actually 'sounds' very much like crossover distortion; it occurs however at moderate to high drive levels and high frequencies instead of on low-level signals.
The effect is caused by the application of an input signal that 'slews' too fast for the feedback system to 'keep up with'.
The drive voltage to the input stage is the difference between the input signal and the feedback signal from the output. Due to the high open-loop gain, this difference is usually very small. However, if the feedback is too slow (due to lag compensation needed to stabilise heavy feedback, for example), this difference signal may be momentarily vastly greater than normal – and it may overdrive the input stage. The saturation or cutoff that results may cause DC shifts that take time to correct themselves. The bursts of 100% distortion, 'holes in the music', are the TIM.
A numerical example: suppose the amplifier has an open-loop gain of





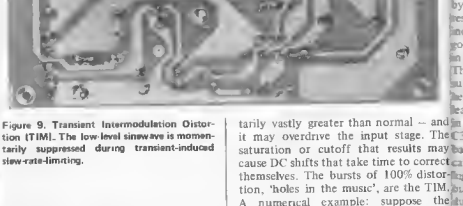


Figure 9. Transient Intermodulation Distortion (TIM). The low-level sinewave is momentarily suppressed during transient-induced slew-rate-limiting.

40 dB (10,000 ×) and is operated with 40 dB (100 ×) feedback. A 'slow' input signal of 100 mV will cause a resultant drive to the first stage of about 1 mV. If the feedback arrives too late, due to a 'faster' 100 mV input, there will obviously be big trouble. The amphfier is down for the count during the actual transient overload and the 'recovery time'. Any other signal present during that interval will not come through. Figure 9 illustrates this. It is precisely this kind of signal, a continuous line with an odd superimposed transient, that is so typical of music.

The speed with which the feedback can react to a fast disturbance at the input depends on the open-loop risetime of the amplifier, i.e. on the open-loop bandwidth. This in turn depends, assuming that the amplifier is to be unconditionally stable, mainly on the output stage gain-bandwidth-product and the amount of feedback used. More feedback and slower devices make for earlier trouble.

The TIM performance of an amplifier improves as the open-loop risetime is reduced to approach the shortest risetime occuring in the input signal. The Equin amphfier, with its good voltage drive, manages an open-loop bandwidth of 10 kHz without stability problems (using 'slow' 2N3055's!). If the amplifier is to handle full-drive inputs at up to, say, 20 kHz (and not be embarrassed by inadvertent ultrasonic drive) one or two extra precautions are desirable. These are to provide an RC rolloff at the input (R4/C4 – well into the ultrasonic range), and to give T1 plenty of elbow-room (low R7).

Final remarks

The output stage drives the loudspeaker via the electrolytic C10. Direct coupling would have introduced a complication with the offset voltage. This offset is critical to really control, whereas DC in the load can upset the stage-balance, leading to 'crossover' (particularly with this circuit's low quiescent current). R25 ensures that C10 is charged when no load is connected.

The diodes D1 . . . D4 form a simple but effective current limiter. Beware of the dissipation when the driven amplifier is 'shorted'.

The positive supply rail is decoupled by R26/C11. The resistor damps the resonance between C11 and the wiring inductance – to prevent the amplifier going into business for itself somewhere in Band I.

The resistor R15 separates the negative supply rail from the input 'earth', the heavy currents taking the 'path of least resistance'. The two signal-earths in a stereo amplifier may be linked.

C3 and C7 cause the degree of AC feedback to differ from the DC value. These capacitors have been given an unusually high value, so that the amplifier DC biasing arrangements will not wander due to momentary asymmetry in low-frequency input signals. ⋈

tv tennis extensions

In the previous article (Elektor 11, p. 318) some extensions of the basic game were described. It was the intention to publish further extensions in this issue – with one printed circuit board for all the additional circuits. However, some readers seem to be having problems with the basic game, so some further suggestions for trouble-shooting seem called for. In the next issue we will publish the remaining extensions and the printed circuit board.

part 2

The additional circuits will extend the scope of the original TV tennis game, but they will also put a heavier load on the power supply. This may mean that a new power supply will be required, or that the existing unit will have to be redesigned. The current consumption, with all extensions added, will be approximately 600 mA.

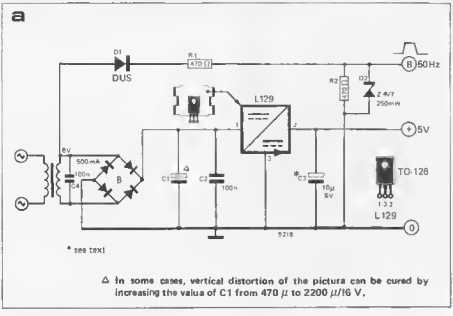
The power supply originally recommended, using the L129, should be adequate (figure A). An alternative solution is the LM309K: this is capable of supplying up to 1 A at 5 V.

It has been found that some fixed voltage stabilisers actually supply approximately 4.8 volts. The consequence may be that practically the entire field remains white. The circuit of figure B shows how this can be remedied by raising the voltage.

Some readers have encountered problems involving vertical distortion of the picture. This can be caused by poorly adjusted horizontal synchronisation, so a word of advice will not be out of place: first of all read the adjustment instructions given in the original article. Carefully check all wiring and other connections, then set all pre-set potentiometers to mid position and carry out the alignment procedure as described. If the problem persists, the modifications described at the end of the article 'TV tennis extensions, part 1' can be carried out ('TV tennis hints'). Readers are also referred to the points already mentioned in the 'Missing Link', January 1976, p. 148.

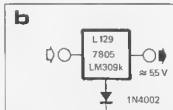
If even these points are not sufficient to completely cure the problem, some further 'brute force' expedients are required:

– the three ICs in the synchronisation circuits (IC7, IC8 and IC10) are sensitive to interference pulses on the positive supply rail. For this reason it is advisable to run completely separate wires from the supply electrolytic (in the power supply shown in the original article, this is C3) to each of these ICs. The simplest way to do this is to unsolder the positive supply pins (pin 14, in each case), bend the pins up from the board and solder the wires on to them in mid-air. The positive supply ends of the decoupling capacitors (C8, Cx and Cx) are also unsoldered from the board and connected via 1 Ω resistors to pin 14 of the corresponding ICs. (Note that IC10 is the one between IC7 and IC8; on the original board

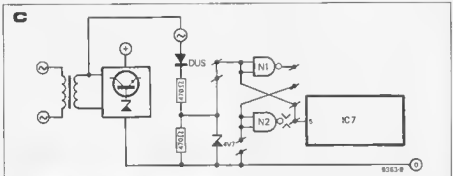


△ In some cases, vertical distortion of the pictura can be cured by increasing the valua of C1 from 470 μ to 2200 μ/16 V.

layout shown in Elektor 7, p. 1117, the indications IC10 and IC11 were interchanged.)
the negative supply to IC10 (pin 7) could also do with some additional decoupling. A 100 µH micro-choke in series with this connection is sufficient. The easiest way to mount this is to unsolder all seven pins on that side of the IC and bend it up so that these pins are in mid-air (pins 1 to 6 are no longer used after the mains sync has been incorporated). The choke is then mounted between the original hole for pin 7 and pin 7 itself.
after the conversion to mains sync has been carried out (Elektor 11, p. 323), there is a wire link in the connection between pins 1 and 2 of IC10 and pin 5 of IC7 (figures C and D). If a 2.2 mH choke is used in place of this link, some further improvement of picture quality can result.



— in some cases, the ball signals interfere with the other signals — causing a dent in the vertical boundaries that moves up and down with the ball, for instance. To prevent this, two 1 kΩ resistors can be added in series with the inputs of N9 (pins 2 and 3 of IC12). On the board, these resistors can be mounted in place of the original wire links between pin 2 of IC12 and pin 1 of IC2 and between pin 3 of IC12 and pin 1 of IC1 respectively. ◀



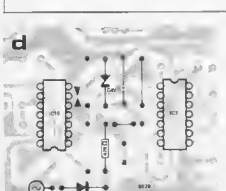


Figure A. The mains powar supply originally suggested, using a fixed voltage regulator.

Figure B. If the regulated output voltage is too low, a dioda in the 'tail' of the regulator will ramedy matters.

Figure C. Circuit for deriving the frama sync pulses from the mains frequency (see Elektor 11, p. 323).

Figure D. Detail of the main p.c. board, after the mains sync modification has been carried out.

THE MIS SING LINK

Modifications to
Additions to
Improvements on
Corrections in
Circuits published in Elektor

Preamp for countar

In the preamp for the frequency counter (Elektor 8, p. 1235) a 47 Ω preset potentiometer is specified for P1. If this is not readily obtainable, a 100 Ω preset can be used instead.

Digital master oscillator

In the circuit for the MOS master oscillator (Elektor 10, p. 246, figure 11) and in the corresponding component layout (figure 15) one output is marked 'F'. Some readers have wondered what this is for . . .
This connection is simply a low-impedance output that can be used when trimming up the oscillator: a TTL frequency counter can be connected to it. The oscillator should be tuned so that the output at 'F' is 1000120 Hz — the actual oscillator frequency is then 2000240 Hz, of course.

Lie dalactor

There is an error in the circuit diagram for the lie detector (Elektor 7, p. 1143). Of the two diodes at the input, the upper is drawn correctly but the lower is the wrong way round. Its cathode should be connected to the 47 k/47 k/ 100 k-preset junction; its anode should be connected to supply common.

what's watt?

The most 'interesting' figures on the specification list of an audio power amplifier are those relating to the rated output power. This article reviews the various kinds of watt that one can meet in a specification. Since the purpose of using the amplifier is to reproduce music at a 'correct' level, it will also be necessary to consider the efficiency of the loudspeakers that are to be driven.

It is rather too easy to manipulate with the 'watts' in the power-amplifier specification to produce an inflated rating. The idea is to sell a relatively low-power job to the unwary – at a high-power price – on the premise that all the fellow wants is a higher watt-rating than the chap next door. This technique has been developed to such a fine art that there are even protests from within the industry – from responsible manufacturers and their associations – hampered, unfortunately, by the fact that it is not immediately obvious just what *is* a realistic watt-rating.

Well, . . . what's watt?

It seems logical to assume that the maximum 'undistorted' sound level a given combination of amplifier and loudspeakers will produce depends on the maximum amount of 'undistorted' drive power available.

The assumption is correct, up to a point – the point at which the loudspeaker becomes the factor limiting a further increase in the 'undistorted' sound pressure.

Whichever factor sets the limit, there comes a setting of the gain control at which the reproduction is no longer 'undistorted'. Some listeners immediately detect this as a 'rough edge' to the loud music passages, others actually like the effect – and happily turn the 'fi' up 'hi'er.

When the system really saturates (so that there is quite unmistakable severe distortion) the usual reaction is to assume that the power amplifier is 'chipping'. That may well be – but it 'ain't necessarily so'. The discovery is invariably made too late, after an investment in new parts or in a new ready-built amplifier of higher rating has failed to noticeably increase the available 'racket'. What *has* happened is that more watts have become available for heating up the speaker's drive-coil (and possibly tearing the cone loose from its moorings). This can easily mean a further considerable investment – and this time without a trade-in!

It is one of the physical facts of life that a high quality loudspeaker of reasonable dimensions inevitably has an efficiency – i.e. the ratio of acoustic watts delivered to electrical watts consumed – in the order of 1 . . . 5%. The balance is simply waste heat!

The distortion in the sound radiation from a loudspeaker, as a function of the applied drive-power, is a difficult thing to measure. One therefore rarely finds figures on this in the manufacturer's published specification. The situation regarding permissible drive power seems to be this: there are two limiting factors to the drive power a given loudspeaker will 'accept'; there is the instantaneous peak power input at which saturation-distortion or even actual mechanical damage will occur, and there is a considerably lower continuous power level (certainly in the case of mid-range and tweeter units) at which the continuous heat production causes the maximum allowable temperature rise in the 'motor' (i.e. the moving coil). A measurement with a steady sinewave as loudspeaker drive will encounter the latter limit first, so that some kind of 'tone burst' seems to be required. The duty-cycle of this tone burst needed to bring the limits together would have to be determined for each type of loudspeaker tested and quoted in the specifications – assuming that this is meaningful to the customer working out the permissible amplifier rating!

Manufacturers would clearly prefer a standardised procedure that would enable dissimilar units to be compared by prospective users. Presently used test signals are therefore obtained by 'frequency-weighting' a wideband noise signal until its spectral power-density (both 'instantaneous peak' and 'continuous') corresponds to that of 'typical' music (whatever that may be). This solves the maximum-power problem nicely – but not the distortion-measurement one.

If the customer is going to use a power amplifier capable of overheating (or mechanically overdriving) any of the loudspeakers in the system, he will simply have to refrain from doing silly things with the volume and tone controls. Damage rarely occurs before severely-distorted reproduction has given fair warning . . .

Amplifier sinewave rating

The amplifier's 'continuous' or 'sine-wave' rating is, to put it crudely, its heating-ability. The rating is obtained by having the amplifier deliver a steady sinewave output of specified frequency, into its rated load resistance – at a level for which a specified small deviation from the input waveform (i.e. a specified amount of distortion) is caused by non-linearities in the output circuit. Manufacturers normally specify a level that the worst product made (due to component tolerances etc.) will reliably meet.

A stereo power amplifier is invariably

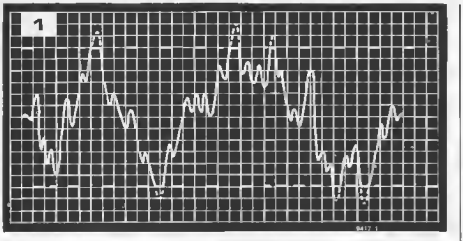
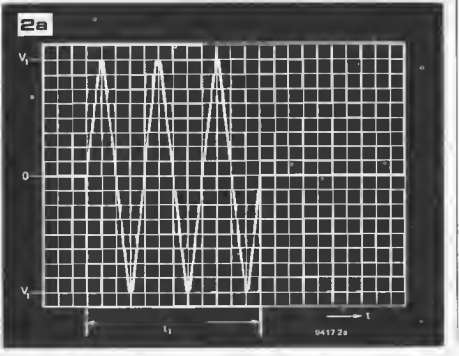
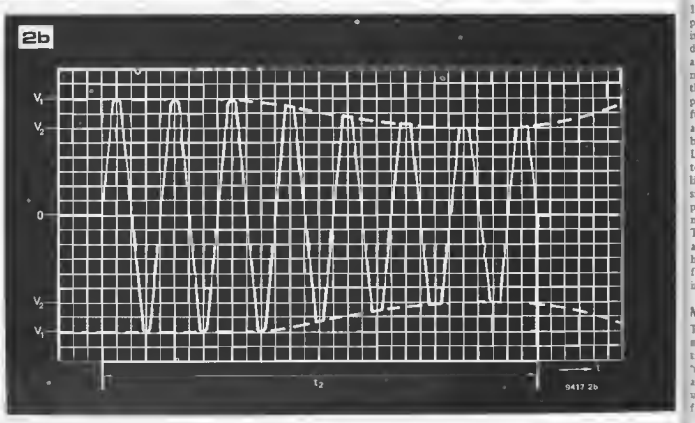


Figure 1. There is a limit to the positive or negative output voltage swing, set by the operating conditions. The dashed curve shows an attempted 'overdrive' waveform, the solid curve shows the 'clipped' output waveform actually obtained.

Figure 2. When the duty cycle of the input signal, in this case a tone burst, is sufficiently small, the clipping levels are approximately those due to the quiescent supply voltage V_1 (2a). Interval t_1 is then short in comparison with the supply time constants. The longer interval t_2 (2b) corresponds to a higher average power, causing the supply voltage to fall (ultimately to 'full load' V_2), so that the originally unclipped waveform becomes distorted. V_2 is the level during the troughs in the ripple waveform, not the 'average' value of the DC supply.





rated on the basis of 'both channels driven' simultaneously – the situation that makes the severest demands on the power supply circuits.
What one actually measures in this test is the maximum *average* power, equal to the product of 'effective' ('RMS') voltage across and 'RMS' current through the load resistor. The *R*oot *M*ean *S*quare value of a time-varying quantity is its mathematically-derived 'effective value': the value of a steady direct voltage or current of the same heating ability. The intermediate values within a representative time-interval are 'squared', then the squares are 'meaned' (averaged) and the 'root' of this average taken as the result ('the root of the mean of the squares'). For a sinewave the RMS value is known to be 'one over root two' (about 0.71) times the peak value.
One occasionally encounters a 'continuous peak' power rating. It is the product of peak voltage and peak current (i.e. 'squarewave power') and is precisely twice the sinewave rating – its only claim to (commercial!) merit.
The value of a 'continuous' rating is that it enables one to make objective comparisons between different amplifiers. It also provides a 'reference' output level at which a distortion measurement (necessarily a steady-state operation) can be carried out. Assuming that the system limitation is not in the loudspeakers, since if it were the whole matter would become rather complicated, the question can be raised: to what extent is the sinewave power rating of an amplifier relevant to its ability to deliver an undistorted music signal?
The waveform of a music signal is rarely even remotely similar to a sine waveform. The ratio of peak value to RMS value (the 'crest factor') can exceed 15 dB for much of the programme, depending of course on the kind of music involved and on the extent to which dynamic-range compression has been applied during recording and transmission. When the music signal is driving the amplifier momentarily just to its peak output (i.e. genuinely undistorted full-drive), one may assume that the average power delivered will be well below the amplifier's continuous rating. Let us not complicate matters by trying to account for the effect of current limiters in the output stage. The simple situation is that the amplifier's peak power capability is determined by the momentarily available supply voltage. There will come a point (see figure 1) at which the 'on' transistor 'bangs its head' against the supply rail – the waveform being flattened ('clipped') by the inability to go higher.

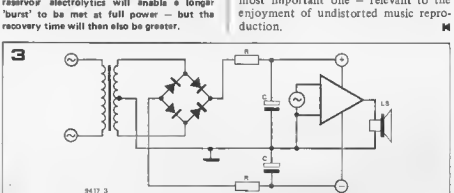
Music power rating

The specification sheets of many commercial amplifiers give not only the continuous power rating, but also the 'music power'. This latter figure is then always higher than the continuous figure. The music power rating does not follow from any standard measurement procedure; it is simply an indication by the manufacturer of the output power his amplifier will *momentarily* deliver (i.e. during instantaneous peaks in the music signal).
One must therefore be careful when comparing amplifiers on the basis of their music power ratings. On the other hand, the rating is quite relevant to the unit's performance in a practical situation and cannot be dismissed as a mere commercial trick.
The essence of the 'music power' concept derives from what (watt) happens when the amplifier's power supply circuit is not voltage-regulated. The situation is that an undriven class B output stage draws only a relatively small standing or 'quiescent' supply current, so that the fairly hefty reservoir capacitor has no difficulty in providing an almost ripple-free feed voltage close to the peak value of the transformer secondary 'open' voltage. When drive is applied there will be a tendency for the feed voltage to drop (and for the ripple to increase) – causing the 'clipping level' of the amplifier to fall. This process takes time however (because of the aforementioned hefty reservoir capacitor) – so that a *momentary* full power demand will be met at full voltage. Only when the *average* demand becomes appreciable will the supply voltage reduction noticeably reduce the available output power. Note that the relative power reduction is roughly proportional to the square of the relative voltage reduction, because a reduced voltage swing inevitably means also a reduced current swing – and the product of voltage and current is power. Figure 2 illustrates the on-load behaviour of the simple supply circuit of figure 3. Charge flows out of the reservoir at a rate proportional to the current demanded (charge is measured in ampère-seconds). The charge loss has to be made good by a surge-current, that occurs one hundred times per second, whenever the instantaneous secondary voltage (minus the drop in the rectifier diodes) exceeds the voltage across the capacitor. The internal resistance of the rectifier circuit (actually the effective 'copper resistance' of the transformer windings) determines the magnitude of these surges – and therefore the drop in supply voltage that must occur with a given combination of capacitor value and load current. V_1 is the no-load (or better 'quiescent load') supply voltage; V_2 is the considerably lower full-load voltage (continuous full drive). The charging process occupies a greater part of the hundredth-of-a-second (mains half-wave) interval – and the voltage drops much faster during the full-load discharge process. It will not be difficult to see why power-electrolytics have a 'permissible ripple-current' rating in addition to their nominal capacitance! The designer of the power supply has to make a difficult choice here. A very low transformer winding resistance (both primary and secondary) will make for a very 'good' supply. It unfortunately also means a relatively bulky and expensive transformer – and a more violent 'switch-on'.
Note that providing electronic regulation of the power supply circuit will enable the 'continuous power' to be made equal to the 'music power' rating – but at the price of more transformer, more electrolytic and more heat sink! The only advantage of regulation is that the output stage can be continuously operated closer to the transistor voltage maxima, without requiring allowances for mains voltage tolerances. In return for the hardware investment one obtains, in essence, that a power rating slightly higher than even the permissible 'music power' can be guaranteed under all load conditions. This may be justifiable under certain professional circumstances.

Figure 3. A typical unregulated power supply circuit, in this case with symmetrical positive and negative output rails. The resistance shown as R is in fact due to the copper-resistance of the transformer windings and the series resistances of the rectifier diodes. At a given load demand, a larger value for the reservoir electrolytics will enable a longer 'burst' to be met at full power – but the recovery time will then also be greater.

Aftar all that . . . what's watt?

The 'continuous' and the 'music' power ratings of an amplifier give information that is relevant to the unit's ability to deliver an undistorted audio signal.
All other power ratings, such as 'square-wave power', 'peak music power', '±2 dB power' etc., reflect more upon the abilities of the advertisement copy-writer.
The amplifier's power rating is by no means the only parameter – or even the most important one – relevant to the enjoyment of undistorted music reproduction. ■



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