

up-to-date electronics for lab and leisure

# ELEKTOR 9

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The use of frequency dividers in electronic organs has been known for many years. The usual procedure is to use divide-by-two stages to divide down the notes of the highest octave to obtain the lower octaves. Until recently it was normal practice to use twelve independent master oscillators for the twelve notes of the top octave. The disadvantages of this approach are that twelve oscillators have to be adjusted when tuning the organ, and that supply voltage variations, temperature changes and component ageing can all make the organ go out of tune. A digital master oscillator, in which the notes of the top octave are derived from a single clock generator, suffers from no such disadvantages.	
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In response to popular demand we publish this design for an FM stereo decoder using the Motorola MC 1310 P. Although nothing is claimed for this circuit by way of originality (it must have been published in some form hundreds of times) it is nevertheless a useful design utilising a device that has become virtually an industry standard.	
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# feedback pll for fm

In a previous issue of *Elektor* the theoretical background of a Feedback Phase-Locked Loop (PLL) tuner was discussed (*Elektor* 3, p. 412). A practical design is now described for a complete receiver, including audio amplifiers, which provides high performance at a moderate cost.

Although many years have passed since the introduction of FM broadcasts in the U.K. it is only recently, with the advent of stereo broadcasting, that interest has really been aroused in this medium. Until now a high quality FM receiver has been either too complicated or too expensive for the home constructor to build. These problems are overcome by the use of PLL techniques in the receiver described here.

The front-end used in this design (i.e. the r.f. and mixer/oscillator section) is a ready-built unit. It is the front-end that determines, for the most part, the usable sensitivity of the receiver, which in this case is about 2.5  $\mu\text{V}$ . It is possible, in principle, to use other front-ends in this design, but the rest of the receiver will have to be adapted and this procedure should be undertaken only by those with the necessary theoretical knowledge. As with other modern receivers the PLL receiver is capable of 'locking-on' to a transmission once it has been tuned to it, but while normally a special Automatic Frequency Control (AFC) circuit is built into the receiver for this purpose, the PLL receiver has this capability inherently. The feedback PLL receiver 'captures' the transmission and adjusts itself continuously to follow it in frequency. Thus the AFC does not operate in the usual way and in fact the AFC input to the front-end forms part of the detector circuitry. As an additional bonus it is possible to reduce the bandwidth of the feedback PLL receiver. This is helpful when listening to a noisy mono transmission, for instance, when reducing the bandwidth will improve the signal-to-noise ratio.

## Principle of operation

Referring to the block diagram of figure 1 the tuner operates as follows: in the front-end a band of frequencies from the aerial input is amplified and then mixed with the oscillator signal (E). As a result of this mixing two new frequencies come into being that are the sum and difference of the two original frequencies. For example, if the in-

### Measurement results:

#### Sensitivity

( $f_{\text{mod}} = 400 \text{ Hz}$ , deviation = 40 kHz):

Mono: 3.2  $\mu\text{V}$  at 87 MHz and  
35 dB S/N,  
2.0  $\mu\text{V}$  at 100 MHz and  
35 dB S/N.

Stereo: 20  $\mu\text{V}$  at 94 MHz and  
26 dB S/N.

#### AF output level

( $f_{\text{mod}} = 400 \text{ Hz}$ , deviation = 40 kHz,

$f_c = 94 \text{ MHz}$ ):

Approx. 130 mV RMS.

#### AM suppression

(deviation = 40 kHz, 30% AM,

$f_{\text{mod}} = 400 \text{ Hz}$ ):

$V_{\text{in}}$	AM suppression
3 $\mu\text{V}$	50 dB
25 $\mu\text{V}$	53 dB
50 $\mu\text{V}$	53 dB
100 $\mu\text{V}$	53 dB
400 $\mu\text{V}$	53 dB
1 mV	48 dB
2 mV	44 dB

#### Hum level

(in metal case):

-70 dB.

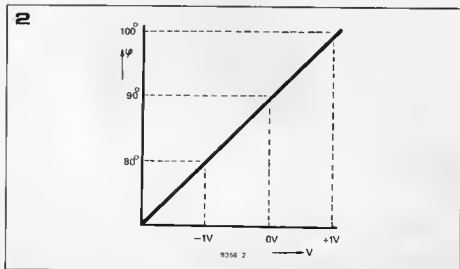
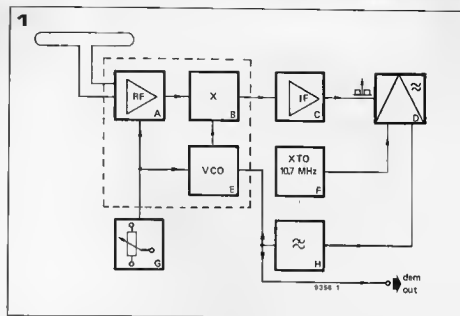
Figure 1. Block diagram showing the Feed-back PLL principle.

Figure 2. Graph of phase difference versus phase comparator output voltage.

Figure 3. Circuit diagram of the Toko EF5600 front-end module.

coming aerial signal has a frequency of 100 MHz and the oscillator frequency is 110.7 MHz then two new signals appear at the mixer output with frequencies of 210.7 MHz and 10.7 MHz respectively. The mixer output is filtered to remove the unwanted components and the 10.7 MHz is amplified by the i.f. amplifier, which is a tuned amplifier with a passband centred on 10.7 MHz. It can thus be seen that the receiver can be tuned by altering the passband of the aerial input stage and by altering the frequency of the oscillator. This is, of course, normal superhet practice, which those familiar with r.f. techniques will recognise.

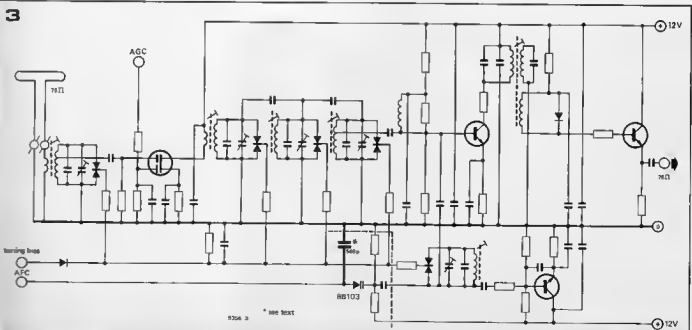
From here on the operation of the circuit differs from more conventional receivers. The output of the i.f. amplifier is fed to a phase comparator (D). The other input of the phase comparator is fed by a high-stability 10.7 MHz signal from a reference oscillator (F). The characteristics of the phase comparator are shown in figure 2. If the phase difference between the i.f. output



and the reference frequency is greater than  $90^\circ$  the output voltage is positive, if it is less than  $90^\circ$  the output is negative. At  $90^\circ$  phase difference the output voltage is, of course, zero.

However, since the input signal to the

aerial is frequency-modulated the only way to keep the phase difference between the i.f. output and the reference oscillator constant is to vary the front-end local oscillator so that it 'tracks' the signal. A constant 10.7 MHz output is



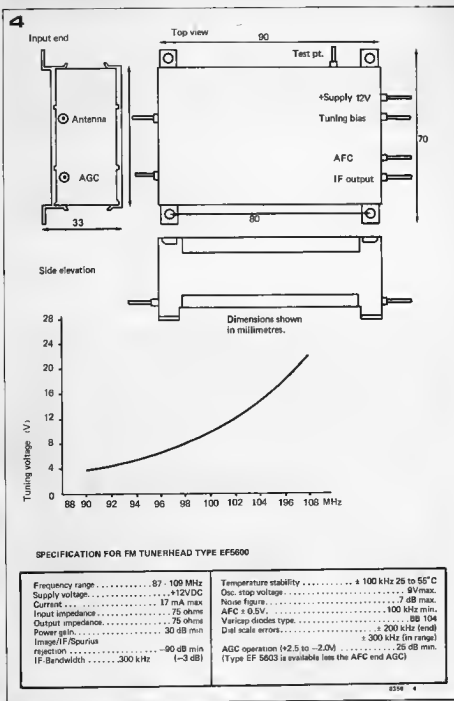


Figure 4. Outline, pin connections and specifications of the EF5600.

Figure 5. These photos show how the modification to the AFC input is carried out.

then produced. This tracking is achieved by feeding the output of the phase comparator back to the AFC input of the front-end so that it attempts to maintain a constant 90° phase difference between the i.f. output and the reference oscillator by varying the local oscillator frequency. The output voltage of the phase comparator is thus a replica of the original modulation of the input signal. It still remains, of course, to extract the stereo information.

### The tuner

The tuner used in this design is a Toko type EF5600. It is one of the best tuners generally available for the home constructor. The circuit is given in figure 3, and the outline, specifications and pinning are shown in figure 4.

The input stage utilises a dual gate MOSFET, which has good linearity — even strong input signals will give rise to very little cross modulation. This RF pre-amplifier stage is followed by three tuned bandpass filters, capacitively coupled. The selectivity of these filters is sufficiently high to make it possible to use a simple bipolar mixer stage.

It is common practice in FM front-ends to take the IF output straight from the secondary winding of the IF output transformer. In this design, however, an extra output stage has been added. This has the advantage that the (tuned) IF coil is scarcely loaded by the IF strip, which means that there is never any need to retrim the coil — no matter what the input impedance of the IF strip is. The tuner is fully aligned at the factory, and one should resist the temptation to twiddle any of the trimmers or cores.

The only modification to the tuner needed for use in the feedback PLL design described here is the AFC input. In the original tuner, this input is decoupled with a 10 n capacitor. This must be removed, and a 560 p capacitor soldered in its place (see photos, figure 5). It would be nice if Toko could supply tuners with this minor modification already built in. . .





The Mark 1 version of the feedback PLL receiver proved to have an input sensitivity of  $8 \mu\text{V}$ . To improve this, an additional RF preamplifier stage was added (figure 6a). The input transformer can be wound on a HF type ferrite bead, using 0.2 mm (36 SWG) enamelled copper wire (figure 6b). If required, both the  $75 \Omega$  and the  $300 \Omega$  winding can be wound on the same coil.

### The i.f. Amplifier

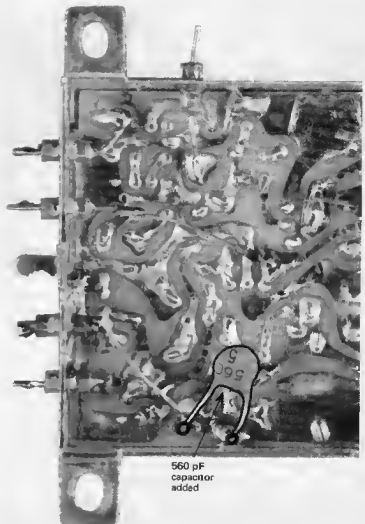
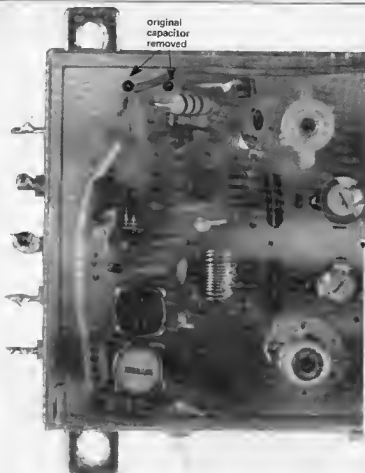
An unusual feature of the i.f. amplifier is the absence of bandpass filters. These are omitted because the tuner itself provides good selectivity and because the PLL has inherent selectivity due to the 10.7 MHz reference oscillator so that it can only lock onto 10.7 MHz. In addition, as the i.f. amplifier is within the feedback loop any filters would have to meet stringent phase distortion criteria, which is another reason for omitting them.

The IF signal is amplified by IC1 (gain approx.  $\times 40$ ) and fed to the OTA (IC3, figure 7). Diodes D1 and D2 limit strong signals. The first stage of the OTA is used as multiplier for phase detection, so there is relatively little IF amplification. For this reason, the bandwidth of the PLL depends on the input signal strength to the extent that for low signal levels (less than  $2 \mu\text{V}$ ) the bandwidth is reduced. This is an advantage when listening to weak transmissions, as it improves the signal-to-noise ratio. The disadvantage is that it can lead to distortion unless the weak transmissions in question were narrow-band to start with. Preset potentiometer P1 is used to set the loop gain, and hence the bandwidth. It is correctly set when a fully modulated stereo transmission is reproduced without audible distortion.

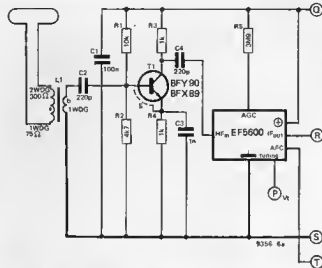
The output impedance of the OTA is relatively high, so a buffer stage (T2) has been added. The RC networks associated with this transistor are compensation networks for the loop.

The holding range of the PLL is so large (certainly for strong transmissions) that some form of tuning indicator is re-

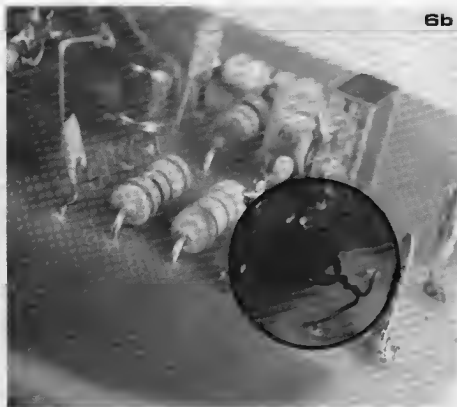
5

original  
capacitor  
removed560 pF  
capacitor  
added

6a



6b



quired. This is the function of T3 and T4. If there is no signal present at point 'R' (output of the tuner) the voltage at the collector of T2 is approximately 3.6 V. P2 is now set so that D3 and D4 light equally brightly. When tuning in to a transmission, the DC voltage on the collector of T2 varies in such a way that D3 lights if the tuning is off to one side and D4 lights if the tuning is off the other way. When the receiver is tuned in correctly both LEDs light equally.

#### The 10.7 MHz oscillator

In the interests of economy a 10.7 MHz ceramic filter is used as the frequency determining element in the oscillator instead of a crystal (figure 7, also shown separately in figure 8). This filter is connected between pins 3 and 7 of IC3.

The oscillation frequency is determined by the ceramic filter: it is simply the frequency at which the phase shift of the filter is  $0^\circ$  (or  $360^\circ$ ). However, most ceramic filters do not have  $0^\circ$  phase shift at their nominal frequency so some phase compensation is necessary. For this reason C17 and C20 have been added. C20 is a trimmer, so that the frequency can be set at exactly 10.7 MHz — provided one has access to a frequency counter. However, this is not so critical; if no frequency counter is available C20 can simply be set in the middle of its range.

The (reference) output signal is taken from pin 3, as this gives a cleaner sine-wave than the output at pin 7.

#### The stereo filter

The stereo multiplex signal consists of

#### Parts list:

##### Resistors:

- R1, R41 = 10 k  
 R2, R9, R31, R36, R37 = 4k7  
 R3, R4, R6, R16, R21, R34, R35 = 1 k  
 R5 = 3M9  
 R7, R14, R23 = 1k5  
 R8, R10 = 47 k  
 R11, R12, R39, R40 = 100 k  
 R13, R32 = 2k2  
 R15 = 470  $\Omega$   
 R17, R18 = 270  $\Omega$   
 R19 = 22 k  
 R20 = 120  $\Omega$   
 R22 = 390  $\Omega$   
 R24, R25 = 470 k  
 R26, R28, R29, R30, R33 = 15 k  
 R27 = 330  $\Omega$   
 R38 = 27 k  
 R42 = 56 k  
 R43, R44, R45 = 560  $\Omega$   
 R46 = 150  $\Omega$ /2 W  
 P1 = 47 k preset  
 P2 = 10 k preset  
 P3 = 4k7 preset  
 P4 = 220 k preset  
 P5 = 2k2 preset  
 P6 = 22 k multiturn

##### Capacitors:

- C1, C6, C7, C8, C10, C18, C19, C45, C46 = 100 n  
 C2, C4 = 220 p  
 C3, C5, C9, C12, C15 = 1 n  
 C11 = 68  $\mu$ /16 V  
 C13, C36, C37, C38 = 10  $\mu$ /16 V  
 C14 = 47  $\mu$ /16 V  
 C16 = 1n8  
 C17 = 68 p  
 C20, C22 = trimmer 10...60 p  
 C21, C32 = 470 n  
 C23 = 150 p  
 C24, C25, C26 = 120 p  
 C27 = 47 p  
 C28 = 2 $\mu$ /16 V  
 C29 = 47 n  
 C30 = 470 p  
 C31, C34 = 220 n  
 C33, C35 = 10 n  
 C39 = 470  $\mu$ /25 V  
 C40 = 47  $\mu$ /6 V  
 C41, C42, C43, C44 = 470  $\mu$ /40 V

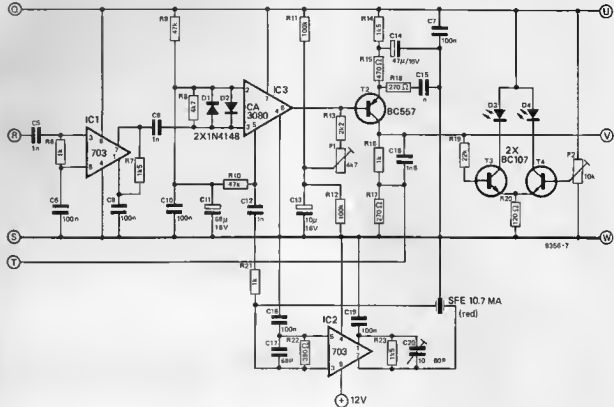
##### Semiconductors:

- T1 = BFY90, BFY89  
 T2, T6 = BC557  
 T3, T4, T7 = BC107  
 T5 = BC547B  
 D1, D2 = 1N4148  
 D3, D4, D5 = LED  
 D6 = ZTK22 (22 V) (see text)  
 B = 4 x 1N4001  
 IC1, IC2 = 703  
 IC3 = CA3080  
 IC4 = MC1310P  
 IC5 = TBA6268

##### Sundries:

- L1 = ferrite bead (see text)  
 ceramic filter SFC 10.7 (red dot)  
 S1 = switch, SPST  
 meter = 400  $\mu$ A  
 fuse = 100 mA  
 TOKO-tuner EF5600

7



8

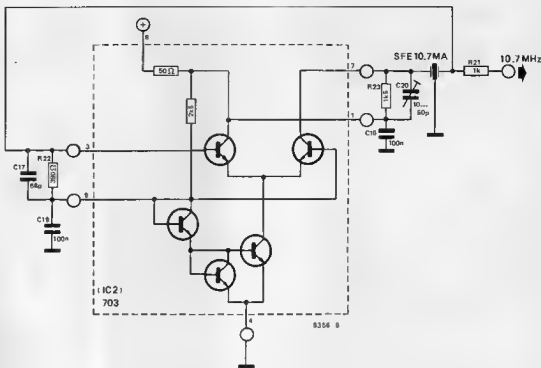


Figure 6a. The RF preamplifier stage and Toko front-end.

Figure 6b. The serial transformer: a ferrite bead.

Figure 7. The circuit of the 'IF stage and detector' and the tuning indicator LEDs.

Figure 8. The 10.7 MHz reference oscillator (also shown in figure 7).

three components:

- an AF signal from 30 Hz to 15 kHz;
- a double sideband suppressed carrier signal centered around 38 kHz, from 23 kHz to 53 kHz;
- a pilot signal, derived from the original 38 kHz carrier, at 19 kHz.

It can be shown that stereo decoders will not only detect the signals in the 23 to 53 kHz band, but also other (un-

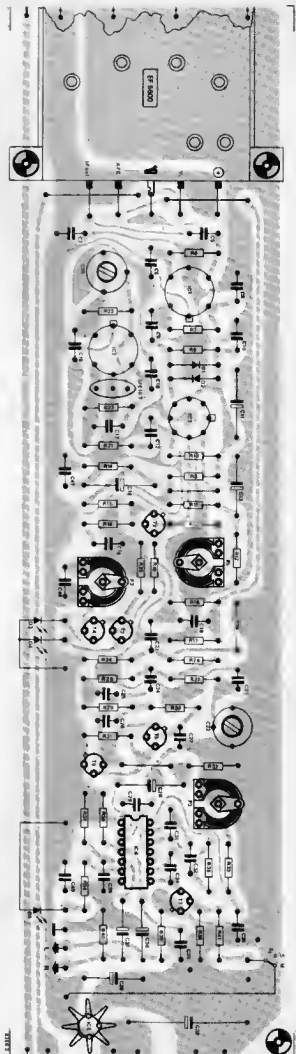
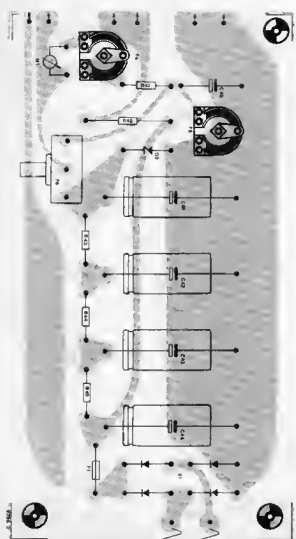
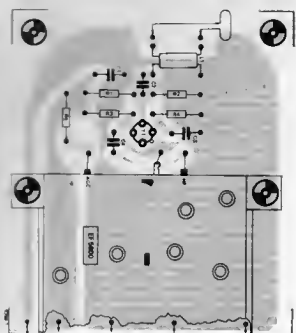
wanted) signals centered around multiples of 38 kHz. For the best signal-to-noise ratio it is thus important that no signals above 53 kHz are fed to the stereo decoder. To this end, the filter shown in figure 9 has been added. The best channel separation is obtained when the phase shift at 38 kHz is zero degrees; this can be set with C22. For this adjustment it is best to use a strong





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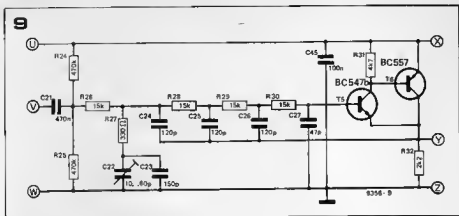


Figure 9. The stereo filter.

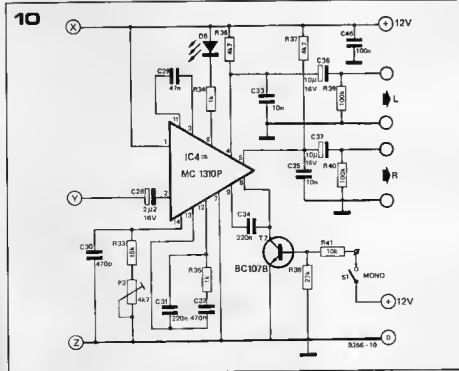


Figure 10. The stereo decoder.

Figure 11. The power supply, including the smoothing and stabilisation for the tuning voltage.

Figure 12. The p.c. board for the complete receiver, including front-end, stereo decoder and power supply (figures 6a, 7, 9, 10 and 11). Note that the board consists of three sections that are joined together with wire links.

Figure 13. Pin configurations of the two types of ceramic filter.

Figure 14. A typical tuning scale meter calibration.

which should be adequate to drive most amplifiers. The amplifier input impedance should be not less than 22 k.

### The power supply

The receiver is relatively insensitive to variations in supply voltage, so that a fairly simple power supply circuit can be used (figure 11). The resistor (R46) in series with the stabiliser IC reduces the power dissipation in the IC and, at the same time, keeps its input voltage safely below the maximum value (24 V). The tuning voltage must be derived from a well smoothed and temperature-independent supply. This consists of C41 to C44, R43 to R45, and a temperature compensated zener diode (D6). If the ZTK22 is difficult to obtain any other 22 V zener can be used, provided it is temperature-compensated. If there is any doubt on this score, however, it is advisable to use four 5.6 V voltage reference diodes in series.

### Construction

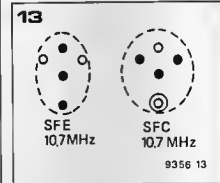
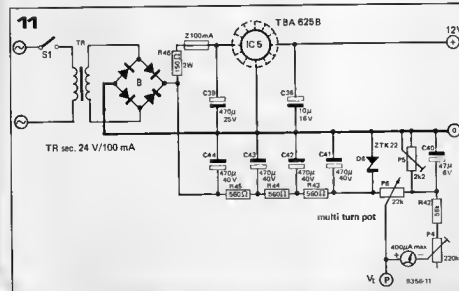
The parts list gives details of all the required components. Equivalent types are given where possible. The p.c. board

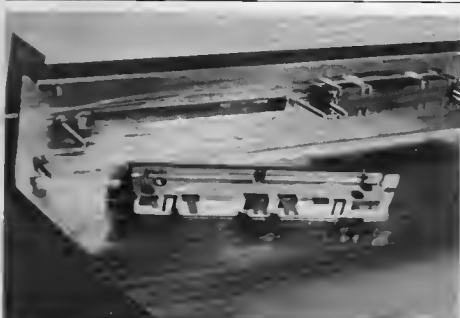
(local) transmission or a stereo test generator. C22 is simply set for maximum separation.

### Stereo Decoder

The stereo decoder (figure 10) uses the now commonplace Motorola MC1310P PLL IC and needs little explanation.

The only setting up required with this type of decoder is to tune the oscillator so that the free-running frequency is 19 kHz. This is accomplished by means of P3. The channel separation is about 40 dB. A LED (D5) is included as a stereo indicator beacon. The decoder outputs provide nominally 100 mV





and component layout are given in figure 12.

Both SFC and SFE type ceramic filters can be used; in both cases they should carry a red dot which shows that they are exact 10.7 MHz types. The pin configurations of the two types of filter are different (figure 13), but the board will accommodate both types. The Toko CFSA 10.7 filters can also be used; the pinning corresponds to that of the SFE 10.7 MHz. For these filters 'no colour code' denotes an exact 10.7 MHz type.

A cheap moving coil meter can be used for the tuning scale; it measures the tuning voltage, but the scale can be calibrated in MHz. Figure 14 gives an example. The actual calibration can be done either by tuning in to several known transmitters in succession and marking them on the scale, or else by measuring the tuning voltage and calibrating the scale in accordance to the graph shown in figure 4. An entirely different possibility is to use a slider potentiometer for P6 and calibrate a scale for it in MHz; the tuning meter then becomes redundant.

The front-end should be mounted on the p.c. board and wired to it with stiff links. Connections to the tuning potentiometer and the tuning scale meter should be as short as possible to avoid hum pickup. It is advisable in any case to use screened cable for these leads. Sockets should be used for the ICs, especially by the less experienced constructor, to avoid damage during soldering.

### Alignment

When construction is complete (check that the ICs are the right way round in the sockets!) turn P1 and P2 fully clockwise, and set all other potentiometers and trimmers in the middle of their range. Now switch on and check the supply voltages. Do not yet connect an aerial. Alignment now proceeds as follows:

— If a frequency counter is available, readjust C20 until the reference oscil-

lator is set at 10.7 MHz. Otherwise simply leave C20 in the middle of its range — the frequency will not be far off.

- Make sure that there is no reception as yet (if necessary, tune away from any station with P6), and adjust P2 until both tuning LEDs (D3 and D4) light equally brightly.
- Plug in the aerial. It should be possible to receive some stations by tuning in with P6. Select the strongest stereo transmission available, then turn P1 anti-clockwise until distortion just becomes inaudible. P1 is correctly set when there is no distortion and slight retuning (with P6) produces no change in volume.
- Now P3 in the stereo decoder should be adjusted as follows: P3 is adjusted until the stereo LED (D5) lights and is then set to the middle of the range over which the LED is lit.
- After this adjustment, recheck the setting of P1 — some minor readjustment may prove necessary.
- Next, set C22 for maximum stereo channel separation.
- Set P6 at minimum; P5 is now adjusted so that the low frequency end of the band is at 87 MHz (tuning voltage approximately 3.5 V).
- Finally, with P6 at maximum, P4 is set for full scale deflection of the tuning meter if this is included. The tuning meter scale (or slider potentiometer) can now be calibrated as described under 'construction'.

C. J. Both

## to drive or not to drive ...

Driving a car immediately after drinking too much alcohol is asking for trouble - even if one doesn't happen to run into a police check. One could all too easily run into something else! Most drivers have found that they can drive safely (?) on the recipe 'one glass per hour'. The trouble is that it is so difficult to keep to that one glass - and that the more one drinks the more one's confidence will override the fear of getting caught. Simultaneously one's ability to react to a critical situation correctly and fast will diminish drastically. The slower reactions of a person 'under the influence' form the basis of this 'drive'/'no drive' tester.

### Editorial note:

The author suggests using the circuit to block the ignition in a car. We do not advise this — think of what would happen if you stelled your engine in the centre of a busy crossing! However, the unit can be quite useful as a reaction tester in its own right — e.g. to test departing guests after a party, so that taxis can be ordered as required. . . .



## Components list:

## Resistors:

R1 = 6k8  
 R2 = 39 k  
 R3, R4, R6 = 1 k  
 R5 = 8k2  
 R7, R13 ... R22 = 470  $\Omega$   
 R8 = 10 k  
 R9 = 100 k  
 R10, R12 = 330  $\Omega$   
 R11 = 3k9  
 P1 = 47 k preset  
 P2 = 22 k preset

## Capacitors:

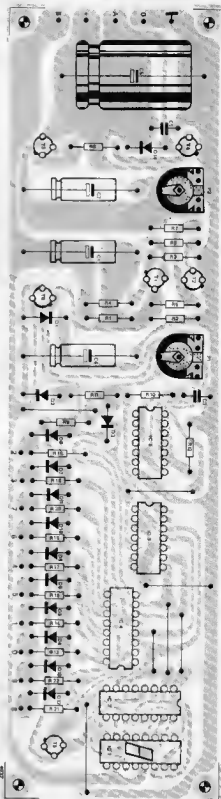
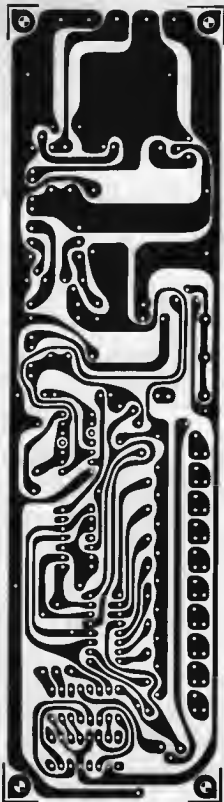
C1, C2 = 1000  $\mu$ /10 V  
 C3 = 2n2  
 C4 = 470  $\mu$ /10 V  
 C5 = 100 n  
 C6 = 1000  $\mu$ /25 V

## Semiconductors:

D1 ... D14 = DUS  
 T1 = TUP  
 T2 ... T6 = TUN  
 IC1 = 3015 F minitron  
 IC2 = 7447  
 IC3 = 7490  
 IC4 = 74141  
 IC5 = 7413

## Miscellaneous:

Re = 6 V/260  $\Omega$  relay  
 (1 break, 3 make)  
 L1, L2 = 6 V/50 mA lamp  
 S0 ... S9 = pushbuttons



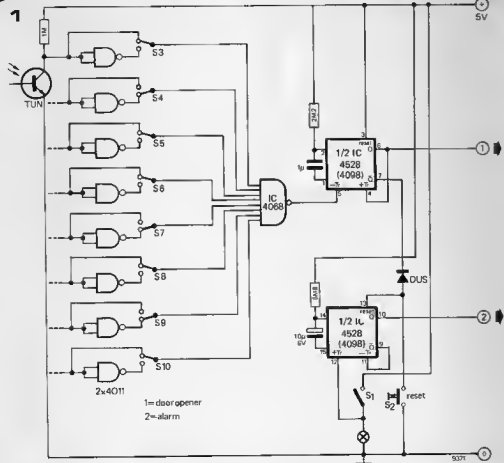
power was turned on. It consists of P2, C2, T3 and T4. The interval that must elapse before this time switch fires can be preset by P2. When the electrolytic is sufficiently charged, the current through T4 will cause the relay to attract. This relay will 'hold' via one of its contacts, so that it can only be released by interrupting the power supply. A second contact turns off the tester proper and replaces the 'no drive' indication by 'drive'. The remaining contacts (in parallel) are wired in series with the car's starter relay circuit, so

that they enable the engine to be started.

Whenever a too-long reaction time causes T1 and T2 to latch, the main timing capacitor (C2) will be discharged, essentially restarting the test period. It is only possible to obtain a 'drive' permit after a sufficient number of sufficiently quick reactions has been successively performed. As already noted above, the tester is cleared by a short interruption of the power supply. Bear in mind that the necessary 5 volt supply will have to be derived from a

vehicle battery of which the voltage can drop quite far during starting!

One could spend hours discussing to what extent a piece of hardware can be expected to stand in for the failing sense of responsibility (or lack of self-discipline) of a human being. Perhaps the final remark could be this: use push-buttons of a recessed type, to prevent the subject of the test from depressing them all simultaneously!



An electronic lock, which is opened using a binary encoded optical key can easily be constructed using 'home-made' phototransistors and CMOS logic ICs. The principle of operation is very simple. The lock consists of a row of phototransistors, which can be illuminated by a lamp. The key is a strip of transparent plastic with sections opaqued to form a binary code.

#### The circuit

Figure 1 shows the circuit of the optical lock. For simplicity only one phototransistor is shown, but there are 8, each connected to the input of a NAND-gate as is the one shown. Each phototransistor has a 1 M collector resistor. When a transistor is illuminated its leakage current increases and the collector voltage falls. When it is not illuminated the leakage current is very small and the collector voltage is almost equal to supply voltage. The illuminated and non-illuminated states therefore correspond to logic '0' and logic '1' respectively on the input of the NAND gates (connected as inverters).

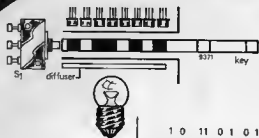
When the key is inserted into the lock it depresses a microswitch (S1) so that the lamp lights (see figure 2). The opaque sections of the key correspond to logic '1', and the transparent sections to logic '0'. The outputs of the phototransistors thus assume the binary code. Switches S3 to S10, which are used to set up the coding of the lock, are so arranged that any '0' outputs are complemented by the inverters, while '1's are connected straight to the inputs of the 8-input NAND-gate.

Thus only when the correct key is inserted will all inputs to the NAND-gate be '1', so its output will go low. This triggers the monostable ( $\frac{1}{2}$  4528) producing an output pulse (1) which can be used to operate a solenoid bolt.

The  $\bar{Q}$  output of this monostable also inhibits a second monostable. Depression of microswitch S1 by the key triggers the second monostable, whose output (2) is connected to an alarm circuit. Should an incorrect key be inserted then the output of the 8-input NAND-gate will not go low and the first monostable will not be triggered.

## optical-lock

santatronics



Thus the second monostable will not be reset by the Q output of the first, and the alarm will sound. The alarm may be reset manually by S2.

#### Practical notes

The coding of the lock is set up using switches S3 to S10. Where a particular bit of the code is to be a '1' then the relevant switch is left in the position where the inverter is bypassed. Where a bit is to be '0' the switch is placed in the position where the output is taken from the inverter, thus complementing the bit and producing a '1' at the input of the 4068 8-input NAND gate. If one

does not wish to change the lock code frequently then the switches may be replaced by hardwired links.

The number of possible codes for the lock depends upon the number of bits used. In the circuit given 8 bits were used for convenience of the IC package count (2 x 4011 and 1 x 4068 required) but there is no reason why the number of bits cannot be extended. Using 8 bits gives  $2^8 - 2$  or 254 possible combinations. The code 00000000 is not used as this corresponds to total illumination, which could be accomplished by an intruder depressing the microswitch with a piece of stiff wire or transparent plastic. Similarly 11111111 is not used, as in the event of lamp failure this code would be registered whatever key was used.

Finally, excellent phototransistors can be made from BC 108s by (carefully) sawing off the top of the can and filling with transparent casting resin as sold in handicraft shops.

## sixpence detector for christmas pudding

This handy metal detector will greatly increase one's chances of obtaining a piece of Christmas pudding with a sixpence in it, or if one is really lucky, a silver threepenny hit (Daddy, daddy, what's a threepenny bit?).

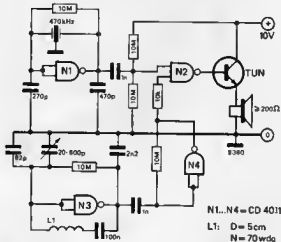
The principle of operation is simple and well-known. It consists basically of two oscillators, one of which is a fixed frequency reference oscillator, and the other an oscillator whose frequency-

determining inductance is a search coil. Initially the two oscillators are adjusted so that their frequencies are nearly the same. The two outputs are fed into a mixer which will produce the sum and difference frequencies and the oscillators are adjusted so that the difference frequency (beat note) is in the audio band. If a metallic object is now brought near the search coil its inductance will vary, altering the oscillator frequency and hence the beat note.

The circuit is very simple and is designed around a CD4011 quad 2-input NAND gate. The reference oscillator uses an inverter (N1) as the maintaining amplifier and a 470 kHz ceramic filter for stability.

The variable frequency oscillator (N3) uses an LC resonant circuit with the search coil (L1) as the inductor. This can be a coil of about 70 turns of insulated wire and a diameter of approximately 50 mm (2"). The mixer is simply a NAND gate (N2), and the 4th NAND gate in the package (N4) is used as a buffer amplifier behind the variable frequency oscillator.

If a crystal earpiece is used, the transistor can be omitted - the output of N2 can drive the earpiece.



N1, N4 = CD 4011

L1: D = 5cm  
N = 70wdg

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# function generator ic 2206

Function generating ICs have been on the market for several years. Now one can refer to a 'second generation' of these ICs, for technical progress has resulted in improved performance at only slightly higher prices.

A commonly used function generator IC is the type IC 8038 (ICL). This IC however has several 'blemishes', which severely limit its application. In particular the distortion factor of the sine signal, the frequency range, the linearity and maximum frequency sweep of the VCOs are not satisfactory. The newer IC XR 2206 (Exar) offers, apart from substantially better performance, additional functions also. The advantages of the IC are summarised in table I, while table II lists the most important applications.

## Description of functions

The IC contains four groups of functions as shown in figure 1, i.e. a voltage controlled oscillator (VCO), a function block 'switchable current sources', an analogue multiplier with sine converter, and a buffer amplifier. The central unit of the function generator is the VCO. This is actually a current controlled oscillator (which by the way applies to most VCO circuits!) The frequency of the VCO is determined by a capacitor and a control current. Integrated current switches switch this current to one of the two current outputs (pin 7 or 8) of the IC, depending on the logic level of the selector input (pin 9). A linear relationship exists between the control current  $I_f$ , flowing from one of these outputs to earth, and the frequency of the VCO as follows:

$$f = \frac{I_f}{3C} \quad (\text{Hz, A, F}).$$

If the current is given in mA and the capacitance in  $\mu\text{F}$ , then:

$$f = \frac{330 I_f}{C}$$

Current values between  $1 \mu\text{A}$  and  $3 \text{mA}$  are permissible for  $I_f$ , but optimum temperature stability will be achieved only in the range  $15$  to  $750 \mu\text{A}$ . The current connection pins 7 and 8 are low resistance outputs, and the voltage at these points is stabilised to  $3 \text{V}$  within the IC. As this reference voltage exhibits only a very small temperature coef-

ficient ( $6 \cdot 10^{-5} \text{V}^\circ\text{C}$ ), the temperature stability of the oscillator frequency is also very good. It is practically only dependent on the temperature coefficients of the external components determining the frequency.

In the simplest case adjustment of the control current is effected by means of a resistance  $R_f$  between pins 7 or 8 and earth. In this case the control current is:

$$I_f = \frac{3V}{R_f}$$

and accordingly

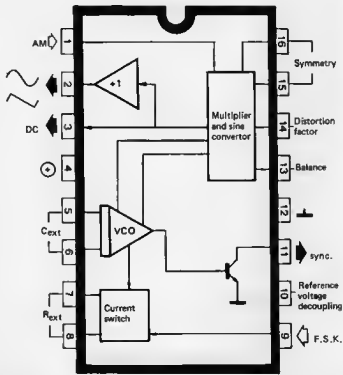
$$f = \frac{I_f}{3C} = \frac{1}{R_f \cdot C}$$

applies for the frequency.

Permissible resistance values lie between  $1 \text{k}$  and  $2 \text{M}$ , and for good temperature stability between  $4 \text{k}$  and  $200 \text{k}$ . The capacitor which determines the frequency can be chosen between  $1 \text{nF}$  and  $100 \mu\text{F}$ . The most important properties of the integrated VCO can be seen in table III.

The VCO signal switches an integrated output transistor, the collector of which is accessible at the synchronisation output, pin 11. At this output a square pulse signal is available. In addition to this, the VCO signal provides the basis for the signal generation carried out in the multiplier and sine converter section. This part of the circuit provides a sine or triangular signal

1



8054 1

Table I: Advantages

- Low distortion factor, typically 0.5%.
- High frequency stability, typically  $2 \cdot 10^{-5} / ^\circ\text{C}$ .
- Large relative frequency deviation, typically 2000 : 1.
- Low frequency dependence on supply voltage, typically 0.01%/V.
- Linear amplitude modulation.
- Wide supply voltage range, 10 to 26 V.

Table II: Applications

Signal generation: sine, triangle, sawtooth, square, wobbulators, AM/FM generators, Frequency shift keying, PLL circuits, Automatic measuring and testing equipment.

at the output, dependent on the external circuitry connected to pins 13 and 14. Provision exists for adjustment of curve shape (distortion factor), symmetry, amplitude and DC level of the output signal. If careful balance of curve shape and symmetry are carried out, the distortion factor of the sine signal is about 0.5%. This is adequate for most applications.

### Basic circuit for function generator

The basic circuit for a function generator incorporating the IC 2206 is shown in figure 2. With relatively few external components, the circuit generates sine,

Table III: VCO specifications

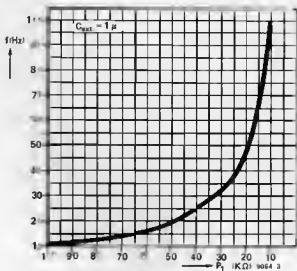
Max. oscillator frequency	500 kHz
(typically)	1 MHz
Min. oscillator frequency	0.1 Hz
(typically)	0.01 Hz
Frequency accuracy	$\pm 2\%$ of $f_0 = 1/R \cdot C$
Temperature stability	$\pm 2 \cdot 10^{-5} / ^\circ\text{C}$
(typically)	
Supply voltage dependence	0.01%/V
(typically)	

Figure 1. Connections to the IC (top view).

Figure 2. A function generator.

Figure 3. Frequency plotted as a function of the value of P1.  $C_{\text{ext}}$  is  $1 \mu\text{F}$ .

3



triangular and square wave forms in five frequency ranges from 1 Hz to 100 kHz. Capacitors C1 to C5 select the frequency range. C1 should be a tantalum electrolytic capacitor if possible. P1 enables a frequency decade to be covered in each range, and for good frequency stability a value of 100 k was chosen. The relationship of frequency to P1 is shown in figure 3.

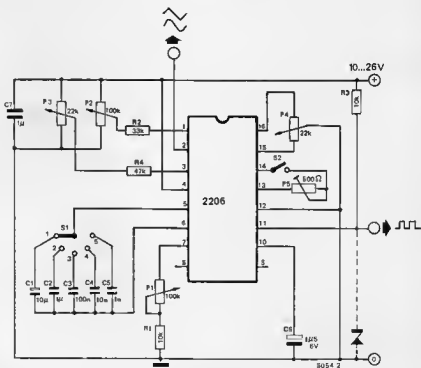
Because of the relationship  $f = 1/R \cdot C$ , the frequency v. P1 graph is not linear but hyperbolic. A more linear relationship may be obtained by the use of a logarithmic potentiometer. Capacitor C6 decouples the internal reference voltage source.

A square wave output is available at

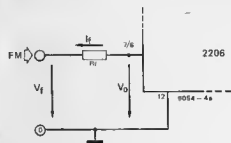
pin 11 and resistor R2 provides a collector load for the internal output transistor. For TTL compatibility the output amplitude must be limited to 4.7 V by the zener diode, shown connected by the broken line. Pin 2 provides a triangular waveform of good linearity (1% departure) if the switch is open, and a sine wave if the switch is closed.

For low distortion balancing of the curve shape is essential. For this purpose the symmetry potentiometer P4 is first turned to its central position and P5 is adjusted to give minimum distortion of the output signal. A further reduction of the distortion factor can then be achieved by readjustment of P4. If a distortion factor of about 2% is accept-

2



4



able, then this adjustment can be waived. P4 is then not required and P5 is replaced by a fixed resistor of 200  $\Omega$ . The potentiometer P2 is used for amplitude adjustment of the sine or triangular signal. The maximum output voltage is equal or greater than  $V_b/2$ . The output impedance at pin 2 is about 600  $\Omega$ .

The DC level at the signal output corresponds approximately to the DC voltage at pin 3 of the IC, and this is adjustable by P3. If the circuit application does not demand otherwise, then one should

adjust to  $V_b/2$ , in which case P3 can be replaced by a symmetrical potential divider ( $2 \times 12$  k).

The most important technical data of the circuit shown in figure 2 are summarised in table IV.

### FM generator and wobulator

As already mentioned in the functional description, the VCO frequency is proportional to a control current  $I_f$ . By changing this current the frequency

can be varied over a wide range (max. 2000 : 1), see table V. A possible form of current control would be the insertion of a controllable current source at outputs 7 or 8 of the IC. This solution turns out to be too complicated in practice and also leads to linearity problems.

A simpler proposal is shown in figure 4a. In this case the control current is changed by means of an opposing voltage applied to  $R_f$ . The difference between the voltage  $V_o$  (3 V) and the control voltage  $V_f$  is dropped across the

Table IV: Specifications, figure 2

Supply voltage	10 to 26 V
Current consumption	20 mA approx.
Max. output voltages ( $V_b = 12$ V)	
Sine/triangle	6 V
Square	12 V
Output impedance	
Sine /triangle	600 $\Omega$ approx.
Square	10 k $\Omega$ approx.
Distortion factor, sine signal	
Without balance	2.5% typical
With balance	0.5% typical
	1.5% max.
Linearity, triangular signal	1%
Amplitude stability (for frequency change 1000 : 1)	0.5 dB typical

Table V: Specifications, figure 4

Max. relative frequency deviation	2000 : 1 typically ( $R_f = 1$ k to 2 M)
Wobble linearity	
10 : 1 Wobble amplitude	2% typically ( $f = 1$ kHz to 10 kHz)
1000 : 1 Wobble amplitude	8% typically ( $f = 100$ Hz to 100 kHz)
FM distortion (Amplitude $\pm 10\%$ of $f_o$ )	0.1% typically

Table VI: Specifications, figure 6

Amplitude	$= V_b$
Rise time	250 ns typically
Decay time	50 ns typically
'0' level	0.2 V typically, 0.4 V max. ( $I_L = 2$ mA)

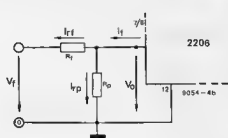
Figure 4a. A wobble generator. The current  $I_f$ , which determines the frequency, is proportional to  $V_f$ .

Figure 4b. Adding resistor  $R_p$  to the circuit shown in figure 4a increases the current  $I_f$ , thereby shifting the frequency.

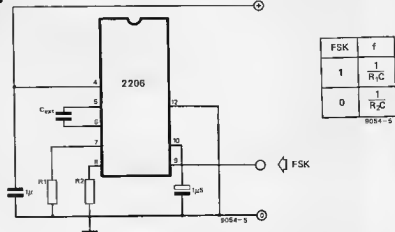
Figure 5. A generator for frequency shift keying (FSK).

Figure 6. A sawtooth/impulse generator.

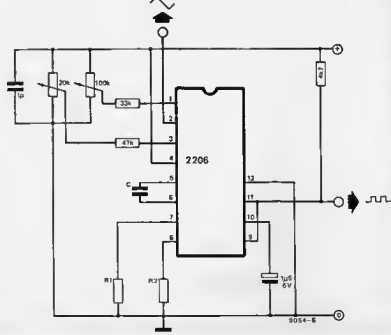
b



5



6



resistor. Thus the current  $I_f$  is proportional to the voltage  $V_f$ , and the frequency changes linearly with the voltage  $V_f$ .

Expressed in mathematical terms the relationship is as follows:

$$I_f = \frac{V_O - V_f}{R_f}$$

For the frequency:

$$f = \frac{I_f}{3C}$$

and after substitution for  $I_f$ :

$$f = \frac{V_O - V_f}{3C \cdot R_f} = \frac{3V - V_f}{3C \cdot R_f}$$

In this it is ESSENTIAL to note that the voltage  $V_f$  under no circumstances exceeds the voltage  $V_O$ , as the current flowing into the IC would lead to its destruction. If linearity is not essential, a diode can be added in series with the current output. The guide lines given in the functional description apply to the choice of the current  $I_f$  and the resistance  $R_f$  respectively.

A second wobulator is shown in figure 4b. It differs from the first proposal only by the additional resistance  $R_p$ , through which the current  $V_O/R_p = I_{Rp}$  flows continuously, and which has to be added to the current  $I_{Rf}$ . Therefore:

$$I_f = I_{Rf} + I_{Rp}$$

applies for  $I_f$ .

The derivation for the frequency results in:

$$f = \frac{I}{R_p \cdot C} \cdot \left[ 1 + \frac{R_p}{R_f} \cdot \left( 1 - \frac{V_f}{3} \right) \right]$$

### Frequency shift keying (FSK)

The term frequency shift keying means the transmission of digital data (e.g. symbol transmission) by two fixed frequencies representing logic '0' and '1'. This mode of operation is also possible with the IC 2206. As two interswitchable current outputs are available, two different frequency determining resistors can be inserted, thus producing two different fixed frequencies.

The change-over takes place by means of a digital input control (FSK input pin 9). The FSK input is TTL compatible. At voltages  $\geq 2V$  or open circuit input, the control current flows via  $R_1$ , and at voltages  $< 1V$  it flows via  $R_2$ . To make the relationships clear, a truth table is given in figure 5.

The circuitry associated with the signal processing section is analogous to figure 2 and depends on the required shape of the output signal.

### Amplitude modulation

The amplitude of the sine/triangular output changes linearly with the voltage at AM input pin 1 of the IC. This makes amplitude modulation of the signal possible. If the modulation voltage reaches the value  $V_b/2$ , then a phase shift of the output signal takes place, and at the same time the amplitude passes through zero. Thus the IC is also suitable for

phase modulation and amplitude modulation with suppressed carrier. This latter permits, for example, the generation of a stereo multiplex signal. The AM dynamic range is 55 dB max, corresponding to a modulation index of almost 1 ( $m = 0.996$ ). The AM input is of relatively high impedance, being at least 50 k $\Omega$ .

### Sawtooth and impulse generator

A link between the square output and the FSK input leads to an 'automatic' frequency shift keying. Two time constants differing from each other and determined by the resistors  $R_1$  and  $R_2$  control the positive and negative half cycles of the output signal. Pulse duration and duty cycle are adjustable between approx. 1% and 99% by means of  $R_1$  and  $R_2$ . The following equations define frequency and duty cycles:

$$f = \frac{2}{C} \cdot \left( \frac{1}{R_1 + R_2} \right)$$

$$\text{Duty Cycle: } \frac{R_1}{R_1 + R_2}$$

Table VI gives information about the 'quality' of the square output signal. The analogue output 2 gives an asymmetric triangular waveform ( $R_1 \neq R_2$ ), and at very low or high duty cycle ( $< 10\%$  or  $> 90\%$ ) the waveform becomes a sawtooth.

### Summary

The examples of application given are intended as a survey of the many possibilities resulting from the IC concept. Wherever there is a requirement for the production of signals of differing wave shape, at frequencies of up to several hundred kilohertz, it is worthwhile to consider whether the requirement could be met by the use of such an integrated component. This applies in particular to the hobby motivated electronic enthusiast because the combination of relatively complex circuit functions in one IC gives greater reliability to the complete circuit.

### Literature:

EXAR Data sheets and application reports.

# announcement

Our offices will be closed on Wednesday, Thursday and Friday 24 - 26 December, and on Newyear's day.

The Monday afternoon technical queries service will not be available on Monday 29 December.

# coming soon

**Front-end for TV sound** — this will convert the existing design (Elektor no. 2, p. 236) into an entirely independent receiver for tv sound.

**Automatic rhythm generators for the minidrum** — add-on units that will give several complete rhythms at the flick of a switch.

**TV tennis extensions** — additions to the basic game (Elektor 7, p. 1111) giving new games, noises and scoring.

**Audio preamplifier** — a low-cost, high performance preamplifier and control amplifier with 'remote control' capability.

**Digital wrist-watch** — using only one IC.

**Morse code units** — a reader, writer and automatic call generator.

# racing car control



For model car track enthusiasts a circuit is described here with which the speed of the racing cars can be controlled very accurately and proportionally and which in addition makes the car motor produce a realistic engine noise. The 'squeezer' belonging to the track remains part of the circuit.

In most cases the current for a racing track is supplied by a mains voltage unit fitted with a three-position switch, with which the maximum voltage, and hence the maximum speed of the car can be adjusted. Although it is likely that in practice only the fastest position will be used, it is in view of the younger racers that the circuit is so designed that (by means of a potentiometer) it can be used with all positions of the switch on the supply unit.

Actual 'acceleration' is done with an external potentiometer, for which the existing squeeze control can be used, although an ordinary 150  $\Omega$  carbon potentiometer will give better results. A handy tinkerer will undoubtedly find a way of also using an ordinary rotary potentiometer with the 'squeezer'! Figure 1 shows what the circuit described here might look like in practice.

## The diagram

The design of the race-track control comprises a monostable multivibrator which is triggered by an astable multi-

vibrator. The motor in the racing car is driven by the negative-going pulses of the monostable.

The width of these pulses is constant; the frequency (and hence the average voltage to the car motor) is governed by the setting of the astable. By means of the squeeze-potentiometer the frequency of the astable and indirectly the speed of the racing car is controlled. Figure 2 shows a circuit diagram.

T1 and T2 are used in the astable. This astable is emitter-coupled, which does slightly decrease temperature stability, but has the advantage that only one capacitor (C2) is needed.

The frequency of the multivibrator can be adjusted by R9 and P1. Here potentiometer P1 represents the squeeze control.

The square wave produced by the astable is differentiated by capacitor C3 and the base-emitter junction of T3. The negative-going pulses are clipped by D1. The remaining positive pulses arrive at the base of T3 thus triggering the monostable consisting of T3 and T4.

The motor of the racing car is included in the collector circuit of T3 and is driven by the negative pulses of the monostable which have a constant width. This is how the 'engine' sound is obtained. The frequency of this pulse train and consequently the speed of the motor is determined by the speed of the astable which as already explained can be varied by means of R9 and P1. D2 and C4 are fitted to suppress any back e.m.f. generated by the motor of the racing car.

Figure 3 shows the board and figure 4 the component layout of the race-track control. If the case of the existing supply unit is sufficiently large, the complete circuit can probably be built in. Should this not be possible, a separate box can be used as illustrated in figure 1.

Figure 5 shows a photograph of a completed board.

## Adjustment

The voltage supplied via the trafo may

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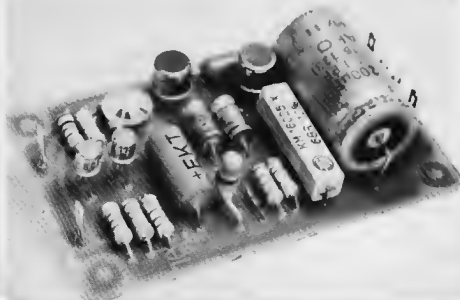


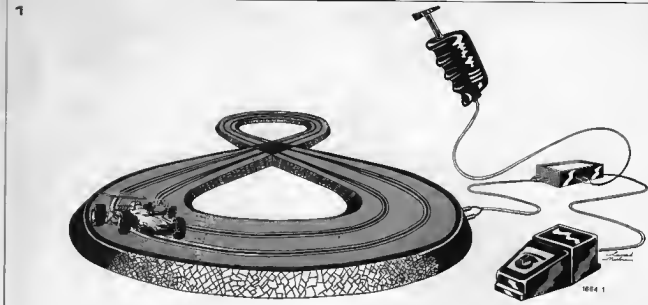
Figure 1. The controller in use, connected between the mains power unit and the race track.

Figure 2. The circuit diagram for race-track control. It is recommended to use a preset potentiometer for R9 (see text); P1 is the external squeeze control.

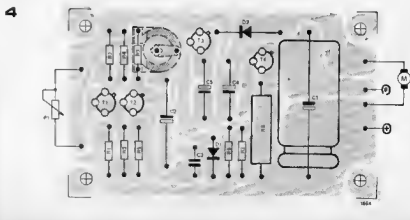
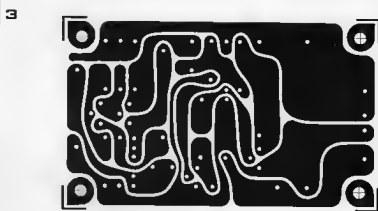
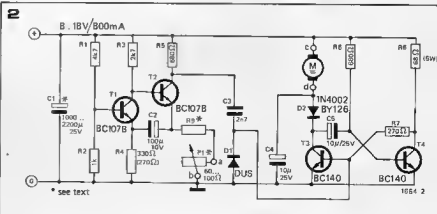
Figure 3. P.C. board for the race-track control.

Figure 4. Component layout of the board shown in figure 3.

Figure 5. A photograph of the board complete with components.



range from 8 to 18 volts. The maximum current consumption may be 800 mA. If a three-position mains supply is available, the value of R9 must, of course, be adapted to the various voltages. In the 'slowest' position R9 must be about 47  $\Omega$ , in the centre position about 56  $\Omega$ , and in the 'fastest' position about 82  $\Omega$ . It would be easy, of course, to use a 100  $\Omega$  adjustment potentiometer for R9; this possibility has been taken into account in the board layout. With the mains supply set in a particular position the best adjustment procedure is as follows: the squeeze control (P1) is first fully depressed and held in that position. Then R9 is so adjusted that the connected racing car runs at the maximum required speed. When the mains supply unit is set to another switch position, this adjustment must be repeated.



#### Parts list

##### Resistors:

- R1 = 4k7
- R2 = 1 k
- R3 = 2k7
- R4 = 330  $\Omega$  (270  $\Omega$ )
- R5, R6 = 680  $\Omega$
- R7 = 270  $\Omega$
- R8 = 68  $\Omega$
- R9 = see text

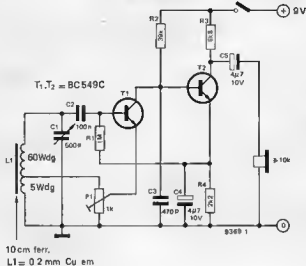
- P1 = existing 'squeezer' control  
60-100  $\Omega$  (or potentiometer 150  $\Omega$ )

##### Capacitors:

- C1 = 1000-2200  $\mu$ /25 V
- C2 = 100  $\mu$ /10 V
- C3 = 2n7
- C4, C5 = 10  $\mu$ /25 V

##### Semiconductors:

- T1, T2 = 8C107B
- T3, T4 = BC140
- D1 = DUS
- D2 = 1N4002, 8Y126



10cm ferr.  
L1 = 0.2 mm Cu em

## mini-MW

This receiver is so simple that very little outlay is required for its construction, and since only a small number of components are used it is ideal for miniaturisation, so that it will easily fit in a coat pocket. Nevertheless it gives good reception of local stations without the need for an external aerial or earth.

Operation of the receiver is exceedingly simple. Transistor T1 functions as an r.f. amplifier and detector with regenerative (positive) feedback. The degree of feedback, and hence the sensitivity of the receiver, can be controlled by P1. Although the output to the base of T1 is taken direct from the 'top' of the tuned circuit L1/C1, rather than via a coupling winding, the impedance presented by T1 is sufficient to ensure that

### Parts list

#### Resistors:

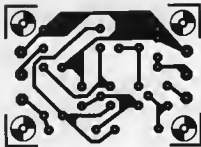
- R1 = 1 M
- R2 = 39 k
- R3 = 6k8
- R4 = 2k2
- P1 = 1 k potentiometer

#### Capacitors:

- C1 = 500 p (variable)
- C2 = 100 n
- C3 = 470 p
- C4, C5 = 4.7 μF

#### Miscellaneous:

- T1, T2 = BC 549C
- L1 = tuning coil (see text)



the resonant circuit is only slightly damped. Since the current gain of T1 reduces towards the high-frequency end of the band, whilst the input impedance increases, the gain of this stage remains fairly constant over the whole band, so that it is generally necessary to adjust P1 only once.

Detection takes place at the collector of T1 and the output impedance of this stage and C3 filter out the r.f. component of the rectified signal. T2 provides additional amplification of the a.f. signal to drive a crystal earpiece.

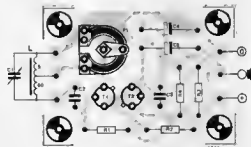
### Construction

A very compact p.c. board layout is shown for the receiver. L1 should be mounted as close as possible to the board to avoid instability problems. Those who wish to miniaturise the design still further can experiment by reducing the dimensions of the ferrite rod and increasing the number of turns to achieve the same inductance, though if L1 is made very small an external aerial may be necessary, which can be connected to the top end of L1 via a 4.7 pF capacitor.

The recommended dimensions for L1 are 65 turns of 0.2 mm (36 S.W.G.) enamelled copper wire on a 10 mm diameter 100 mm long ferrite rod, with the tap 5 turns from the 'earthy' end of the coil.

C1 can be a miniature (solid dielectric) 500 pF variable capacitor, or for reception of a single station only it may be replaced by a fixed capacitor of just less than the required value in parallel with a 4-60 pF trimmer. This will enable the size of the receiver to be further reduced.

Finally, the current consumption of the receiver is extremely low (approx. 1 mA) so that it will operate for several months on a PP3 battery.



R. ter Mijtlen

# battleships

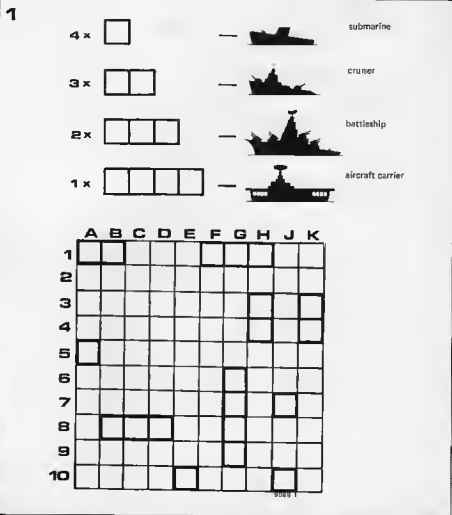
It would seem that fanatical electronic engineers will apply their skills to just about anything — the means justifying the end. This article describes an electronic version of the well known game of 'battleships'. The pencil and paper have been replaced by switches and LED's — under the control of a boxful of TTL. The proposal, as it stands, should provide plenty of fun — as well as a challenge to experienced battleshipsplayers to improve on the details!

The game is played by two participants, each of whom has a control panel. Each player also has a 10-by-10 cross-bar 'sea' in which he positions 10 ships by inserting jacks at the desired coordinates. The opponent can 'shell' any position by setting up a coordinate on switches before 'firing'. Any hit is displayed by LEDs. The players fire shells in turn, until one of them has lost all his ships.

### The original game

The original game of 'battleships' is

played with pencil entries on 10-by-10 sheets of squared paper. Each square is identified by a coordinate-pair, such as A-1. The ships are positioned by outlining the squares that they occupy. In one version of the game, each player has a 'fleet' consisting of: 4 submarines (one square each), 3 cruisers (two squares each), 2 battleships (3 squares in-line) and an aircraft carrier (4 squares in-line). Ships may be laid out horizontally or vertically, with an unoccupied zone of at least one square all around. (See





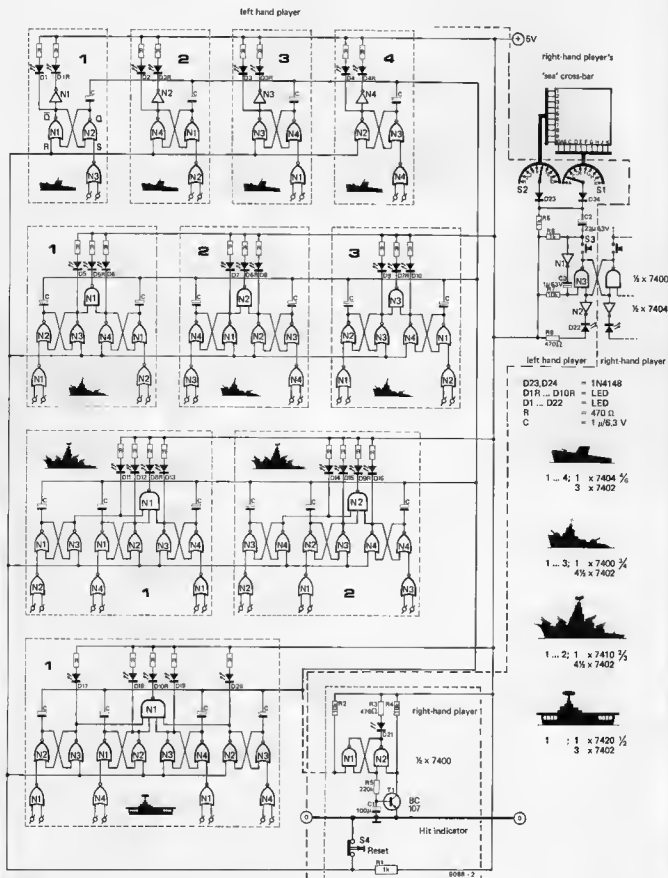


figure 1). Neither player knows (for obvious reasons!) where his opponent has positioned ships.

Suppose now that player 1 opens up by announcing 'shell on A-1'. The answer is 'hit'. (If the ship on A-1 had been a submarine, player 2 would have had to answer 'hit and sunk'.) Player 1 now only knows that the ship is not a submarine - just what it is and how it is laid out he will have to determine during later turns.

It is now player 2's turn to announce a coordinate and receive an answer. Player 1 has to guess the lie of the ship he has already hit. If he is lucky (or, at later stages of the game, clever enough), he will call 'shell on B-1' - and the answer will be 'hit and sunk'. He now knows that the ship was a cruiser and that there is no need to waste ammunition on the squares A-2, B-2, C-1 or C-2. The unoccupied-zone rule prevents his opponent from using them. The game continues shell-turn by shell-turn until one player has lost his entire fleet, so that his opponent is the winner.

**The electronic game**

As already mentioned the ship-positioning in the electronic form of the game is done by inserting jacks at the appropriate points on a 10-by-10 cross-bar. There are several mechanical approaches to this. What in fact happens is that the paired inputs of the logic gates that represent shipping are plugged into the crossed busbars of the 'sea'. One input goes to one of the vertical busbars A to K (the letter I is omitted), the other input to one of the horizontal busbars 1 to 10. The sea area occupied by each player is scanned by the coordinate-switches on his opponent's playingdesk.

**The logic circuitry**

Figure 2 gives the logic circuitry inside the left-hand playingdesk. Note that the 'sea area' drawn upper right is that mounted in the right-hand desk.

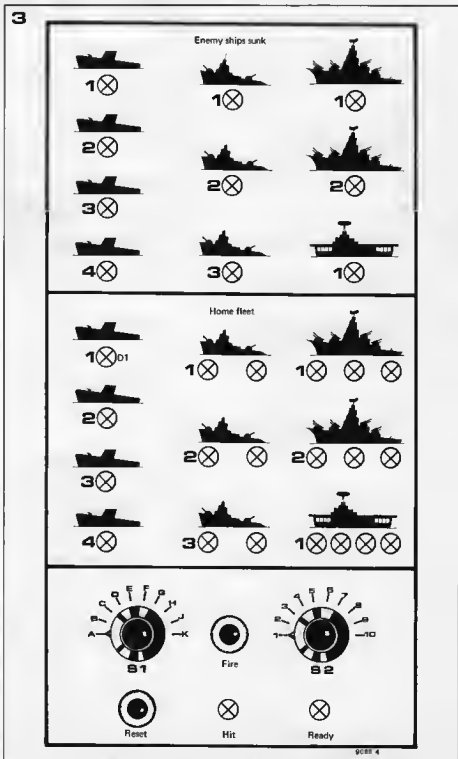
Suppose now that it is the left-hand player's turn, indicated by the glowing of LED 22 ('ready to fire'). The output of N3 is '0'. The player selects the square he wishes to shell by means of the coordinate switches (in the earlier example A and 1). When he presses the 'fire' button, any gate connected to the selected busbars will be pulled down to '0' via C2. The capacitor will prevent an unsporting player from sweeping his opponent's sea area by rotating the coordinate switches while holding down the 'fire' button.

When S3 was pushed the input of N1 became '1'. The release of this button causes N1 output to go to '0', so that one of the inputs of N3 is momentarily pulled down via C3. The set-reset flip-flop will now change state. The output of N3 is '1', so that a second push on the 'fire' button has no effect. A glowing LED on the right-hand playing desk indicates to the other player that it is now his turn.

Figure 2. Circuit diagram of one half of the complete game, in this case the part that is installed mainly in the left-hand playing desk. The parts that inform the opponent of successful 'hits' and the 'ships sunk', the reset button and the 'sea' cross-bar on which he lays out his fleet, are installed (as given in the figure) in the right-hand playing desk.

Figure 3. A possible layout for the controls and indicators on one playing desk, designed to provide a good survey of operations. The 'sea' cross-bar (that could for instance be a jack-field) is not shown.

In the example given above the shell on A-1 was a 'hit'. What happened in the circuit when the left-hand player pushed his firing button? It is convenient to trace the 'hit' in the circuit of submarine 1, to the upper left of figure 2. The two NOR gates N1 and N2 together form a set-reset flipflop. The reset input R is connected via S4 (push to reset) to the negative rail, so that it is at '0' level. If the output Q of N1 is at '0', the flip-flop will change state when a '1' arrives at the set-input S. This will occur whenever both inputs of N3 go to '0' - which is precisely what happens when these inputs are momentarily grounded via the sea-busbars and the opponent's coordinate switches and firing button. As long as Q is '0' LED D1 will glow



and LED D1R will be dark. D1 indicates the unsunk member of the home fleet - D1R would indicate to the opponent that he had sunk the submarine. This indication is given when the flipflop N1/N2 changes state, causing DIR to glow and D1 to extinguish.

Each player clearly needs four of these circuits to represent his submarines. The other ships are represented by similar circuits, having one SR-flipflop for each square the ship occupies. When all the LED's associated with any ship have extinguished, the NAND gate that monitors the wellbeing of the ship concerned will indicate to the opponent that this target has been sunk. Only then does this player know what type of ship he has sunk; up to then he was only informed by a 'hit' indicator that illuminates for a few seconds after each successful push on the firing button. The 'hit' indicator consists of a SR-flipflop, transistor T1 and LED 21. The input of N1 is normally at '1', because this input is connected via R2 to the positive rail. Whenever a '0' impulse arrives from a Q output of one of the shipflips (sorry!) the SR-flipflop in the 'hit' indicator will switch, causing LED 21 to glow. The output of N1 will go to '1', so that C1 will charge through R5. After about 3 seconds this results in T1 starting to conduct, thereby pulling down the N2 input. This resets the flipflop, extinguishing LED 21 until the next hit is made. Each player has one 'hit' indicator, which is connected to the Q outputs associated with the enemy ships.

Before a game can start it is necessary to reset all the shipflips. This is done by pressing the push-to-break button S4. To make it unattractive to a player to accidentally-on-purpose use the reset facility during the actual game, it is arranged that the left-hand player's fleet is reset from the right-hand playing desk (and vice-versa). A player who presses the reset button on his desk, during the game, puts himself at a great disadvantage - since he cancels the record of all his own successful hits.

### The display

Figure 3 shows a possible layout for either playing desk, intended to provide a good survey of operations during the game. The upper section indicates the damage done to the enemy fleet - which ships have been sunk. The drive to the 10 LED's in this section comes from the opponent's desk. Figure 3 shows the LED's D1L through D10L, corresponding to D1R through D10R on the circuit diagram of the left-hand desk.

The centre section provides full information on all hits placed on ships of the home fleet. A ship is sunk when all the LED's associated with its display are glowing.

## LED FM scale

With home-made FM-tuners, the design and construction of the tuning scale often causes much brain racking. A mechanical solution is excluded from the very beginning because of the constructional difficulties. In many cases the only option left is a display of the tuning voltage (in the case of varicap tuners) by means of a voltmeter with its scale calibrated in frequency.

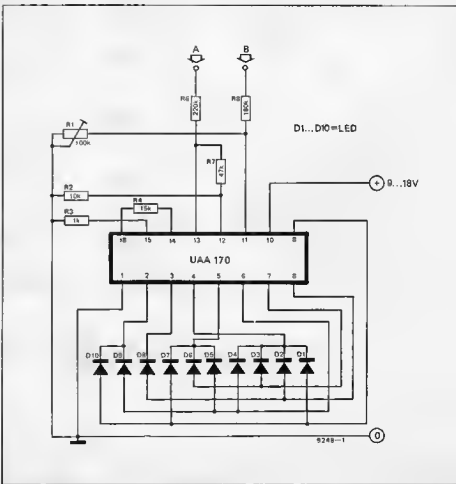
A Siemens IC type UAA 170, together with a few external components, provides an electronic scale. The table shows the relationship between tuning voltage, frequency, and LED read-out. Only one LED is lit at any time.

The maximum available tuning voltage is connected to input A. This voltage must be kept constant as a reference voltage. The variable tuning voltage is fed to input B as control voltage. The resistance ratios  $R_6$  and  $R_7$  over  $R_7$  and  $R_2$  determine the voltage difference required for each step of the LED display. The circuit values are chosen such that the voltage difference corresponds to a frequency change of 2 MHz.

The preset potentiometer R1 is used for scale adjustment. While R1 is being adjusted, the tuning voltage must be checked with a voltmeter. The adjustment is correct if the corresponding LEDs light up at the voltages given in the table.

Table

Tuning Voltage	Tuning Range	LED
< 4	< 88	D1
4	88	D2
5	90	D3
6	92	D4
7	94	D5
8	96	D6
10	98	D7
12	100	D8
15	102	D9
18	104	D10



# alarm

An alarm which gives its alarm signal at certain repetitive times, does not need to know what the actual time is. It is sufficient if it can measure the time between the alarm time points (for instance 24 hours). An electronic alarm which operates according to this principle, is less expensive than a digital clock with added alarm. The circuit described here is an independent unit, but it can be combined with an electronic or electromechanical clock. With a switch, alarm intervals of 6, 12 or 24 hours can be set. Thus the apparatus can also be used as an aquarium time switch, among other applications. The switching off of the alarm signal is carried out by hand, or occurs automatically after 10 minutes. In addition to the alarm signal, second, 10 minute, and hour impulses are also available.

The circuit contains four CMOS IC's type MC 14566 (Motorola). These are available in versions suffixed AL, CL and CP. The letters A and C indicate the temperature range and the maximum permissible supply voltage. The L-types have ceramic packages, whereas the P-type is the plastic version. In the 24h-alarm, all types are usable.

Figure 1 shows the block diagram of the IC. The circuit contains a  $\div 10$  counter (block A) and a programmable  $\div 5$  or  $\div 6$  counter (block B). Both dividers are preceded by pulse shapers (blocks C and D). The inputs react to the negative-going edges of the clock pulses. Both dividers can be simultaneously reset by means of the reset input (pin 2). Apart from this the IC contains a monostable which can be triggered positively (at pin 9) or negatively (at pin 7). The

monostable is primarily intended as a pulse shaper for the reset- or timing-signal.

With pin 11 of the IC connected to  $+V_b$ , block B functions as a  $\div 5$  counter and with pin 11 connected to supply common, one obtains a  $\div 6$  counter. By connecting the two dividers of the IC in cascade, one can therefore choose a division ratio of 1:50 or 1:60.

A  $\div 50$  counter produces 1 Hz pulses if it is fed with 50 Hz pulses obtained from the mains. This divider can therefore also be used as a time base for six digit digital clocks. In the 1:60 division circuit the IC is used as a second or minute counter.

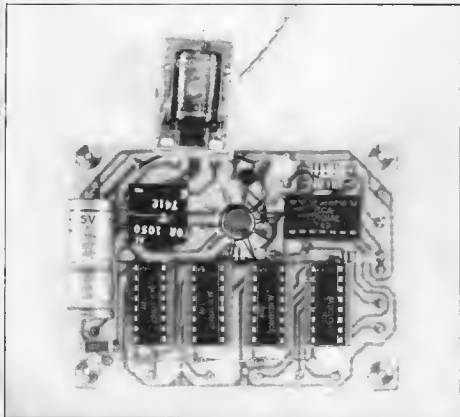
The outputs of the two dividers provide a BCD-coded signal. By means of BCD-decoders, displays can be controlled, so

that by this means a digital clock can be produced.

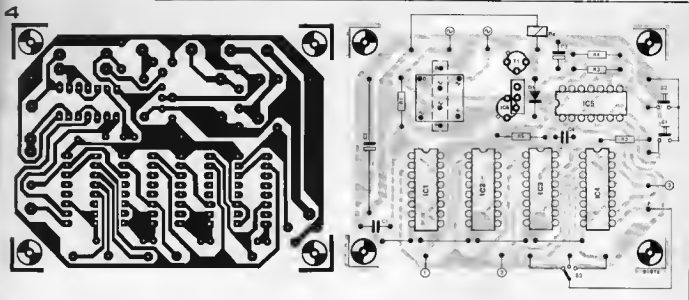
In the case of the 'alarm only' decoder and displays are superfluous. When the alarm is in operation, after a predetermined count is reached automatic reset occurs, and at the same time the alarm is restarted. The reset signal thus occurs at regular intervals, and it can therefore be used to trigger the alarm signal. This is initiated by a flipflop which is triggered by the reset pulse. The alarm signal then continues, until a manual or automatic reset impulse arrives at the flipflop. Alarm time intervals of 6, 12 or 24 hours can be set with a selector switch.

## The circuit

In figure 2 the complete circuit is given with the exception of the power supply. The alarm contains four IC's, MC 14566. The first IC (IC1) divides the 50 Hz signal, which is fed to its input via the RC-filter R1/C1, down to 1 Hz. At its output there are second pulses. This output is taken to the edge of the printed circuit board, and is easily accessible (connection 1 on the printed circuit board). From this point digital clocks without a time base can be provided with a 1 Hz timing signal. The 1:50 divider is followed by two 1:60 dividers. Hour pulses are available at the output of the second divider (IC3). This output is brought out, as is also a further output which gives 10-minute pulses. If required the 10-minute output can be used to switch off the alarm note after 10 minutes. For this purpose, this output (connection 2 on the printed circuit board) is connected via a diode to the input of gate N4, (pin 8), the cathode being connected to the divider output. An hourly chime can be connected, for instance, to the hour-output (connection 3 on the printed circuit). The output is almost permanently connected to the input of C4. This has division ratios 1:6, 1:12 and 1:24 which are selected by switch S3. The alarm sounds, therefore, every six, twelve or twenty-







the first alarm period is started. If one wishes to connect the alarm to a digital clock, then for the alarm time to agree with the clock display it is essential to operate both devices from the same time base.

#### The power supply

Figure 3 shows a stabilised power supply which can be mounted on the alarm printed circuit board.

The power supply uses an integrated 5 V regulator (IC6), and one can choose between types TBA 625A and L 129. To prevent excessive loading of the regulator, the relay is connected to the unregulated voltage (+10 V). At the output of the mains supply there is an electrolytic capacitor to suppress any oscillatory tendency. It is best to use a tantalum electrolytic capacitor in this position because of its low self-inductance.

The printed circuit board is laid out in such a manner, that two alternative bridge rectifiers can be used, the TBR 1050 and the BY 164.

#### Parts list for figures 2 and 3.

##### Resistors:

R1 = 100 k  
R2, R4, R5 = 1 M  
R3 = 27 k

##### Capacitors:

C1 = 47 n  
C2 = 470  $\mu$ /25 V  
C3 = 10  $\mu$ /10 V (Tantalum)  
C4 = 100 p

##### Semiconductors:

R1 = TUN  
D1 = DUS  
B1 = TBR 1050 or BY 164  
IC1 to IC4 = MC 14566  
IC5 = CD 4011  
IC6 = L129 or TBA625A

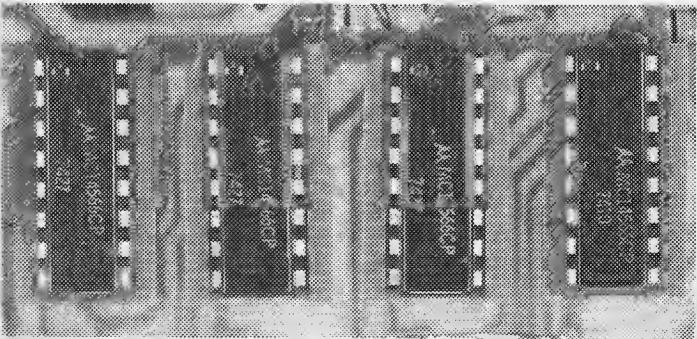
##### Miscellaneous:

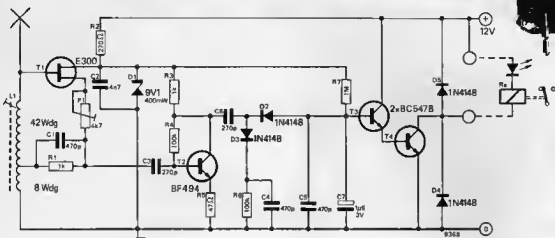
Re = Relay 10 V, min. 100  $\Omega$   
S1, S2 = key 1 x ON  
S3 = switch single-pole 3 way

#### The printed circuit board

The printed circuit board (figure 4) contains the complete alarm circuit, including the power supply. From the component layout-out (figure 5) it can readily be seen that the printed circuit board is suitable for two different types of bridge rectifier, or regulator IC's respectively.

When mounting the components it is best to start with the power supply. When this is completed, one can check whether the stabilised voltage of +5 V is present. If this check is satisfactory, then the rest of the circuit can be completed. It should be noted that although the MOS-IC's are already protected by internal diodes, care should nevertheless be taken in handling these components.





L: 0.2 mm Cu em  
6 mm  $\phi$  HF

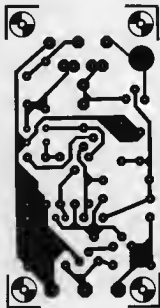
## capacity relay

The capacity relay consists basically of an oscillator, a detector and a relay driver stage.

A length of wire is connected to a 'sensitive' point in the oscillator circuit. Any object in the vicinity of this wire will load and detune the oscillator; the extent to which this occurs depends on the size of the object, how 'lossy' it is, how close it is to the wire, and, of course, how stable the oscillator is. A large salt water container, such as the human body, is particularly effective. The preset potentiometer P1 is used to

so adjust the oscillator stage (T1) that it will only just start to oscillate. This adjustment should be made with the 'aerial' connected, so it becomes a question of trial and error: after each readjustment one must step back a few paces to see whether the oscillator will start again.

The oscillator drives an amplifier and detector stage (T2, D2, D3). As long as the oscillator is running, the base of T3 is driven negative. If a sufficiently large object approaches the aerial, however, the negative drive to T3 disappears. R7



### Parts list:

#### Resistors:

R1, R3 = 1k  
R2 = 270  
R4, R6 = 100k  
R5 = 47  
R7 = 1M  
R8 = 4k7

#### Capacitors:

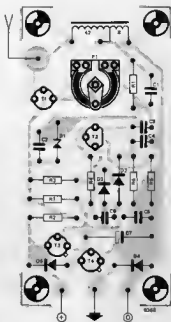
C1, C4, C5 = 470p  
C2 = 4n7  
C3, C6 = 270p  
C7 = 47n ... 10  $\mu$ /3V

#### Semiconductors.

T1 = E300  
T2 = BF494  
T3, T4 = BC547B  
D1 = 9.1 V zener (400 mW)  
D2 ... D5 = 1N4148

#### Misc.:

L1 = 50 turns 0.2 mm (36 SWG) Cu em on HF core  
Relay: 10 V 50 mA max.



santatronics

then supplies sufficient current to turn on the Darlington configuration (T3, T4), so that the relay will attract. The relay current should not be more than 50 mA. C7 determines the speed with which the circuit reacts.

When properly adjusted, the circuit should detect a person within three feet of the aerial. The sensitivity in-

creases if a longer wire is used.

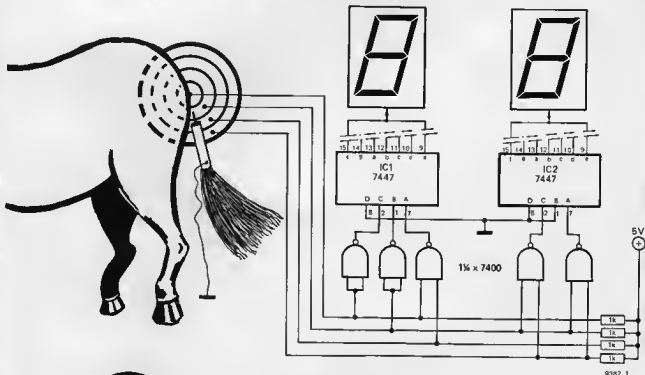
The coil consists of 50 turns of 0.2 mm enamelled copper wire (36 SWG) on a high frequency type core.

## Pin the tail on the donkey

This is an electronic version of an aged children's party game. The game is extremely simple. A large picture of a donkey (less tail) is pinned up on the wall. The contestant is blindfolded and provided with a 'tail' which must be pinned in the appropriate location on the donkey's posterior. The area around the tail location on the donkey is marked off with concentric circles denoting scores; 50 for 'bull's-eye' (or should we say 'donkey's...?!), 25 for first circle and so on.

The electronic version provides automatic indication of the score. Operation is extremely simple. The 'target' is made up of four concentric circles of aluminium foil glued to the back of the card on which is drawn the donkey. An output lead is taken from each circle to one of the inputs of a decoder made up of 2-input NAND-gates. This decodes the 4 outputs into BCD to drive the 7447 seven segment decoder-drivers,

which drive the display. The four codes hardwired into the decoder correspond to scores 50, 25, 10 and 5. Normally, all inputs to the decoder are high and the display is zero. When the tail (an earthed probe) is pinned to the donkey one of the inputs to the decoder is grounded and the appropriate score is displayed. If the tail is outside the outer circle the score remains at zero. If the tail is pinned in the gap between two circles then the contestant takes his turn again.



9252 1



# simple mw receiver

The quest for 'superhet' sensitivity and selectivity dates from the time when a valve was an expensive item, and the licence fee depended on the number of valves in the set! The simple construction and lack of alignment of the 'superregen' are of course achieved at the cost of selectivity and stability.

The circuit is a fairly classic design, but the performance is much improved due to the use of modern components in a well thought-out circuit. Using a ferrite aerial good reception of local stations is possible, and use of a longer ferrite rod results in an even better performance. For long distance reception an external aerial and earth can be used.

The design also provides the basis for a simple short wave receiver by winding the aerial coil to suit the required frequency range.

## The circuit

The tuned circuit consists of L1 and C1. No coupling winding is used on this coil, as this can often pick up interference from powerful short wave transmitters. Instead the output is taken direct from the 'live' end of the coil, and the use of a (high input impedance) source follower T1 ensures that the tuned circuit is not unduly damped. Positive feedback is taken from the source of T1 via C2 to a tapping on the coil, and is adjustable by P1. The highest sensitivity occurs just before the feedback is sufficient to cause the onset of oscillation.

T3 provides substantial r.f. gain with T2 as its constant current collector load and also functions as detector. Rectification of the r.f. signal takes place at the collector of T3 rather than the base, as this offers a lower detector threshold. The a.f. amplifier embodies one or two unusual design features. The a.f. amplifiers of common commercial receivers often have such a high quiescent current that battery life is severely curtailed. In this circuit the Darlington output stage has zero quiescent current, which, in addition to reducing the power consumption of the receiver, also eliminates one adjustment potentiometer. The

quiescent current of the whole receiver is only 1 mA, rising to 50 mA at full output. This is not achieved without some compromise, which is of course the inevitable crossover distortion associated with pure class B output stages. Fortunately most of this distortion appears at high audio frequencies and, since the bandwidth of AM transmissions is limited anyway, it is possible to roll off the h.f. response of the amplifier, reducing the distortion without noticeably affecting the frequency range of the signal.

This is provided by a filter in the feedback loop comprising R12-R14 and C10-C12, which gives a sharp roll-off in the amplifier gain above about 6 kHz. To ensure amplifier stability with varying loads R18 and C14 are connected across the output. The set can thus be used equally well with a high (or low) impedance earphone instead of the loudspeaker. The maximum output with an 8  $\Omega$  speaker is 250 mW and, provided the speaker is reasonably efficient, this will provide adequate volume for an average room.

## Construction

Figure 2 gives a printed circuit board and component layout for the set, which considerably simplifies the assembly. Care should be taken, however, to keep the connections to C1, L1 and P1 as short as possible, as otherwise the set may be unduly sensitive to hand capacitance and will be difficult to keep stable. For this reason also a long insulated spindle is recommended for P1.

The aerial coil on a 10 mm diameter ferrite rod 100 mm long consists of 70 turns close wound enamelled copper wire 0.3 to 0.5 mm diameter (31 to 25 S.W.G.) tapped 20 turns from the earth end. An external aerial can be connected to point A via a 4.7 pF capacitor C<sub>x</sub>, or by a 4-20 pF trimmer. Pin configurations for the transistors used are given in figure 1. It may be possible to use alternative types for T1 and T2, and three equivalents are listed for T3. There are numerous alternatives to T4

The alignment of superhet receivers presents problems that may deter some enthusiasts from undertaking their construction. A simple MW superregenerative receiver presents no such difficulties, and the results obtained can be quite satisfactory when one has achieved the necessary 'touch' for the reaction control. The circuit described here performs quite favourably compared with a superhet, especially if an external aerial is used.

## Parts list.

### Resistors:

R1 = 1 k  
R2, R14 = 4k7  
R3 = 10 M  
R4 = 3M9  
R5 = 22 k  
R6, R10 = 100 k  
R7, R19 = 10 k  
R8 = 1 M  
R9 = 68 k  
R11, R15 = 47 k  
R12, R13 = 470  $\Omega$   
R16, R17 = 2.2  $\Omega$   
R18 = 10  $\Omega$   
P1 = 4k7 lin.  
P2 = 470 k log.

### Semiconductors:

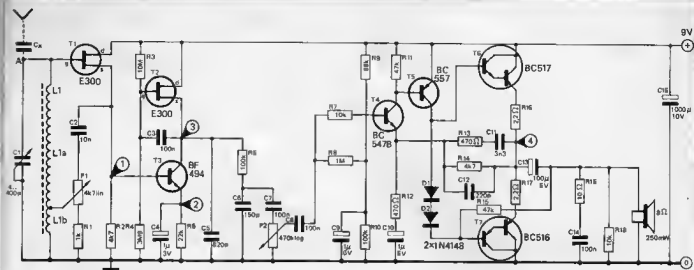
T1, T2 = E 300  
T3 = BF 494/BF 495 (BF 194/BF 195)  
T4 = BC 547B  
T5 = BC 557  
T6 = BC 517  
T7 = BC 518  
O1, O2 = 1N4148

### Capacitors:

C1 = 4...365 p or 4...500 p  
C2 = 10 n (ceramic)  
C3, C7, C8, C14 = 100 n  
C4 = 1  $\mu$ /3 V  
C5 = 820 p (ceramic)  
C6 = 150 p (ceramic)  
C9, C10 = 1  $\mu$ /6 V  
C11 = 3n3  
C12 = 220 p  
C13 = 100  $\mu$ /6 V  
C15 = 1000  $\mu$ /10 V  
C<sub>x</sub> = see text

### Misc.:

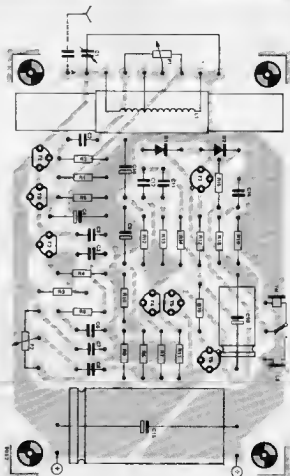
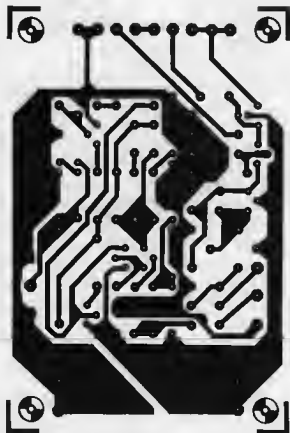
L1 = see text



L1a=50Wdg 0.3mm }  
 L1b=20Wdg 0.3mm } 10mm x10cm



Bottom views



and T5, but the types specified for T6 and T7 must be used as there are no alternatives. These Darlingtons offer the advantage of high current gain (typically 30000) in a single can.

### Test points

Four test point voltages are given in figure 1. The minimum voltages at these points should be:

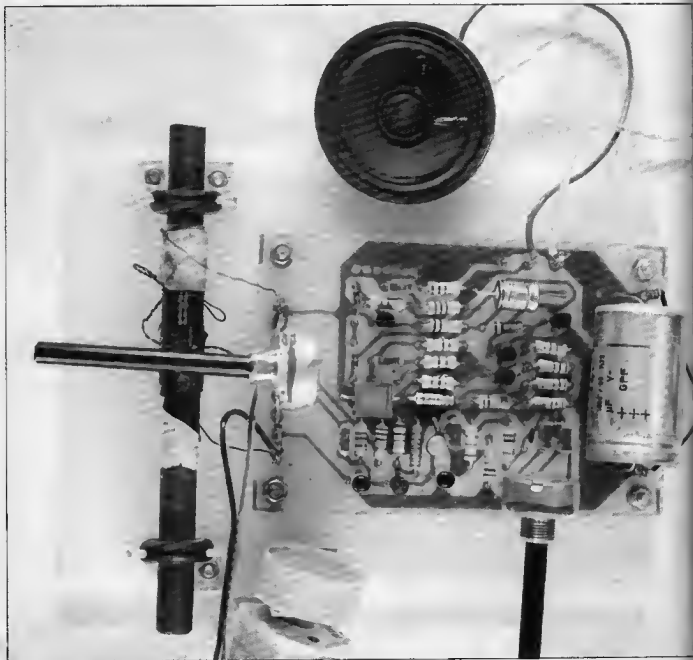
- voltage at point 1: 1 V
- voltage at point 2: 0.5 V
- voltage at point 3: 1.5 V
- voltage at point 4: 4.5 V

### Operation of the receiver

When tuning the receiver the reaction control P1 must be carefully adjusted. It is best to turn up P1 until the receiver oscillates. The tuning capacitor may now be adjusted to tune the set, and when a transmitter is being received the level of the oscillation will change. P1 can then be backed off until the oscillation just ceases. If desired P1 can be replaced by a 4k7 preset, in series with a

1 k potentiometer for the fine reaction control. With the 1 k pot, in its central position the preset can be adjusted so that the receiver is on the verge of oscillation. Adjustment of the 1 k will then take it into or out of oscillation. The best long-distance reception is achieved by using an external aerial and earth. Some improvement can also be obtained, whilst still retaining the directional properties of a ferrite aerial, if a larger ferrite rod is used for L1. Alternatively, two small rods can be mounted side by side and sellotaped together, and the coil wound over the combined rods. If either of these methods is used the number of turns on the coil must be reduced to achieve the same inductance. For instance, when using two 10 mm diameter rods 55 to 60 turns was found to be the optimum, with the tapping 15 to 20 turns from the earthy end of the coil. The receiver will also operate on the short-wave bands using air cored coils. On the prototype L1 was replaced by a coil of about 80 mm diameter, having

6 turns 1 mm diameter wire (19 S.W.G.) with the tap 1 turn from the earthy end. These modifications resulted in the reception of several transmitters in the range 3 - 13 MHz, and other wavebands could be obtained by further experimentation.

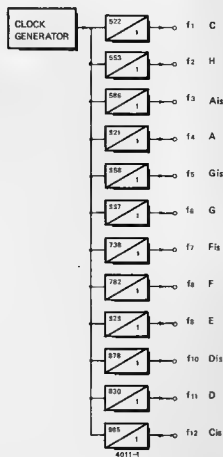




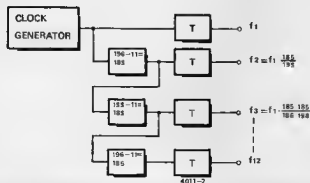
# digital master oscillator [1]

The use of frequency dividers in electronic organs has been known for many years. The usual procedure is to use divide-by-two stages to divide down the notes of the highest octave to obtain the lower octaves. Until recently it was normal practice to use twelve independent master oscillators for the twelve notes of the top octave. The disadvantages of this approach are that twelve oscillators have to be adjusted when tuning the organ, a procedure that requires a skilled ear. Since the oscillators are independent, supply voltage variations, temperature changes and component ageing can all make the organ go out of tune. A digital master oscillator, in which the notes of the top octave are derived from, and are all locked to, a single clock generator, suffers from no such disadvantages. Tuning is accomplished simply by altering the clock frequency, and if the clock frequency does drift this will not be noticed when playing solo, since the relative pitch of the notes will remain the same.

1



2



There are various digital methods of tone generation, which all have their peculiar advantages and disadvantages, and the most interesting of these will be discussed in the following text.

A semitone interval in the tempered tonic scale is equal to  $\sqrt[12]{2}$  or 1.0594631... That is to say the frequency of any note is 1.0594631 times the frequency of the note a semitone below it. The most obvious method of achieving this frequency ratio would be to divide down the output of a clock generator, using a separate divider chain for each of the twelve notes. This method is shown in figure 1. The accuracy of each note depends on the length of the divider chain used, and with the division ratios shown a three-decade counter is required for each note. The use of long divider chains requires a high clock frequency, and the component cost is high.

A second approach to the problem uses the fraction  $\frac{196}{185}$ , which is a good approximation to  $\sqrt[12]{2}$ .

The principle of this system is shown in figure 2. The output of the clock generator is fed to a circuit that passes 185 out of every 196 clock pulses and inhibits the remaining eleven. The output of this circuit is fed to a similar circuit. Thus each output produces 185 output pulses for 196 input pulses.

If the average frequency of any output was measured using a frequency meter with a long gate period it is obvious that it would be  $\frac{185}{196}$  of the frequency of the preceding output. However, though the long-term average frequency is correct, the output waveform is very irregular due to the fact that there is a gap where the 11 pulses are missing. If the outputs

A practical realisation of a  $\frac{185}{196}$  divider is given in figure 3. Here two 7493 4-bit binary counters are connected as divide-by-14 counters and cascaded to make a divide-by-196 counter (since 196 conveniently equals  $14^2$ ). Initially flip-flop IC3 is reset so clock pulses cannot pass through AND-gate A4. The 7493's count the clock pulses, and on the 11th clock pulse a pulse from the output of A3 clocks the flip-flop.

The Q output of the flip-flop goes high, allowing clock pulses through A4. On the 196th clock pulse the output of N1 goes low, resetting the flip-flop, and the cycle repeats.

The accuracy of the semitone interval achieved by this method is high, but the long divider chains required to suppress jitter increase the cost.

At this point it is worth looking at a commercially available IC that makes

## 3

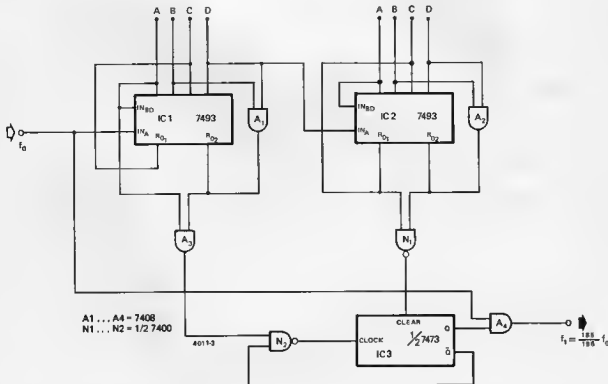


Figure 1. Master oscillator system in which each note is divided down individually from a common clock generator.

Figure 2. System which makes use of the division ratio  $\frac{196}{185}$  as an approximation to  $\sqrt[12]{2}$  by inhibiting 11 out of every 196 pulses. The output dividers (blocks T) reduce jitter.

Figure 3. Practical realisation of a  $\frac{185}{196}$  divider. Only 185 of every 196 input pulses are allowed through gate A4 to the output.

of the  $\frac{185}{196}$  dividers were used directly this would give rise to an audible effect known as 'jitter'. Fortunately jitter can be reduced by taking the divider outputs through a series of binary (divide-by-two) stages, when the mark-space ratio of the waveform will tend to unity (a timing diagram will demonstrate this). This is the function of blocks 'T' in figure 2. Since the number of divider stages required to reduce jitter to a reasonable level is about 7, this means that the clock frequency must be  $2^7$  times the highest note.

use of this principle. This is the Intermetall SAH190, an internal block diagram of which is given in figure 4. Since jitter becomes worse the more  $\sqrt[12]{2}$  stages are cascaded, the number of subsequent divide-by-two stages required for jitter suppression depends on the jitter at the output of the final  $\sqrt[12]{2}$  stage. Intermetall overcame this difficulty by not using 12 cascaded  $\sqrt[12]{2}$  dividers, but by using four cascaded three-semitone or  $\sqrt[3]{2}$  dividers (represented by the fraction  $\frac{44}{37}$ ) and a one-semitone ( $\sqrt[2]{2}$ ) and two-semitone ( $\sqrt[4]{2}$ ) divider, represented by the

4

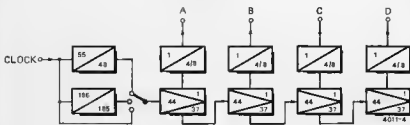


Figure 4. Block diagram of the Intermetal SAH 190 IC. This makes use of the principles of figures 2 and 3, but the basic interval used is 3 semitones, for reasons explained in the text.

Figure 5. A complete master oscillator using 3 SAH 190 ICs.

Figure 6. Showing the timing diagram for frequency synthesis by the addition of partial frequencies. The symmetrical outputs of the binary dividers must have their mark-space ratios altered so that the pulse trains may be interleaved without pulses ever coinciding.

Figure 7. Block diagram of a master oscillator using frequency synthesis by the addition of partial frequencies.

5

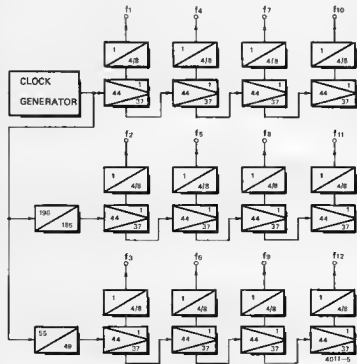
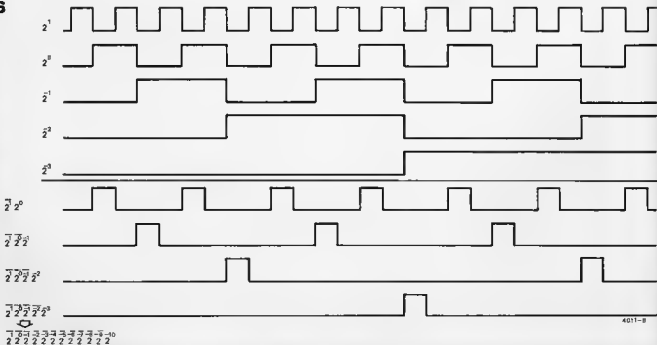


Table 1. Showing the frequency ratios of notes in the octava in decimal and binary.

	2 <sup>1</sup>	2 <sup>0</sup>	2 <sup>-1</sup>	2 <sup>-2</sup>	2 <sup>-3</sup>	2 <sup>-4</sup>	2 <sup>-5</sup>	2 <sup>-6</sup>	2 <sup>-7</sup>	2 <sup>-8</sup>	2 <sup>-9</sup>	2 <sup>-10</sup>
c <sup>6</sup>	1	0	0	0	0	0	0	0	0	0	0	0
b <sup>#</sup>	1	1	1	0	0	0	1	1	0	1	0	0
a <sup>#</sup>	1	1	0	0	1	0	0	0	0	0	0	1
a <sup>##</sup>	1	1	0	1	0	1	1	0	1	0	1	0
g <sup>#</sup>	1	1	0	0	1	0	1	1	0	1	0	1
g <sup>##</sup>	1	0	1	1	1	1	1	1	1	1	1	0
f <sup>#</sup>	1	0	1	1	0	1	0	1	0	0	0	0
f	1	0	1	0	1	0	1	0	1	1	1	1
e <sup>#</sup>	1	0	1	0	0	0	0	1	0	1	0	1
d <sup>#</sup>	1	0	0	1	1	0	0	0	0	0	0	1
d <sup>##</sup>	1	0	0	0	1	1	1	1	1	0	1	0
c <sup>#</sup>	1	0	0	0	0	1	1	1	1	0	1	0
c	1	0	0	0	0	0	0	0	0	0	0	0

6



fractions  $\frac{196}{185}$  and  $\frac{55}{49}$  respectively.

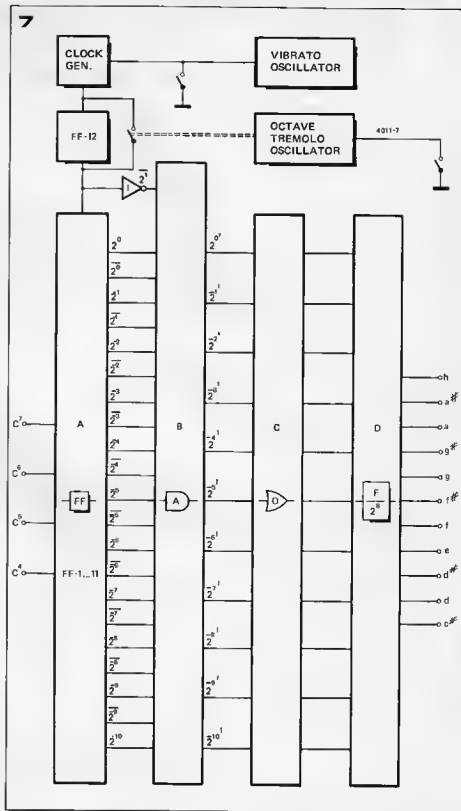
A complete master oscillator using three of these ICs is shown in figure 5. The first IC receives its input direct from the clock generator. The second receives its input from the  $\sqrt[2]{2}$  divider of the first IC, and the third receives its input from the  $\sqrt[4]{2}$  divider of the first IC. The first IC thus produces 4 notes with a three-semitone interval between each note. The outputs of the second IC are also three semitones apart, but each is a semitone below the corresponding output of the first IC. Similarly the outputs of the third IC are all two semitones below the corresponding output of the first IC. Thus, if say C is obtained from output  $f_1$  of the first IC, then B will be obtained from the  $f_3$  output of the second IC, and B<sup>b</sup> will be obtained from the  $f_3$  output of the third IC and so on. In this way the use of 12 cascaded  $\sqrt[2]{2}$  dividers is avoided, thus simplifying the anti-jitter circuitry, which the IC also contains.

The fourth system involves the expression of  $\sqrt[2]{2}$  as a power series of negative powers of two. The equation  $\sqrt[2]{2} = 2^0 + \frac{2^{-1} + 2^{-4} + 2^{-5} + 2^{-7} + 2^{-10}}{10}$

represents  $\sqrt[2]{2}$  with an error of only  $2 \cdot 10^{-7}$ , and gives  $\sqrt[2]{2}$  as 1.059462890625. This seems rather an elegant solution, but unfortunately, since powers up to  $2^{-10}$  are required, this means that 10 divide-by-two stages are required for each  $\sqrt[2]{2}$  divider. In addition the outputs of these dividers must be OR'd together. Furthermore the mark-space ratios of the individual pulse trains must be modified so that no pulses coincide, as all must be counted separately after passing through the OR-gate.

The fifth and final system to be described also makes use of combinations of powers of two, but for direct synthesis of the required frequencies rather than for obtaining a chosen division ratio. Any frequency can be produced by addition of pulse trains of partial frequencies. The practical aspects are, of course, more complicated than this simple statement suggests. Frequencies whose ratios correspond to intervals in the tempered tonic scale cannot be synthesised precisely, since the semitone interval  $\sqrt[2]{2}$  is an irrational number. They can, however, be approached as closely as required by making the lowest partial frequency element very small compared to the largest one in any given frequency. Since in this case the partial frequencies will be obtained by dividing down a clock frequency in a series of binary (divide-by-two) stages, the achievable accuracy will be one part in  $2^n$ , where n is the number of divider stages.

From musical publications it is evident that the maximum permissible frequency error that will remain undetected is about 0.05% or one part in 2000. The use of 11 binary divider



stages will give an accuracy of one part in  $2^{11}$  or 2048.

Jitter also occurs when adding partial frequencies, and must be removed by divider chains on the output of the synthesiser. 8 binary divider stages are required to produce a sufficiently jitter-free output, so to obtain C<sup>5</sup> (4186 Hz) the output frequency of the synthesiser must be around 2 MHz.

To see how the individual notes are synthesised it is necessary to refer to figure 6 and table 1. Table 1 expresses the twelve notes of the octave as frequency ratios. Thus if C<sup>5</sup> is taken as 1,000... (binary 1.0000) then C<sup>6</sup>, which is twice

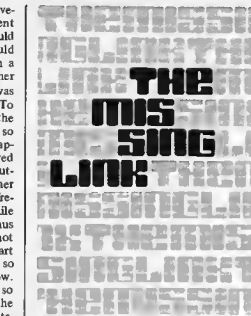
the frequency, is decimal 2.000... (binary 10.00...) and the other notes lie in between. Thus a particular note may be synthesised by taking an input to the synthesiser from a divider stage when there is a '1' in the corresponding column of the binary number. Thus, for example, E is represented by binary 1.0100001010, so inputs are required from the  $2^0$ ,  $2^{-2}$ ,  $2^{-7}$  and  $2^{-9}$  dividers. However, the frequencies provided by these dividers cannot simply be OR'd together. The reason for this is apparent in figure 6. If, for instance, the  $2^0$  and  $2^{-3}$  outputs were OR'd together, then the output of the OR-gate would follow



the  $2^0$  waveform while the  $2^{-3}$  waveform was low, but immediately it went high the output of the OR gate would go high and the  $2^0$  waveform would have no effect. This would result in a frequency lower than  $2^0$  but higher than  $2^{-3}$ , whereas the desired result was the sum of the two frequencies. To avoid this it is necessary to modify the mark-space ratio of the waveforms so that no two pulses coincide when applied to the OR-gate. This is achieved by AND-ing the lower frequency outputs with the complement of the higher frequency ones, so that the lower frequency outputs can only go high while the higher frequency ones are low, thus ensuring that two high outputs cannot coincide. This is shown in the lower part of figure 6.  $2^0$  is ANDed with  $2^1$ , so that it may only go high when  $2^1$  is low.  $2^{-1}$  is ANDed with  $2^0$  and  $2^1$ , and so on, until finally  $2^{-10}$  is ANDed with the complements of all the other outputs. The various pulse trains can thus be interleaved by OR-ing them together without any of the pulses ever coinciding.

Figure 7 shows the block diagram of a master oscillator using the principles outlined above. The partial frequencies are obtained from a clock generator by dividing down using a series of flip-flops. Since the flip-flops have Q as well as Q outputs the complements of the various outputs are available. As outputs from  $2^0$  (half the clock frequency) down to  $2^{-10}$  are required, 11 flip-flops are necessary. The outputs are ANDed with the complements of other outputs as described earlier to give 11 outputs shown as  $2^0$  to  $2^{-10}$ . These outputs are then OR'd together as required to give the correct frequency ratios. Finally each output passes through 8 divide-by-two stages to remove jitter, at the outputs of which 11 notes of the top octave are available. The two  $C_5$  and  $C_6$ , being an integral negative power of two times the clock frequency, do not need to be synthesised but are simply obtained from the appropriate flip-flops of the input divider stages (FF1 to FF11).

As a refinement, vibrato can be introduced into the system simply by modulating the frequency of the clock generator. The effect known as 'octave tremolo', in which the pitch of the notes jumps up and down by an octave, can also be obtained by interposing an additional flip-flop (FF12) between the clock generator and the input dividers and switching it in and out of circuit by means of an octave tremolo oscillator. A practical circuit and constructional details of this master oscillator will be given in the second part of this article.



**Modifications to Additions to Corrections in Circuits published in Elektor**

**TV tennis**

Based on experience gained in our laboratories while developing extensions for the tv tennis (elektor 7, p. 1111), and also during non-stop operation at the audio fair last October, we feel that the following points bear further comment:

- the IC numbers IC10 and IC11 on the component layout for the main p.c.b. (figure 7) are interchanged. Reading from top to bottom down the left-hand row of ICs, the order should be: IC8, IC10, IC7, IC12, IC9, IC11, IC13. Since both ICs are 7400s, this error will not effect the performance of the design; however, if the mains sync modification of figure 3a is being carried out it can lead to misunderstandings as to which track on the board should be broken.
- improved picture definition and sync pulses can be obtained by changing the values of C34 and C38 in the modulator unit: C34 can be increased to  $10 \mu/6.3 \text{ V}$  (+ to R55, - to point A), whereas C38 can be decreased to 47 p.
- in some cases a minor improvement of the picture can be obtained by adding small resistors ( $1 \dots 2.2 \Omega$ ) in series with the decoupling capacitors C4, C8, C11, C14, C17, C20, C23 and  $C_x$ . The improvement depends on how 'lossy' the capacitors were in the first place.
- $C_x$  was not listed in the parts list. It is 100 n.
- it was perhaps not made sufficiently clear in the text that we do not advise using the circuit on 405 lines VHF, as this calls for several modifications to the line sync and horizontal bat and ball position circuits. The

modulator can easily be tuned to give a good picture at the low-frequency end of the UHF band, on 625 lines, without any circuit modifications.

- a further point which was not specifically stated in the text is that the power supply should be short-circuit protected. The reason for this is that inadvertently pressing both 'serve' buttons simultaneously connects R42 and R38 ( $10 \Omega$ ) across the supply - the current consumption then becomes more than 1 A. The supply which we 'strongly recommended' (figure 4) is designed to withstand this.

- for the extensions to the game which will be published shortly (new games, boundaries, net, sounds and scoring) various connections will have to be made to the existing board. This should present no problems, but to simplify matters a new board with additional markings will be introduced as soon as stocks of the original board have run out. There are no circuit modifications required for this, so both boards can be used equally well for the extended version.



**TCA730/740**

The layout for the p.c.b. for the TCA730/740 preamplifier contains one error: the junction C3/R7 should be connected to the junction C5/R5 (pin 5 of 730. The boards supplied with the eps print service (no. 9191) are correct.

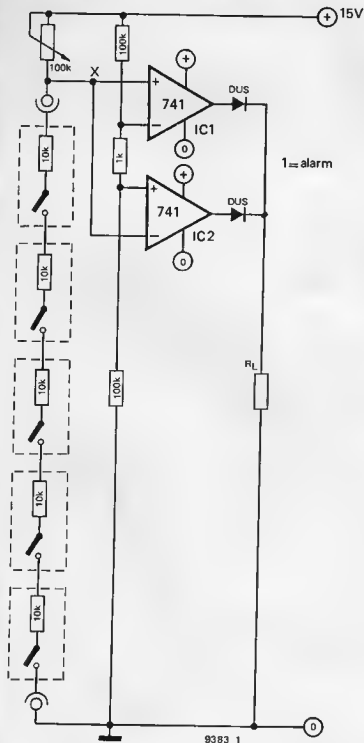
Furthermore, the latest Philips application notes show a minor design modification: R5 and R5' are now shown as 68 k instead of 120 k, and R2 and R2' are now shown as 33 k instead of 18 k. We have not yet experimented to see what difference this makes.



**Selektor**

Owing to an error in the final stage before going to print, the article 'Realisation between the lines' was included in Elektor 8, p. 1207. The art editor offers his apologies.

## High security burglar alarm sensor



Low-cost domestic burglar alarms often operate on the loop principle. A number of normally closed microswitches protect points of entry. These are all connected in series, so that opening a door or window will open one of the switches and break the circuit, thus setting off the alarm. Similarly any attempt to cut the wires leading to the switches will set off the alarm. However, this type of circuit is not proof against bridging out a switch with a link, which can easily be done if the wires are not concealed. Concealment of the wires increases the difficulty of installing an alarm, and a surface run of twin core bell flex is a much more attractive proposition to the home constructor.

Fortunately it is a simple matter to construct an alarm operating on the loop resistance principle. The idea is that a resistor is included in series with each microswitch, mounted in the microswitch housing. When the alarm is in operation the loop resistance is monitored. If the wires are cut the loop resistance immediately becomes infinite and the alarm is set off, while any attempt to bridge out a switch will decrease the loop resistance, also setting off the alarm. The alarm system can be defeated (find out how yourself) but it is considerably more difficult.

Operation of the circuit is very simple. The loop resistors form a potential divider with a 100 k pot. The pot is adjusted until the voltage at point X is between the thresholds of the two comparators. The outputs of both comparators are thus low. Any increase in voltage (due to breaking the loop) will exceed the threshold of IC1, causing the output to swing positive and producing a 1 on the output of the OR gate. Any decrease in voltage due to bridging a switch will cause the output of IC2 to go positive.



3

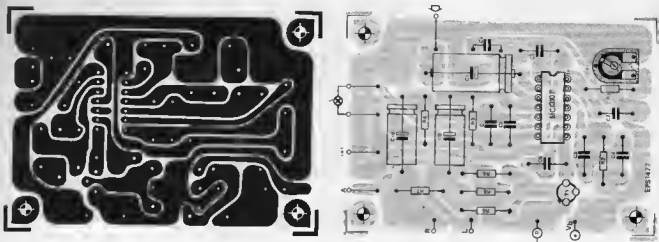


Figure 1. Block diagram of the MC1310P - a complete stereo decoder on one chip.

Figure 2. Circuit diagram of the stereo decoder. For setting up, the set is tuned to a stereo transmission and P1 is adjusted until the stereo indicator lights.

Figure 3. The p.c. board and component layout.

the amplitude of the pilot frequency is a measure of the 'stereo goodness', as well as an indication of the availability of a stereo transmission, the DC voltage can be used as the drive voltage for a Schmitt trigger.

The Schmitt trigger operates both the stereo switch and the stereo indicator lamp.

The regenerated 38 kHz auxiliary carrier then passes to the channel switch at the outputs of which the left-right signals are available.

**The practical circuit**

The complete circuit of the stereo decoder using the MC1310P is shown in figure 2. The LF signal arrives via the capacitor C1 to the input (pin 2) of the IC. The oscillator frequency (76 kHz) is set by the combination of P1, R1 and C2, the frequency drift of the oscillator is compensated within the range -10°C...+50°C. C2 is a styroflex type with the tightest possible tolerance (1%...2%).

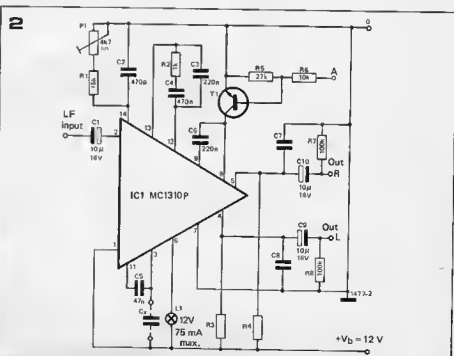
The low-pass filter for the control voltage of the 76 kHz oscillator consists of components C3, C4 and R2, and an internal resistance within the IC. The de-emphasis network used to equalise the pre-emphasis of the transmitted stereo signal consists of the output impedance of the amplifier and of both RC networks R3, C8 and R4, C7.

The input impedance of the LF amplifier which follows the decoder should be at least 22 k otherwise a marked effect on the de-emphasis is introduced. Because capacitors C3, C4, C7 and C8 are frequency determining components, low temperature coefficient types must be used, preferably polystyrene.

The coupling of the phase comparator circuit is done via C5. If this capacitor is 47 nF, the subcarrier waveform generated will lead by 3.5°. This, together with the phase shift introduced within the IC, amounts to a total phase advance of 5.5°. This phase shift is compensated by a capacitor (Cx) between pin 3 and +Vb. A capacitor of 820 pF will compensate an advance of 5.5°.

**Parts list:**

- Capacitors:
- C1, C9, C10 = 10 µ/16 V
- C2 = 470 p
- C3, C6 = 220 n
- C4 = 470 n
- C5 = 47 n
- C7, C8 = 10 n
- Cx = 820 p (typ, see text)
- Note: The temperature coefficient of capacitors C2, C3, C4, C7 and C8 should be as low as possible.
- Resistors:
- R1 = 15 k
- R2 = 1 k
- R3, R4 = 4k7
- R5 = 27 k
- R6 = 10 k
- R7, R8 = 100 k
- P1 = 4k7 lin (preset)
- Semiconductors:
- T1 = BC107
- IC1 = MC1310P
- Misc.:
- L1 = indicator lamp, 12 V/75 mA max. (see text)



Larger values would cause the subcarrier waveform to lag. In this way, possible phase shift which may occur in the IF amplifiers can be compensated for. This possibility can also be used if the channel separation should not be satisfactory. This fault is usually only plainly apparent in the case of stereo test transmissions or by using a stereo signal generator. The low-pass filter prior to the stereo-switch consists of an internal resistance together with C6.

It offers the possibility of externally setting the mono/stereo switch to the position 'mono', this is done by applying +0.3 V to point 8.

This positive bias is taken from the supply voltage via R6, T1 and R5. The supply voltage can be taken to point A in figure 2 via a single pole switch or via a sensor switch.

In combined AM/FM receivers, interference due to the oscillator waveform of the IC may arise, particularly during AM reception. In such cases the 76 kHz oscillator can be made inactive in two ways. Either by connecting pin 14 to supply common, or by connecting pin 14 to the positive supply via a 3.3 k resistor. The latter can be combined with the external mono switch-over, connecting point A to pin 14 via a 3.3 k resistor.

A 12 V/75 mA type is intended for the indicator lamp. Other types, including an LED, may of course be used with a suitable series resistance. With the usual LED the series resistance is calculated for a 20 mA max. current. The IC has an internal resistance which limits the switch-on current of the indicator lamp to 250 mA. Although the IC has a wide supply current range, a 12 V supply is recommended, the component values given in figure 2 are for this supply voltage. Lower supply voltages would necessitate changes in some values. The main characteristics of the MC1310P are summarised in table 1.

Table 1

MC1310P Data	
Maximum input voltage $V_{eff}$ in (Stereo, distortion factor 0.5%)	560 mV
Maximum input voltage $V_{eff}$ in (Mono, distortion factor 1%)	560 mV
Input impedance	50 k
Channel separation (50 Hz ... 15 kHz)	40 dB
Balance in 'mono' position	< 1.5 dB
Pilot tone suppression (19 kHz)	34 dB
Subcarrier suppression (38 kHz)	45 dB
Output voltage for channel $V_{eff, out}$	485 mV
Capture range of the oscillator (valid only for the component values given in figure 2)	3%
Current consumption (without stereo-indicator)	13 mA

## elektor shorthand

A large number of queries at the Audio Fair in London show that many new readers have started buying Elektor from no. 7 on. They have not seen the full explanation of the terms 'TUP' and 'TUN' that we gave in Elektor 1, p. 9, nor have they read the further explanation of other 'Elektor shorthand' in no. 4, p. 660. For this reason, we are re-printing the latter article in full. We will also regularly reprint the 'TUP-TUN' page and the pages of IC-pinning for TTL, CMOS and linear ICs as originally published in Elektor no. 5.

From various enquiries it has become clear that some of our readers feel that they have been plunged in at the deep end. Elektor's 'shorthand' style of symbols and conventions seems to have led to some confusion, in spite of our efforts to the contrary, so some further explanation seems to be called for.

### Resistor and capacitor codes

When giving the values of resistors and capacitors, decimal points and large numbers of zeros are avoided as far as possible. To this end, extensive use is made of the international abbreviations:

p (pico-) = $10^{-12}$ =	one millionth of one millionth;
n (nano-) = $10^{-9}$ =	one thousandth of one millionth;
$\mu$ (micro-) = $10^{-6}$ =	one millionth;
m (milli-) = $10^{-3}$ =	one thousandth;
E = $10^0$ =	unity;
k (kilo-) = $10^3$ =	one thousand times;
M (mega-) = $10^6$ =	one million times;
G (giga-) = $10^9$ =	one thousand million times;
T (tera-) = $10^{12}$ =	one million million times.

Furthermore, the symbols  $\Omega$  (ohm) and F (farad) are usually omitted, since it is

normal practice to state resistance values in ohms and capacitance values in farads. Finally, the decimal point is usually replaced by one of the abbreviations (p, n,  $\mu$  ...) listed above (This has also been accepted practice for some years).

A few examples may serve to clarify all this:

Resistance value 2k7: this is 2.7 k $\Omega$ , or 2700  $\Omega$ .

Resistance value 470: this is 470  $\Omega$ .

Resistance value 3M9: this is 3.9 M $\Omega$ , or 3,900,000  $\Omega$ .

Capacitance value 4p7: this is 4.7 pF, or 0.000 000 000 004 7 F ...

Capacitance value 100  $\mu$ : this is 100  $\mu$ F.

Capacitance value 4700  $\mu$ : this is 4700  $\mu$ F, and could have been written as 4m7 — but never is.

Capacitance value 10n: this is 10 nF, and is also sometimes written (but not in Elektor!) as 10,000 pF or 0.01  $\mu$ F; or even as 10 kpF (10 kilo-pico-Farad), which is a horrible confusion of symbols. In the same way, one sometimes finds  $\mu\mu$ F (micro-micro-Farad) instead of pF.

### Semiconductor type numbers

Very often, a large number of equivalent types for one integrated circuit exist with different type numbers. On closer examination, a group of digits are often found to be identical, but they are pre-suffixed with letters and digits which denote the manufacturer. As an example, a popular op-amp is variously denoted as  $\mu$ A741, LM741, L741, MC1741, MIC741, RM741, SN72741 or ZLD741, to name a few. To cut through the confusion, this IC is referred to in Elektor as a '741' — which means that we couldn't care less who makes it, provided it meets the specifications...

In the same way, '7400' (or sometimes even '00') stands for SN7400, SN74HC00, DM7400, MC7400, etc., and the last two figures are used in the same way for other ICs in the 7400 series.

Finally, transistors are sometimes listed as 'TUP' or 'TUN'. This is explained elsewhere. Transistors can also be listed as BC107, for instance; a long list of equivalent types for the BC107 series is also given in the TUP/TUN list.

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BC238	NPN	20	200mA	120-860	12p	15p
BC239	NPN	20	200mA	120-860	12p	15p
BC307	PNP	45	200mA	70-460	15p	15p
BC308	PNP	25	200mA	70-460	12p	15p
BC309	PNP	20	200mA	120-460	12p	15p
BC317A	NPN	45	150mA	110-220	18p	18p
BC318B	NPN	30	cont.	200-450	18p	18p
BC319C	NPN	20	300 Pk.	420-800	20p	20p
BC320A	PNP	45	150mA	110-220	20p	20p
BC321A	PNP	30	cont.	200-450	20p	20p
BC322B	PNP	20	300 Pk.	200-450	20p	20p
BC327	PNP	45	1A Peak	40 Min.	20p	20p
BC318B	PNP	25	Peak	40 Min.	18p	18p
BC337	NPN	45	Peak	40 Min.	18p	18p
BC338	NPN	25	Peak	40 Min.	18p	18p
BC347	NPN	45	100mA	40-450	12p	12p
BC348	NPN	30	100mA	40-450	12p	12p
BC349	NPN	20	100mA	40-450	12p	12p
BC350	PNP	45	100mA	40-450	15p	15p
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